9.1 A 95GHz Receiver with Fundamental-Frequency VCO and Static Frequency Divider in 65nm Digital CMOS

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Recently, several integrated radio receivers and transmitters operating at 60GHz have been developed in SiGe BiCMOS [1] and CMOS [2-4] technologies, by both industry and academia. As CMOS transistor gate lengths continue to scale downward, integration becomes possible at even higher frequencies. This paper presents a fully integrated receiver, with LNA, mixer, IF amplifier, fundamental-frequency quadrature VCO, and static frequency divider, operating at 95GHz in a 65nm general-purpose (GP) CMOS technology. The receiver consumes 206mW from a 1.2V/1.5V supply. With large RF and IF bandwidths of over 19GHz and 16GHz, respectively, it is suitable for passive-imaging applications, and for wireless chip-to-chip communication at data-rates exceeding 20Gb/s. Together with the recently reported 60GHz receiver in 90nm CMOS [4], this 95GHz receiver in 65nm CMOS demonstrates that scaling of entire mm-wave receivers is possible in both frequency coverage and across technology nodes, as predicted by Gordon Moore in the last paragraph of [5]. Furthermore, with the reduction of the die area occupied by lumped passives at higher frequencies, and with the intrinsic speed improvement anticipated in future CMOS technology nodes, one can expect that entire CMOS transceivers can be scaled to 120GHz in 45nm, and to 160GHz in 32nm technologies, and can be integrated with antennas and other systems as wireless I/Os for chip-to-chip communication at 40Gb/s.

The architecture of the fabricated receiver is illustrated in Fig. 9.1.1. It uses an improved version of a shunt-series transformer-feedback 3-stage cascode LNA with a measured peak gain of 13dB and noise figure of 6 to 7dB [6]. The LNA is coupled to a double-balanced Gilbert-cell mixer through transformer T1 which performs single-ended to differential conversion. The insertion loss of the transformer, measured on a separate test structure, is 1.7dB in the 57-to-94GHz range. A differential CML pair with 50Ω loads is used as the broadband IF amplifier. The LO signal is fed to the mixer using short transmission lines and transformer T2. A static-frequency divider [7] is connected to the VCO to demonstrate the feasibility of a robust integrated 90GHz PLL. Due to space limitations, only one of the two divider outputs is made available for testing, and the other is terminated on-chip. A fundamental-frequency quadrature VCO, whose schematic is shown in Fig. 9.1.2, is used to generate the LO signals on-chip. The differentially tuned VCO is composed of 4 symmetrically coupled Colpitts oscillators. An RC filter is used in the VCO bias network to minimize the injection of supply noise, and thus prevent the degradation of the VCO phase noise. Four buffers, also shown in Fig. 9.1.2, are used to increase the output power of the VCO, and to differentially drive the mixer on one side, and the divider on the opposite side. Each of the VCO buffers is implemented as a single-stage common-source amplifier, which is matched to 50Ω at the output. A differential buffer topology with common-mode current source is avoided in order to suppress common-mode instabilities and to maximize the gain. The LNA, mixer, and IF amplifier, employing topologies with two vertically stacked transistors, are designed to operate from 1.5V supply. The VCO and static frequency divider operate from a nominal supply of 1.2V.

The entire receiver, along with several breakouts, is fabricated in a 65nm GP CMOS technology, with 7 metal copper backend. An f_T and f_{MAX} of 170GHz and 250GHz are measured for devices with a 1μm gate finger width contacted on one side of the gate and biased at a V_{DS} of 0.7V. To overcome the problem of integrating the receiver blocks together, without degrading their performance, ample ground metallization and vias are used everywhere to minimize parasitic source degeneration and gate resistances. Metal-over-metal (MOM) capacitors of 0.5pF are placed close to each circuit block to provide local ground and supply decoupling. A dense alternating-metal mesh is used for ground, bias, and power-supply distribution and decoupling. The mesh is designed to simultaneously meet the stringent metal-density manufacturing rules. The receiver is measured on-wafer and characterized over temperature from 25°C up to 100°C.

Figure 9.1.3 shows the tuning range and output power of the quadrature VCO over temperature, measured on a breakout of the VCO, which includes all buffers and the divider. The VCO can be tuned from 88.3GHz to 91.3GHz, irrespective of temperature. The tuning range remains constant over a wide range of temperatures thanks to the Colpitts topology, the use of lumped inductors, MOM capacitor C_1, and accumulation-mode MOS varactors, whose inductance and capacitance depend mostly on the metallization characteristics and dielectric permittivity, which hardly vary over temperature. The total output power of the VCO with four buffers is +2 to +3dBm in 50Ω at 25°C. The VCO achieves a phase noise of –95dBc/Hz at 1MHz offset from the 90.3GHz signal. The single-side-band (SSB) conversion gain, measured using a spectrum analyzer, is plotted in Fig. 9.1.4, along with the input return loss of the receiver. At the nominal supply voltage of 1.5V for the LNA, mixer, and IF amplifier, and 1.2V for the VCO and divider, the peak gain is 12.5dB and the 3dB bandwidth of the receiver is 19GHz, from 76 to 95GHz. In the receiver, the gain of the mixer compensates for the losses of the transformers that couple the LNA and VCO to the mixer. The S_{11} of the receiver (measured on the LNA breakout) is lower than –15dB from 77GHz up to at least 94GHz. Figure 9.1.5 illustrates the double-side-band (DSB) noise figure and gain of the receiver, plotted versus the current density in the first stage of the LNA at 3 temperatures. The optimal bias current density for lowest noise figure is 0.25mA/μm. In Fig. 9.1.6, the DSB noise figure and conversion gain, measured using an Agilent N8975A noise-figure analyzer and a 75-to-110GHz ELVA noise source, are plotted versus the IF frequency for different supply voltages of the LNA, mixer, and IF amplifier, and up to 100°C with the nominal 1.5V supply. The DSB noise figure is 7 to 8dB for the nominal bias and temperature, and increases by 2.2dB at 75°C. All components of the receiver are verified to work from 25°C up to 100°C, except the divider, which divided the VCO signal only up to 50°C. The input 1dB compression point of the receiver was measured to be –18dBm. The total DC power consumption of the receiver is 206mW from the nominal 1.2V (for the VCO and divider) and 1.5V (for the LNA, mixer and IF amplifier) supplies, with 28% of the power in the VCO, 17% in the LNA, 11% in the divider, and 6.5% in the mixer. A die micrograph of the receiver chip is shown in Fig. 9.1.7, demonstrating that a small active circuit area of 225×940μm² is achieved by using only lumped transformers, inductors and capacitors in the design.

Acknowledgements:
The authors acknowledge Christophe Garnier and Bernard Sautreuil of STMicroelectronics for facilitating access to technology. This work was funded by an NSERC Strategic Grant.

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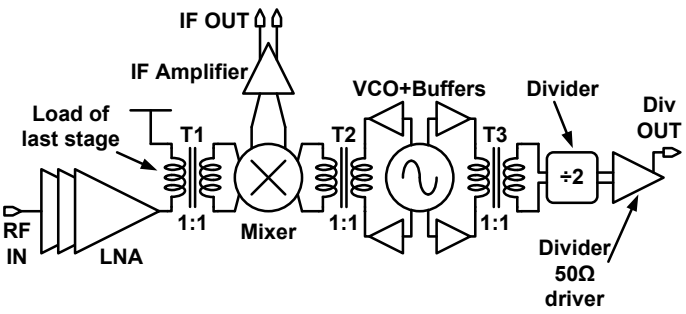

Figure 9.1.1: Top-level block diagram of the receiver chip.

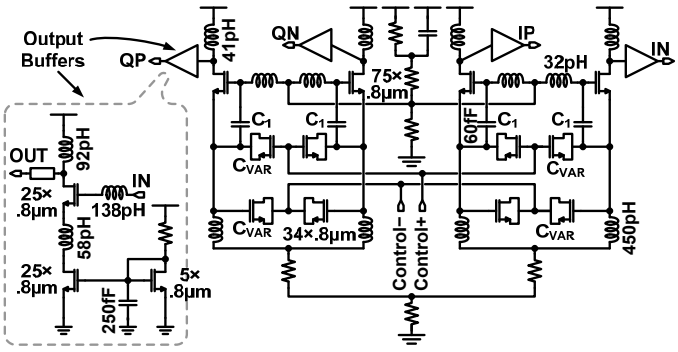

Figure 9.1.2: Quadrature VCO and VCO buffer schematics. All transistors and varactors use 65nm gate length.

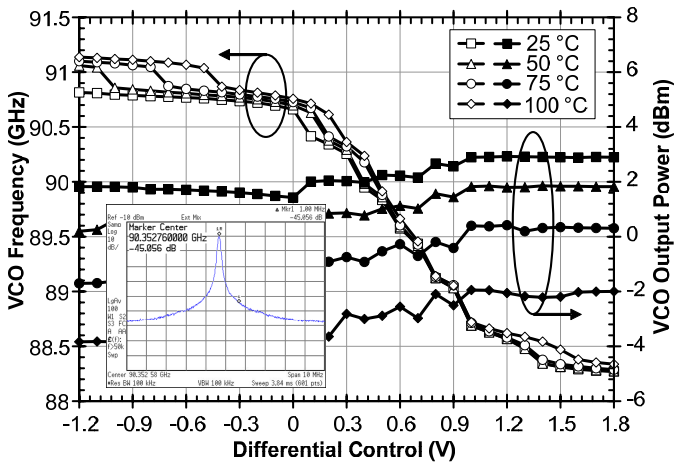

Figure 9.1.3: Measured tuning range, output power, and phase noise of the VCO with output buffers.

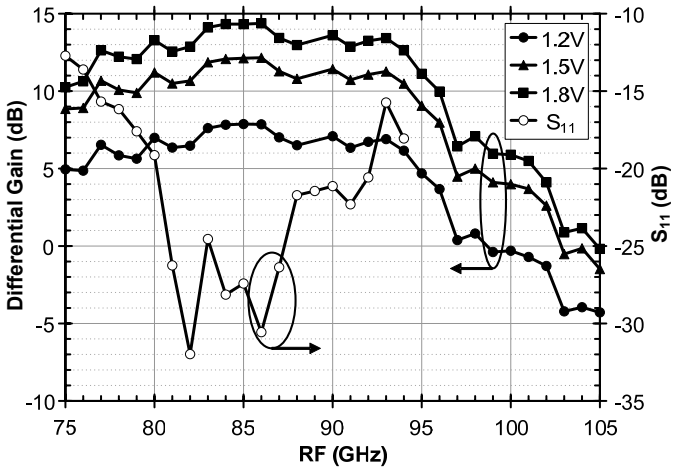

Figure 9.1.4: Measured SSB receiver conversion gain and S_{11} versus RF.

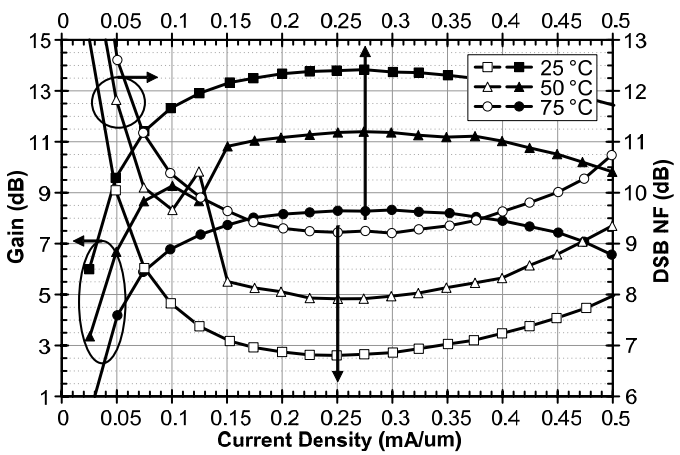

Figure 9.1.5: Measured receiver conversion gain and NF variation with the current density of the LNA input transistor (LO=89GHz and IF=6.3GHz DSB).

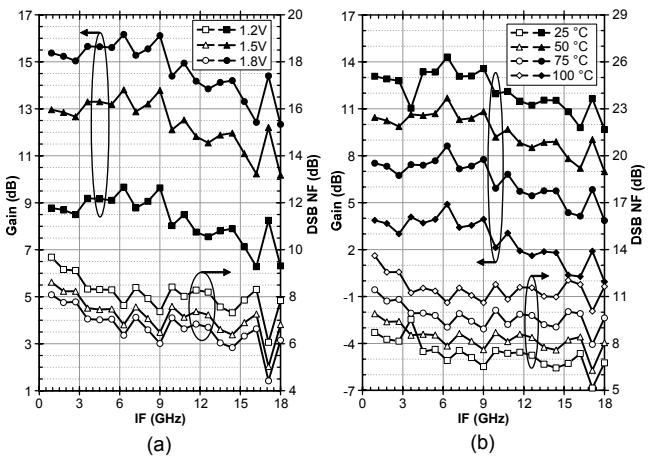

Figure 9.1.6: Receiver gain and NF versus IF, for (a) different LNA, mixer and IF amplifier supplies, and (b) at different temperatures for the nominal supply (LO=89GHz).

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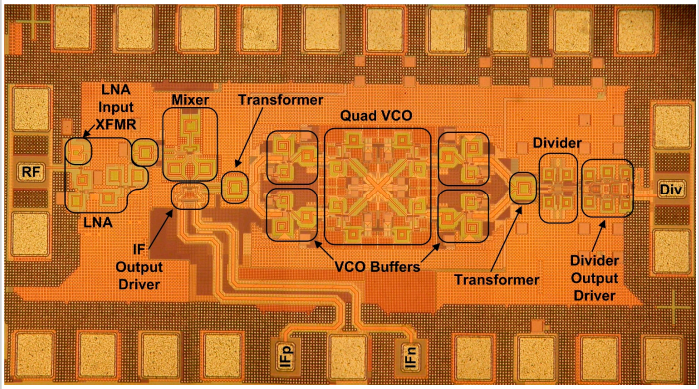

Figure 9.1.7: Receiver die micrograph. The pad-limited chip size is 600×1100μm².

