BSIM4 High-Frequency Model Verification For 0.13 μm RF-CMOS Technology

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Abstract **— A compact model capable of simulating both DC and RF characteristics is highly desirable. This work is the first report of an extensive experimental evaluation of the accuracy of the BSIM4 model at high frequencies using a 0.13μm RF-CMOS process. The accuracy of the model is verified on both N-channel and P-channel devices through small-signal S-parameter measurements up to 50 GHz, 1/f noise measurements, and noise figure measurements in the 2-GHz to 6-GHz range.**

Index Terms **— 0.13μm, BSIM4, Compact model, CMOS, MS/RF.**

I. Introduction

As the cutoff frequency (fT) of deep sub-micron MOSFETs now exceeds 130 GHz, many high-speed and microwave ICs are likely to be implemented in CMOS technology. Coupled with the low cost, high level of integration and easy access to technology, these high fT values open the door for highly integrated full CMOS solutions for next-generation wireless applications. The availability of a compact MOS model that is valid for a broad range of bias conditions and operating frequencies is essential in the development of microwave circuits using MOS transistors. Such a model is critical for accurate design of high-frequency integrated circuits with 'first pass' success. Unfortunately, most of the commercially available MOS transistor models are not particularly suited for high frequencies. Although the BSIM3v3 model has been extensively validated in DC and low-frequency measurements, not much attention has been paid to high-frequency modeling. Recent papers have extended the validity of BSIM3v3 to RF applications by adding a complicated substrate network and a gate resistance to the BSIM3v3 core [1].

In the development of foundry technologies, a compact model capable of simulating both DC and RF characteristics is highly desirable. BSIM4 features several major improvements and additions over BISM3v3 and was developed to explicitly address deficiencies in modeling sub-0.13 μm CMOS transistors and for RF and high-speed circuit simulation [2]. It includes three critical modules for accurate high-frequency design: the intrinsic-input resistance (IIR) model, the substrate resistance network model, and the holistic thermal noise model. So far only the DC performance of the BSIM4 model has been investigated [3]. This work is the first report of an extensive experimental evaluation of the accuracy of the BSIM4 model at high frequencies.

This paper is organized as follows: Section II describes the CMOS technology for mixed-signal and RF system-on-a-chip (MS/RF SOC) applications. Section III presents the BSIM4 high-frequency model verification and experimental results. Finally, concluding remarks are summarized in section IV.

II. CMOS Technology for MS/RF SoC

N-channel and P-channel MOSFETs were fabricated in a 0.13 μm RF CMOS process with full Cu damascene metallization. The main features of this process flow were reported in [4]. In addition to standard CMOS logic technology components and embedded memory cells, passive components such as resistors, capacitors, inductors, varactors, and transmission lines, as well as adequate on-chip electrical noise-isolation (DNW), are mandatory ingredients in support of MS/RF SOC. A more detailed description of all the available devices in TSMC's 0.13 μm RF CMOS process can be found in [5] and [6].

The BSIM4 model parameters were extracted using on-wafer DC and S-parameter measurements performed with GSG probe. A two-step series-shunt de-embedding of pad and interconnect parasitics was employed.

III. BSIM4 Model Verification

A. *DC-IV Characteristics Verification*

Fig. 1 shows the measured and simulated output characteristics of N- and P- channel 0.13 μm MOSFETs.

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The modeled and measured transconductance and output resistance are compared in Figs. 2 and 3, respectively. Furthermore, the VIP3, important in power amplifier linearity simulations, is evaluated in Fig. 4. The excellent match between measurements and simulations is attributed to the improvements in the BSIM4 mobility and physics-based output resistance models. Both are essential in accurately predicting high-frequency gain and output power behavior.

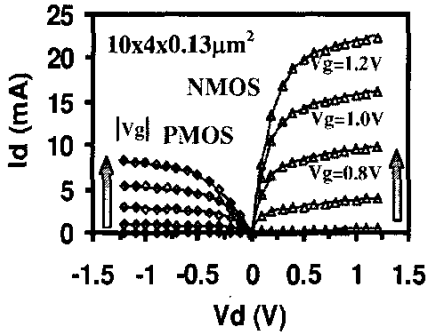

Fig. 1. Output characteristic fitting of N-(Δ)/P-(◊)MOS with 10x4x0.13 μm² at |Vg |=0.4, 0.6, 0.8, 1.0 and 1.2V

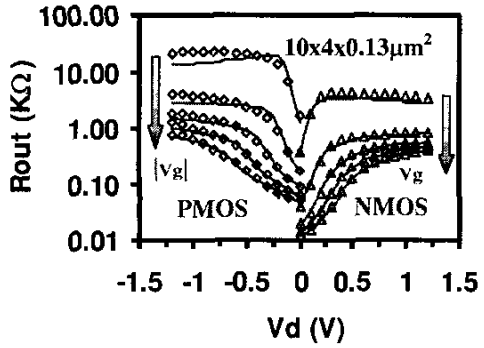

Fig. 2. Small-signal output resistance fitting of N-(Δ)/P-(◊)MOS with 10x4x0.13 μm² at |Vg |=0.4, 0.6, 0.8, 1.0 and 1.2V.

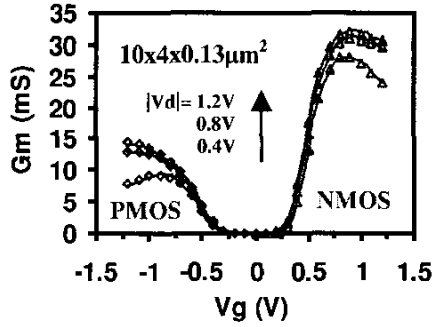

Fig. 3. Small-signal transconductance fitting of N-(Δ)/P-(◊)MOS with 10x4x0.13 μm² at |Vd |=0.4, 0.8 and 1.2V.

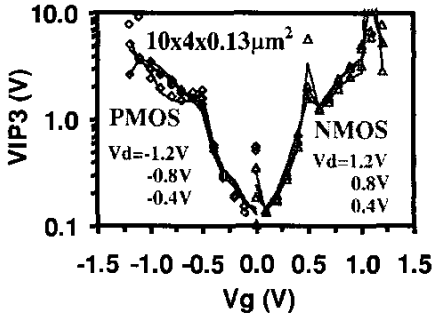

Fig. 4. The VIP3 ($\sqrt{24xgm/|gm_3|}$) fitting of N-(Δ)/P-(◊) MOS with 10x4x0.13 μm² at |Vd |=0.4, 0.8 and 1.2V.

B. HF Characteristics Verification

Next, the measured and simulated S-parameters of 0.13μm RF CMOS transistors were compared at different bias points and frequencies ranging from 1GHz up to 50 GHz. The device has a multi-fingered gate structure with a unit width of 4μm and the bulk and source nodes are grounded. Fig. 5 depicts the BSIM4 equivalent circuit used in the RF and noise analysis. The model parameters $R_{D/S,eltd}$ were determined from DC-IV measurements. $R_{G,eltd}$ and RBPD/S/B, which are associated with the gate electrode and lossy Si substrate, respectively, were extracted from the real part of the input admittance *Y11* and of the output admittance *Y22*. Figs. 6 and 7 show excellent S-parameter fitting for both N- and P-MOS devices under various bias conditions, thus validating the model and the parameter extraction methodology. The RF and noise related model selectors and their corresponding extracted parameter values, are depicted in Table I. Several RF figures of merit (FOM) such as current gain *H21*, *fT*, Unilateral power gain *U*, and stability factor K are also analyzed and shown in Figs. 8 through 12. In all cases good agreement between measurements and simulations has been demonstrated.

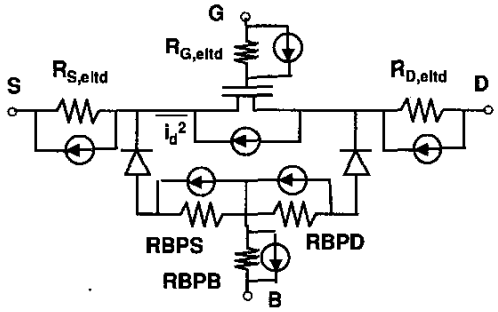

Fig. 5. The BSIM4 equivalent circuit used for DC, RF and Noise simulation. Input intrinsic resistance (IIR), substrate resistance network and holistic thermal noise are integrated internally.

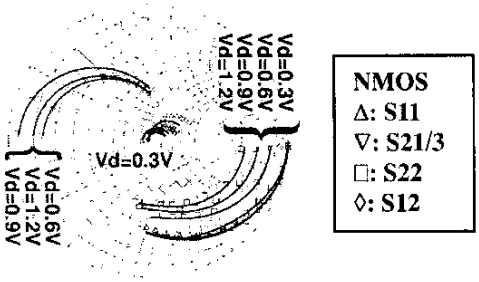

Fig. 6. S-parameter fitting of NMOS at Vd=0.8V; Vg=0.3, 0.6, 0.9 and 1.2V with frequency sweep from 1GHz to 50GHz.

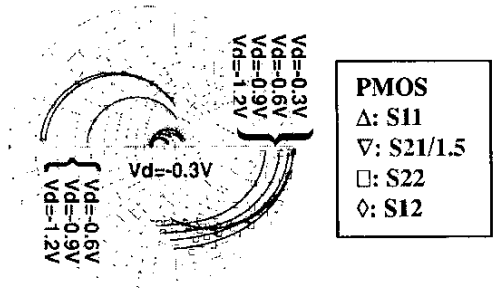

Fig. 7. S-parameter fitting of PMOS at Vd=-0.8V; Vg=-0.3, -0.6, -0.9 and -1.2V with frequency sweep from 1GHz to 50GHz.

TABLE I
SUMMARY OF MODEL SELECTORS AND EXTRACTED PARAMETERS

Model Selector	Fitting Parameter	
	NMOS	PMOS
RGATEMOD=1	RSHG=13; NF=10	RSHG=30; NF=10
RDSMOD=0	NRD=19; RSH=67m	NRS=22; RSH= 122m
PERMOD=0	ASeff=25p; PSeff=13u	ADeff=21p; PDeff=10u
RBODYMOD=1	RBPS=RBPD=1; RBPB=47.5	RBPS=RBPD=1.5; RBPB=36
FNOIMOD=1	NOIA=2E43; NOIB=4E26; NOIC=5E8; EF=1;EM=4.1E7	NOIA=2E40; NOIB=2E24; NOIC=6E8; EF=1;EM=4E6
TNOIMOD=1	TNOIA=1.5E6; TNOIB=3.5E6	TNOIA=1.5E6;TNOIB=3.5E6

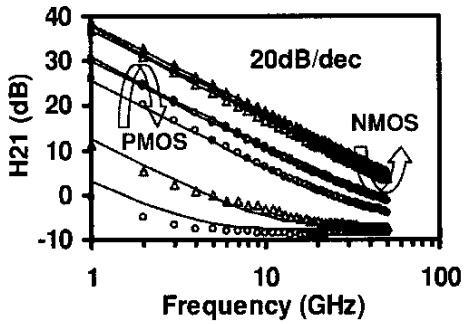

Fig. 8. Current gain (H21) frequency response fitting of N-(Δ)/P-(◊)MOS at |Vd |=0.8V; |Vg |=0.3, 0.6, 0.9 and 1.2V.

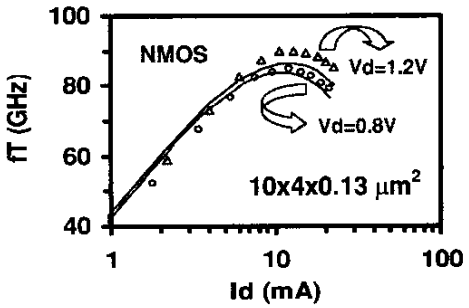

Fig. 9. Current gain cutoff frequency (fT) as function of the drain current fitting of NMOS at Vd =0.8V (o) and 1.2V(Δ).

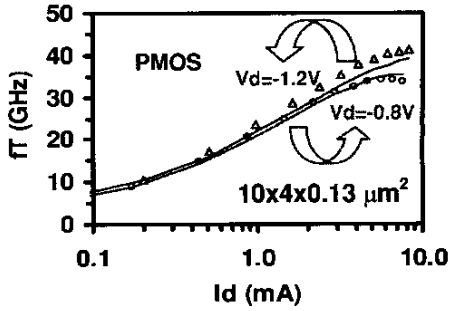

Fig. 10. Current gain cutoff frequency (fT) as function of the drain current fitting of PMOS at Vd =-0.8V (o) and -1.2V(Δ).

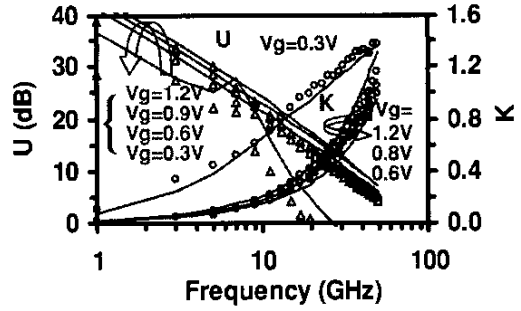

Fig. 11. Power gain (U; Δ) and stability factor (K; o) frequency response fitting of NMOS at Vd=0.8V; Vg=0.3, 0.6, 0.9 and 1.2V.

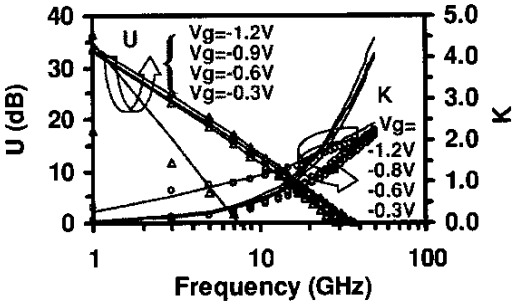

Fig. 12. Power gain (U; Δ) and stability factor (K; o) frequency response fitting of PMOS at Vd=-0.8V; Vg=-0.3, -0.6, -0.9 and -1.2V.

C. Noise Characteristics Verification

Finally, the ability of the model to accurately capture low-frequency flicker noise and high-frequency thermal noise was assessed. The former is demonstrated in Fig. 13 at various biases from 100 Hz up to 100 kHz with BSIM4 noise model to immunity from discrepancy for multiple identical devices connected in parallel. The measured and simulated noise figure for a 50Ohm signal source impedance is shown in Fig. 14 as a function of frequency, and as a function of bias at 4.8 GHz in Fig.15.

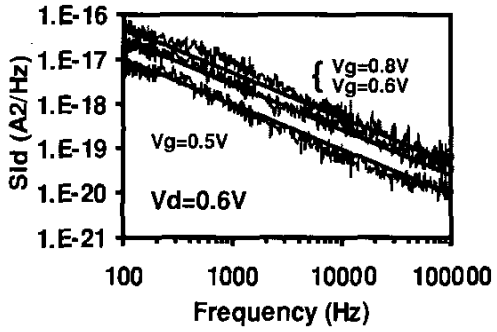

Fig. 13. Low-frequency 1/f noise (Sid) fitting of NMOS with 10x0.18 μm^2 at Vd =0.6V; Vg=0.5V, 0.6V and 0.8V.

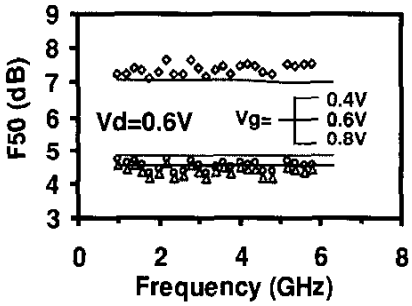

Fig. 14. HF thermal noise with 50 Ω termination (F50) fitting of NMOS at Vd=0.6V; Vg=0.4 (◊), 0.6(o), and 0.8V(Δ).

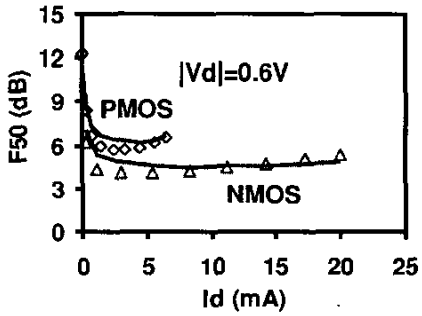

Fig. 15. High-frequency thermal noise with 50 Ω termination (F50) fitting of N-(Δ)/P-(◊)MOS at |Vd |=0.6V.

V. Conclusion

The BSIM4 high-speed/RF Spice model featuring distributed gate and substrate resistance was evaluated and verified for the first time in terms of 0.13 μm RF CMOS. The measured and modeled characteristics of DC-IV, small-signal gm and gds, high-frequency FOMs, and noise of 1/f and F50 with excellent agreement have been demonstrated. The improvements in the BSIM4 mobility and physics-based output resistance models facilitate the mimic of linearity and output impedance simulations. To yield correct simulation result we have modeled the access source/drain resistance in terms of absorbed-resistance approach instead of with lumped-resistance approach. It is necessary to include R_{Geltd} to account for the NQS effect due to the convergence of simulation NQS deficiency, which is important in accurate prediction of bandwidth. As to the substrate network, we have observed that a simple 3-R T-shape resistive network is good enough for output impedance model. Issue for scalable parameter for rapid growth in RF circuit applications should be improved. The ability of the model to accurately capture low-frequency Flicker noise and high-frequency thermal noise was also assessed. A unified Flicker noise model and Holistic thermal noise model improvement the excess noise associated with short-channel effect and immunity from the inaccurate for multiple identical devices as well.

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