A 1.2V, 140GHz Receiver with On-Die Antenna in 65nm CMOS

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***Abstract* — This paper presents a 1.2V, 100mW, 140GHz receiver with on-die antenna in a 65nm General Purpose (GP) CMOS process with digital back-end. The receiver has a conversion loss of 15-19dB in the 100-140GHz range with 102GHz LO, and occupies a die area of only 580µm × 700µm including pads. The LNA achieves 8dB gain at 140GHz, 10GHz bandwidth, at least -1.8dBm of saturated output power, and maintains 3dB gain at 125°C. The on-chip antenna, which meets all density fill requirements of 65nm CMOS, has -25dB gain, and occupies 180µm × 100µm of die area. Additionally, design techniques which maximize the millimeter-wave performance of CMOS devices are discussed.**

***Index Terms* — CMOS millimeter-wave integrated circuits, millimeter-wave amplifiers, MOS devices, millimeter-wave antenna arrays.**

I. Introduction

CMOS technologies at the 90nm and 65nm nodes perform well in 60GHz radio applications for short-range data communications. Complete receivers have also been fabricated in the 80-95GHz range for millimeter-wave imaging systems [1]. Indeed, the f_{MAX} of 65nm GP CMOS devices exceeds 200GHz, making this technology suitable for applications well above 100GHz.

To date, CMOS VCOs with oscillation frequencies up to 192GHz are commonplace [2], whereas the highest frequency amplifier in CMOS reported to date is centered at 104 GHz and has 9dB gain [3]. A SiGe HBT transceiver has been shown at 160GHz [4], and CMOS down-conversion mixers and amplifiers operating well above 100GHz have not been demonstrated. Therefore, the bottle-necks in pushing CMOS radio receivers and transmitters above 100GHz are the LNA, PA, and mixer circuit blocks. Furthermore, in some applications, millimeter-wave radios will be integrated alongside a larger digital system which operates from a supply of 1.2V or less. Consequently, a digital back-end (without MiM capacitors or thick RF metal) is used in all circuit designs presented here, as are circuit topologies capable of 1V operation.

D-band (110-170GHz) applications include data-communications, and imaging. In some passive imaging applications, the only RF circuit blocks required are an LNA and a detector, as shown in Fig. 1 [5], whereas other imaging systems may require an entire transceiver. To avoid wafer level assembly in massively parallel imaging systems, an on-die antenna (reasonably small at these frequencies) may be necessary. The block diagram of such a receiver is illustrated in Fig. 2.

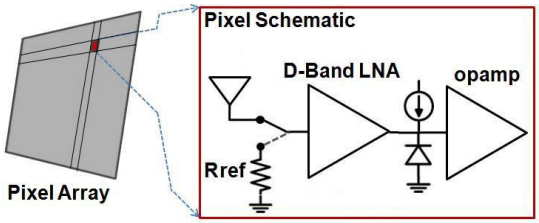

Fig. 1. Illustration of a passive mm-wave pixel array [5].

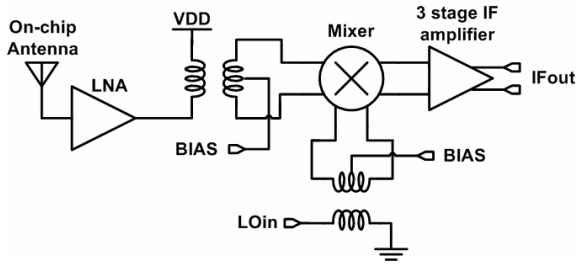

Fig. 2. 140GHz CMOS receiver block diagram.

II. Circuit Design

A. 140GHz Low-Noise Amplifier and Power Amplifier

The LNA schematic is illustrated in Fig. 3, and a layout micro-photograph of the first two stages is shown in Fig. 4. All transistors are biased at 0.25mA/µm, which corresponds to peak f_{MAX} current density in this 65nm GP CMOS technology at V_{DS} = 1V. The transistor size of each stage is scaled upward by 25%, resulting in a total current consumption of 52mA.

First, cascode stages are split into separate Common-Source (CS) and Common-Gate (CG) stages to maximize the V_{DS} of each transistor, and therefore circuit performance above 100GHz, for a supply voltage of 1.2V. A series-connected 15pH inductor and 87fF capacitor between each CS and CG stage provide DC blocking, but together represent a short circuit at 140GHz. Capacitance at the center node is now tuned out with the parallel drain inductor of the CS stage and the source inductor of the CG stage. As opposed to the series inductor commonly used between the transistors in cascode stages, tuning with parallel inductors provides higher Q and hence higher gain, albeit lower

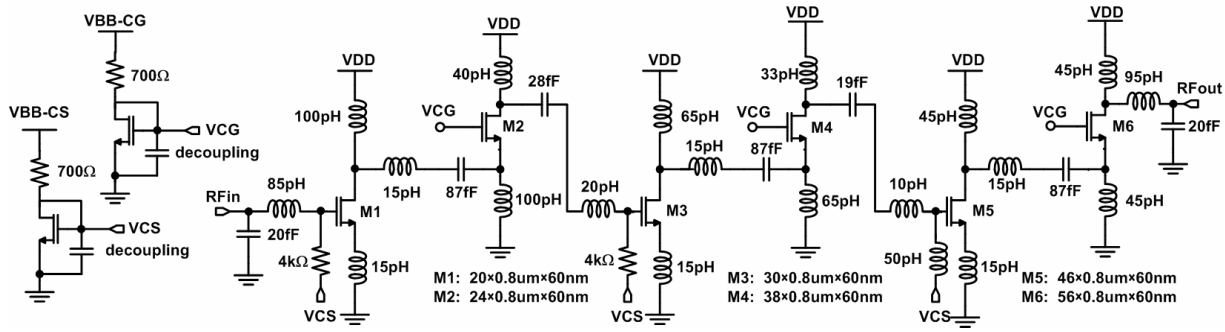

Fig. 3. 1.2V, 140GHz LNA schematic.

bandwidth. Inductors are modeled as lumped elements, implemented in 2µm wide top-metal, approximately 4.5µm above the substrate.

The gates of the first two CS stages (M1 and M3) are biased through 4kΩ resistors. The final CS stage (M5) uses an inductor instead which partially tunes out its gate capacitance. Decoupling of the common-gate node (VCG) and at the ends of all parallel inductors is provided by interdigitated MoM capacitors, not RF MiM capacitors, indicating that a pure digital CMOS process is usable at 140GHz. As shown in Fig. 4, decoupling capacitors must be placed directly beside the node they decouple to minimize parasitic inductance.

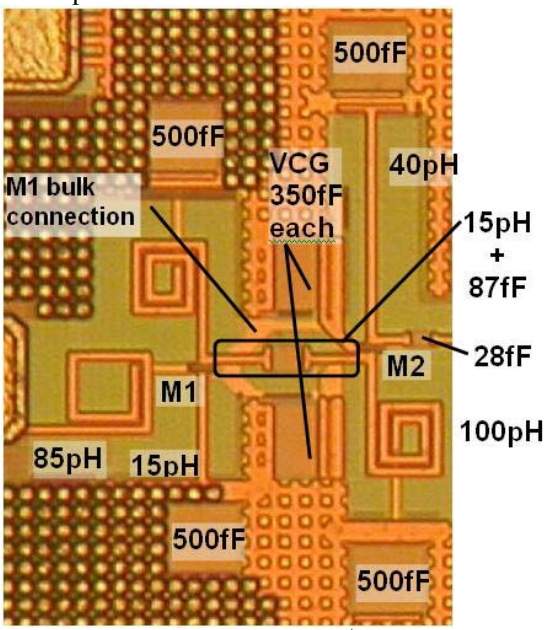

Fig. 4. Micro-photograph of the 1st two LNA stages.

The power amplifier is identical to the LNA, except that an additional common-source stage, illustrated in Fig. 5, is added to the output. High power amplifier stages are difficult to design at 140GHz because the small inductances required to resonate their large capacitances leave little design margin.

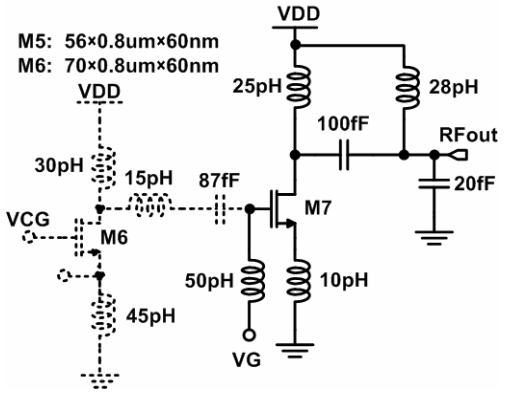

Fig. 5. 140GHz power amplifier output stage.

B. Down-conversion Mixer and IF Amplifier

The down-conversion mixer is illustrated in Fig. 6. A transformer is placed between the RF pair (M5-M6) and the mixing quad (M1-M4) to avoid stacking two transistors and the load resistor from 1.2V. The mixer transistors are biased at 0.15mA/µm for minimum noise figure, and the mixer consumes a total of 12mA.

The IF-amplifier contains 3 cascaded, resistively loaded, differential pair stages without inductive peaking, and provides 7dB gain into a 50Ω load, while consuming 24mA from a 1.2V supply.

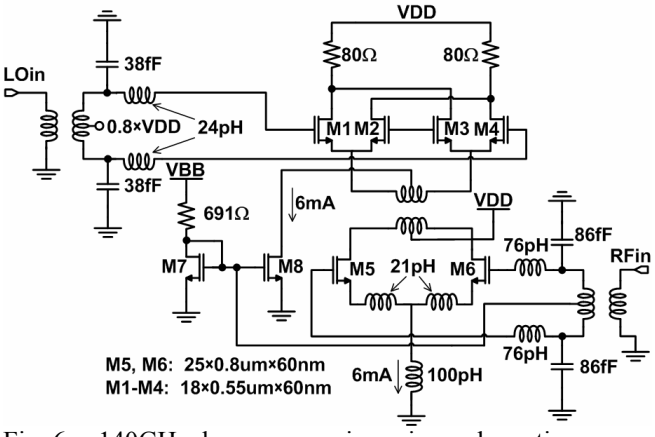

Fig. 6. 140GHz down-conversion mixer schematic.

II. Fabrication and Layout With On-Chip Antenna

All circuits were fabricated in STMicroelectronics 65nm general purpose CMOS process with f_T/f_{MAX} of 170/240GHz and digital back-end [6]. Fig. 7 shows a micro-photograph of the 140GHz receiver with on-chip antenna, which occupies 580µm × 700µm of die area.

The on-chip antenna, illustrated in Fig. 8, is a differential tapered slot design [7]. The antenna is coupled to the single-ended LNA through a transformer, and meets all metal density fill rules.

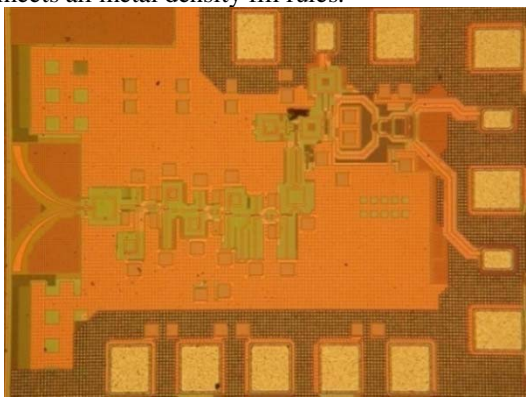

Fig. 7. Micro-photograph of the 140GHz receiver.

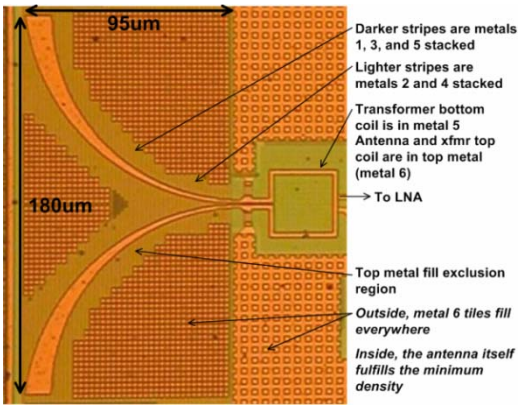

Fig. 8. Layout of the on-chip antenna.

III. Measurement Results

A. Low-Noise Amplifier and Power Amplifier

The gain of the LNA versus power supply is illustrated in Fig. 9, indicating that 8dB gain is achieved at 140GHz, with 10GHz bandwidth, 63mW power consumption, and 1.2 supply. At 1.0V supply, the gain is 5.5dB. Compared to simulations, the gain has shifted upward in frequency by 14GHz, or 10%. The simulated S_{22} is poor because the LNA output is designed to be matched to the mixer input, not to 50Ω. In contrast to the LNA, the power amplifier (containing an additional stage) has only 6dB gain at 140GHz and 1.2V supply, indicating that a common-gate output stage may have been a superior design choice. Five separate dies were measured and the peak gain was found to be in the 7.5 to 9dB range. The input and output return loss could not be measured above 94GHz due to lack of a network analyzer in this frequency range. Finally, the LNA gain versus temperature is illustrated in Fig. 10, showing 3dB gain even at 125°C.

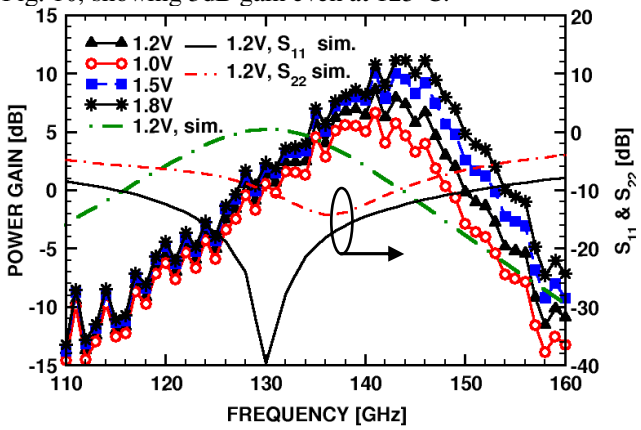

Fig. 9. LNA power gain versus supply voltage.

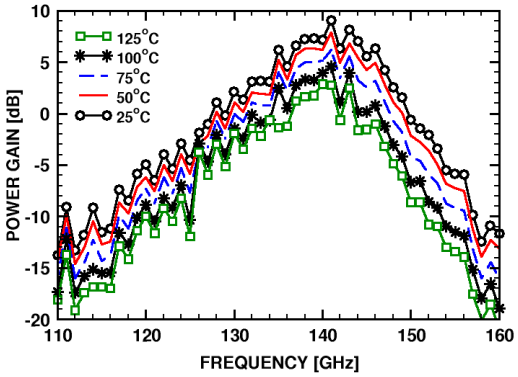

Fig. 10. LNA power gain versus temperature.

Illustrated in Fig. 11 is the 1dB compression point measurement of the LNA at 1.2V supply and 144GHz. The amplifier achieves an IP1dB of -12dBm, and P_{SAT} of at least -1.8dBm. In this measurement, the LNA is not fully saturated because the output power of the signal source used to drive the LNA is limited to -10dBm.

B. Down-conversion Mixer and Receiver

The conversion gain and NF of the down-conversion mixer were measured versus drain current density (J_D) in the transconductor pair, and are shown in Fig. 12 for 102GHz LO and 2GHz IF. Transformer coupling between the transconductor pair and mixing quad allows the mixing quad and the transconductor pair to be biased at the same current density independent of their sizes. The minimum NF is 22dB at J_D = 0.185mA/µm and the peak conversion gain is -4dB at J_D = 0.25mA/µm.

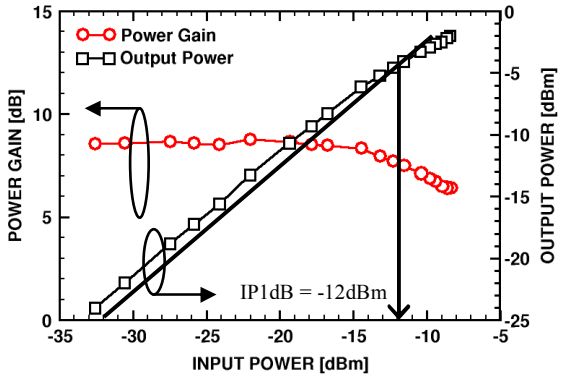

Fig. 11. LNA compression point and saturated output power measured at 144GHz.

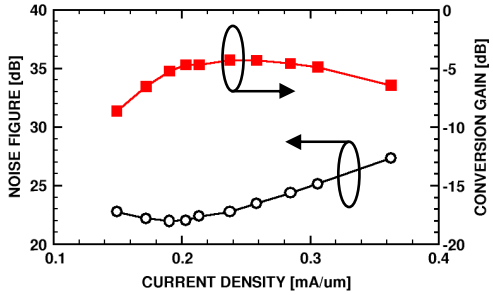

Fig. 12. Mixer noise figure and conversion gain versus current density for 102GHz LO.

The receiver conversion gain was measured on receivers with and without an on-chip antenna, using a 1.2V supply, and an external LO-signal of +1dBm (at the LO probe tip) at 102GHz as shown in Fig. 13. The conversion gain is expected to improve when a 140GHz LO is used, but could not be measured because a second 140GHz signal source was not available. Nonetheless, the conversion gain is comparable to that achieved in a 1st generation SiGe BiCMOS 160GHz receiver [4].

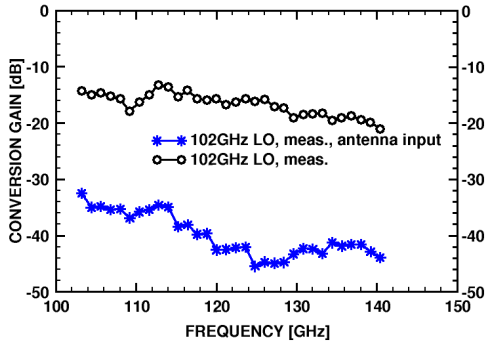

Fig. 13. Measured conversion gain of the 140GHz receivers with/without on-chip antenna.

The relative gain of the antenna was measured at 10mm height and a horizontal distance of 18mm (overall radial distance of 10λ), producing the radiation pattern illustrated in Fig. 14. The optimum elevation angle is 54°.

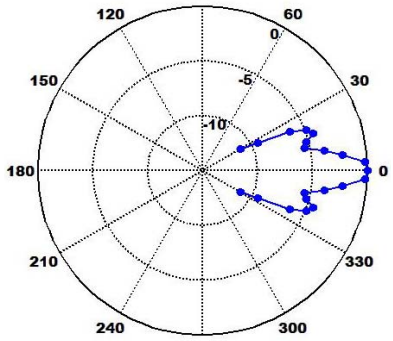

Fig. 14. Measured relative antenna pattern [dBr].

VII. Conclusion

Receivers at with and without on-chip antenna have been demonstrated in 65nm GP CMOS technology with digital back-end, consuming 100mW at 1.2V, and a 140GHz CMOS amplifier shows 8dB gain. The circuits use single-transistor stacking topologies to maximize performance at low supply voltage and at 140GHz. They pave the way for CMOS mm-wave radio beyond 100GHz.

Acknowledgement

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