Characterization and Modeling of an SiGe HBT Technology for Transceiver Applications in the 100–300-GHz Range

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***Abstract*—This paper describes a methodology for extracting and verifying the high-frequency model parameters of the HICUM L0 and L2 models of a silicon–germanium HBT from device and circuit measurements in the 110–325-GHz range. For the first time, the non-quasi-static effects, missing in the HICUM/L0 model, are found to be essential in accurately capturing the frequency dependence of the transistor maximum available power gain beyond the inflection frequency for unconditional stability. Furthermore, it is demonstrated that the optimal partitioning of the area and periphery components of the junction base–emitter, base–collector, and collector–substrate capacitances, and of the internal and external base and collector resistances can only be determined from S-parameter measurements beyond 200 GHz. The extracted models are validated on state-of-the-art linear and nonlinear circuits (amplifier, voltage-controlled oscillator (VCO), and VCO + divider chain) operating at frequencies as high as 240 GHz.**

***Index Terms*—Amplifier, D-band, device modeling, divider, G-band, H-band, heterojunction bipolar transistors (HBTs), HICUM, prescaler, silicon-germanium (SiGe), voltage-controlled oscillator (VCO).**

I. Introduction

A new generation of silicon–germanium (SiGe) heterojunction bipolar transistors (HBTs) with f_T/f_{MAX} of 300/400 GHz and thick metal back-end makes it possible to design highly integrated low-power transceivers with on-die antennas operating in the 100–300-GHz range [1]. The availability of an HBT compact model, accurate throughout the millimeter-wave range up to 300 GHz, is essential for the development of new millimeter-wave integrated circuit (IC) and system-on-chip (SoC) products. For a variety of reasons, until now, the accuracy of HBT compact models has not been verified at frequencies above 170 GHz [2]. The most difficult challenges facing compact modeling of SiGe and InP HBTs in the D-band (110–170 GHz), G-band (140–220 GHz) and H-band (220–325 GHz) are: 1) on-wafer S-parameter measurement and de-embedding uncertainty above 110 GHz [2] and 2) the validity of the small-signal equivalent circuit (Fig. 1) at frequencies beyond 110 GHz. From the point of view of small-signal behavior, each diode in Fig. 1 represents a bias-dependent capacitance in parallel with a bias-dependent junction resistance. All three junctions (base–emitter, base–collector, and collector–substrate) are described by area (subscript i) and periphery (subscript p) components. The collector resistance is broken into internal (R_{CI}) and external (R_{CX}) components, and non-quasi-static (NQS) effects are described by the capacitor $C_{r\mathrm{Bi}}$ across the internal base resistance R_{BIO}, and by the transconductance delay t_n.

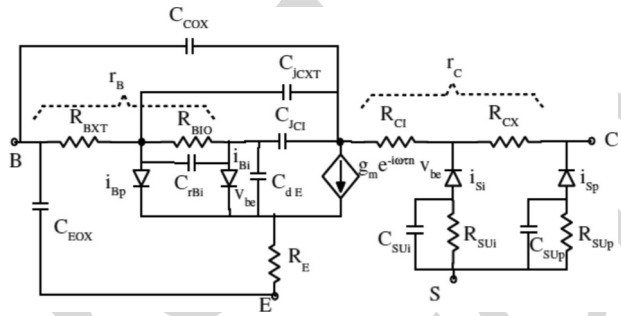

Fig. 1. HBT small-signal equivalent circuit required at the upper millimeter-wave frequencies.

In order to accurately model these devices, de-embedded S-parameter data must be acquired and extraction procedures for HBT model parameters must be validated in the same range of very high frequencies. Because inductances of a few picohenrys can have a sizable impact at 200 GHz, the accurate evaluation and de-embedding of the parasitic elements of the wiring stack surrounding the intrinsic device has become very important [2].

One of the most successful compact models for bipolar transistors is the HICUM model. In its most complex Level2 (L2) version, this model addresses high current, NQS, self-heating, and avalanche breakdown, but currently lacks a transconductance delay parameter and the internal collector resistance RCI. In the last few years, a new HICUM/L0 model has

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been developed [3]. Compared to L2, the HICUM/L0 version employs a simpler lumped element equivalent circuit, ignores NQS effects, and a simplified set of equations. Although the HICUM/L0 model presents some deficiencies in describing the HBT at very high current injection beyond two times the peak-f_T current density, J_{pfT}, that region is rarely used in circuit design. As a result, HICUM/L0 is expected to provide adequate accuracy, including self-heating, while requiring a significantly reduced set of model parameters and simulation time. One of the goals of this paper is to confirm or invalidate this expectation.

After an experimental investigation of the best calibration and de-embedding methods for on-wafer silicon transistor measurements up to 325 GHz, this paper presents a single-transistor extraction methodology of the HICUM/L0 model for an experimental SiGe HBT process with 280/400 GHz f_T/f_{MAX}. The accuracy of the L0 model is contrasted with that of the HICUM/L2 version at the transistor and circuit level and is found to be lacking at frequencies beyond 100 GHz. It is believed that this marks the first time that a semiconductor device model was verified at D-, G-, and H-band, demonstrating good agreement between measurements and simulations.

II. Calibration and De-Embedding up to 325 GHz

Calibration and de-embedding are critical and necessary steps to achieve precise on-wafer S-parameter measurements. If the test structures are carefully designed [2], both LRRM and TRL first-tier calibrations, followed by either transmission-line or OPEN-SHORT de-embedding, have recently been shown to provide "device modeling grade" S-parameters for silicon devices from dc to 170 GHz [2]. However, the suitability of these techniques beyond 170 GHz has not yet been established.

Figs. 2 and 3 illustrate the measured characteristic impedance and effective permittivity and attenuation, respectively, for a 3.2-mm long nominally 50-W coplanar-waveguide transmission line fabricated on a commercial alumina impedance standard substrate (ISS) obtained after line-reflect-reflect-match (LRRM) and thru-reflect-line (TRL) calibrations on the same ISS. Remarkably, throughout the H-band, the permittivity and attenuation are identical for the two calibration methods. A difference of less than 2% appears between the characteristic impedance values and can be attributed to the fact that, in the TRL calibration, the absolute value of the line impedance is unknown until corrected based on some reference impedance, e.g., the laser-trimmed 50-W load on the ISS used in the LRRM calibration. An important observation that can be made from Fig. 3 is that the attenuation of the transmission line on the commercial alumina ISS increases from 2.1 dB/mm at 220 GHz to 5 dB/mm at 325 GHz. These values are comparable to those measured on microstrip lines fabricated in the silicon back-end-of-line (BEOL). They suggest that the use of microstrip matching networks should be avoided in G- and H-band circuits.

Since the S-parameters measurements collected with an LRRM calibration require no further correction, the following calibration and de-embedding procedures were applied throughout the rest of the paper.

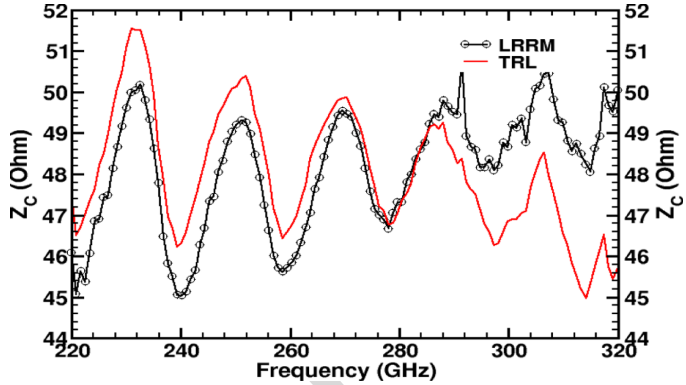

Fig. 2. Characteristic impedance of a 3.2-mm-long coplanar lines on the commercial alumina ISS: TRL versus LRRM calibration.

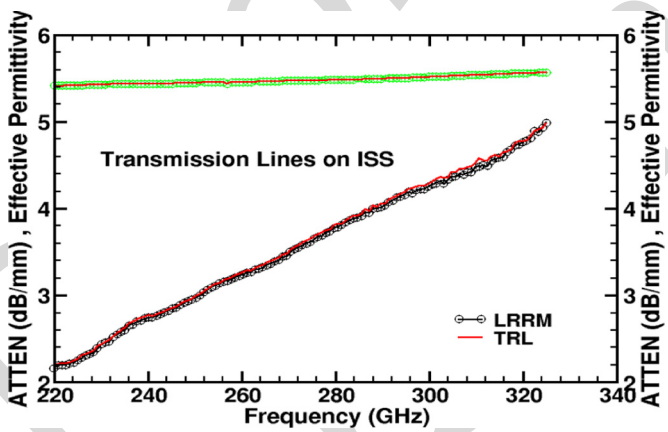

Fig. 3. Loss and effective permittivity of alumina coplanar lines on ISS: LRRM versus TRL calibration.

First, an LRRM calibration is performed on the commercial ISS. Next, a transmission-line de-embedding step [4], using microstrip lines fabricated on the silicon wafer, is applied to remove the pad and interconnect parasitics up to the device edge in metal 6 (M6 is the uppermost metal in the back-end). This leaves in place all the wiring stack above the device, up to M6. Optionally, a subsequent OPEN-SHORT de-embedding step is finally applied using a local M6-M2 OPEN and a local SHORT from M6 to ground to remove the impact of the wiring stack on top of the HBT between M6 and M2. M1 is not de-embedded. Full-color cross sections of the BEOL and 3-D layout views of the wiring stack on the transistor test structures and of the OPEN and SHORT de-embedding dummy structures can be found in [2]. Although the SiGe HBTs described in this paper are from a faster process run than those in [2], the BEOL, transistor test structure layout, and de-embedding structures are identical.

This two-step de-embedding technique allows to accurately predict the performance of the fully wired HBT, as well as to remove the metal stack down to and including M2, as needed for device modeling purposes. The contribution of the M2–M6 metals and vias is thus precisely quantified in an effort to understand the need for L–R–C extraction at the device level in future D-, G, and H-band circuits.

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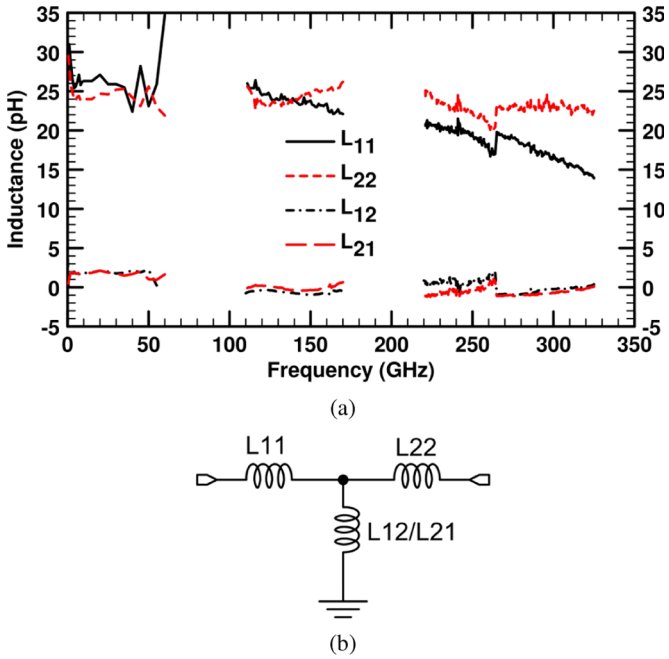


Fig. 4. (a) Measured input/output and ground inductance of the on-wafer global SHORT dummy. (b) Equivalent circuit of the SHORT dummy showing only the inductive parasitics.

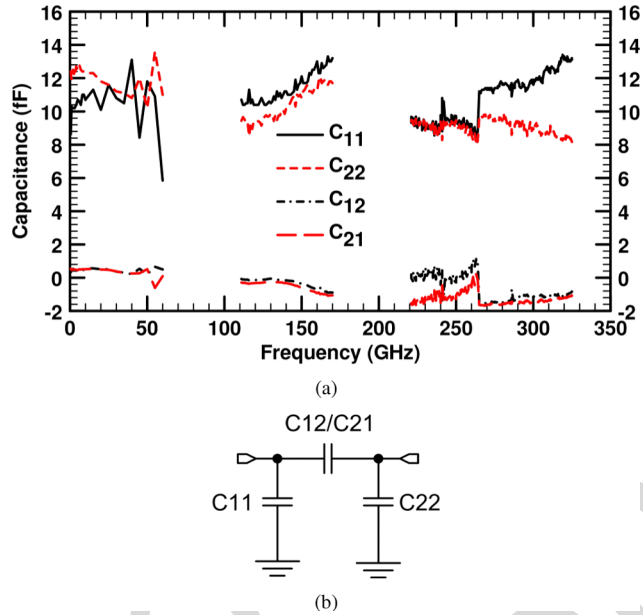


Fig. 5. Measured input/output and coupling capacitance of the on-wafer global OPEN dummy. (b) Equivalent circuit of the OPEN dummy showing only the capacitive parasitics.

for device modeling purposes. The contribution of the M2–M6 metals and vias is thus precisely quantified in an effort to understand the need for *L–R–C* extraction at the device level in future *D*-, *G*-, and *H*-band circuits.

An alternate de-embedding approach, where the LRRM calibration on the ISSS is followed by a conventional OPEN-SHORT de-embedding was also investigated. For the remainder of this paper, we will call this technique: global OPEN-SHORT de-embedding to distinguish it from the t-line de-embedding followed by local OPEN-SHORT de-embedding. The global OPEN and global SHORT both include the pad and the interconnect from the pads to the device down to metal 6 and metal 2, respectively [2]. Fig. 4 reproduces the measured inductive parasitics (from the measured Z-parameters) of the global SHORT dummy fabricated in the silicon BEOL. The extracted ground inductance ($L_{12} = \mathrm{Im}\{Z_{12}\}/\omega$) of only 1 pH remains practically constant throughout the D-band, while the interconnect leading to the device from the input ($L_{11} = \mathrm{Im}\{Z_{11}\text{-}Z_{12}\}/\omega$) and output ($L_{22} = \mathrm{Im}\{Z_{22}\text{-}Z_{12}\}/\omega$) pads has inductance values of approximately 20 and 24 pH, respectively. Similarly, Fig. 5 shows the measured capacitances of the global OPEN standard extracted from the measured Y-parameters where $C_{11} = \mathrm{Im}\{Y_{11} + Y_{12}\}/\omega$), $C_{12} = \mathrm{Im}\{-Y_{12}\}/\omega$), $C_{21} = \mathrm{Im}\{-Y_{21}\}/\omega$), and $C_{22} = \mathrm{Im}\{Y_{22} + Y_{12}\}/\omega$).

The impact of 5 pH of base and collector inductances and of a 0.5-pH inductance placed between the emitter and ground on maximum available power gain (MAG) and H_{21} is simulated in Fig. 6. As can be seen, the inductance of the wiring stack increases H_{21} and f_T by up to 10% at very high frequencies while MAG remains practically unchanged.

The simulations are confirmed by the experimental data in Fig. 7. The measured $H_{21}(f)$ and $\mathrm{MAG}(f)$ characteristics are

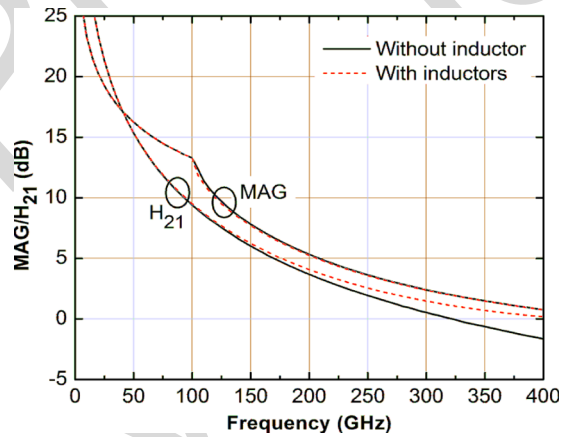
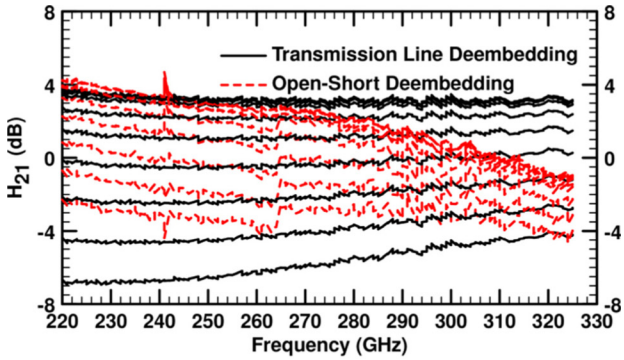
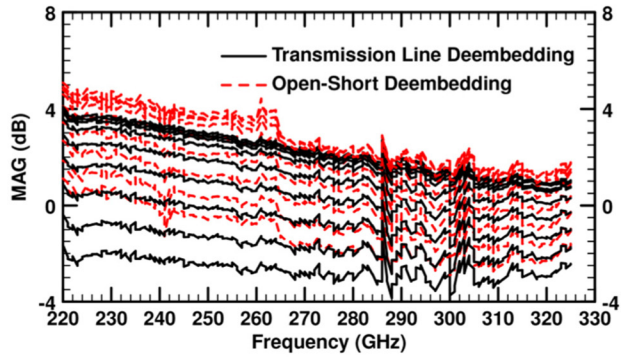


Fig. 6. Simulated impact of series base, collector, and emitter inductors de-embedding on MAG and H_{21}.

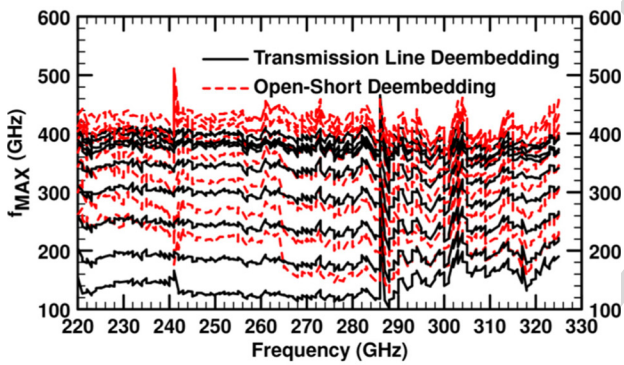
shown for several bias points of the HBT at $V_{\mathrm{CE}} = 1.2$ V, and V_{BE} varying in 15 mV steps from 750 to 960 mV. The global OPEN-SHORT de-embedding method [2] removes the pads, interconnect between pads, and the device, as well as the inductance associated with the wiring stack above the HBT between Metal #6 and Metal #2. The Global SHORT standard includes all the vias on the collector and base terminals of the HBT from Metal #6 down to Metal #2, with Metal #2 and Metal #1 shunted together everywhere to form a low-resistance low-inductance ground plane. Transmission-line de-embedding removes the interconnect between the pads and the device only up to the edge of the device and leaves the inductance of the entire wiring stack from Metal #1 to Metal #6 in place above the HBT [2], leading to a flattening out of the $H_{21}(f)$ characteristics at frequencies beyond 250 GHz [see Fig. 7(a)]. In contrast, the slope of the $\mathrm{MAG}(f)$ characteristics does not change with the de-embedding method [see Fig. 7(b)]. Moreover, because it removes the



(a)



(b)



(c)

Fig. 7. Measured impact of global OPEN-SHORT (dashed red lines in online version) versus t-line de-embedding (solid black lines) to metal 6 on: (a) H_{21} at H-band. (b) $\mathrm{MAG}(f)$, and (c) H-band measured $f\mathrm{MAX}(f)$, extrapolated with a 20-dB/decade slope from $U(f)$ at every frequency point. The 120 nm $\times$ 4.5 mm HBT is biased at $V_{\mathrm{CE}} = 1.2$ V, $V_{\mathrm{BE}} = 750$ mV to 960 mV in 15-mV steps.

inductance and resistance of the interconnect on top of the device, global OPEN-SHORT de-embedding leads to lower f_T and larger $\mathrm{MAG}(f)$, $U(f)$ and f_{MAX} [see Fig. 7(c)] than t-line de-embedding up to the edge of the device.

III. Single-Transistor HICUM LO Extraction Strategy

To minimize the interdependency of the extracted parameters, the following step-by-step parameter-extraction sequence was applied:

1) junction capacitances and substrate network;
2) parasitic resistances: R_E, R_{CX}, R_{BX}, R_{BIO};
3) low and moderate dc currents and breakdown parameters;
4) transit time parameters;
5) critical currents;

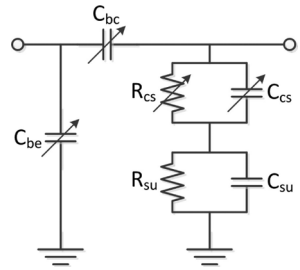


Fig. 8. "Cold" HBT small-signal equivalent circuit showing bias-dependent capacitances and collector–substrate network.

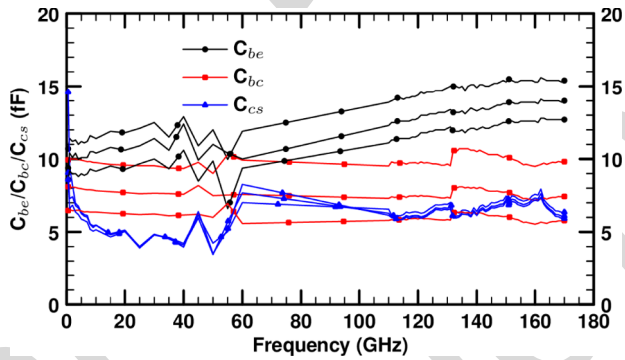


Fig. 9. Extraction of the bias-dependent C_{be}, C_{bc}, and C_{cs} for a 120 nm $\times$ 4.5 mm CBEBC SiGe HBT from cold HBT Y-parameters. For 0 V, and $+/-0.5$ V junction bias conditions (measurements: University of Toronto, Toronto, ON, Canada).

6) transit time parameters at high injection;
7) thermal resistance;
8) high injection current parameters.

The extraction methodology was first tested on simulated data generated using the HICUM/L0 model. Next the HICUM/L0 parameters of a 120 nm $\times$ 4.5 μm CBEBC SiGe HBT were extracted from dc and S-parameter measurements in the 0.1–60- and 110–170-GHz frequency range. Later, measurements in the 220–325-GHz range were employed to fine tune the splitting of the base resistance and of the junction capacitances in area and periphery components to better match $\mathrm{MAG}(f)$, $U(f)$, and the Y-parameters as a function of frequency up to 325 GHz. Version 1.2 of the HICUM/L0 model and HSPICE were used in all simulations.

A. Junction Capacitances and Substrate Network

These were extracted under "cold" ($V_{\mathrm{BE}}, V_{\mathrm{BC}}, V_{\mathrm{SC}}, < 0.5\,\mathrm{V}$) bias conditions. Consequently, the small-signal equivalent circuit in Fig. 1 reduces to that shown in Fig. 8.

The base–emitter and base–collector capacitances were extracted from $\mathrm{Im}\{Y_{11}+Y_{12}\}/\omega$, $\mathrm{Im}\{-Y_{12}\}/\omega$, respectively. As can be seen from Fig. 9, either low-frequency or D-band data can be used, although C_{be} shows a slight increase with frequency in the D-band.

In contrast, because the substrate network consists of the R_{SU} and C_{SU} in parallel, connected in series with the collector–substrate diode, the collector–substrate capacitance, C_{cs}, and the components of the substrate network require both low- and high-frequency measurements. Fig. 10 shows that C_{cs} can be extrapolated from $\{-\mathrm{Im}[(Y_{22}+Y_{21})-1]\}-1/\omega$

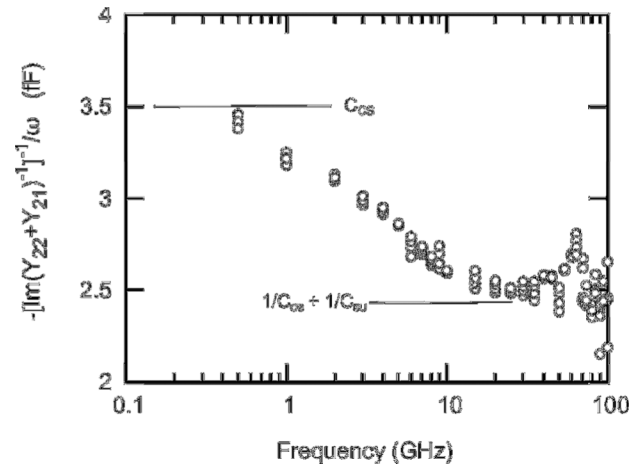


Fig. 10. Extraction of the collector–substrate capacitance and of $C_{\rm SU}$ from low- and high-frequency data for a 120 nm × 5 mm SiGe HBT (measurements using different test structures: STMicroelectronics, Crolles, France).

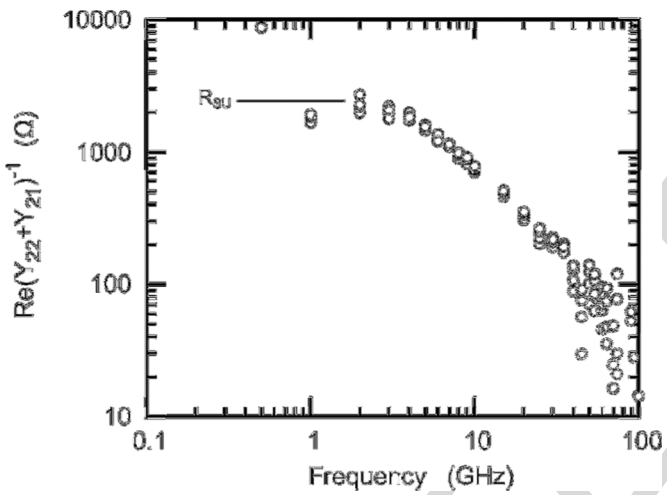


Fig. 11. Extraction of the substrate resistance from cold HBT Y-parameter for a 120 nm × 5 mm SiGe HBT (measurements: STMicroelectronics, Crolles, France).

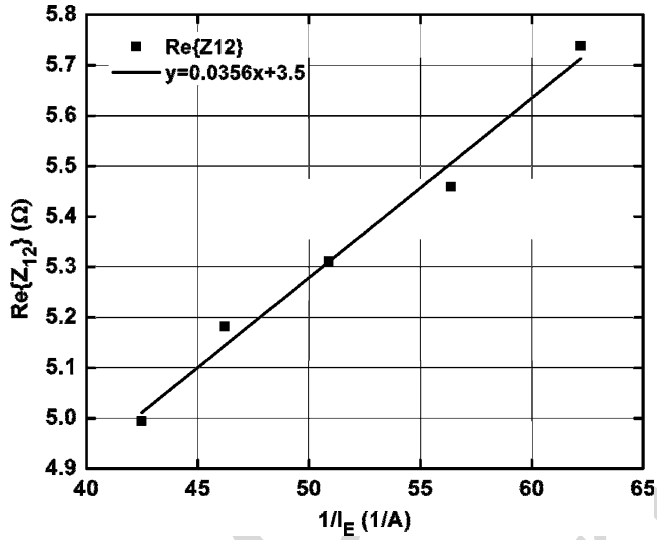


Fig. 12. Extrapolation of R_E extraction from Z_{12} under normal forward bias conditions and $V_{\rm CE}$-0.5 for a 120 nm × 4.5 mm CBEBC SiGe HBT.

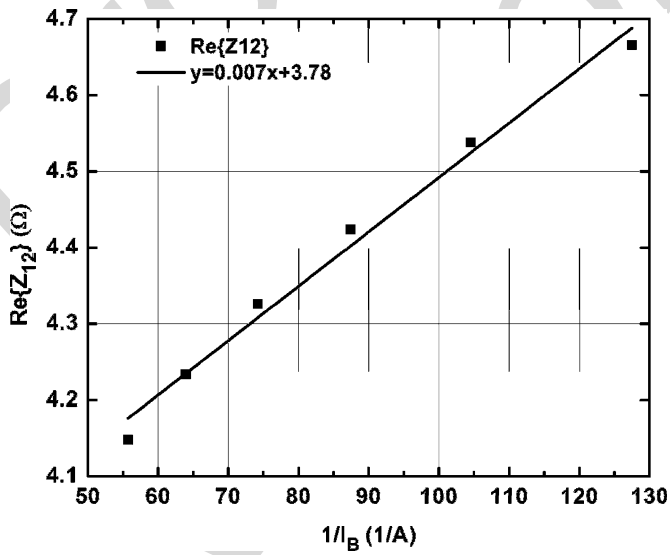


Fig. 13. Extrapolation of R_E using the Johansen method [5] in the saturation region at very large currents and $I_C = 0$ for a 120 nm × 4.5 mm CBEBC SiGe HBT.

at frequencies below 500 MHz. Once $C_{\rm cs}$ is known, $C_{\rm Su}$ can be obtained from the same plot at high enough frequencies, in the W- or D-bands, where the substrate network can be approximated by the series combination of $C_{\rm cs}$ and $C_{\rm SU}$.

Similarly, as illustrated in Fig. 11, the substrate resistance $R_{\rm SU}$ can be obtained from $\mathrm{Re}\{\{Y_{22}+Y_{12}\}^{-1}\}$ at low frequencies when the collector–substrate diode is biased at 0.5 V to minimize the contribution of $R_{\rm CS}$.

B. Junction Capacitances and Substrate Network

First, R_E is extracted from the intercept of $\mathrm{real}\{Z_{12}\}$ versus $1/I_C$ (Fig. 12) under typical forward bias conditions, either from low frequency or from D-band data, only at low VCE (0.5 V) to avoid self-heating effects [4]

$$\mathrm{R}(Z_{12}) = R_E + \frac{nKT}{qI_E}. \tag{1}$$

R_E was also obtained at large forward bias of the base–emitter junction with an open collector ($I_C = 0$) from $\mathrm{Re}(Z_{12})$ according to the Johansen method [5]. Again, either low-frequency or D-band Z-parameter data can be employed. The two values are within 10% (Fig. 13). Under the same bias conditions, $R_{\rm CX}$ was extrapolated from $\mathrm{Re}(Z_{22} - Z_{12})$ at low or high frequencies [5], as shown in Figs. 14 and 15.

Finally, Fig. 16 illustrates how the bias-independent part of $R_{\rm BX}$ is determined from $\mathrm{Re}(Z_{11} - Z_{12})$ at D-band under the same open collector bias condition as in the $R_{\rm CX}$ extraction [5]. A somewhat larger and bias-dependent $R_{\rm BX}$ value is obtained from $\mathrm{Re}(Z_{11}-Z_{12})$ at D-band under nominal forward bias conditions. $R_{\rm BIO}$ can be estimated from the same set of data at low current densities and low frequency. Aside from this strategy, $H_{11}(f)$ has been used to implement the so-called circle method (Fig. 17) [6], [7], which, along with fitting $\mathrm{MAG}(f)$, Mason's $U(f)$, and $Y12(f)$ at D- and G-bands, has helped in optimizing $R_{\rm BIO}$ and to fine tune the optimal splitting between $R_{\rm BX}$ and

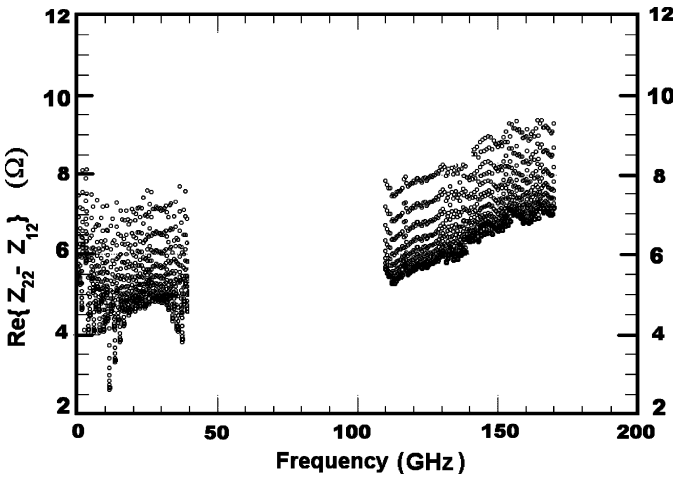


Fig. 14. Measured $\mathrm{Real}\{Z_{22} - Z_{12}\}$ versus frequency for R_{CX} extraction from the saturation region for a 120 nm × 4.5 mm CBEBC SiGe HBT.

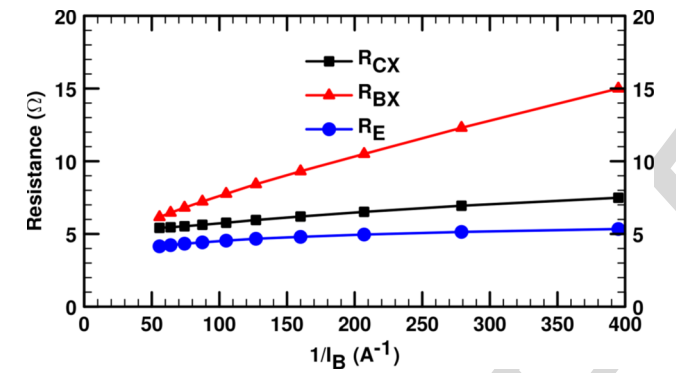


Fig. 15. R_{CX}, R_{BX}, and R_E extrapolation from Z-parameter data in the saturation region for a 120 nm × 4.5 mm CBEBC SiGe HBT.

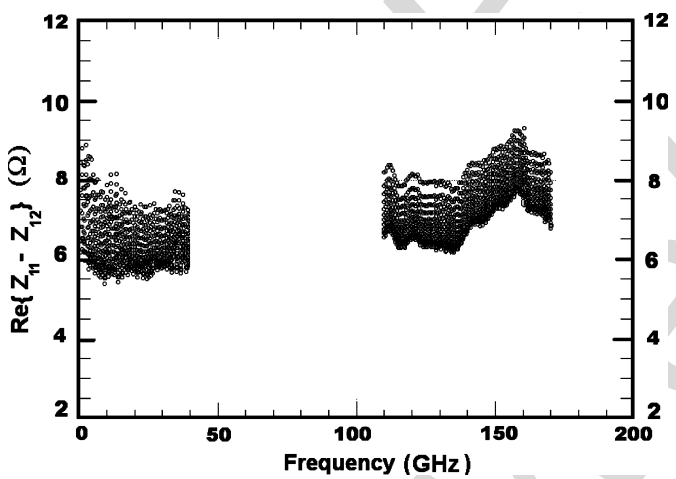


Fig. 16. $\mathrm{Real}\{Z_{11} - Z_{12}\}$ versus frequency for R_{BX} extraction from saturation region in a 120 nm × 4.5 mm CBEBC SiGe HBT.

R_{BIO}, C_{bci} and C_{bcxt}. This approach is necessary in the absence of tetrode test structures [8], [9], which were not available in this fabrication run.

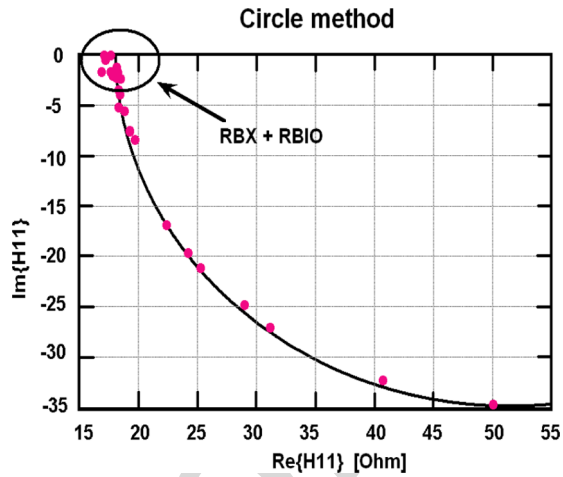


Fig. 17. Circle method employed for $R_{\mathrm{BX}} + R_{\mathrm{BIO}}$ extraction for 120 nm × 4.5 mm CBEBC HBT.

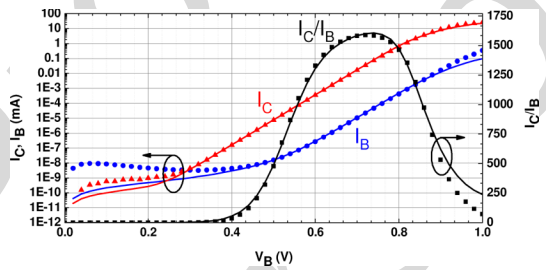


Fig. 18. Measured versus HICUM/L0 simulated Gummel characteristics for a 120 nm × 4.5 mm CBEBC SiGe HBT at $V_{\mathrm{BC}} = 0$.

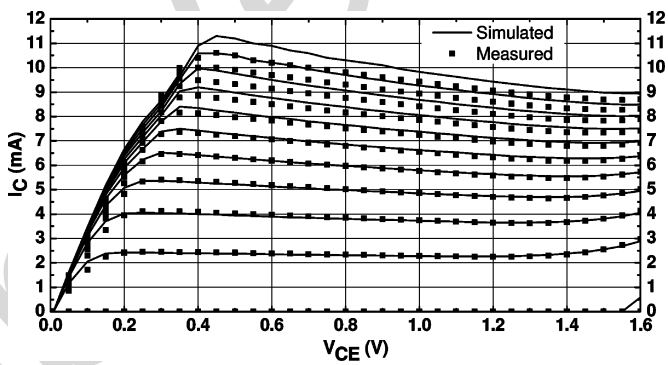


Fig. 19. Measured versus HICUM/L0 simulated output characteristics for a 120 nm × 4.5 mm CBEBC SiGe HBT.

C. Junction Capacitances and Substrate Network

The model parameters for the collector and base currents at low and medium injection levels, and the avalanche breakdown parameters, were extracted next (Fig. 18).

The thermal resistance was obtained from the relative change in V_{BE} in the output characteristics (Fig. 19) as a function of $I_C \times V_{\mathrm{CE}}$. Note the strong self-heating effect ($\Delta T \approx 50\,^{\circ}\mathrm{C}$) apparent in the negative slope of the output characteristics making the model parameter extraction particularly challenging.

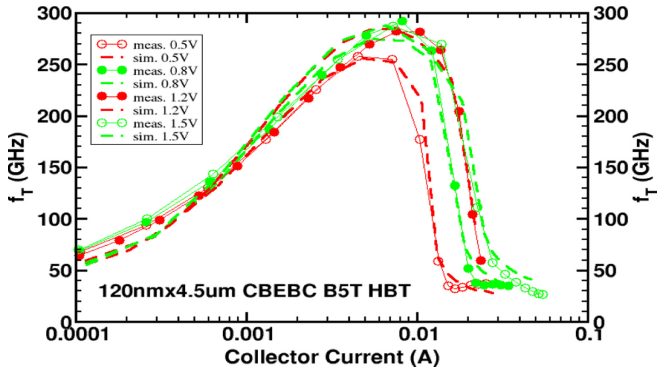


Fig. 20. Measured versus HICUM/L0 simulated $f_T(I_C)$ for a 120 nm × 4.5 mm CBEBC SiGe HBT biased at $V_{\rm CE} = 0.5$ V to 1.5 V.

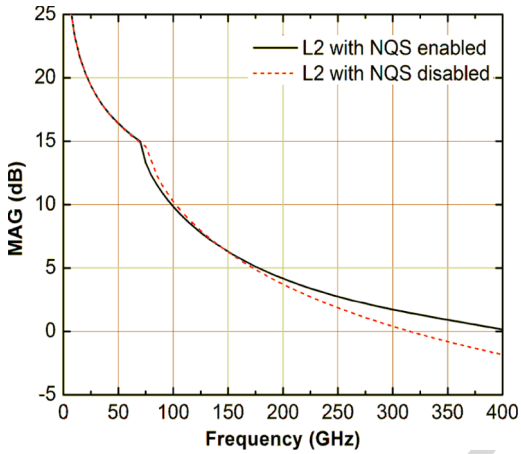


Fig. 21. Impact of NQS on $\mathrm{MAG}(f)$ characteristics using HICUM L2 for a 120 nm × 4.5 mm CBEBC SiGe HBT.

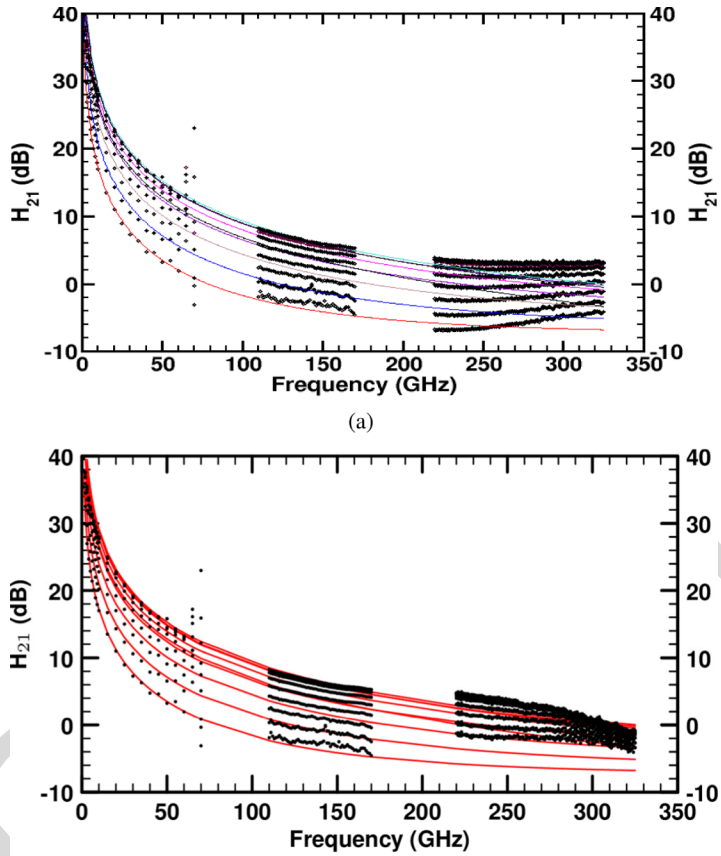


Fig. 22. Measured versus simulated $H_{21}(f)$ at $V_{\rm CE} = 1.2$ V, $V_{\rm BE} = 750$ mV to 960 mV in 15-mV steps: (a) using t-line de-embedding up to the edge of the device and (b) using global OPEN-SHORT de-embedding to metal 2.

D. Transit Time Parameters

Finally, the transit time and transfer current parameters at high injection were extracted from f_T versus I_C and f_T versus $V_{\rm CE}$ measured data and Gummel plot at large injection levels. H_{21} data conducted throughout the D-band were used to extrapolate f_T because the slope of H_{21} remains approximately constant at 20 dB/decade in this range. As can be seen in Fig. 20, it is relatively easy to obtain excellent agreement between the measured and simulated f_T versus I_C characteristics for $V_{\rm CE}$ values as low as 0.5 V and as high as 1.5 V (close to $\mathrm{BV_{CEO}}$).

Since the HICUM/L0 model has a simplified lumped equivalent circuit for the base–collector region, and since the exact geometrical dimensions of the internal and external base–collector regions are unknown, the accurate partition of the base–collector capacitance and base resistance was obtained by fine tuning $R_{\rm BX}$ and $R_{\rm BIO}$, while their sum was kept constant, to fit $\mathrm{Re}\{Y_{12}(f)\}$ as a function of bias and in the D-band, and by fitting $\mathrm{MAG}(f)$, $U(f)$ and $f_{\rm MAX}$. $U(f)$ and $\mathrm{MAG}(f)$, are particularly important when designing amplifiers, oscillators, and dividers at D- and G-band.

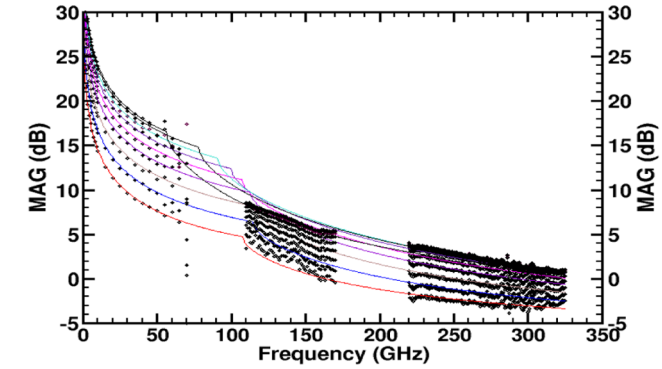
As can be seen from Fig. 21, even when using HICUM/L2, if NQS effects are ignored, the maximum available gain is overestimated immediately above the stability inflection point, and seriously underestimated above 150 GHz. This poses a rather formidable challenge to D-, G-, and H-band circuit design using the standard HICUM/L0 model.

IV. Transistor-Level Verification

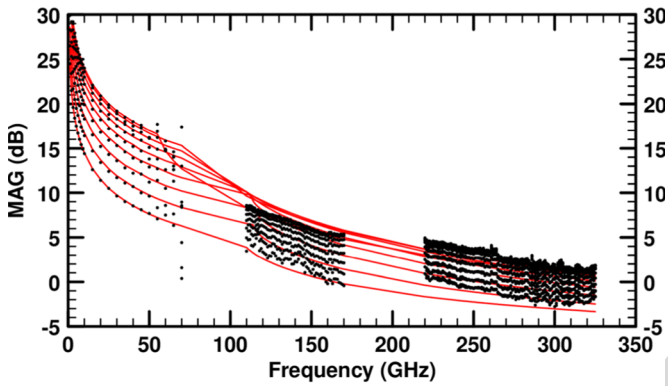
HICUM/L0 model parameters were extracted for HBTs with 120-nm emitter width and different emitter lengths (2, 3.75, 4.5, and 7.5 mm). In this section, a comparison of simulated and measured high-frequency characteristics are illustrated for a 120 nm × 4.5 mm HBT with one emitter stripe, two base, and two collector contacts.

Even when the HICUM/L0 was enhanced with a subcircuit similar to the one in Fig. 1, but without $C_{r\rm Bi}$ and t_n, it was difficult to compensate for the lack of NQS modeling to simultaneously match $\mathrm{MAG}(f)$, $H_{21}(f)$, and $U(f)$ from 110 to 325 GHz. However, by moving most of the junction capacitances to the periphery and by optimizing the $R_{\rm BIO}$-$R_{\rm BX}$ and $R_{\rm CIO}$-$R_{\rm CX}$ splits to compensate for the lack of an internal collector resistance, reasonable agreement could be obtained from dc to 170 GHz. This, however, proved inadequate to model circuits operating at 240 GHz. Instead, the HICUM/L2 model was employed for better device and circuit performance agreement between measurements and simulation.

Fig. 22 demonstrates the excellent agreement between the measured and HICUM/L2 simulated $H_{21}(f)$ characteristics up to the D-band, and even up to the G-band if global OPEN-SHORT de-embedding is employed to remove the inductance of the



(a)



(b)

Fig. 23. Measured versus simulated $\mathrm{MAG}(f)$ at $V_{\mathrm{CE}} = 1.2$ V, $V_{\mathrm{BE}} = 750$ mV to 960 mV in 15-mV steps: (a) using t-line de-embedding up to the edge of the device and (b) using global OPEN-SHORT de-embedding to metal 2.

wiring stack above the device. Similar agreement can be observed for $\mathrm{MAG}(f)$ in Fig. 23 and $S_{21}(f)$ characteristics in Fig. 24.

V. Validation on D- and G-Band Circuits

The single-transistor models, validated on small-signal transistor S-parameter measurements up to 325 GHz, were next used to fine-tune geometry-scalable HICUM/L2 and HICUM/L0 models. The latter were employed to confirm the measured performance of linear and nonlinear circuits in the 140–240-GHz range. It is important to note that these benchmark circuits employ different transistor sizes than those measured for parameter extraction.

A. 240-GHz Amplifier

A three-stage cascode amplifier, whose schematic is shown in Fig. 25, was designed using a preliminary model based on device simulation. To ensure the stability of the cascode stages in the presence of the unavoidable inductance associated with the bias-decoupling capacitor, feedback resistors were connected between the base and the collector of the common base HBTs [11]. All stages are biased at the peak f_T current density of 14 mA/mm^2 for a total power consumption is 34 mW from a 2.5-V supply. The die photograph of the amplifier is reproduced in Fig. 26.

The input, output, and interstage matching networks were implemented with coupled line impedance transformers [12] since the simple shunt L- series C matching networks in this

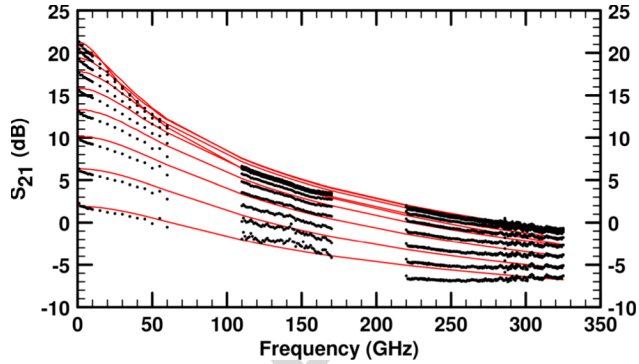


Fig. 24. Measured versus simulated $S_{21}(f)$ at $V_{\mathrm{CE}} = 1.2$ V, $V_{\mathrm{BE}} = 750$ mV to 960 mV in 15-mV steps.

frequency range would require very small capacitors. The coupled microstrip lines were formed in the top, 3-mm-thick copper layer with the bottom three metals shunted together to form the ground plane. The measured loss of a 50-W microstrip line, with identical cross section and ground plane to the one used in the coupled lines, varies between 2.5–3 dB/mm from 220 to 270 GHz. A large proportion of the power gain of the cascode is therefore lost on the coupled transmission-line network. In retrospect, as in SiGe HBT D-band amplifiers [13] and in recent 300-GHz SiGe HBT signal sources [14] fabricated in the same back-end, matching networks with transformers and inductors may prove less lossy than coupled line matching networks. This aspect needs to be systematically investigated.

Fig. 27 compares the measured with the simulated S-parameters using the HICUML2 model and the HICUML0 model, which does not capture NQS effects. The inductance of the decoupling capacitor, in the 1–2-pH range, was found to have a significant impact on the simulated power gain. All passive elements, including larger areas of the amplifier layout, were simulated as multiports using the commercial electromagnetic (EM)-field simulator EMX.[1] These results demonstrate the importance of the NQS effects in predicted the gain of the amplifier at frequencies approaching the f_T and f_{MAX} of the transistor.

B. 150-GHz VCO and Prescaler

A breakout consisting of a fundamental Colpitts–Clapp VCO and a divide-by-16 prescaler was fabricated as the most critical blocks required in the phase-locked loop (PLL) of future fundamental 150- or 300-GHz harmonic transceivers. Their schematics are shown in Fig. 28 and are similar to those fabricated in an older production technology [1]. The only difference are the varactors in the VCO, which are realized from SiGe HBTs with short-circuited base–emitter junctions. At the input of the prescaler is a dynamic divider followed by three static divider stages, all operating from a nominal supply voltage of 1.5 V. The VCO-prescaler operates from 138 to 148 GHz, limited by the tuning range of the VCO. Its phase noise was measured throughout the band, at the divider output, and was found to vary from -80 to -81 dBc/Hz, at 1-MHz offset when accounting for the divider ratio (24 dB). The output

[1]Integrand Softw. Inc., Berkeley Heights, NJ. [Online]. Available: http://www.integrandsoftware.com/

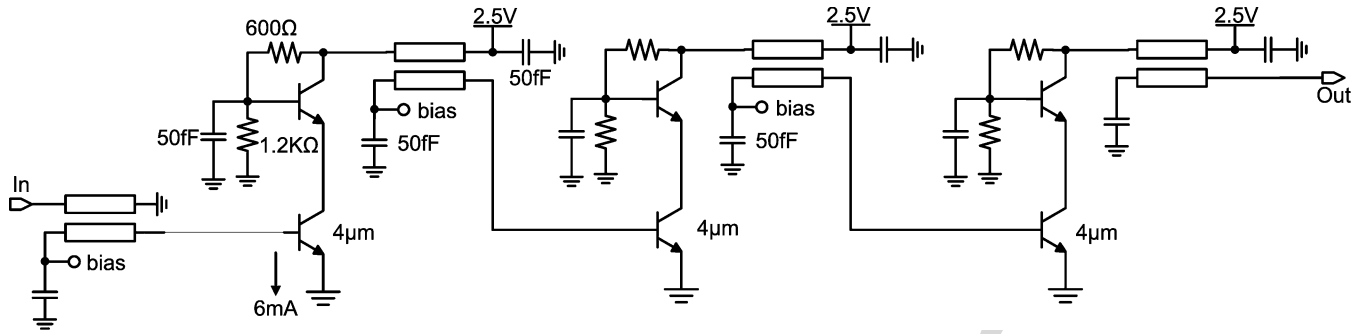


Fig. 25. Amplifier schematic.

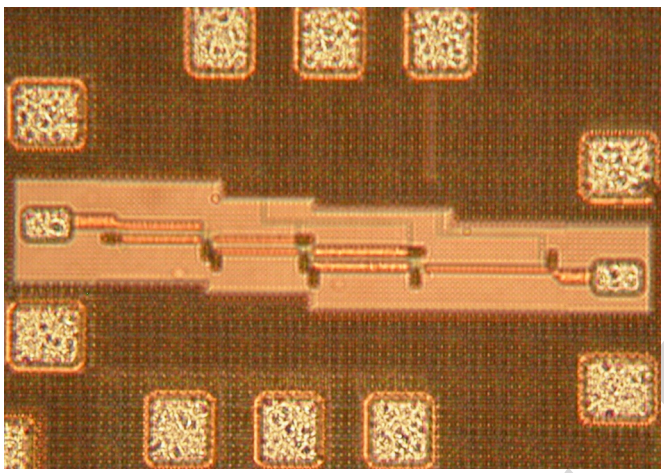


Fig. 26. Die photograph of the 240-GHz amplifier.

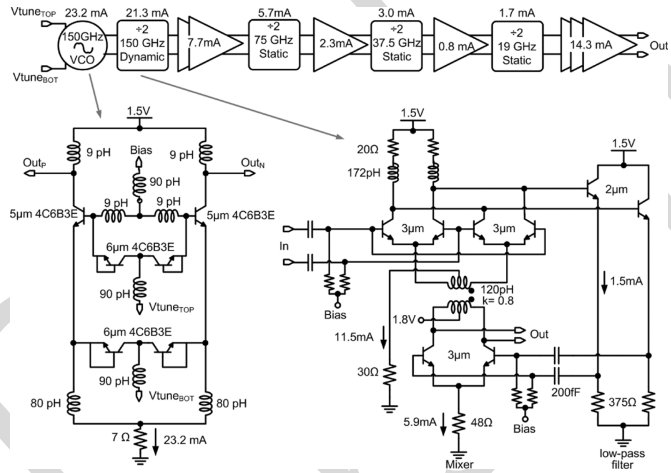


Fig. 28. VCO and prescaler schematics.

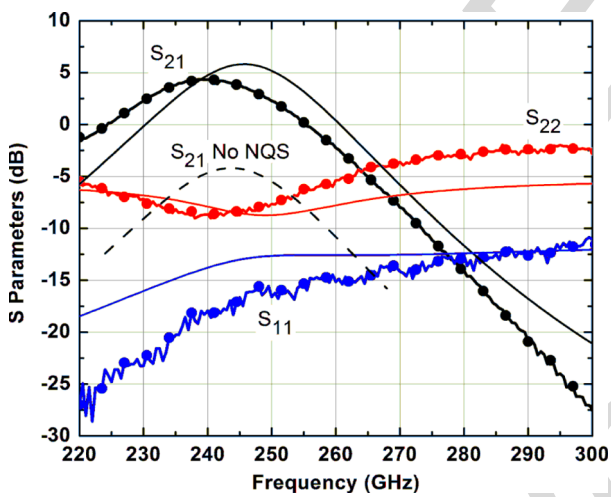


Fig. 27. Comparison of measured and simulated amplifier S-parameters.

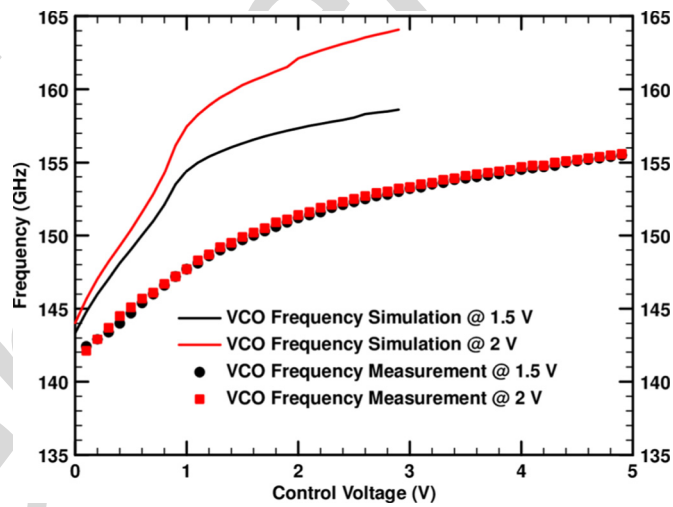


Fig. 29. Measured versus simulated VCO tuning range.

power of the standalone VCO breakout varies from −5 to −11 dBm in the 138–148-GHz tuning range. The prescaler was verified to divide correctly by 16 when the supply voltage was varied between 1.4–1.8 V. Similarly, the VCO oscillates for VCC values ranging from 1 to 2 V. The VCO core consumes 35 mW from 1.5 V, and the divider chain, without output buffers, draws 42.5 mA from 1.5 V. The VCO, prescaler, and buffers consume a total of 120 mW from a 1.5-V supply.

Fig. 29 illustrates the measured and HICUM/L2 simulated tuning characteristics of the standalone VCO at two supply voltages of 1.5 and 2 V, respectively. The agreement is better than 8%. However, for varactor control voltages larger than 3 V, the avalanche breakdown model causes convergence problems. The match between measurements and simulations could be further improved by optimizing the area and periphery junction capacitance parameters VD and Z. Note that in the measured tuning, characteristics are insensitive to the supply voltage, whereas the

simulation results show some VCO pulling. Finally, it should be noted that the simulations predicted a decrease of about 2 GHz in the VCO tuning frequency when the VCO was loaded by the divider chain. A larger decrease of about 4 GHz was observed in measurements.

Despite these promising results, unsolved problems remain regarding the accuracy of t-line and global OPEN-SHORT de-embedding in the H-band, and the ability of the HICUM model both L0 and L2 in predicting the correct frequency dependence of $\mathrm{Re}\{H_{11}(f)\}$ in the 5–50-GHz range.

VI. Conclusion

The HICUM L0 and L2 models were extracted for the first time from D-, G-, and H-band S-parameter measurements for a 400-GHz f_{MAX} SiGe HBT process. Good agreement between the measured and simulated transistor Z- and Y-parameters, H_{21}, and U, in the dc to 170-GHz range was demonstrated for the L0 model. However, when tested on circuits, the L0 model was found to underestimate the gain of a three-stage 240-GHz amplifier and the negative resistance of a 150-GHz VCO. It was only when measurements in the 220–325-GHz range were performed that the limitations of the L0 model in correctly predicting the NQS effects and the $\mathrm{MAG}(f)$ characteristics became apparent. In contrast, the HICUM/L2 model, including NQS effects and a more sophisticated distributed small-signal equivalent circuit appears to be adequate for circuit simulation up to 325 GHz. Its accuracy was validated on a 240-GHz three-stage cascode amplifier and on a low-power fundamental-frequency 120-mW 150-GHz VCO prescaler.

Acknowledgment

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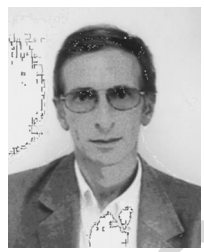

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Characterization and Modeling of an SiGe HBT Technology for Transceiver Applications in the 100–300-GHz Range

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***Abstract*—This paper describes a methodology for extracting and verifying the high-frequency model parameters of the HICUM L0 and L2 models of a silicon–germanium HBT from device and circuit measurements in the 110–325-GHz range. For the first time, the non-quasi-static effects, missing in the HICUM/L0 model, are found to be essential in accurately capturing the frequency dependence of the transistor maximum available power gain beyond the inflection frequency for unconditional stability. Furthermore, it is demonstrated that the optimal partitioning of the area and periphery components of the junction base–emitter, base–collector, and collector–substrate capacitances, and of the internal and external base and collector resistances can only be determined from S-parameter measurements beyond 200 GHz. The extracted models are validated on state-of-the-art linear and nonlinear circuits (amplifier, voltage-controlled oscillator (VCO), and VCO + divider chain) operating at frequencies as high as 240 GHz.**

***Index Terms*—Amplifier, D-band, device modeling, divider, G-band, H-band, heterojunction bipolar transistors (HBTs), HICUM, prescaler, silicon-germanium (SiGe), voltage-controlled oscillator (VCO).**

I. Introduction

A new generation of silicon–germanium (SiGe) heterojunction bipolar transistors (HBTs) with f_T/f_{MAX} of 300/400 GHz and thick metal back-end makes it possible to design highly integrated low-power transceivers with on-die antennas operating in the 100–300-GHz range [1]. The availability of an HBT compact model, accurate throughout the millimeter-wave range up to 300 GHz, is essential for the development of new millimeter-wave integrated circuit (IC) and system-on-chip (SoC) products. For a variety of reasons, until now, the accuracy of HBT compact models has not been verified at frequencies above 170 GHz [2]. The most difficult challenges facing compact modeling of SiGe and InP HBTs in the D-band (110–170 GHz), G-band (140–220 GHz) and H-band (220–325 GHz) are: 1) on-wafer S-parameter measurement and de-embedding uncertainty above 110 GHz [2] and 2) the validity of the small-signal equivalent circuit (Fig. 1) at frequencies beyond 110 GHz. From the point of view of small-signal behavior, each diode in Fig. 1 represents a bias-dependent capacitance in parallel with a bias-dependent junction resistance. All three junctions (base–emitter, base–collector, and collector–substrate) are described by area (subscript i) and periphery (subscript p) components. The collector resistance is broken into internal (R_{CI}) and external (R_{CX}) components, and non-quasi-static (NQS) effects are described by the capacitor $C_{r\mathrm{Bi}}$ across the internal base resistance R_{BIO}, and by the transconductance delay t_n.

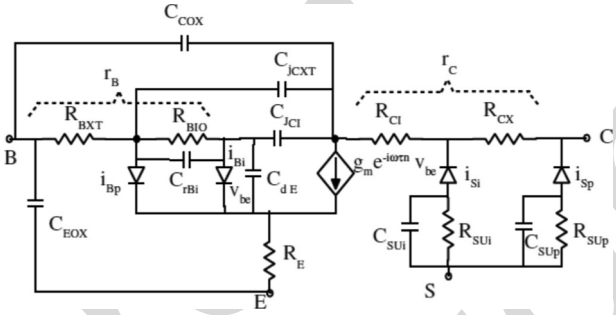

Fig. 1. HBT small-signal equivalent circuit required at the upper millimeter-wave frequencies.

In order to accurately model these devices, de-embedded S-parameter data must be acquired and extraction procedures for HBT model parameters must be validated in the same range of very high frequencies. Because inductances of a few picohenrys can have a sizable impact at 200 GHz, the accurate evaluation and de-embedding of the parasitic elements of the wiring stack surrounding the intrinsic device has become very important [2].

One of the most successful compact models for bipolar transistors is the HICUM model. In its most complex Level2 (L2) version, this model addresses high current, NQS, self-heating, and avalanche breakdown, but currently lacks a transconductance delay parameter and the internal collector resistance RCI. In the last few years, a new HICUM/L0 model has

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been developed [3]. Compared to L2, the HICUM/L0 version employs a simpler lumped element equivalent circuit, ignores NQS effects, and a simplified set of equations. Although the HICUM/L0 model presents some deficiencies in describing the HBT at very high current injection beyond two times the peak-f_T current density, J_{pfT}, that region is rarely used in circuit design. As a result, HICUM/L0 is expected to provide adequate accuracy, including self-heating, while requiring a significantly reduced set of model parameters and simulation time. One of the goals of this paper is to confirm or invalidate this expectation.

After an experimental investigation of the best calibration and de-embedding methods for on-wafer silicon transistor measurements up to 325 GHz, this paper presents a single-transistor extraction methodology of the HICUM/L0 model for an experimental SiGe HBT process with 280/400 GHz f_T/f_{MAX}. The accuracy of the L0 model is contrasted with that of the HICUM/L2 version at the transistor and circuit level and is found to be lacking at frequencies beyond 100 GHz. It is believed that this marks the first time that a semiconductor device model was verified at D-, G-, and H-band, demonstrating good agreement between measurements and simulations.

II. Calibration and De-Embedding up to 325 GHz

Calibration and de-embedding are critical and necessary steps to achieve precise on-wafer S-parameter measurements. If the test structures are carefully designed [2], both LRRM and TRL first-tier calibrations, followed by either transmission-line or OPEN-SHORT de-embedding, have recently been shown to provide "device modeling grade" S-parameters for silicon devices from dc to 170 GHz [2]. However, the suitability of these techniques beyond 170 GHz has not yet been established.

Figs. 2 and 3 illustrate the measured characteristic impedance and effective permittivity and attenuation, respectively, for a 3.2-mm long nominally 50-W coplanar-waveguide transmission line fabricated on a commercial alumina impedance standard substrate (ISS) obtained after line-reflect-reflect-match (LRRM) and thru-reflect-line (TRL) calibrations on the same ISS. Remarkably, throughout the H-band, the permittivity and attenuation are identical for the two calibration methods. A difference of less than 2% appears between the characteristic impedance values and can be attributed to the fact that, in the TRL calibration, the absolute value of the line impedance is unknown until corrected based on some reference impedance, e.g., the laser-trimmed 50-W load on the ISS used in the LRRM calibration. An important observation that can be made from Fig. 3 is that the attenuation of the transmission line on the commercial alumina ISS increases from 2.1 dB/mm at 220 GHz to 5 dB/mm at 325 GHz. These values are comparable to those measured on microstrip lines fabricated in the silicon back-end-of-line (BEOL). They suggest that the use of microstrip matching networks should be avoided in G- and H-band circuits.

Since the S-parameters measurements collected with an LRRM calibration require no further correction, the following calibration and de-embedding procedures were applied throughout the rest of the paper.

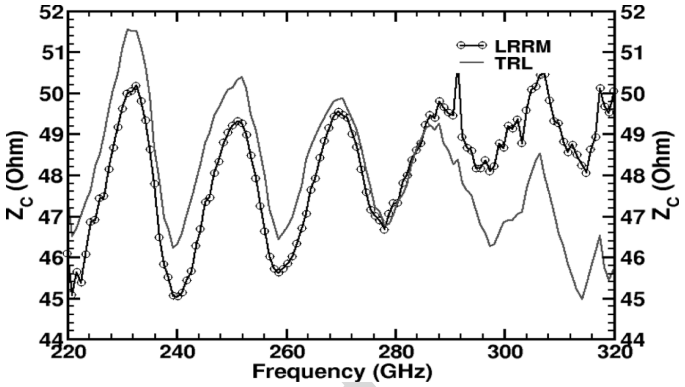


Fig. 2. Characteristic impedance of a 3.2-mm-long coplanar lines on the commercial alumina ISS: TRL versus LRRM calibration.

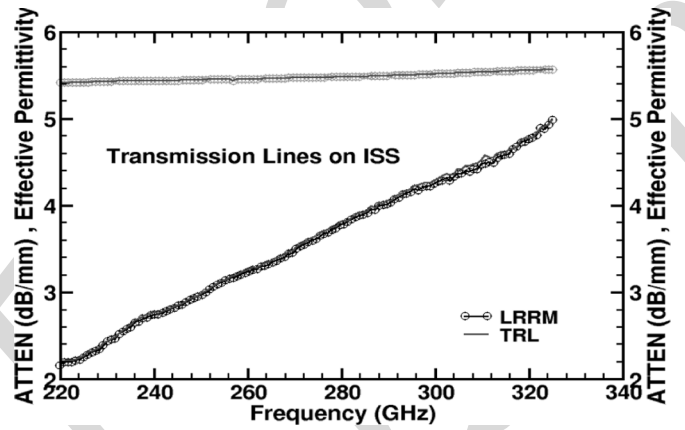


Fig. 3. Loss and effective permittivity of alumina coplanar lines on ISS: LRRM versus TRL calibration.

First, an LRRM calibration is performed on the commercial ISS. Next, a transmission-line de-embedding step [4], using microstrip lines fabricated on the silicon wafer, is applied to remove the pad and interconnect parasitics up to the device edge in metal 6 (M6 is the uppermost metal in the back-end). This leaves in place all the wiring stack above the device, up to M6. Optionally, a subsequent OPEN-SHORT de-embedding step is finally applied using a local M6-M2 OPEN and a local SHORT from M6 to ground to remove the impact of the wiring stack on top of the HBT between M6 and M2. M1 is not de-embedded. Full-color cross sections of the BEOL and 3-D layout views of the wiring stack on the transistor test structures and of the OPEN and SHORT de-embedding dummy structures can be found in [2]. Although the SiGe HBTs described in this paper are from a faster process run than those in [2], the BEOL, transistor test structure layout, and de-embedding structures are identical.

This two-step de-embedding technique allows to accurately predict the performance of the fully wired HBT, as well as to remove the metal stack down to and including M2, as needed for device modeling purposes. The contribution of the M2–M6 metals and vias is thus precisely quantified in an effort to understand the need for *L–R–C* extraction at the device level in future D-, G, and H-band circuits.

This two-step de-embedding technique allows to accurately predict the performance of the fully wired HBT, as well as to remove the metal stack down to and including M2, as needed

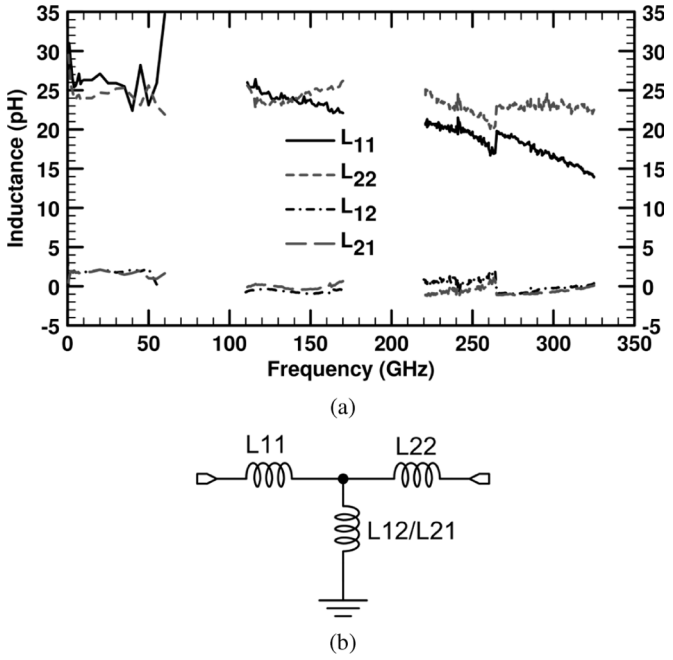


Fig. 4. (a) Measured input/output and ground inductance of the on-wafer global SHORT dummy. (b) Equivalent circuit of the SHORT dummy showing only the inductive parasitics.

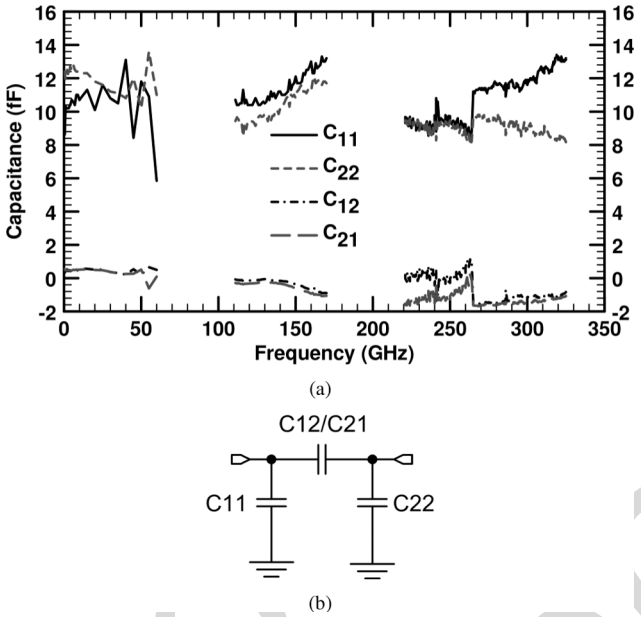


Fig. 5. Measured input/output and coupling capacitance of the on-wafer global OPEN dummy. (b) Equivalent circuit of the OPEN dummy showing only the capacitive parasitics.

for device modeling purposes. The contribution of the M2–M6 metals and vias is thus precisely quantified in an effort to understand the need for *L–R–C* extraction at the device level in future D-, G-, and H-band circuits.

An alternate de-embedding approach, where the LRRM calibration on the ISSS is followed by a conventional OPEN-SHORT de-embedding was also investigated. For the remainder of this paper, we will call this technique: global OPEN-SHORT de-embedding to distinguish it from the t-line de-embedding followed by local OPEN-SHORT de-embedding. The global OPEN and global SHORT both include the pad and the interconnect from the pads to the device down to metal 6 and metal 2, respectively [2]. Fig. 4 reproduces the measured inductive parasitics (from the measured Z-parameters) of the global SHORT dummy fabricated in the silicon BEOL. The extracted ground inductance ($L_{12} = \mathrm{Im}\{Z_{12}\}/\omega$) of only 1 pH remains practically constant throughout the D-band, while the interconnect leading to the device from the input ($L_{11} = \mathrm{Im}\{Z_{11}\text{-}Z_{12}\}/\omega$) and output ($L_{22} = \mathrm{Im}\{Z_{22}\text{-}Z_{12}\}/\omega$) pads has inductance values of approximately 20 and 24 pH, respectively. Similarly, Fig. 5 shows the measured capacitances of the global OPEN standard extracted from the measured Y-parameters where $C_{11} = \mathrm{Im}\{Y_{11} + Y_{12}\}/\omega$), $C_{12} = \mathrm{Im}\{-Y_{12}\}/\omega$), $C_{21} = \mathrm{Im}\{-Y_{21}\}/\omega$), and $C_{22} = \mathrm{Im}\{Y_{22} + Y_{12}\}/\omega$).

The impact of 5 pH of base and collector inductances and of a 0.5-pH inductance placed between the emitter and ground on maximum available power gain (MAG) and H_{21} is simulated in Fig. 6. As can be seen, the inductance of the wiring stack increases H_{21} and f_T by up to 10% at very high frequencies while MAG remains practically unchanged.

The simulations are confirmed by the experimental data in Fig. 7. The measured $H_{21}(f)$ and $\mathrm{MAG}(f)$ characteristics are

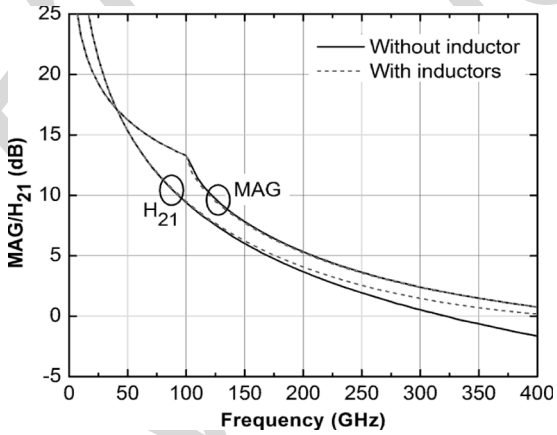


Fig. 6. Simulated impact of series base, collector, and emitter inductors de-embedding on MAG and H_{21}.

shown for several bias points of the HBT at $V_{\mathrm{CE}} = 1.2$ V, and V_{BE} varying in 15 mV steps from 750 to 960 mV. The global OPEN-SHORT de-embedding method [2] removes the pads, interconnect between pads, and the device, as well as the inductance associated with the wiring stack above the HBT between Metal #6 and Metal #2. The Global SHORT standard includes all the vias on the collector and base terminals of the HBT from Metal #6 down to Metal #2, with Metal #2 and Metal #1 shunted together everywhere to form a low-resistance low-inductance ground plane. Transmission-line de-embedding removes the interconnect between the pads and the device only up to the edge of the device and leaves the inductance of the entire wiring stack from Metal #1 to Metal #6 in place above the HBT [2], leading to a flattening out of the $H_{21}(f)$ characteristics at frequencies beyond 250 GHz [see Fig. 7(a)]. In contrast, the slope of the $\mathrm{MAG}(f)$ characteristics does not change with the de-embedding method [see Fig. 7(b)]. Moreover, because it removes the

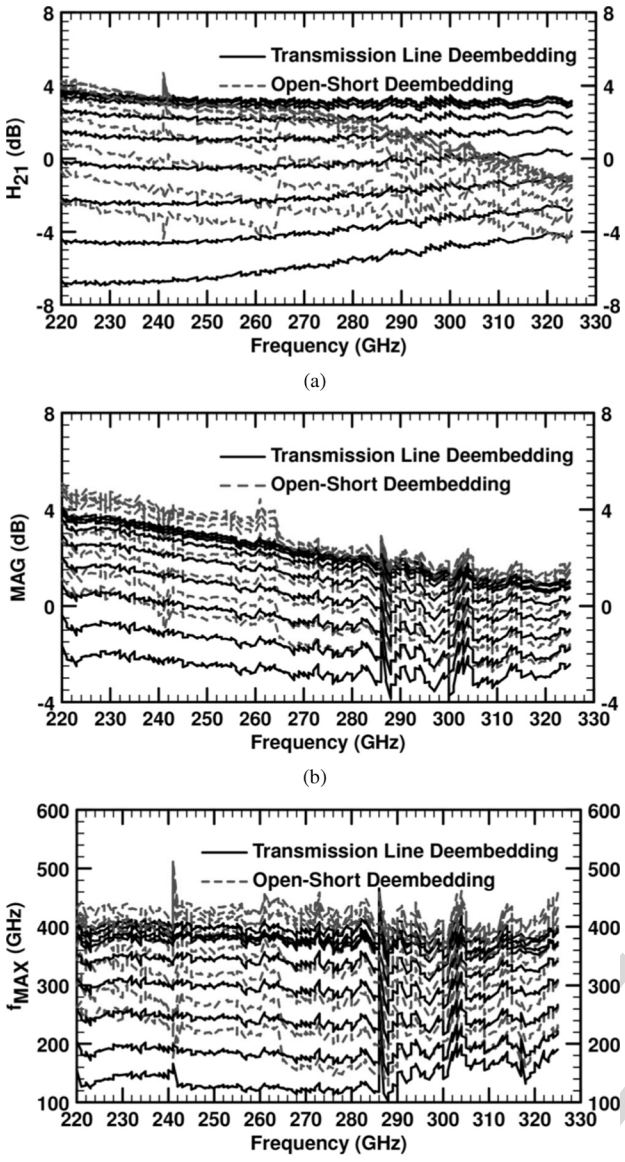


Fig. 7. Measured impact of global OPEN-SHORT (dashed red lines in online version) versus t-line de-embedding (solid black lines) to metal 6 on: (a) H_{21} at H-band. (b) $\mathrm{MAG}(f)$, and (c) H-band measured $f\mathrm{MAX}(f)$, extrapolated with a 20-dB/decade slope from $U(f)$ at every frequency point. The 120 nm $\times$ 4.5 mm HBT is biased at $V_{\mathrm{CE}} = 1.2$ V, $V_{\mathrm{BE}} = 750$ mV to 960 mV in 15-mV steps.

inductance and resistance of the interconnect on top of the device, global OPEN-SHORT de-embedding leads to lower f_T and larger $\mathrm{MAG}(f)$, $U(f)$ and f_{MAX} [see Fig. 7(c)] than t-line de-embedding up to the edge of the device.

III. SINGLE-TRANSISTOR HICUM LO EXTRACTION STRATEGY

To minimize the interdependency of the extracted parameters, the following step-by-step parameter-extraction sequence was applied:

1) junction capacitances and substrate network;
2) parasitic resistances: R_E, R_{CX}, R_{BX}, R_{BIO};
3) low and moderate dc currents and breakdown parameters;
4) transit time parameters;
5) critical currents;

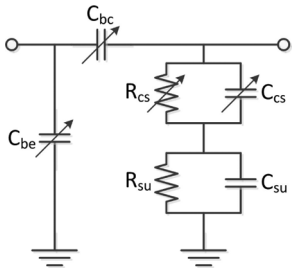


Fig. 8. "Cold" HBT small-signal equivalent circuit showing bias-dependent capacitances and collector–substrate network.

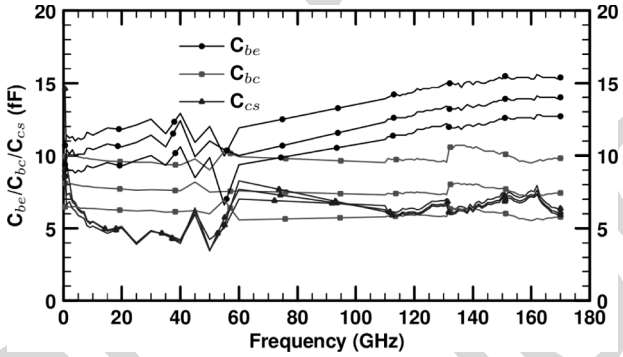


Fig. 9. Extraction of the bias-dependent C_{be}, C_{bc}, and C_{cs} for a 120 nm $\times$ 4.5 mm CBEBC SiGe HBT from cold HBT Y-parameters. For 0 V, and $+/-0.5$ V junction bias conditions (measurements: University of Toronto, Toronto, ON, Canada).

6) transit time parameters at high injection;
7) thermal resistance;
8) high injection current parameters.

The extraction methodology was first tested on simulated data generated using the HICUM/L0 model. Next the HICUM/L0 parameters of a 120 nm $\times$ 4.5 μm CBEBC SiGe HBT were extracted from dc and S-parameter measurements in the 0.1–60- and 110–170-GHz frequency range. Later, measurements in the 220–325-GHz range were employed to fine tune the splitting of the base resistance and of the junction capacitances in area and periphery components to better match $\mathrm{MAG}(f)$, $U(f)$, and the Y-parameters as a function of frequency up to 325 GHz. Version 1.2 of the HICUM/L0 model and HSPICE were used in all simulations.

A. Junction Capacitances and Substrate Network

These were extracted under "cold" ($V_{\mathrm{BE}}, V_{\mathrm{BC}}, V_{\mathrm{SC}}, < 0.5\,\mathrm{V}$) bias conditions. Consequently, the small-signal equivalent circuit in Fig. 1 reduces to that shown in Fig. 8.

The base–emitter and base–collector capacitances were extracted from $\mathrm{Im}\{Y_{11}+Y_{12}\}/\omega$, $\mathrm{Im}\{-Y_{12}\}/\omega$, respectively. As can be seen from Fig. 9, either low-frequency or D-band data can be used, although C_{be} shows a slight increase with frequency in the D-band.

In contrast, because the substrate network consists of the R_{SU} and C_{SU} in parallel, connected in series with the collector–substrate diode, the collector–substrate capacitance, C_{cs}, and the components of the substrate network require both low- and high-frequency measurements. Fig. 10 shows that C_{cs} can be extrapolated from $\{-\mathrm{Im}[(Y_{22}+Y_{21})-1]\}-1/\omega$

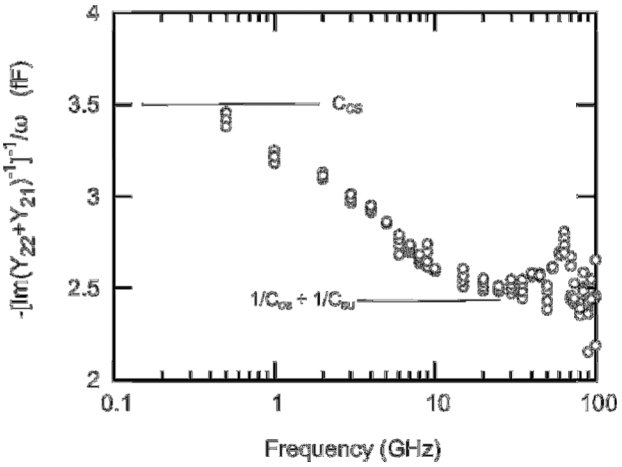


Fig. 10. Extraction of the collector–substrate capacitance and of $C_{\rm SU}$ from low- and high-frequency data for a 120 nm × 5 mm SiGe HBT (measurements using different test structures: STMicroelectronics, Crolles, France).

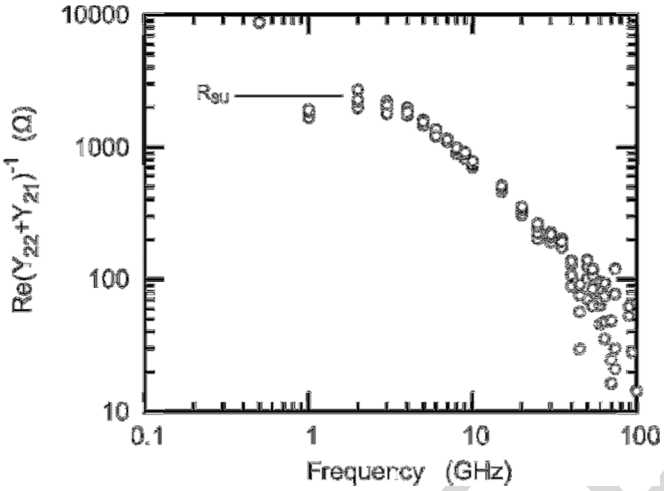


Fig. 11. Extraction of the substrate resistance from cold HBT Y-parameter for a 120 nm × 5 mm SiGe HBT (measurements: STMicroelectronics, Crolles, France).

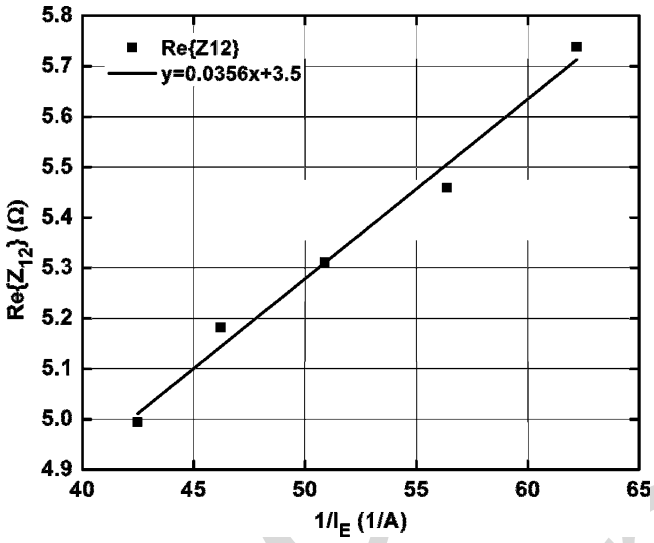


Fig. 12. Extrapolation of R_E extraction from Z_{12} under normal forward bias conditions and $V_{\rm CE}$-0.5 for a 120 nm × 4.5 mm CBEBC SiGe HBT.

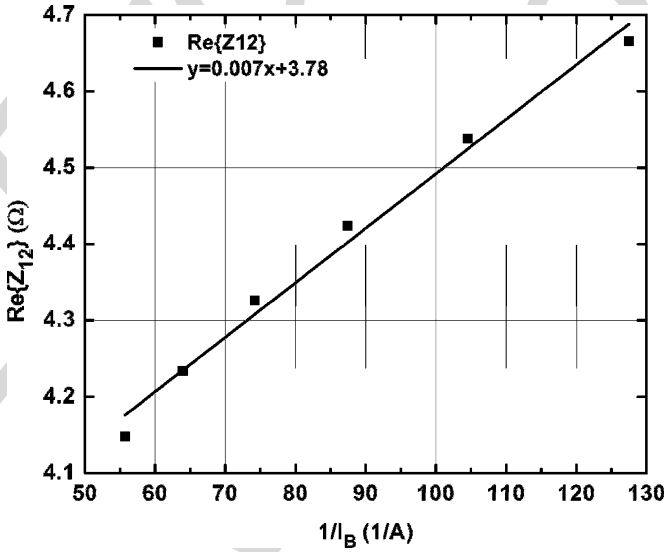


Fig. 13. Extrapolation of R_E using the Johansen method [5] in the saturation region at very large currents and $I_C = 0$ for a 120 nm × 4.5 mm CBEBC SiGe HBT.

at frequencies below 500 MHz. Once $C_{\rm cs}$ is known, $C_{\rm Su}$ can be obtained from the same plot at high enough frequencies, in the W- or D-bands, where the substrate network can be approximated by the series combination of $C_{\rm cs}$ and $C_{\rm SU}$.

Similarly, as illustrated in Fig. 11, the substrate resistance $R_{\rm SU}$ can be obtained from $\mathrm{Re}\{\{Y_{22}+Y_{12}\}^{-1}\}$ at low frequencies when the collector–substrate diode is biased at 0.5 V to minimize the contribution of $R_{\rm CS}$.

B. Junction Capacitances and Substrate Network

First, R_E is extracted from the intercept of real$\{Z_{12}\}$ versus $1/I_C$ (Fig. 12) under typical forward bias conditions, either from low frequency or from D-band data, only at low VCE (0.5 V) to avoid self-heating effects [4]

$$\mathrm{R}(Z_{12}) = R_E + \frac{nKT}{qI_E}. \tag{1}$$

R_E was also obtained at large forward bias of the base–emitter junction with an open collector ($I_C = 0$) from $\mathrm{Re}(Z_{12})$ according to the Johansen method [5]. Again, either low-frequency or D-band Z-parameter data can be employed. The two values are within 10% (Fig. 13). Under the same bias conditions, $R_{\rm CX}$ was extrapolated from $\mathrm{Re}(Z_{22} - Z_{12})$ at low or high frequencies [5], as shown in Figs. 14 and 15.

Finally, Fig. 16 illustrates how the bias-independent part of $R_{\rm BX}$ is determined from $\mathrm{Re}(Z_{11} - Z_{12})$ at D-band under the same open collector bias condition as in the $R_{\rm CX}$ extraction [5]. A somewhat larger and bias-dependent $R_{\rm BX}$ value is obtained from $\mathrm{Re}(Z_{11} - Z_{12})$ at D-band under nominal forward bias conditions. $R_{\rm BIO}$ can be estimated from the same set of data at low current densities and low frequency. Aside from this strategy, $H_{11}(f)$ has been used to implement the so-called circle method (Fig. 17) [6], [7], which, along with fitting $\mathrm{MAG}(f)$, Mason's $U(f)$, and $Y12(f)$ at D- and G-bands, has helped in optimizing $R_{\rm BIO}$ and to fine tune the optimal splitting between $R_{\rm BX}$ and

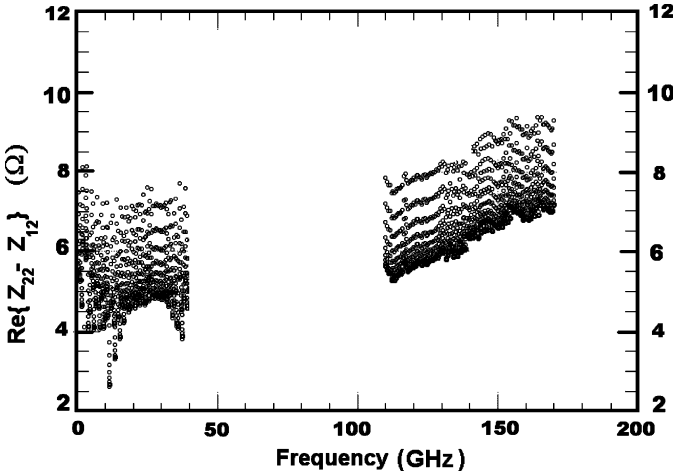


Fig. 14. Measured $\mathrm{Real}\{Z_{22} - Z_{12}\}$ versus frequency for R_{CX} extraction from the saturation region for a 120 nm × 4.5 mm CBEBC SiGe HBT.

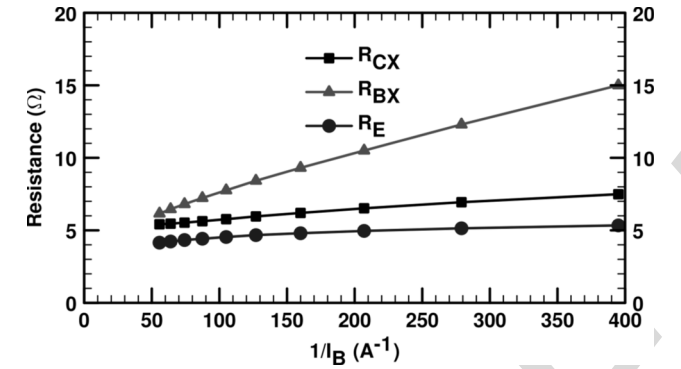


Fig. 15. R_{CX}, R_{BX}, and R_E extrapolation from Z-parameter data in the saturation region for a 120 nm × 4.5 mm CBEBC SiGe HBT.

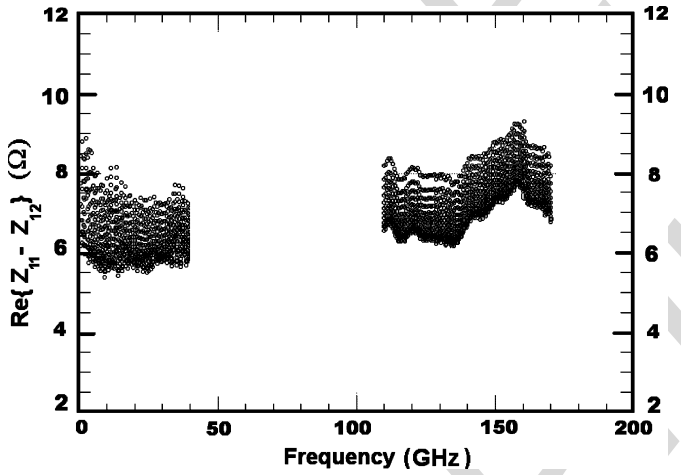


Fig. 16. $\mathrm{Real}\{Z_{11} - Z_{12}\}$ versus frequency for R_{BX} extraction from saturation region in a 120 nm × 4.5 mm CBEBC SiGe HBT.

R_{BIO}, $C_{\mathrm{bc}i}$ and $C_{\mathrm{bc}x t}$. This approach is necessary in the absence of tetrode test structures [8], [9], which were not available in this fabrication run.

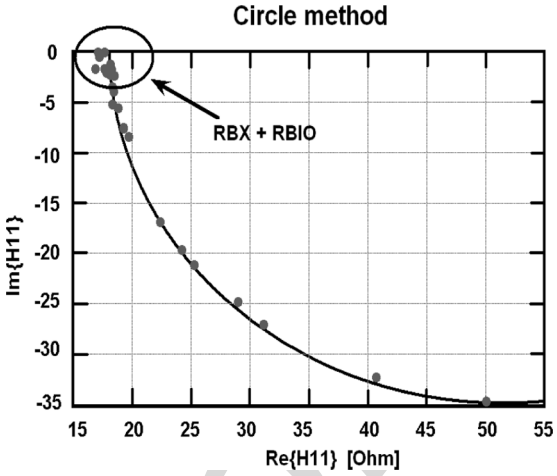


Fig. 17. Circle method employed for $R_{\mathrm{BX}} + R_{\mathrm{BIO}}$ extraction for 120 nm × 4.5 mm CBEBC HBT.

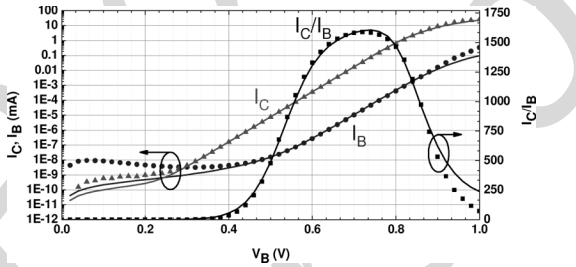


Fig. 18. Measured versus HICUM/L0 simulated Gummel characteristics for a 120 nm × 4.5 mm CBEBC SiGe HBT at $V_{\mathrm{BC}} = 0$.

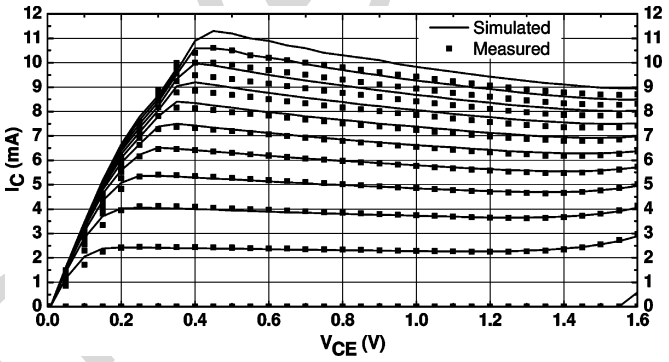


Fig. 19. Measured versus HICUM/L0 simulated output characteristics for a 120 nm × 4.5 mm CBEBC SiGe HBT.

C. Junction Capacitances and Substrate Network

The model parameters for the collector and base currents at low and medium injection levels, and the avalanche breakdown parameters, were extracted next (Fig. 18).

The thermal resistance was obtained from the relative change in V_{BE} in the output characteristics (Fig. 19) as a function of $I_C \times V_{\mathrm{CE}}$. Note the strong self-heating effect ($\Delta T \approx 50\,^{\circ}\mathrm{C}$) apparent in the negative slope of the output characteristics making the model parameter extraction particularly challenging.

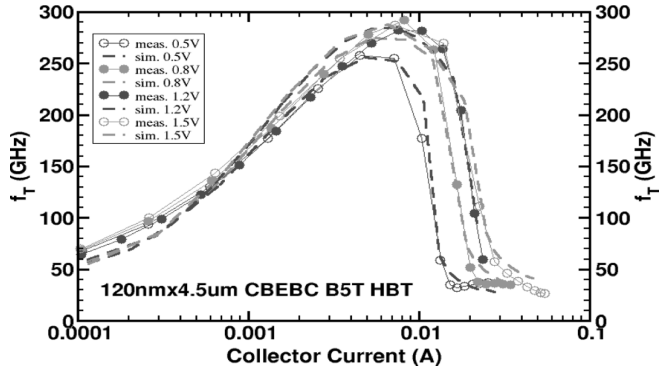


Fig. 20. Measured versus HICUM/L0 simulated $f_T(I_C)$ for a 120 nm $\times$ 4.5 mm CBEBC SiGe HBT biased at $V_{\rm CE} = 0.5$ V to 1.5 V.

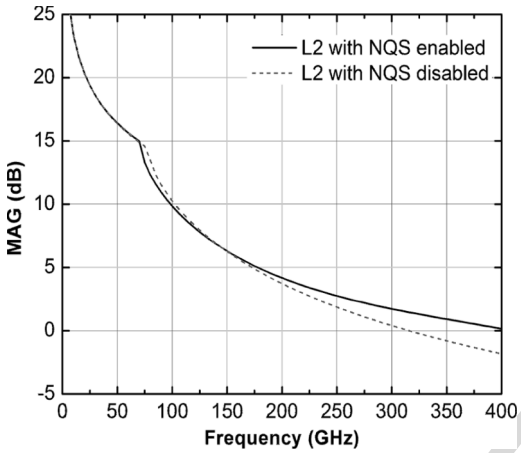
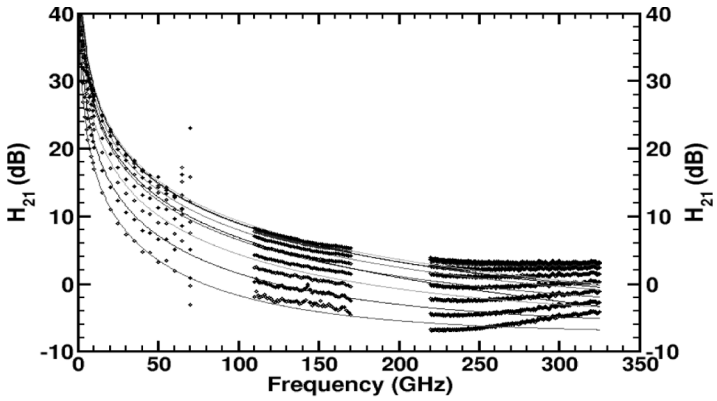
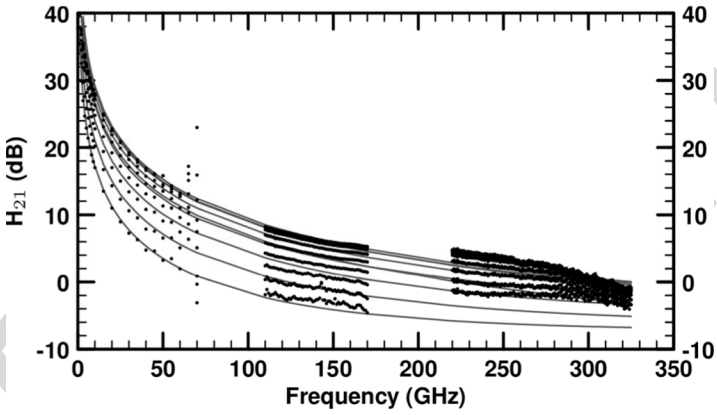


Fig. 21. Impact of NQS on $\mathrm{MAG}(f)$ characteristics using HICUM L2 for a 120 nm $\times$ 4.5 mm CBEBC SiGe HBT.



(a)



(b)

Fig. 22. Measured versus simulated $H_{21}(f)$ at $V_{\rm CE} = 1.2$ V, $V_{\rm BE} = 750$ mV to 960 mV in 15-mV steps: (a) using t-line de-embedding up to the edge of the device and (b) using global OPEN-SHORT de-embedding to metal 2.

D. Transit Time Parameters

Finally, the transit time and transfer current parameters at high injection were extracted from f_T versus I_C and f_T versus $V_{\rm CE}$ measured data and Gummel plot at large injection levels. H_{21} data conducted throughout the D-band were used to extrapolate f_T because the slope of H_{21} remains approximately constant at 20 dB/decade in this range. As can be seen in Fig. 20, it is relatively easy to obtain excellent agreement between the measured and simulated f_T versus I_C characteristics for $V_{\rm CE}$ values as low as 0.5 V and as high as 1.5 V (close to $\mathrm{BV_{CEO}}$).

Since the HICUM/L0 model has a simplified lumped equivalent circuit for the base–collector region, and since the exact geometrical dimensions of the internal and external base–collector regions are unknown, the accurate partition of the base–collector capacitance and base resistance was obtained by fine tuning $R_{\rm BX}$ and $R_{\rm BIO}$, while their sum was kept constant, to fit $\mathrm{Re}\{Y_{12}(f)\}$ as a function of bias and in the D-band, and by fitting $\mathrm{MAG}(f)$, $U(f)$ and $f_{\rm MAX}$. $U(f)$ and $\mathrm{MAG}(f)$, are particularly important when designing amplifiers, oscillators, and dividers at D- and G-band.

As can be seen from Fig. 21, even when using HICUM/L2, if NQS effects are ignored, the maximum available gain is overestimated immediately above the stability inflection point, and seriously underestimated above 150 GHz. This poses a rather formidable challenge to D-, G-, and H-band circuit design using the standard HICUM/L0 model.

IV. Transistor-Level Verification

HICUM/L0 model parameters were extracted for HBTs with 120-nm emitter width and different emitter lengths (2, 3.75, 4.5, and 7.5 mm). In this section, a comparison of simulated and measured high-frequency characteristics are illustrated for a 120 nm $\times$ 4.5 mm HBT with one emitter stripe, two base, and two collector contacts.

Even when the HICUM/L0 was enhanced with a subcircuit similar to the one in Fig. 1, but without $C_{r\rm Bi}$ and t_n, it was difficult to compensate for the lack of NQS modeling to simultaneously match $\mathrm{MAG}(f)$, $H_{21}(f)$, and $U(f)$ from 110 to 325 GHz. However, by moving most of the junction capacitances to the periphery and by optimizing the $R_{\rm BIO}$-$R_{\rm BX}$ and $R_{\rm CIO}$-$R_{\rm CX}$ splits to compensate for the lack of an internal collector resistance, reasonable agreement could be obtained from dc to 170 GHz. This, however, proved inadequate to model circuits operating at 240 GHz. Instead, the HICUM/L2 model was employed for better device and circuit performance agreement between measurements and simulation.

Fig. 22 demonstrates the excellent agreement between the measured and HICUM/L2 simulated $H_{21}(f)$ characteristics up to the D-band, and even up to the G-band if global OPEN-SHORT de-embedding is employed to remove the inductance of the

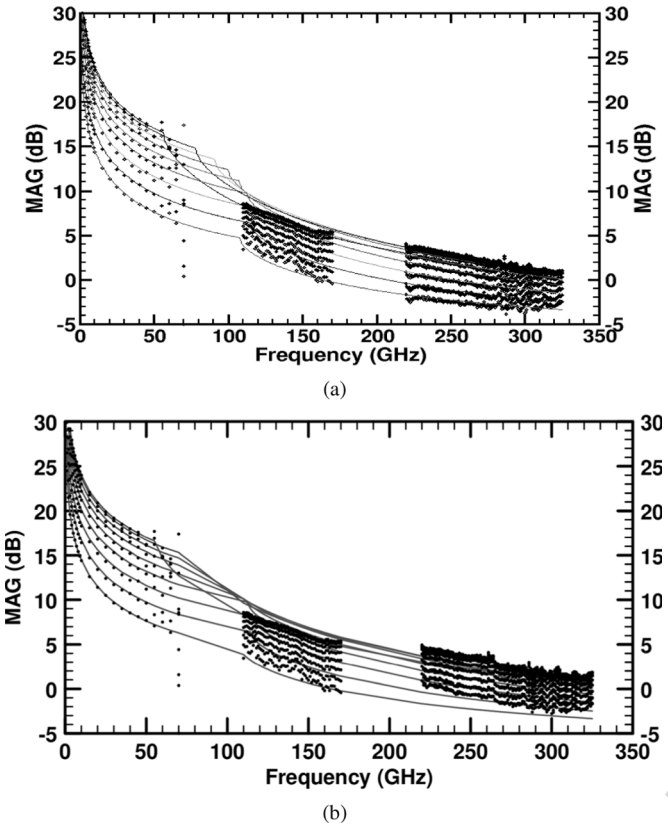


Fig. 23. Measured versus simulated $\mathrm{MAG}(f)$ at $V_{\mathrm{CE}} = 1.2$ V, $V_{\mathrm{BE}} = 750$ mV to 960 mV in 15-mV steps: (a) using t-line de-embedding up to the edge of the device and (b) using global OPEN-SHORT de-embedding to metal 2.

wiring stack above the device. Similar agreement can be observed for $\mathrm{MAG}(f)$ in Fig. 23 and $S_{21}(f)$ characteristics in Fig. 24.

V. Validation on D- and G-Band Circuits

The single-transistor models, validated on small-signal transistor S-parameter measurements up to 325 GHz, were next used to fine-tune geometry-scalable HICUM/L2 and HICUM/L0 models. The latter were employed to confirm the measured performance of linear and nonlinear circuits in the 140–240-GHz range. It is important to note that these benchmark circuits employ different transistor sizes than those measured for parameter extraction.

A. 240-GHz Amplifier

A three-stage cascode amplifier, whose schematic is shown in Fig. 25, was designed using a preliminary model based on device simulation. To ensure the stability of the cascode stages in the presence of the unavoidable inductance associated with the bias-decoupling capacitor, feedback resistors were connected between the base and the collector of the common base HBTs [11]. All stages are biased at the peak f_T current density of 14 mA/mm^2 for a total power consumption is 34 mW from a 2.5-V supply. The die photograph of the amplifier is reproduced in Fig. 26.

The input, output, and interstage matching networks were implemented with coupled line impedance transformers [12] since the simple shunt L- series C matching networks in this

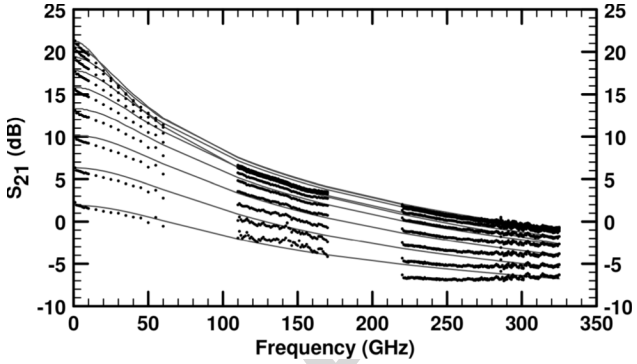


Fig. 24. Measured versus simulated $S_{21}(f)$ at $V_{\mathrm{CE}} = 1.2$ V, $V_{\mathrm{BE}} = 750$ mV to 960 mV in 15-mV steps.

frequency range would require very small capacitors. The coupled microstrip lines were formed in the top, 3-mm-thick copper layer with the bottom three metals shunted together to form the ground plane. The measured loss of a 50-W microstrip line, with identical cross section and ground plane to the one used in the coupled lines, varies between 2.5–3 dB/mm from 220 to 270 GHz. A large proportion of the power gain of the cascode is therefore lost on the coupled transmission-line network. In retrospect, as in SiGe HBT D-band amplifiers [13] and in recent 300-GHz SiGe HBT signal sources [14] fabricated in the same back-end, matching networks with transformers and inductors may prove less lossy than coupled line matching networks. This aspect needs to be systematically investigated.

Fig. 27 compares the measured with the simulated S-parameters using the HICUML2 model and the HICUML0 model, which does not capture NQS effects. The inductance of the decoupling capacitor, in the 1–2-pH range, was found to have a significant impact on the simulated power gain. All passive elements, including larger areas of the amplifier layout, were simulated as multiports using the commercial electromagnetic (EM)-field simulator EMX.[1] These results demonstrate the importance of the NQS effects in predicted the gain of the amplifier at frequencies approaching the f_T and f_{MAX} of the transistor.

B. 150-GHz VCO and Prescaler

A breakout consisting of a fundamental Colpitts–Clapp VCO and a divide-by-16 prescaler was fabricated as the most critical blocks required in the phase-locked loop (PLL) of future fundamental 150- or 300-GHz harmonic transceivers. Their schematics are shown in Fig. 28 and are similar to those fabricated in an older production technology [1]. The only difference are the varactors in the VCO, which are realized from SiGe HBTs with short-circuited base–emitter junctions. At the input of the prescaler is a dynamic divider followed by three static divider stages, all operating from a nominal supply voltage of 1.5 V. The VCO-prescaler operates from 138 to 148 GHz, limited by the tuning range of the VCO. Its phase noise was measured throughout the band, at the divider output, and was found to vary from -80 to -81 dBc/Hz, at 1-MHz offset when accounting for the divider ratio (24 dB). The output

[1]Integrand Softw. Inc., Berkeley Heights, NJ. [Online]. Available: http://www.integrandsoftware.com/

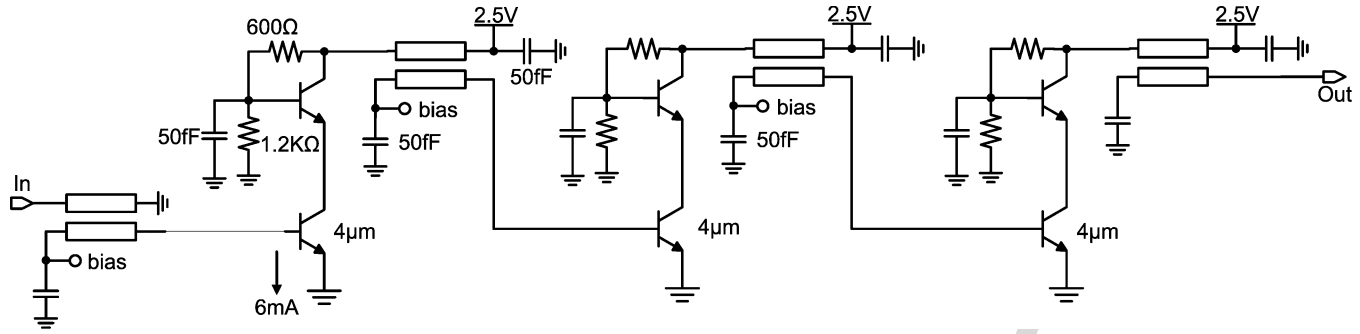


Fig. 25. Amplifier schematic.

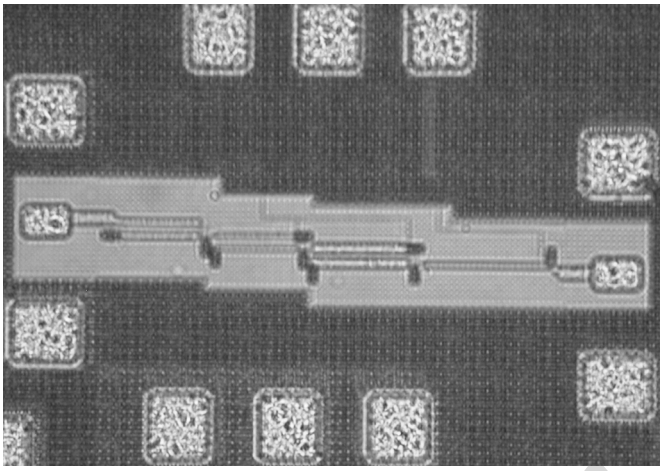


Fig. 26. Die photograph of the 240-GHz amplifier.

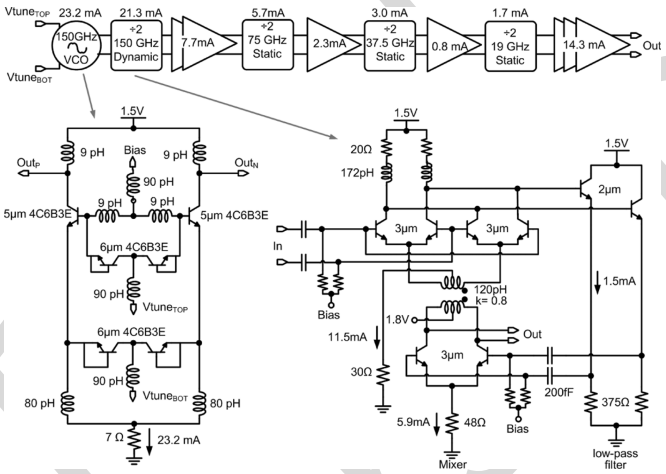


Fig. 28. VCO and prescaler schematics.

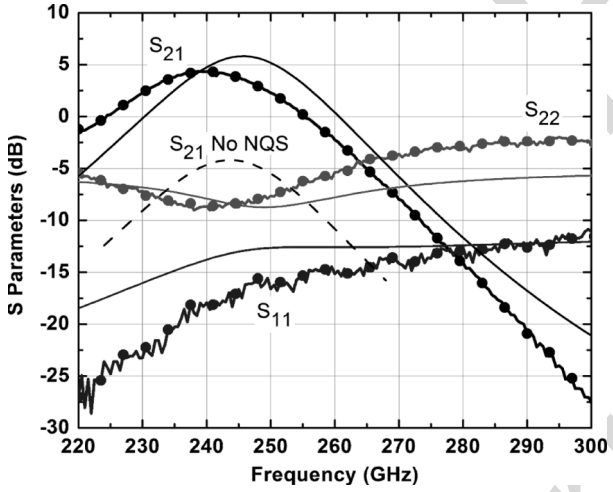


Fig. 27. Comparison of measured and simulated amplifier S-parameters.

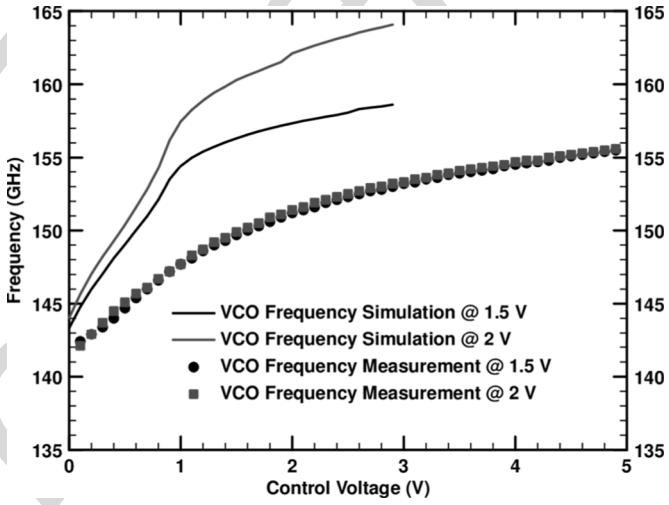


Fig. 29. Measured versus simulated VCO tuning range.

power of the standalone VCO breakout varies from −5 to −11 dBm in the 138–148-GHz tuning range. The prescaler was verified to divide correctly by 16 when the supply voltage was varied between 1.4–1.8 V. Similarly, the VCO oscillates for VCC values ranging from 1 to 2 V. The VCO core consumes 35 mW from 1.5 V, and the divider chain, without output buffers, draws 42.5 mA from 1.5 V. The VCO, prescaler, and buffers consume a total of 120 mW from a 1.5-V supply.

Fig. 29 illustrates the measured and HICUM/L2 simulated tuning characteristics of the standalone VCO at two supply voltages of 1.5 and 2 V, respectively. The agreement is better than 8%. However, for varactor control voltages larger than 3 V, the avalanche breakdown model causes convergence problems. The match between measurements and simulations could be further improved by optimizing the area and periphery junction capacitance parameters VD and Z. Note that in the measured tuning, characteristics are insensitive to the supply voltage, whereas the

simulation results show some VCO pulling. Finally, it should be noted that the simulations predicted a decrease of about 2 GHz in the VCO tuning frequency when the VCO was loaded by the divider chain. A larger decrease of about 4 GHz was observed in measurements.

Despite these promising results, unsolved problems remain regarding the accuracy of t-line and global OPEN-SHORT de-embedding in the H-band, and the ability of the HICUM model both L0 and L2 in predicting the correct frequency dependence of $\mathrm{Re}\{H_{11}(f)\}$ in the 5–50-GHz range.

VI. Conclusion

The HICUM L0 and L2 models were extracted for the first time from D-, G-, and H-band S-parameter measurements for a 400-GHz f_{MAX} SiGe HBT process. Good agreement between the measured and simulated transistor Z- and Y-parameters, H_{21}, and U, in the dc to 170-GHz range was demonstrated for the L0 model. However, when tested on circuits, the L0 model was found to underestimate the gain of a three-stage 240-GHz amplifier and the negative resistance of a 150-GHz VCO. It was only when measurements in the 220–325-GHz range were performed that the limitations of the L0 model in correctly predicting the NQS effects and the $\mathrm{MAG}(f)$ characteristics became apparent. In contrast, the HICUM/L2 model, including NQS effects and a more sophisticated distributed small-signal equivalent circuit appears to be adequate for circuit simulation up to 325 GHz. Its accuracy was validated on a 240-GHz three-stage cascode amplifier and on a low-power fundamental-frequency 120-mW 150-GHz VCO prescaler.

Acknowledgment

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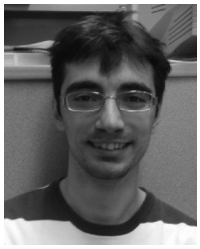

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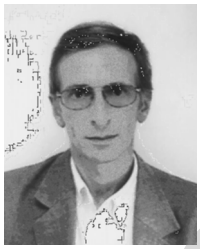

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