Foundry 0.13 μm CMOS Modeling for MS/μWave SOC Design At 10 GHz and Beyond

M.T. Yang[1], T.J. Yeh[1], Y. J. Wang[1], Patricia P.C. Ho[1], Y. R. Lin[1], Darry C.W. Kuo[1], Sorin P. Voinigescu[2], Mihai Tazlauanu[3], Y.T. Chia[1], K.L. Young[1]

[1]TSMC, 9 Creation Rd. I, Science-Based Industrial Park, Hsin-Chu, Taiwan 300-77, R.O.C.,
[2]ECE Department, University of Toronto, 10 King's College Rd. Toronto, ON, M5S 3G4, Canada,
[3]Quake Technologies Inc., 80 Hines Rd. Ottawa, ON, K2K 2T8 Canada.

Abstract **This paper reports on the first unitary set of geometry-scalable, wide-band compact models for all the components of a 0.13 μm RF CMOS technology and which are valid up to 50 GHz. Verification of the active and passive device models is achieved at the device level as well as by comparing measurements and simulation results of the S parameter response and jitter generation of high-speed circuits operating above 10 GHz from a single 1.2-V supply.**

Index Terms — **0.13μm, CMOS modeling, foundry, MS/μWave, SOC.**

I. Introduction

The silicon foundry industry emerged in the early 90s primarily with processes geared towards digital applications. It has since expanded and blossomed to encompass both analog and RF applications [1]. To maintain this growth in the next decade, foundries should be able to provide the leading technologies and the design services that combine high-speed digital, analog, and μWave capability on the same chip. While the key technology components necessary for CMOS MS/μWave SOC have been developed over the last few years [2], a critical issue for the implementation of μWave circuits in silicon CMOS remains the lack of production-proven Spice models that accurately capture high-frequency passive components and device parasitic beyond 10 GHz. For the foundry industry, modeling of both passive and active integrated components for μWave applications is highly desirable. This paper reports for the first time on an unitary set of geometry-scalable, wide-band compact models for all the components of a 0.13 μm RF CMOS technology and which are valid up to 50 GHz. Verification of the active and passive device models is achieved at the device level as well as by comparing measurements and simulation results of the S parameter response and jitter generation of high-speed circuits operating above 10 GHz from a single 1.2-V supply.

This paper is organized as follows: Section II describes the CMOS technology for MS/μWave SOC, section III depicts the modeling for MS/μWave including both compact CMOS model and lumped-equivalent passive models, and section IV presents the benchmark circuit verification and experimental results. Finally, we add some concluding remarks in section V.

II. CMOS Technology For MS/μWave SOC

The devices were fabricated in a 0.13 μm RF CMOS process with full Cu damascene metallization. The main features of this process flow were reported in [3]. In addition to standard CMOS logic technology components and embedded memory cells, passive components such as resistors, capacitors, inductors, varactors, and transmission lines, as well as adequate on-chip electrical noise-isolation, are mandatory ingredients in support of MS/RF SOC. A more detailed description of all the available devices in TSMC's 0.13 μm RF CMOS process can be found in [4] and [5].

The parameters of compact BSIM4 and lump-equivalent models were extracted using on-wafer DC, and S-parameter measurements performed with GSG probes. A two-step series-shunt de-embedding of pad and interconnect parasitics was employed.

III. Modeling For MS/μWave

A. Compact BSIM4 CMOS Model

As process technology advances into 100-nm lithography, CMOS has become attractive for RF and μWave applications due to the very high f_T and f_{MAX}, now reaching 100 GHz. In fact, at terminal voltages below 0.8 V, 0.13 μm CMOS f_T and f_{MAX} values surpass those of the most advanced SiGe HBTs. Figure 1 shows the measured vs. modeled f_T characteristics of a n-MOSFET at different biases. The BSIM4 high-speed/RF Spice model [6] featuring distributed gate and substrate resistance was

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employed. The device has a multi-fingered gate structure with a unit width of 4 μm. The ability of the model to accurately capture low-frequency Flicker noise and high-frequency thermal noise was also assessed.

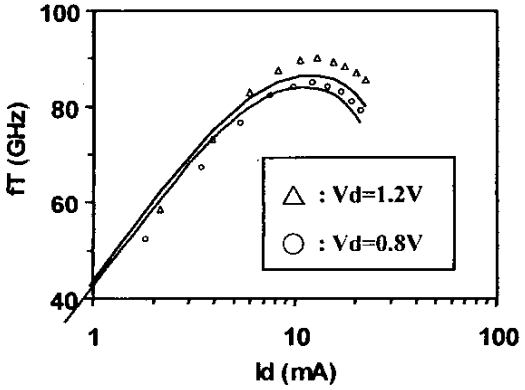

Figure 1: Measured vs. simulated current gain cutoff frequency (f_T) as function of the drain current for NMOS with 10x4x0.13 μm^2 at Vd =0.8V (○) and 1.2V(Δ).

B. Lumped-Equivalent Passive Models

Several passive components are required to fully integrate analog and μWave circuits in mixed-signal SOC ICs. These include analog capacitors, inductors, varactors, and transmission lines. The analysis and modeling of passive elements is critical in the design and optimization of basic high-speed and μWave building blocks, especially when the quality of passive elements determines the overall achievable performance.

Figure 2 compares the measured and modeled effective capacitance and Q-factor vs. frequency characteristics of a MiM capacitor with an area of 25x40μm^2, which is integrated with one of the standard back-end metal layers as bottom electrode. Direct access using one interconnecting level to form its contacts results in a high Q-factor beyond 20 GHz. The capacitance density is 1.0 $fF/\mu m^2$. To isolate the substrate noise coupling at high frequency, a shielding N-well is included in the design. The lumped-element model of the N-well and substrate region below the MiM structure is depicted in the inset of the figure.

In applications exceeding 10 GHz where substrate and skin effect losses are dominant, instead of using the patterned ground shield and wide metal stripes which degrade the self-resonant-frequency (SRF) of the inductor, an 8-layer multi-level metal interconnect featuring an ultra-thick (3μm) top Cu and thick dielectric on top of the un-doped P-substrate is employed. In conjunction with narrow (2-5μm) metal stripes, this improves the losses associated with the conductor and the substrate to boost the Q-factor at μWave frequencies. The high-frequency performance is shown in Figure 3 for a 0.6-nH inductor. The Q is larger than 15 between 10 GHz and 30 GHz and the SRF exceeds 60 GHz. A 2-Π equivalent circuit was used to model the high-Q on-chip inductors. As shown in the inset, this new model incorporates a frequency independent RL network that mimics the skin effect behavior and can accurately predict the inductive behavior as well as the Q of this device up to 50 GHz.

Accumulation-mode NMOS varactors in N-well have been designed and modeled. The salient feature of this structure is its fishbone configuration that reduces the parasitic resistance for a high Q, without requiring any change in the process. A charge-based model was derived based on hyperbolic tangent characteristics. The measured and modeled C-V and Q-V vs. frequency characteristics up to 50 GHz with excellent agreement are shown in Figure 4 for a W/L/B=4/1/6 μm^2 structure. A 3:1 capacitance ratio has been achieved.

As the frequency for μWave applications in silicon technology increases, the modeling of transmission lines becomes important. An analytical process- and geometry-scalable model was developed, which was employed to extract interconnect parasitic as transmission lines rather than as lumped capacitances. S-parameters were measured on 1-mm-long transmission lines with different widths for structures with and without metal ground plane. Figure 5 demonstrates excellent agreement between measurements and simulations for both characteristic impedance and transmission loss. For long controlled-impedance transmission lines, ultra-thick metal (M8) with metal ground plane microstrip lines are recommended due to reduced loss which is as low as 0.5 dB/mm at 50-GHz.

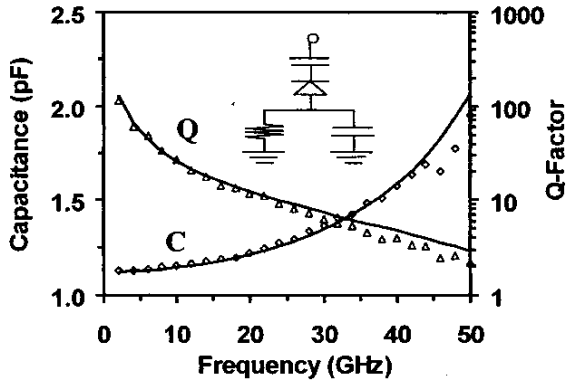

Fig. 2 Measured vs. simulated Capacitance (□) and Q-factor (□) of a 1.1pF MiM Capacitor.

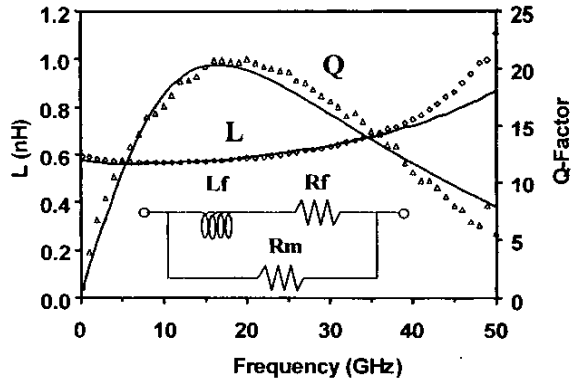

Fig.3 Inductance (Δ) and Q-factor (□) measured and simulated data for a single-ended inductor with an inductance of 0.6nH.

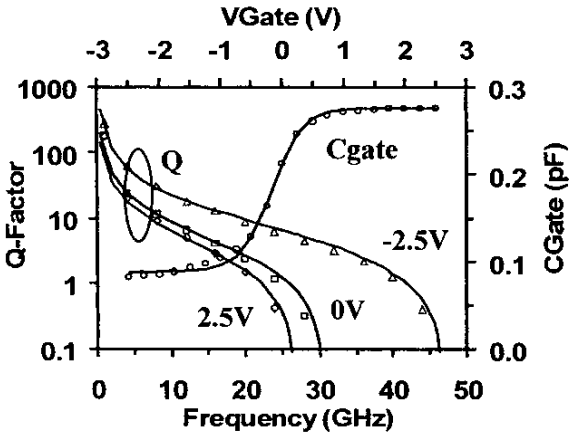

Fig.4 Capacitance (○) versus voltage fitting at 2GHz (left-bottom) and Q-factor versus frequency fitting (right-top) at 2.5V (□), 0V (□) and –2.5V (Δ).

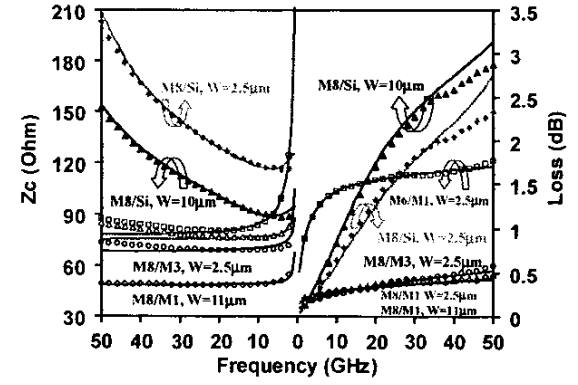

Fig.5 Measured and simulated characteristic impedance and attenuation loss of T-line for M8/M1, W=11μm (□); M8/M3, W=2.5μm (○); M8/M1, W=2.5μm (Δ); M6/M1, W=2.5μm (□); M8/Si, W=10μm (▲); M8/Si, W=2.5μm ( ).

IV. Benchmark Circuit Verification and SOC Illustration

A combined input-buffer/output-driver test circuit was designed and fabricated as a process and RF-model monitor. The circuit, whose photomicrograph and schematic are shown in Figure 6, operates from a single 1.2-V supply, consumes 60 mW, and features a source-follower input for low-input reflection, either three or five MOS-CML inverters with t-coil inductive peaking, and an output buffer with adjustable swing from 200 mVp-p to 500 mVp-p per side. All MOSFETs have low-voltage threshold to facilitate operation with low supply voltage. Figure 7 illustrates the measured S parameters and compares them with simulation results using the RF-MOSFET model and the baseband logic MOSFET model. The small-signal single-ended gain is 16 dB and 27 dB, for the 3-inverter and 5-inverter cell versions, respectively, while the input return loss is lower than -10 dB up to 20 GHz in both circuits. The logic model, optimistic in terms of bandwidth, also fails to capture the 2 dB drop in S21 in the 1-GHz to 4-GHz range. The latter also has implications on the large signal behavior, contributing to a 5.6 $ps_{p\text{-}p}$ degradation (from 1.3 $ps_{p\text{-}p}$) in the deterministic jitter of the output eye diagram at 10.5 Gb/s. The on-wafer measured eye diagram is also depicted in Figure 8. With rise/fall times of 16ps the driver is operational beyond the 14-Gb/s range of the BERT used in measurements.

Finally, all the features of the 0.13 μm RF-CMOS process: LVT transistors, inductors, transmission lines, MIM capacitors and varactors, were exercised in a 3rd. generation 10Gb Ethernet mixed-signal single-chip transceiver [7]. The chip features 10 mV input sensitivity per side, 0.7 ps rms jitter generation, at the 10-Gb/s IOs, consumes 0.9 W from a single 1.2 V supply and is fully compliant with the IEEE802.3ae standard.

V. Conclusions

Foundry 0.13 μm CMOS technology has been characterized and modeled for MS/μWave SOC design at 10 GHz and beyond. The BSIM4 high-speed/RF Spice model employed for CMOS transistors. Good agreement between measurements and simulations in fT has been demonstrated. In addition, the ability of the model to accurately capture low-frequency Flicker noise and high-frequency thermal noise were also assessed. Integrated passive components are also analyzed and

modeled using lumped-equivalent circuit. High-frequency parasitic including loss, skin effect and substrate effect are modeled to accurately capture C, L, and Zc so as to the Q-factor and SFR up to 50 GHz. Model verification is achieved by comparing measurements and simulation results of the S parameter response and jitter generation of high-speed circuits operating above 10 GHz.

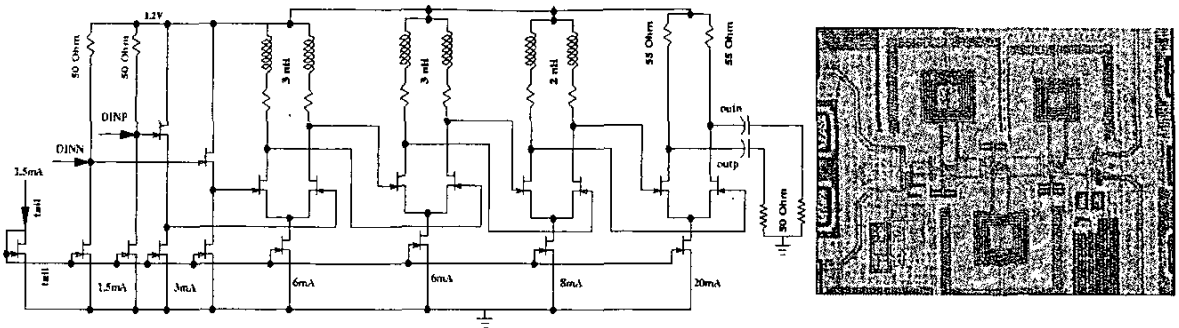

Fig.6 Schematic and photomicrograph of the 3-Cell driver/ comparator test structure.

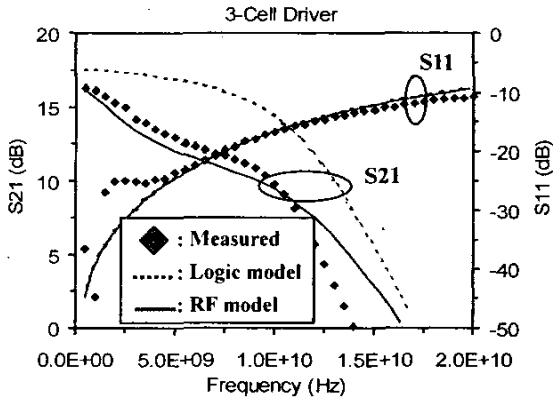

Fig. 7 Comparison of measurement and simulation of S21 using the RF-MOSFET model and the conventional logic model.

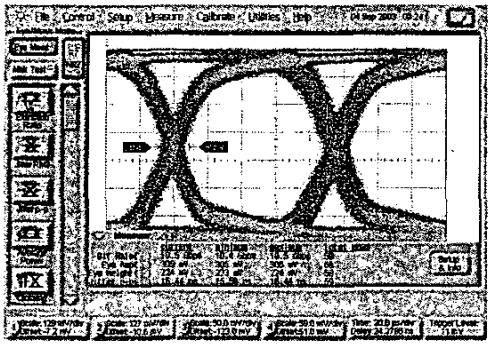

Fig. 8 10.7-Gb/s differential output data eye diagram for 3-cell driver with 50 mVp-p input per side.

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