Design of Low-Power Active Tags for Operation With 77–81-GHz FMCW Radar

M. Sadegh Dadash, *Student Member, IEEE*, Jürgen Hasch, *Senior Member, IEEE*, Pascal Chevalier, *Member, IEEE*, Andreia Cathelin, *Senior Member, IEEE*, Ned Cahoon, and Sorin P. Voinigescu, *Fellow, IEEE*

***Abstract*— The system and transistor-level design of low-power millimeter wave (mm-wave) active tags in silicon is discussed in detail. Two active mm-wave tags with identical system architecture, padframe, and chip size were designed and fabricated in 55-nm SiGe BiCMOS and 45-nm SOI CMOS technologies, respectively. They feature a three-stage low-noise amplifier (LNA), a wake-up detector, a BPSK modulator, and two variable gain output stages, each driving a separate transmit antenna in antiphase. The wake-up detector can be used to switch OFF all the blocks except for the LNA and detector, thus further reducing power consumption. The measured performance of the SiGe and SOI chips is remarkably similar: 19- and 20-dB gain, 9- and 8-dB noise figure, and 25-/10.8-mW (active/idle) and 18-mW power consumption, respectively. The SiGe tag was flip-chip-mounted on a mini-PCB with one receive and two transmit antennas for system level functionality tests carried out over a distance of 5 m. The SiGe-tag wake-up sensitivity was verified to be −62 dBm, in excellent agreement with simulation results.**

***Index Terms*— Active tag, antenna, BPSK modulator, detector, FMCW radar, low-noise amplifier (LNA), millimeter wave (mm-wave), SiGe BiCMOS, SOI CMOS, wake-up function.**

I. Introduction

In RECENT years, we have witnessed the proliferation of vehicles equipped with FMCW long-range and medium-range radars operating in the 77–81-GHz band. The impending introduction of autonomous vehicles will make these radar systems ubiquitous. Therefore, a low-power millimeter wave (mm-wave) tag (also referred to as backscatterer or reflector) operating in this band [1], [2] can act as a very useful aid for target identification in autonomous navigation.

In a would-be usage scenario illustrated in Fig. 1, the FMCW radar installed in the vehicle acts as the base station. It first interrogates the tag and then reads back the signal amplified and modulated with local information by the tag. Initially, the tag is in idle mode, consuming little power.

Manuscript received July 1, 2017; revised August 28, 2017; accepted September 22, 2017. Date of publication November 21, 2017; date of current version December 12, 2017. This work was supported by Robert Bosch GmbH. *(Corresponding author: M. Sadegh Dadash.)*

M. S. Dadash and S. P. Voinigescu are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada (e-mail: dadashmo@ece.utoronto.ca).

J. Hasch is with Corporate Sector Research and Advance Engineering, Robert Bosch GmbH, 71272 Renningen, Germany.

P. Chevalier and A. Cathelin are with STMicroelectronics, F-38926 Crolles, France.

N. Cahoon is with GlobalFoundaries, Essex, VT 05452 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2017.2769079

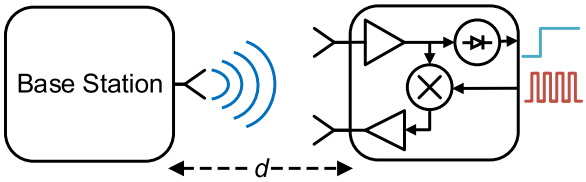


Fig. 1. FMCW radar system consisting of base station and active tag.

Once it preamplifies and detects the incoming FMCW signal, it powers up to modulate and further amplify the signal before it "reflects" it back to the base station.

Other possible applications include perimeter definition for autonomous lawn mowers, snow blowers, and similar autonomous robots.

Until recently, with the exception of an active tag operating at 34 GHz, which consumes 122 mW [3], only passive tags have been reported in the mm-wave range [1], [2], [4]. Despite their ultra-low power, passive tags suffer from signal loss and poor sensitivity, severely limiting the range over which they can operate. Recently, we have presented two ultra-low power 77–81-GHz active tags manufactured in 55-nm SiGe BiCMOS [5] and 45-nm SOI CMOS [6] technologies with dedicated mm-wave back-end-of-line (BEOL).

This paper discusses the system-level specification of those tags in Section II and explores which technology back-end and transistor figures of merit (FoMs) determine the minimum power consumption in Section III. Section IV presents the low-power circuit topologies and design methodology and compares the specific implementations of each circuit block in 55-nm SiGe BiCMOS and 45-nm SOI CMOS technologies. Fabrication and packaging is briefly reviewed in Section V, whereas the experimental characterization at the die level and in-the-package is covered in detail in Section VI, where new system-level experiments conducted in an anechoic chamber over 5 m are reported.

II. Radio-Link Budget

The design goal is to establish a 10-m link using existing FMCW long-range and medium-range radar systems and an ultrasmall size tag with minimal power consumption. It is assumed that the base station has a transmitter output power, P_{TX}, of 10 dBm, an antenna gain, G_{TRX}, of 20 dBi, and a receiver noise figure of 10 dB. The tag is specified for an antenna gain of 6 dBi, a receiver noise figure of 9 dB, a gain

TABLE I
BASE STATION AND ACTIVE TAG SYSTEM PARAMETERS

Block	Symbol	Description	Value
FMCW base station	f_0	frequency range	77-81 GHz
	P_{TX}	transmit power	10 dBm
	G_{TRX}	transceiver antenna gain	20 dB
	NF_{RX}	receiver noise figure	10 dB
	d	distance between base station and target	> 10 m
mm-wave tag	BW	operation bandwidth	5 GHz
	G_{tag}	antenna gain	6 dB
	A_{tag}	amplification gain	20 dB
	NF_{tag}	noise figure	9 dB
	BW_{mod}	modulation frequency	< 100 kHz

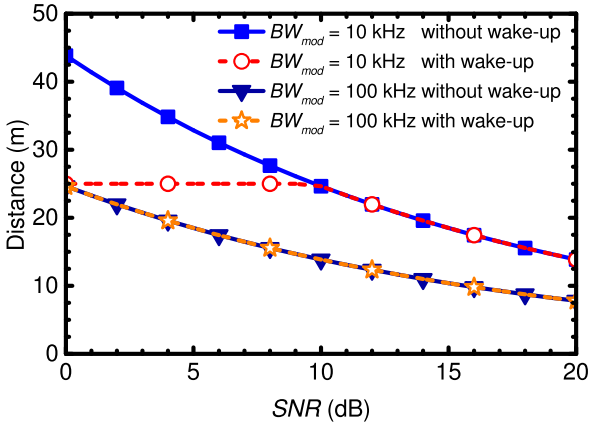


Fig. 2. Link distance versus base station receiver SNR for two different values of the tag modulation bandwidth, with and without wake-up functionality.

of 20 dB, and a modulation bandwidth of 10–100 kHz. The 3-dB bandwidth of the tag must be at least 5 GHz, covering the 77–81-GHz band with some margin.

It is important to clarify that, while in the idle mode, the tag operates as a low-noise radiometer. The wake-up function sensitivity is determined by the responsivity (*RESP*) and the noise equivalent power (*NEP*) of the low-noise amplifier (LNA)-detector block. A large RF bandwidth degrades its sensitivity. The wake-up function sensitivity of the tag is assumed to be better than −62 dBm. A summary of the base station and active tag parameters used in the link budget analysis can be found in Table I.

Friis's transmission equation can be used to calculate the signal power received by the tag in the downlink

$$P_{R,\text{tag}} = \frac{P_{\text{TX}} G_{\text{TRX}} G_{\text{tag}} \lambda^2}{(4\pi d)^2} \tag{1}$$

where λ is the free-space wavelength and d is the distance between the base station and the tag.

For a 77-GHz signal traveling over a distance of 25 m, the free space loss (*FSL*) becomes

$$\text{FSL} = 20 \times \log\left(\frac{4\pi d}{\lambda}\right) = 98 \text{ dB}. \tag{2}$$

Using (1) and (2), the received signal power at the tag is calculated as

$$P_{R,\text{tag}} = P_{\text{TX}} + G_{\text{TRX}} + G_{\text{tag}} - \text{FSL} = -62 \text{ dBm}. \tag{3}$$

This value is equal to the sensitivity of the wake-up detector and limits its downlink operation. Therefore, given that the tag gain, A_{tag}, is 20 dB, its output power becomes

$$P_{T,\text{tag}} = P_{R,\text{tag}} + A_{\text{tag}} \quad \text{if } P_{R,\text{tag}} > -62 \text{ dBm}. \tag{4}$$

The lowest detectable power level in the base station receiver, S_i, can be expressed as

$$S_i = -174 \text{ dBm} + \text{SNR}_{\text{min}} + \text{NF}_{\text{RX}} + 10\log(\text{BW}_{\text{mod}}) \tag{5}$$

where SNR_{min} denotes the minimum required SNR at the base station receiver, NF_{RX} is its receiver noise figure, and BW_{mod} is the baseband modulation frequency of the tag. For a given sensitivity of the base station receiver, the maximum distance between the base station and the tag is given as

$$\begin{aligned} d &= \frac{\lambda}{4\pi} 10^{(P_{T,\text{tag}} + G_{\text{TRX}} + G_{\text{tag}} - S_i)/20} \\ &= \frac{\lambda}{4\pi} 10^{(P_{\text{TX}} + 2G_{\text{TRX}} + 2G_{\text{tag}} + A_{\text{tag}} - S_i)/40}. \end{aligned} \tag{6}$$

Fig. 2 illustrates the maximum link distance as a function of the base station receiver SNR for two different values of the tag modulation bandwidth, with and without wake-up functionality.

If all the circuits in the tag are active all the time, the link distance can be longer than 20 m at a modulation bandwidth of 10 kHz and SNR of 14 dB. However, in the case where the wake-up function is desired and most of the tag is idle, the maximum link distance is determined by the wake-up function sensitivity of the tag in the downlink. Based on previously published work [7], [8], the tag wake-up sensitivity is expected to be dominated by the tag *RESP* and *NEP*. Therefore, an LNA with large gain (over 25 dB [8]) and low noise figure must be placed in front of the wake-up detector to improve the *NEP*. Moreover, the tag *RESP* must be large enough for the desired wake-up function sensitivity.

III. TECHNOLOGY FIGURES OF MERIT AT *W*-BAND

The 55-nm SiGe BiCMOS technology from STMicroelectronics and GlobalFoundries' 45-nm SOI CMOS technology were used for the physical implementation of the mm-wave active tag ICs.

The first process features 55-nm MOSFETs with high and low V_t and fully wired nMOSFET f_T/f_{MAX} of 280/300 GHz, three flavors of 100-nm emitter width SiGe HBTs with fully wired f_T/f_{MAX} of 300/330 GHz, and a nine-metal BEOL with 3-μm-thick top Cu layer and 1.4-μm-thick Alucap layer [13].

The BEOL of the partially depleted SOI-CMOS process has 11 metal layers with two 1.2-μm-thick top Cu layers and 2.1-μm-thick Alucap. The measured f_T and f_{MAX} of fully wired nMOSFETs with 770-nm gate-finger width and minimum gate length of 40 nm are both 250 GHz [9].

Both technologies use a standard silicon p-type substrate with 10−Ω×cm resistivity.

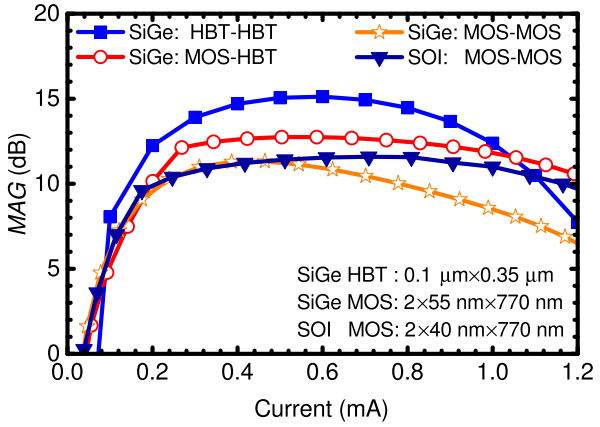


Fig. 3. Simulated MAG at 80 GHz as a function of current for minimum-size cascode stages in 55-nm SiGe BiCMOS and 45-nm SOI CMOS technologies.

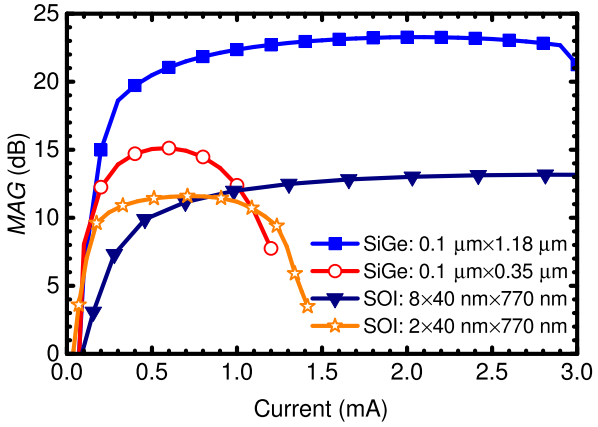


Fig. 4. Simulated MAG for HBT-HBT and MOS-MOS cascodes of two different sizes in 55-nm SiGe BiCMOS and 45-nm SOI CMOS technologies, respectively.

Since a critical design goal in this application is minimizing the power consumption of the tag, the most important technology FoMs are: 1) the power gain of the minimum-size amplifier stages and 2) the quality factor of W-band matching networks. The latter depends on the BEOL and on the resistivity of the Si substrate.

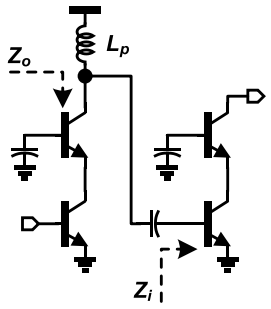
A. Power Gain of Minimum-Size Cascodes

For a given bias current, cascodes provide more than 3-dB higher gain and better isolation than common-emitter/source and common-base/gate topologies. Fig. 3 compares the simulated maximum available gain (MAG) of different minimum-size cascode stages at 80 GHz in both technologies as a function of bias current. The HBT–HBT and the MOS–HBT cascodes in the 55-nm SiGe BiCMOS process show the highest peak gain of 15 and 12.5 dB, respectively, at 0.5 mA. Their gain is larger than those of the 45-nm SOI-CMOS and 55-nm MOSFET cascodes at all bias currents smaller than 1 mA. The peak stable power gain of the 45-nm SOI CMOS cascode is 11.5 dB at 0.7 mA, while that of the 55-nm MOS-MOS cascode is 11 dB at 0.5 mA. All MOSFETs have the gate fingers contacted on both sides to minimize the gate resistance and maximize f_{MAX}.

As already mentioned, to minimize power consumption, one might be tempted to use the minimum-size HBTs and MOSFETs in all circuit blocks. However, Fig. 4 indicates that the power gain of minimum-size HBTs is significantly degraded by periphery effects, such as parasitic and fringing capacitances. Using larger-size HBT cascodes results in larger gain at all bias currents. This effect is less pronounced in the MOS–MOS cascodes whose MAG only depends on the gate finger width (fixed at 770 nm) and not on the number of fingers connected in parallel. All the above-mentioned simulations were performed after extraction of layout parasitic.

B. Impact of Matching-Network Q on Cascode-Stage Gain

Fig. 5 summarizes the values of the input and output impedances of the cascodes in Fig. 4 and the value of the inductors needed for interstage matching in each case. It is apparent that, besides the lower gain, minimum-size cascodes



	0.1 µm ×0.35 µm	0.1 µm ×1.18 µm	2×40 nm ×770 nm	8×40 nm ×770 nm
Z_i	225-j365	88-j95	100-j680	31-j203
Z_o	85-j640	20-j306	460-j1060	137-j410
L_p	~650 pH	~250 pH	~650 pH	~250 pH
I_{bias}	0.5 mA	1.5 mA	0.475 mA	1.9 mA

Fig. 5. Simulated input and output impedances and matching inductor values at 80 GHz for different HBT–HBT and 45-nm SOI MOSFET cascodes.

exhibit very large interstage impedances with large quality factor Q. The corresponding matching networks require very large inductor values, which are not realizable at 80 GHz with sufficiently high self-resonance frequency (SRF).

To evaluate the performance of the two BEOLs and understand their limitations, a 210-pH vertically series-stacked inductor, with identical layout formed in the top-three metal layers, was simulated in both BEOLs using a quasi-3-D EM simulator. The inductor layout, with 30-μm diameter and 4-μm metal width, is illustrated in Fig. 6. The effective inductance L and quality factor Q extracted from the simulated S-parameters are plotted as a function of frequency in Fig. 7. Although the two BEOLs have somewhat different top metal thickness and different total dielectric thickness, similar peak quality factors of 16.5 and SRF of 155/160 GHz are obtained for the SiGe BiCMOS and SOI technologies, respectively. The effective Q peaks at 70–75 GHz. A third set of curves is included for the case where the SOI substrate resistivity is changed from 10 $\Omega \times$ cm to the high-resistivity option of 1000 $\Omega \times$ cm. As can be seen, the resistivity of the substrate has practically no impact on these mm-wave inductor designs,

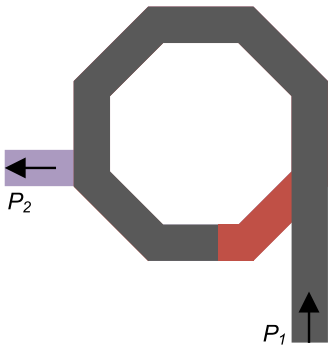


Fig. 6. Three-turn inductor layout realized in the aluminum and top two copper layers.

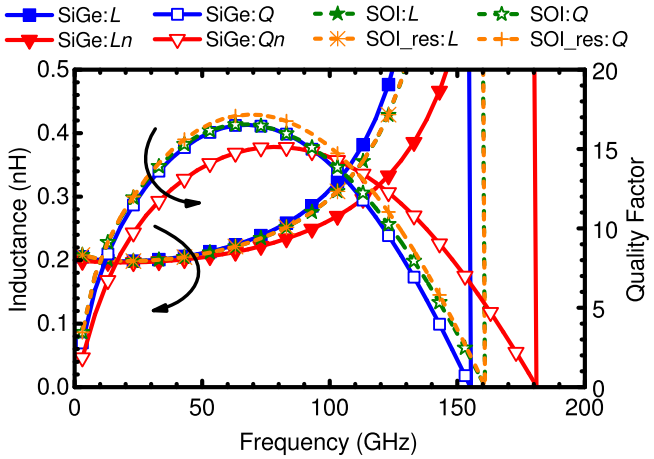


Fig. 7. EM simulation of effective inductance L and quality factor Q of the same inductor realized in the 55-nm SiGe BiCMOS BEOL (SiGe) and 45-nm SOI CMOS BEOL with 10−Ω×cm (SOI) and 1000−Ω×cm (SOI_res) silicon substrates. L and Q describe the inductor with 30-μm diameter in both BEOLs, whereas Ln and Qn describe the 26-μm-diameter inductor in the SiGe BEOL.

because the inductor footprint is small and vertical coupling is employed. The $L \times$ SRF product is 32 GHz×nH. Since the SRF of the inductor has to be at least two times larger than the frequency at which it is used, it is also clear that inductor values larger than 200 pH should not be used at 80 GHz in these technologies.

Finally, a better $L \times$ SRF product of 36 GHz×nH with similar peak-Q value of 15 can be achieved in the SiGe BiCMOS process if 2-μm-wide metal lines are used in the inductor design. For the same inductance value of 210 pH, the inductor footprint is reduced to a diameter of 26 μm, increasing the SRF to 180 GHz.

The effect of the quality factor of the matching network on the gain of the SiGe HBT-HBT and SOI CMOS cascode stages at 80 GHz is simulated in Fig. 8 as a function of bias current. MAG improves by more than 3 dB when the inductor Q increases from 10 to 20. It is also important to note that the gain of the HBT-cascode with infinite-Q inductor decreases from 23 dB in Fig. 4 to 17 dB when the inductor Q is 20. There is negligible degradation in the MAG of the SOI MOSFET cascode when the matching network Q changes from infinity to 20. The latter can be explained by examining the data in the table of Fig. 5. The quality factor of the output impedance of the SOI MOS–MOS cascode is 3, whereas the

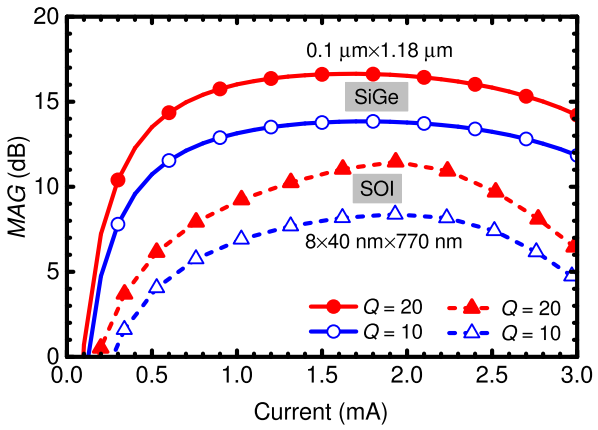


Fig. 8. Simulated MAG at 80 GHz versus current of HBT–HBT cascode in 55-nm SiGe BiCMOS and MOS–MOS cascode in 45-nm SOI CMOS technologies for output matching quality factors of 10 and 20.

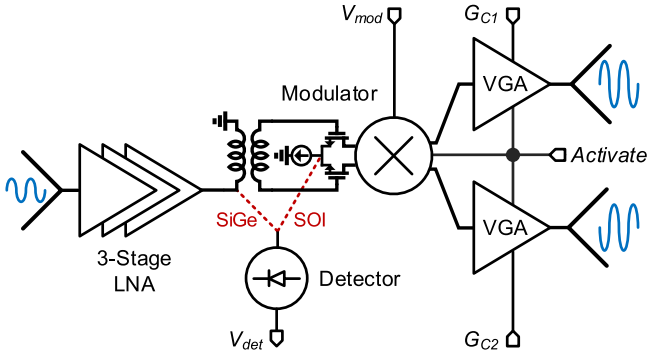


Fig. 9. Block diagram of the mm-wave tag. The detector block connection in the SiGe and SOI implementation is shown with the dashed line.

output impedance of the HBT–HBT cascode has a Q of 15. As a result, the MAG of the HBT cascode is more sensitive to the variation of the quality factor of the output matching network.

IV. Transistor-Level Design for Ultra-Low Power Consumption

The block diagram of the proposed mm-wave tags is shown in Fig. 9. The received FMCW-signal is amplified by a three-stage LNA after which it is simultaneously applied to the detector and to the BPSK modulator. The p and n outputs from the BPSK-modulator are connected to two different variable-gain output stages, each driving a separate transmit antenna with opposite sign. If the signal at the LNA input pad is larger than −62 dBm, the detector output voltage trips and can be used to wake up the BPSK modulator and the two variable-gain output stages, which are otherwise in sleep mode, unbiased. Since the signals at the two transmit antennas are 180° out of phase and have independently adjustable levels, the leakage into the receive antenna can be canceled, or at least minimized, to avoid positive feedback and possible oscillation. The antenna-to-antenna isolation can be further minimized by appropriate antenna spacing and orientation. In a real application scenario, a processor chip will be copackaged with the tag. The processor will read the detector output signal and provide the bias wake-up, modulation, and gain control signals to the tag.

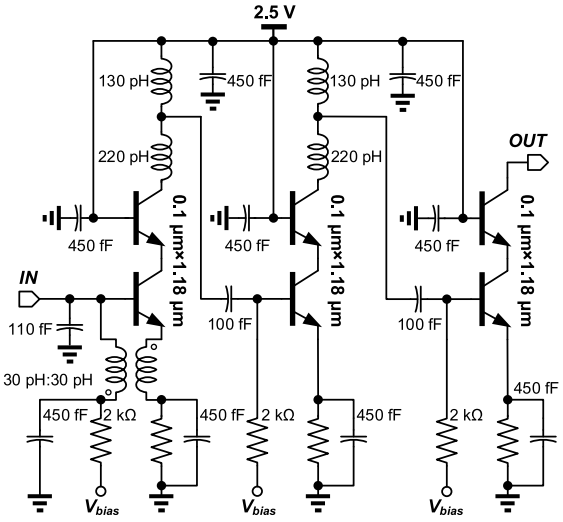


Fig. 10. Schematic of the LNA block implemented in 55-nm SiGe BiCMOS technology.

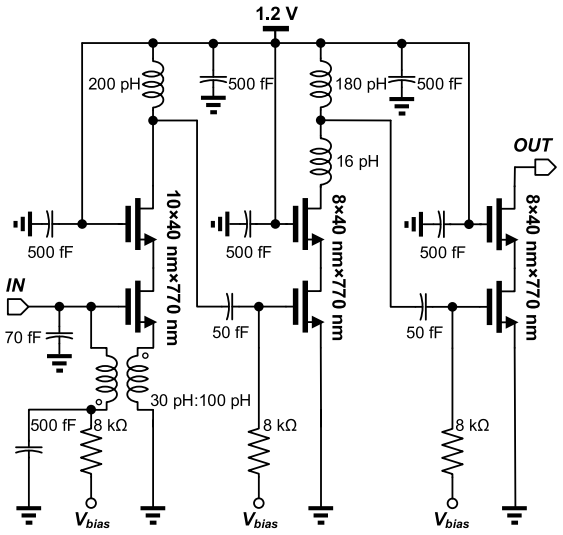


Fig. 11. Schematic of the LNA block implemented in 45-nm SOI CMOS technology.

The design and implementation of each circuit block are discussed in more detail in Sections IV-A–D. The SOI tag operates from a single 1.2-V supply, while the SiGe tag was designed to operate with a supply voltage from 1.8 to 2.5 V.

A. LNA

The schematics of the three-stage SiGe and SOI LNAs are identical and are reproduced in Figs. 10 and 11, respectively. The input stage features shunt–series transformer feedback for broadband impedance and noise matching. The role of the 450- and 500-fF capacitors is to provide low-inductance ac ground at the supply node and at the base/gate of the top HBT/MOSFET in each cascode stage. In the SiGe LNA, resistive emitter degeneration is used to stabilize the dc operating point over temperature and process variation and to make it insensitive to layout ground resistance. The noise generated by the emitter degeneration resistors is shunted by 500-fF capacitors at high frequency.

Resistive degeneration is not needed in the SOI LNA, since the MOSFET bias current is less sensitive to ground resistance variation due to the linear (rather than exponential) dependence of drain current on V_{GS}. Based on the analysis in Section III, all HBTs were sized with an emitter length of 1.18 μm and are biased at the peak-f_{MAX} collector current density of 1.3 mA/μm for maximum gain. In the SOI LNA, all transistors have 40-nm physical gate length and 770-nm gate finger width, and are biased at the peak-f_{MAX} current density of 0.3 mA/μm to maximize gain while also minimizing the noise figure. Furthermore, the input stage is slightly larger than the following stages to facilitate input noise matching. No effort was made to minimize the noise figure of the SiGe LNA by increasing the size of the input HBT cascode for improved noise matching.

B. BPSK Modulator

The BPSK modulator was realized using the double-balanced Gilbert cell topology as shown in Fig. 12(a) and (b). A transformer was used for single-ended-to-differential conversion and to conjugately match the modulator input impedance to the output of the preceding stage. As a compromise between power consumption and matching network realizability, close-to-minimum-size SiGe HBTs, with 0.5-μm emitter length, four-finger nMOSFETs were used in the SiGe and SOI tags, respectively. All transistors in the mixing quad are biased at half the peak-f_{MAX} current density to maximize switching speed and gain [14].

C. Detector

In the case of the SiGe tag, the wake-up detector is connected in parallel with the input of the BPSK modulator [Fig. 12(a)]. It employs a common-emitter differential pair with wide-swing pMOSFET current-mirror load for differential-to-single-ended conversion. The current-mirror output drives a 2.5-V, thick-oxide CMOS inverter which switches ON and OFF the bias current in the BPSK modulator and in the two variable-gain output stages. The differential pair has minimum size HBTs, to maximize the detector *RESP*. The active cascode load provides large gain, maximizing the detector *RESP* with minimal current consumption. For a given supply voltage, this arrangement provides higher output resistance and therefore higher responsivity compared with a resistive load [7], [8]. However, the pMOSFET load increases the 1/f noise corner. The role of the 270-fF MoM capacitors is to filter out any mm-wave signal leakage to the detector output.

In the SOI tag, the wake-up detector is embedded in the modulator stage and employs a common-gate differential topology with a dummy BPSK modulator inserted for symmetry and power-supply rejection. The detector amplifies the common-mode signal formed at the source of the input differential pair, which is proportional to the input signal power. Since nanoscale CMOS detectors have significantly worse *NEP* and *RESP* at mm-wave frequencies than SiGe

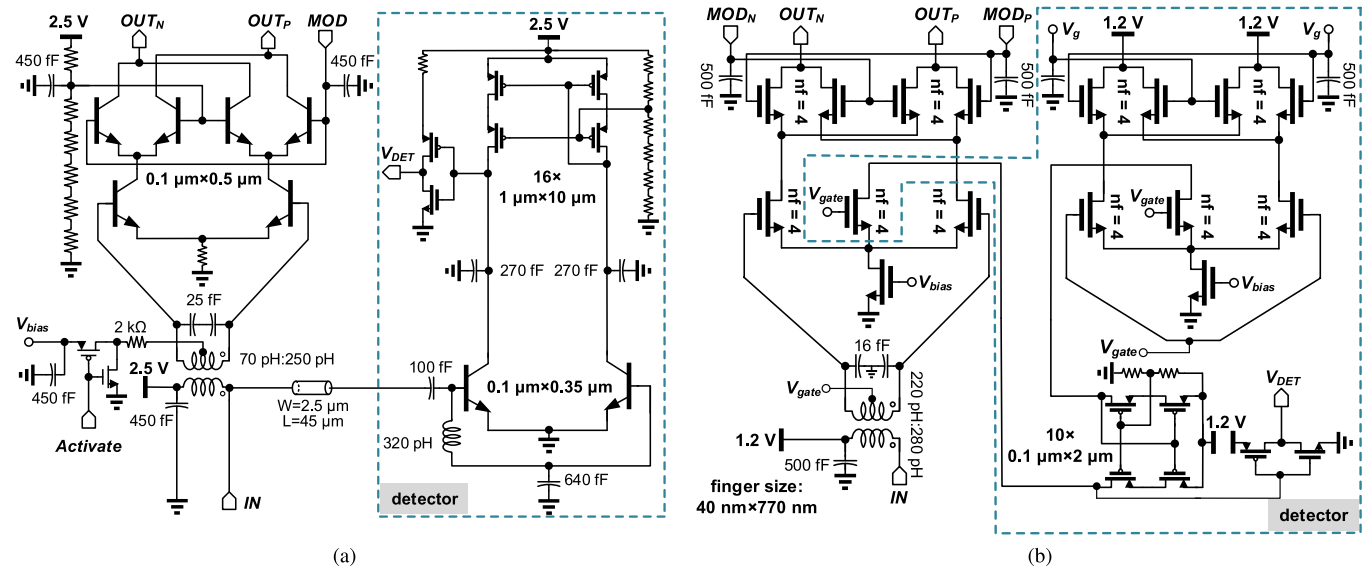


Fig. 12. Schematic of the modulator and detector block implemented in (a) 55-nm SiGe BiCMOS and (b) 45-nm SOI CMOS technologies.

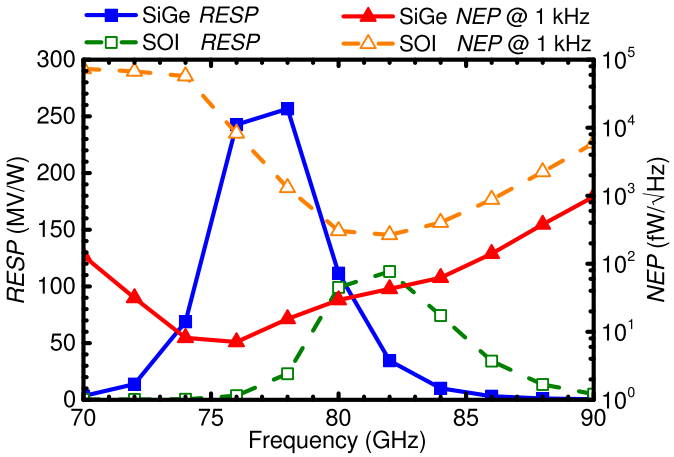


Fig. 13. Simulated *RESP* and *NEP* versus frequency for SiGe and SOI detectors.

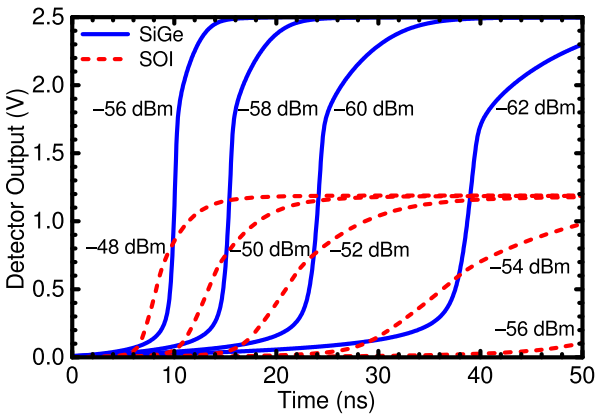


Fig. 14. Simulated SiGe and SOI tags wake-up time as a function of input signal power at 80 GHz.

HBT ones [7], [8], an additional gain stage was inserted after the CMOS detector to further increase its *RESP*. The small MOSFET sizes and the extra gain stage make the CMOS detector sensitive to offset voltage. This is not a problem in the SiGe HBT detector.

The *RESP* and *NEP* are simulated in Fig. 13 for both tags, showing a clear advantage for the SiGe version, as expected [8].

Fig. 14 reproduces the simulated detector output waveforms as a function of the received input signal power. The SiGe tag wakes up at −62 dBm, whereas the SOI version triggers at −56 dBm and takes a longer time to settle because of its lower responsivity.

D. Variable Gain Amplifier

The schematics of the SiGe and SOI variable gain amplifiers (VGAs) are illustrated in Fig. 15. The first uses a common-base topology, whereas a cascode topology is implemented in SOI. Gain control is achieved with classical topology by steering current from the main amplifier path, Q_1, to ac ground through Q_2. In the SOI version, a second, smaller size nMOSFET Q_2 was placed in parallel with the main common-gate transistor, Q_1. To minimize the capacitive parasitic of Q_2 and to maintain a symmetrical layout, the active area of Q_2 was merged with that of Q_1. Only two extra gate fingers were added, one on each side of Q_1. The gate voltage of Q_2 was fixed at 0.85 V through a resistive voltage divider, whereas the voltage at the gate of Q_1 was connected to an external pad for gain control.

V. Chip Fabrication and Packaging

The die microphotographs of the SiGe and SOI tags are shown in Fig. 16. The dies have identical dimensions and padframe and occupy 0.57 × 0.88 mm^2. The input pad is located at the bottom and the two outputs pads are at the top.

The dies were flip-chip mounted on a 23 × 20 mm^2 mini-PCB, which includes the receive and two transmit antennas,

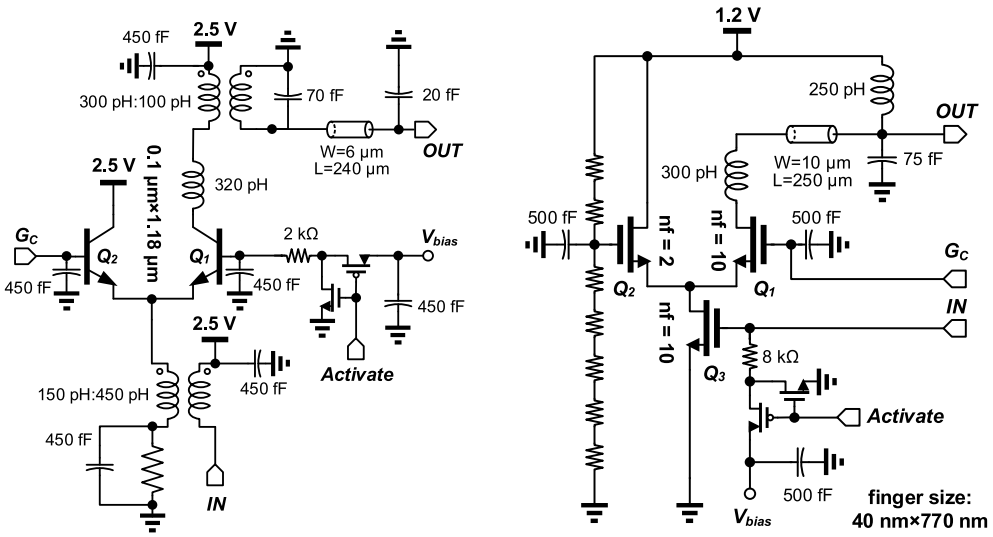


Fig. 15. Schematic of the VGA block implemented in (a) 55-nm SiGe BiCMOS and (b) 45-nm SOI CMOS technologies.

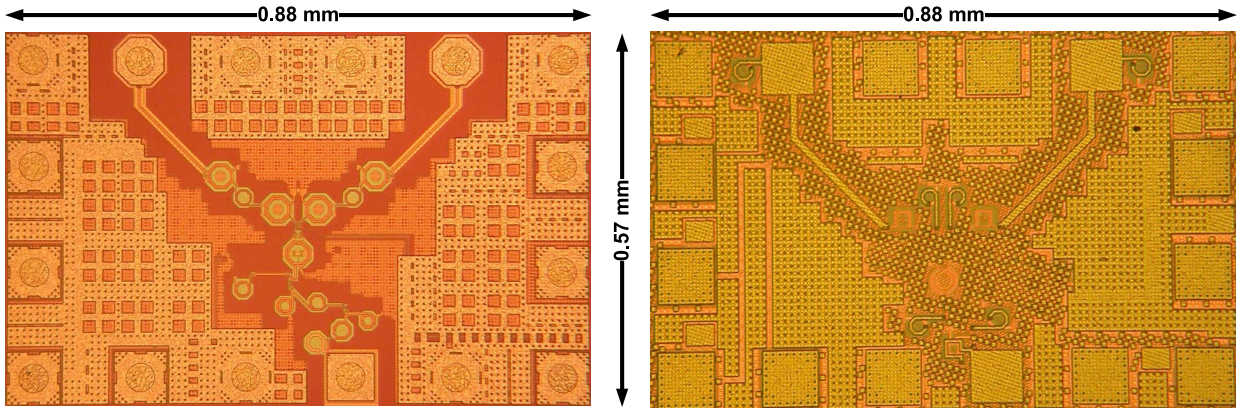


Fig. 16. Chip microphotograph of the mm-wave tag in (a) 55-nm SiGe BiCMOS and (b) 45-nm SOI CMOS technologies. Both chips have a size of 0.57 × 0.88 mm^2.

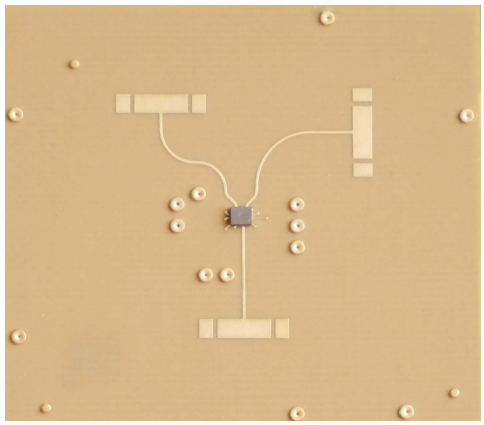


Fig. 17. Tag chip flip-chip mounted on a 23 × 20 mm^2 mini-PCB with two transmit and one receive antennas.

as illustrated in Fig. 17. To improve gain and isolation, the antennas are spaced farther apart and at different orientations than on the 7 × 7 mm^2 flexible interposer in [5] and [6].

VI. Experimental Results

The SiGe BiCMOS and SOI tags were first probed on die. The wake-up detector functionality was verified only in the SiGe tag. The SOI detector output was activated even in the absence of an input signal. It is suspected that the offset voltage of the MOSFET differential pair in the detector is too large and trips the CMOS inverter. Link demonstration experiments were conducted only on the packaged SiGe BiCMOS tags.

A. On-Die Measurements

Fig. 18 compiles the measured S-parameters and 50-Ω noise figure, NF_{50}, for both tags. The Agilent 75–88-GHz N8975A-K88 single-sideband downconverter and the N8975A noise figure analyzer were used together with the ELVA W-band noise source with built-in isolator to measure NF_{50}. In these measurements, the SiGe tag draws 10 mA from 2.5 V, whereas the SOI tag was biased at 15 mA from 1.2 V. The SiGe and SOI tags have almost identical performance, with 19- and 20-dB gain, respectively, between the LNA input and each VGA output. The input reflection coefficient, S_{11},

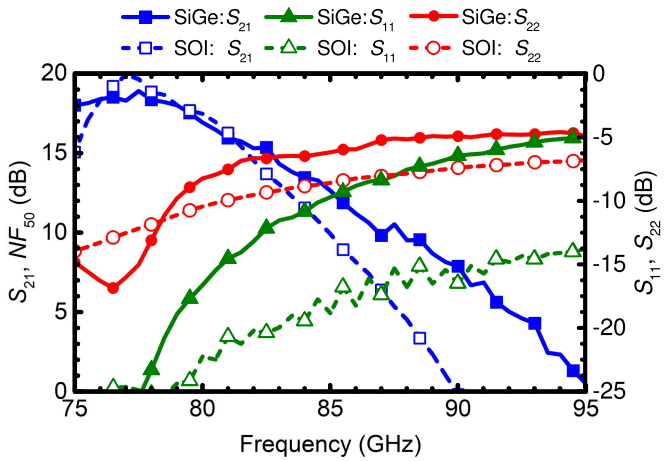


Fig. 18. Measured tag S-parameters in the W-band. Solid and dash lines correspond to SiGe and SOI tags, respectively.

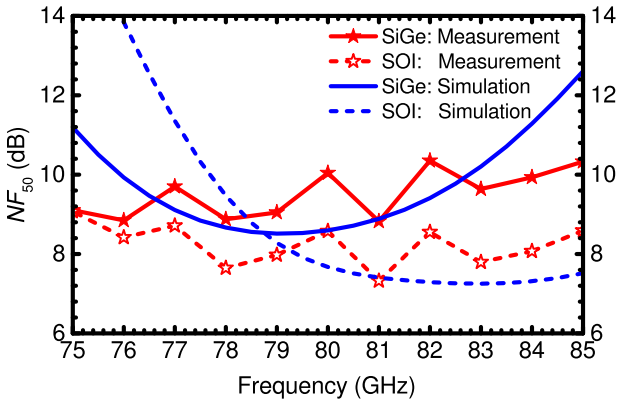


Fig. 19. Measured and simulated tag NF_{50} in the W-band. Solid and dash lines correspond to SiGe and SOI tags, respectively.

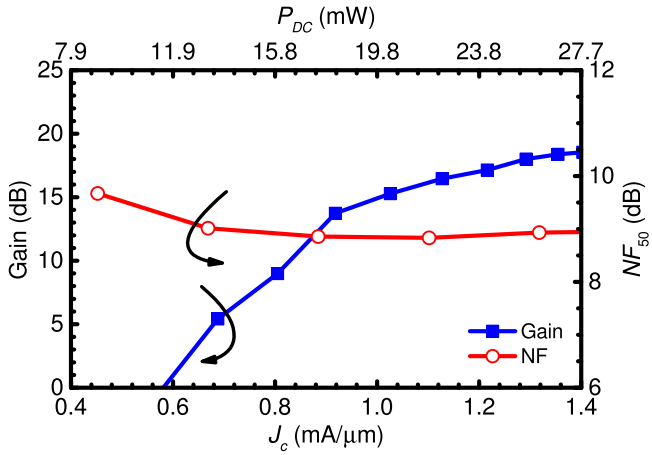


Fig. 20. Measured gain from the input to one output and NF_{50} versus current density for the SiGe tag at 79 GHz.

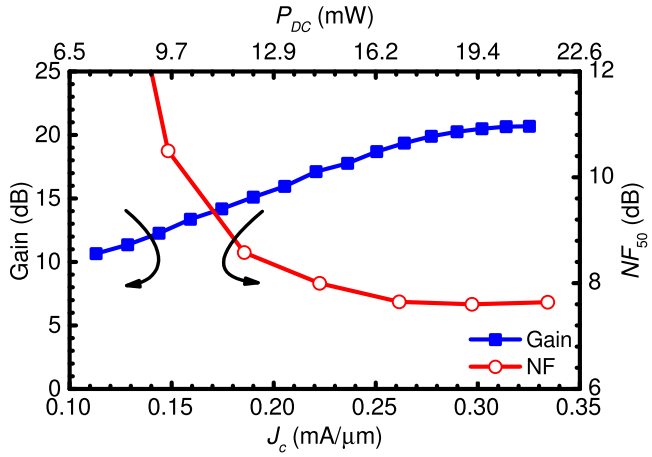


Fig. 21. Measured gain from the input to one output and NF_{50} versus current density for the SOI tag at 78 GHz.

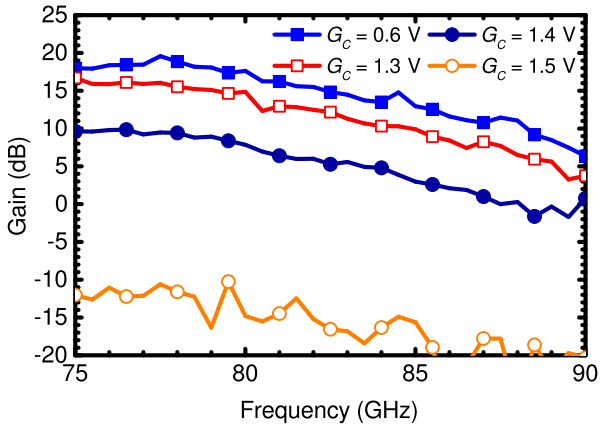


Fig. 22. Measured tag gain from the input to one output as a function of the gain control voltage and frequency in SiGe tag.

remains lower than −15 dB from 75 to 81 GHz and from 75 to 86 GHz for the SiGe and SOI tags, respectively.

Although the available VNA does not cover the 67–75-GHz range, measurements below 67 GHz reported in [5] and [6] indicate that the 3-dB bandwidth is 9 GHz for the SiGe tag and 5 GHz for the SOI tag. The measured 50-Ω noise figure is less than 9 and 8 dB, respectively. A comparison between measured and simulated noise figure for both SiGe BiCMOS and the SOI CMOS tags is provided in Fig. 19. It shows good agreement between measurements and simulations. Nevertheless, the simulated noise figure of the SOI tag has a minimum at a slightly higher frequency than that of the measured noise figure.

A breakout of the SiGe LNA was also fabricated and measured. It showed excellent S_{11} and S_{22} and a peak gain of 30 dB while consuming 11.25 mW from 2.5 V. The LNA gain decreases to 26 dB and the power consumption reduces to 8.1 mW when the supply voltage is 1.8 V [5].

To illustrate the tradeoff between gain, noise figure, and power consumption, Figs. 20 and 21 show the measured gain and NF_{50} of the SiGe and SOI tags as a function of the current density in the input cascode at 79 and 78 GHz, respectively. The optimum noise figure current density is 1.15 and 0.3 mA/μm for the SiGe and SOI tags, respectively. Figs. 20 and 21 also show that the power consumption can be reduced almost in half, with minimal degradation of noise figure, if the tag gain is reduced to 15 dB.

The gain control is demonstrated in Figs. 22 and 23. Both chips allow for more than 20 dB of the gain control, although only a small range of that is needed to balance the outputs.

The measured output spectrum of the SOI tag die is reproduced in Fig. 24 when a 77.4-GHz input signal is BPSK-modulated by a 500-kHz sine wave. More than 35 dB

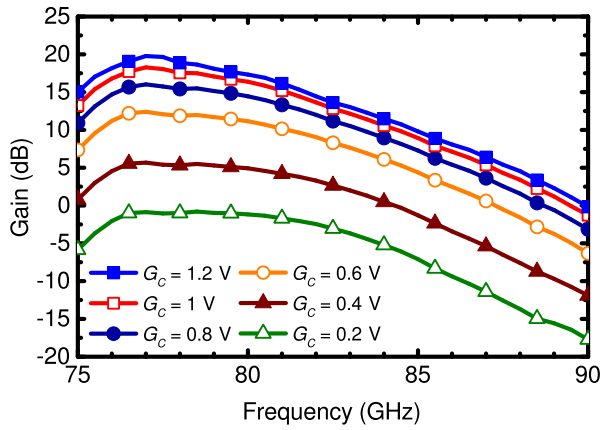


Fig. 23. Measured tag gain from the input to one output as a function of the gain control voltage and frequency SOI tag.

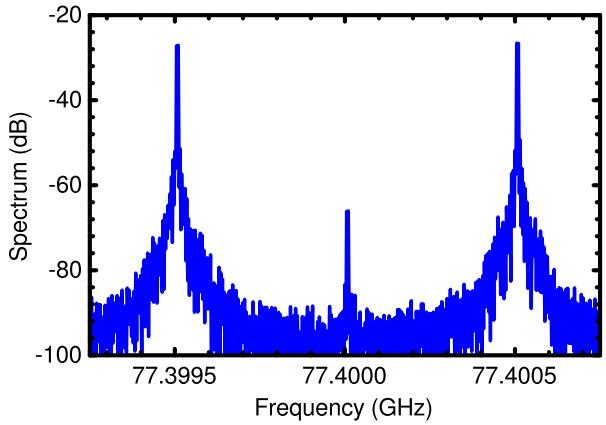


Fig. 24. Spectra of a 77.4-GHz carrier BPSK-modulated with a 500-kHz sinusoid for SOI tag.

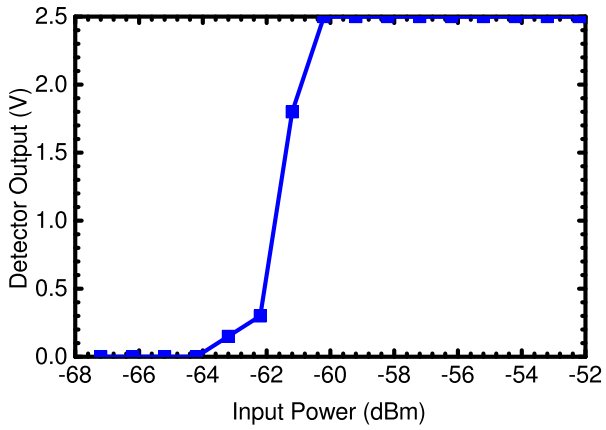


Fig. 25. Measured SiGe tag detector output voltage versus input power.

of carrier suppression can be observed, indicating negligible parasitic amplitude modulation.

Fig. 25 shows the detector output of the SiGe tag switching at $P_{\text{in}} = -61.2$ dBm, in very close agreement with the simulations in Fig. 25.

B. In-Package Measurements

The measurement setup in Fig. 26 was used to verify the functionality and link distance of the packaged SiGe tag. It consists of a *W*-band multiplier signal source with 0-dBm output power and a 20-dBi horn antenna as the FMCW base station transmitter, and a second 20-dBi horn antenna connected to a *W*-band harmonic downconvert mixer as the base station receiver. The packaged SiGe tag was placed at a distance of 5 m from the FMCW source.

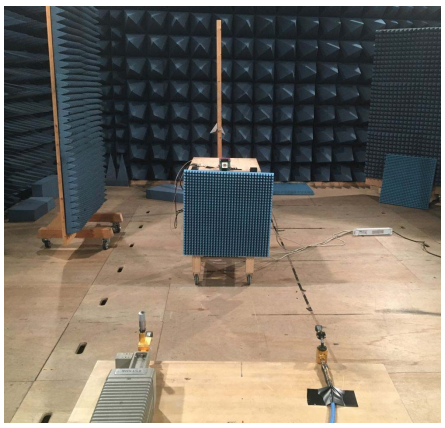


Fig. 26. Photograph of the measurement setup in an anechoic chamber.

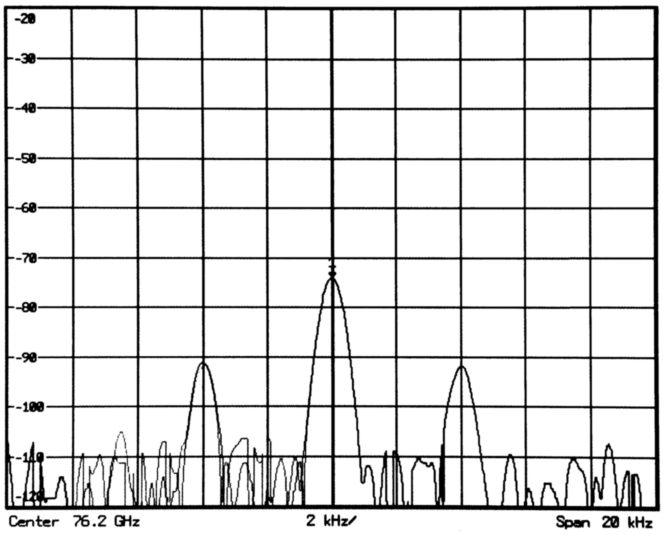


Fig. 27. Measured spectra, in dB, of a received 76.2-GHz carrier BPSK-modulated by a 4-kHz sinusoid applied at BPSK pad of the packaged SiGe tag placed 5 m away from the base station.

Propagation experiments were conducted with BPSK modulation at 4 kHz and with AM modulation at 10 kHz. In both the cases, the carrier frequency was 76.2 GHz. The AM modulation was applied to the variable gain pads. The corresponding spectra, captured by the spectrum analyzer connected to the base station receiver, are provided in Figs. 27 and 28, respectively. The SNR is better than 18 dB in both the cases, in agreement with the system link simulations in Section II.

Finally, Fig. 29 reproduces the measured power of the sideband received from a 76.2-GHz carrier BPSK-modulated with a 4-kHz sine wave by the SiGe tag as a function of the distance between the tag and the base station. Both copolarized and cross-polarized antenna measurements are reported and compared with theory. Again, close agreement is obtained with the theoretical power calculations using Friis's transmission equation.

Table II summarizes the performance of the two tags and compares it with the state of the art. The 55-nm SiGe BiCMOS

TABLE II
COMPARISON WITH THE STATE OF ART

	This Work	This Work	[3]	[11]	[2]	[10]	[12]
Type	Active	Active	Active	Active	Passive	Passive	Passive
Technology	55-nm BiCMOS	45-nm SOI CMOS	250-nm BiCMOS	180-nm CMOS	GaAs PIN diode	GaAs Shottkey diode	180-nm CMOS
f_0 [GHz]	78	77	34.45	5.8	76	61	24
BW [GHz]	9	5	0.5	0.15	1	0.5	0.25
NF [dB]	9	8	N.A.	N.A.	N.A.	N.A.	N.A.
Gain [dB]	19	20	N.A.	N.A.	N.A.	N.A.	N.A.
Sensitivity [dBm]	−62	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.
Wake-up Functionality	Yes	No	No	No	No	No	Yes
P_{DC} [mW]	25/10.8*	18	122§§	54	N.A.	5	0.039/0.013*

* Active/Idle §§ Includes interface and pulse generation

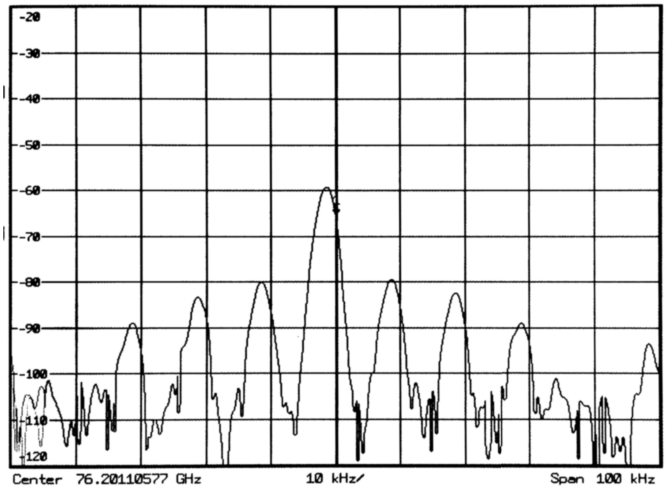


Fig. 28. Measured spectra, in dB, of a received 76.2-GHz carrier AM-modulated by a 10-kHz sinusoid applied at the gain-control pads of the packaged SiGe tag placed 5 m away from the base station.

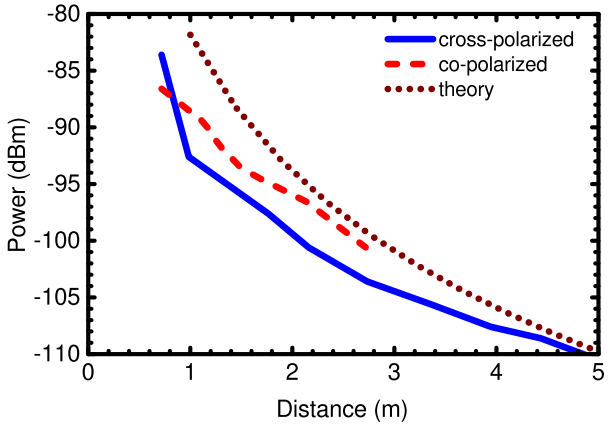


Fig. 29. Received copolar and cross-polar sideband power versus distance in the base station-tag measurement setup. The dotted line shows the theoretical expected power level.

tag has the highest functionality, with similar gain, noise figure, and power consumption as the 45-nm SOI CMOS tag operating in the same frequency range. It includes a wake-up function with a sensitivity of −62 dBm. In the idle mode, only the LNA and the detector are ON, consuming 10.8 mW from 1.8 V. When the input signal exceeds −62 dBm, the output of the wake-up detector changes logic states and activates all blocks in the tag. In active mode, the SiGe tag consumes 25 mW from 2.5 V and has 19-dB gain, 9-dB noise figure, and 9-GHz bandwidth centered on 77 GHz.

VII. CONCLUSION

Active mm-wave reflectors with one receive and two transmit channels were studied and demonstrated for the first time at the W-band, in 55-nm SiGe BiCMOS and 45-nm SOI CMOS commercial technologies. A comparative study was conducted for SiGe HBT and SOI CMOS cascode topologies and the impact of the quality factor of the passive matching networks on amplifier gain and power consumption in order to establish the best system architecture and best circuit topologies in both technologies were studied. Simulations and on-die measurements have confirmed that similar performance can be achieved for SiGe and SOI tags. The SiGe and SOI tag measurements show 19- and 20-dB gain, 9- and 5-GHz bandwidth, a noise figure of 9 and 8 dB, respectively, and 20 dB of independent gain control for each transmit channel. The built-in wake-up detector on the SiGe tag has an input sensitivity level of −62 dBm and can be used to put the tag in either active or idle mode, further saving power in the absence of an interrogating signal from the FMCW radar base station.

ACKNOWLEDGMENT

The authors would like to thank STMicroelectronics and Globalfoundaries for chip fabrication and donation. They would also like to thank CMC for CAD tools, Integrand for the EMX simulation software, and J. Pristupa for CAD support.

REFERENCES

[1] A. Müller, D. Neculoiu, P. Pursula, T. Vähä-Heikkilä, F. Giacomozzi, and J. Tuovinen, "Hybrid integrated micromachined receiver for 77 GHz millimeter wave identification systems," in *Proc. Eur. Conf. Wireless Technol.*, Munich, Germany, Oct. 2007, pp. 276–279.

[2] C. M. Schmid, R. Feger, and A. Stelzer, "Millimeter-wave phase-modulated backscatter transponder for FMCW radar applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Baltimore, MD, USA, Jun. 2011, pp. 1–4.
[3] A. Strobel, C. Carlowitz, R. Wolf, F. Ellinger, and M. Vossiek, "A millimeter-wave low-power active backscatter tag for FMCW radar systems," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 1964–1972, May 2013.
[4] T. Kiuru, P. Pursula, J. Rajamäki, and T. Vähä-Heikkilä, "A 60-GHz semipassive MMID transponder for backscattering communications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Seattle, WA, USA, Jun. 2013, pp. 1–3.
[5] M. S. Dadash, J. Hasch, P. Chevalier, A. Cathelin, and S. P. Voinigescu, "A W-band active millimeter-wave tag IC with wake-up function," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Honolulu, HI, USA, Jun. 2017, pp. 1531–1534.
[6] M. S. Dadash, J. Hasch, and S. P. Voinigescu, "A 77-GHz active millimeter-wave reflector for FMCW radar," in *Proc. IEEE RFIC Symp.*, Honolulu, HI, USA, Jun. 2017, pp. 312–315.
[7] A. Tomkins, P. Garcia, and S. P. Voinigescu, "A passive W-band imaging receiver in 65-nm bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 1981–1991, Oct. 2010.
[8] E. Dacquay *et al.*, "*D*-band total power radiometer performance optimization in an SiGe HBT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 813–826, Mar. 2012.
[9] A. Balteanu *et al.*, "A 2-bit, 24 dBm, millimeter-wave SOI CMOS power-DAC cell for watt-level high-efficiency, fully digital m-ary QAM transmitters," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1126–1137, May 2013.
[10] W. Stein, A. Aleksieieva, S. Roehr, and M. Vossiek, "Phase modulated 61 GHz backscatter transponder for FMCW radar-based ranging," in *Proc. German Microw. Conf. (GeMiC)*, Aachen, Germany, Mar. 2014, pp. 1–4.
[11] S. Wehrli, R. Gierlich, J. Huttner, D. Barras, F. Ellinger, and H. Jackel, "Integrated active pulsed reflector for an indoor local positioning system," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 2, pp. 267–276, Feb. 2010.
[12] H. Dagan *et al.*, "A low-power low-cost 24 GHz RFID tag with a C-flash based embedded memory," *IEEE J. Solid-State Circuits*, vol. 49, no. 9, pp. 1942–1957, Sep. 2014.
[13] P. Chevalier *et al.*, "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz f_T/370 GHz f_{MAX} HBT and high-Q millimeter-wave passives," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2014, pp. 3–9.
[14] S. P. Voinigescu, *High-Frequency Integrated Circuits*. New York, NY, USA: Cambridge Univ. Press, 2013, chs. 9–11.

M. Sadegh Dadash (S'11) received the B.A.Sc. degree in electrical engineering from Isfahan University of Technology, Isfahan, Iran, in 2009, and the M.Sc. degree in electrical engineering from McMaster University, Hamilton, ON, Canada, in 2011. He is currently pursuing the Ph.D. degree at the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada.

His current research interests include millimeter-wave integrated circuits, low-power sensors, and integrated passive components.

Jürgen Hasch (M'99–SM'13) received the Dipl.-Ing. degree and Dr.-Ing. degree from the University of Stuttgart, Stuttgart, Germany, in 1996 and 2007, respectively.

He is a Senior Expert on RF technology at the corporate research of Robert Bosch GmbH, Renningen, Germany, where he is responsible for several EU and German public funded projects and university cooperations.

Dr. Hasch is a member of MTT TCC-27 and ITG-FA Mikrowellentechnik. He serves as Reviewer for several journals and conferences. His main interests are RF based sensing technologies, integrated millimeter-wave sensors in the 60-240 GHz range, and on-chip antennas. He has authored or co-authored more than 40 scientific papers and holds more than 15 patents.

Pascal Chevalier (M'06) received the Ph.D. degree in electronics from the University of Lille, in 1998 for his work on AlInAs/GaInAs InP-based HEMT.

He joined Alcatel Microelectronics, Oudenaarde, Belgium, in 1999, where he contributed to the start of RF BiCMOS and led the development of 0.35-μm SiGe BiCMOS technologies. Since joining STMicroelectronics, Crolles, France, in 2002, he has been involved in the development of SiGe BiCMOS technologies, from 0.13-μm to 55-nm nodes, and led the research on advanced RF and millimeter-wave silicon-based devices such as SiGe HBTs and Si LDMOS transistors for CMOS derivatives technologies. He is currently managing the Mixed Signal & BiCMOS Technologies R&D team and is a Senior Member of Technical Staff. He has authored or co-authored over 150 technical journal papers and conference publications.

Dr. Chevalier has served the Technical Program Committee of the IEEE Bipolar / BiCMOS Circuits and Technology Meeting (BCTM) from 2005 to 2009. He has been a member of the RF & AMS Technologies section of the ITRS from 2006 to 2015 of which he led the Silicon Bipolar & BiCMOS subgroup. He serves the ECS SiGe Symposium Committee since 2014 and joined again the BCTM Technical Program Committee in 2015.

Andreia Cathelin (M'04–SM'11) started electrical engineering studies at the Polytechnic Institute of Bucarest, Romania and graduated with the engineering degree and M.S. degree from the Institut Supérieur d'Electronique du Nord (ISEN), Lille, France in 1994. In 1998 and 2013 respectively, she received the Ph.D. and habilitation à diriger des recherches (French highest academic degree) from the Université de Lille 1, France.

Since 1998, she has been with STMicroelectronics, Crolles, France, now a Fellow in digital front-end manufacturing and technology. Her major fields of interest are in the design of RF/mmW/THz and ultra-low-power circuits and systems. She has had numerous responsibilities inside the IEEE community since more than 10 years.

Dr. Cathelin has been the RF Sub-Committee Chair from 2012 to 2015 of ISSCC, and since 2016 is the Forums Chair and a member of the Executive Committee. She is a member of ESSCIRC TPC since 2005. Since September 2013, she is on the Steering Committee of ESSCIRC-ESSDERC conferences, where she has been the Chair from 2015 to September 2017. During her mandate as ESSxxRC Steering Committee Chair, two major MoUs have been signed with, respectively, SSCS and EDS societies, bringing now both conferences among the top ranked conferences in the respective fields, as financially fully sponsored events. She has served different positions on the Technical Program Committees of VLSI Symposium on Circuits from 2010 until 2016. She has been Guest Editor of the IEEE JOURNAL ON SOLID-STATE CIRCUITS Special Issue on VLSI Symposium in April 2016. She has authored or co-authored 130+ technical papers and 7 book chapters, and has filed more than 25 patents. She was a co-recipient of the ISSCC 2012 Jan Van Vessem Award for Outstanding European Paper and of the ISSCC 2013 Jack Kilby Award for Outstanding Student Paper, as well as the winner of the 2012 STMicroelectronics Technology Council Innovation Prize. She is an elected member of the IEEE SSCS Adcom for the term January 2015 to December 2017, and an active member of the IEEE SSCS Women in Circuits group.

Ned Cahoon received the A.B. degree in physics from Harvard University in 1980.

In 1980, he joined IBM, Poughkeepsie, NY, USA, where he worked in engineering and management positions responsible for DRAM reliability and assurance in IBM's Data System Division. In 1988, he moved to IBM's Microelectronics Division where he contributed to the research and development of AlGaAs and InP laser technology. Beginning in 1991, he managed engineering teams in IBM's MLC packaging lab and manufacturing plant. In 1995, he was part of a new business initiative within IBM with the mission to develop and commercialize SiGe technology, and he has been involved in the RF Business Unit of IBM and now GLOBALFOUNDRIES ever since. He is currently a Director at GLOBALFOUNDRIES, responsible for business development of SiGe and RFSOI technologies.

Sorin P. Voinigescu (M'90–SM'02–F'17) received the M.Sc degree in electronics from the Polytechnic Institute of Bucharest, Romania, in 1984, and the Ph.D. degree in electrical and computer engineering from the University of Toronto, Canada, in 1994.

He holds the Stanley Ho Chair in Microelectronics and is the Director of the VLSI Research Group in the Electrical and Computer Engineering Department at the University of Toronto, which he joined in 2002. During the 1984-1991 period, he worked in microwave and quantum semiconductor device and circuit research, and as an Assistant Professor in Bucharest. Between 1994 and 2002 he was first with Nortel and later with Quake Technologies in Ottawa, Canada. From 2008 to 2009 and 2015 to 2016, he spent sabbatical leaves at Fujitsu Laboratories of America, Sunnyvale, California, at NTT's Device Research Laboratories in Atsugi, Japan, at UNSW in Sydney, Australia, and at Robert Bosch GmbH in Germany, exploring technologies and circuits for 128 GBaud fiber-optic systems, 300Gb/s mm-wave radio transceivers, imaging and radar sensors. He co-founded and was the CTO of two fabless semiconductor start-ups: Quake Technologies and Peraso Technologies.

Dr. Voinigescu was a member of the International Technology Roadmap for Semiconductors RF/AMS Committee between 2008 and 2015, served on the TPC and ExCom of the IEEE CSICS from 2003 until 2013, and is a member of the ExCom of the IEEE BCTM. He received Nortel's President Award for Innovation in 1996 and is a co-recipient of the Best Paper Award at the 2001 IEEE CICC, the 2005 IEEE CSICS, and of the Beatrice Winner Award at the 2008 IEEE ISSCC. His students have won several Best Student Paper Awards at IEEE VLSI Circuits Symposium, IEEE IMS, IEEE RFIC, and IEEE BCTM. In 2013 he was recognized with the ITAC Lifetime Career Award for his contributions to the Canadian Semiconductor Industry.