Design and Scaling of W-Band SiGe BiCMOS VCOs

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Abstract — This paper discusses the design of 87-105GHz Colpitts VCOs fabricated in two generations of SiGe BiCMOS technology, with MOS and HBT varactors and with integrated inductors. Based on a study of the optimal biasing conditions for minimum phase noise, it is shown that VCOs can be used to monitor the mm-wave performance of SiGe HBTs. Measurements show a 105GHz VCO operating from 2.5V with phase noise of -101dBc/Hz at 1 MHz offset, which delivers +2.7dBm of differential output power at 25°C, with operation up to 125°C. A BiCMOS VCO with a differential MOS-HBT cascode output buffer using 130nm MOSFETs delivers +10dBm of output power at 87GHz.

Index terms — Millimeter-wave integrated circuits, phase-noise, SiGe BiCMOS technology, voltage-controlled oscillators, W-band voltage-controlled oscillators, process monitor.

I. INTRODUCTION

Millimeter wave applications in the W-band, particularly automotive and weather radar at 77GHz and 94GHz, have typically been the territory of III-V technology. However, the latest SiGe processes with f_T/f_{MAX} above 150GHz [1-6] allow them to compete directly with III-V technologies for applications in the W-band (75-110GHz). Many W-band radar transceivers and communications circuits require a phase-locked loop, in which the VCO [7] and the frequency divider are the most critical components. Fig. 1 compares the phase noise of state-of-the-art W-band SiGe and CMOS VCOs [8-13] along with those presented in this paper.



Fig. 1. Phase noise of state-of-the-art SiGe HBT and CMOS W-band oscillators (with process f_T/f_{MAX}) *(this work shown with open symbols).*

As the level of integration in W-band circuits increases, high yield processes must be developed, and circuit scaling between successive SiGe technology generations must be understood. Key process monitor circuits are required to investigate both issues. Given the complexity and variability of noise parameter measurements above 50 GHz, Colpitts oscillators can be employed to monitor the W-band noise performance of SiGe HBTs just as ring oscillators are used as CMOS process speed monitors. While such a monitoring technique does not allow the direct determination of SiGe HBT noise parameters, comparing the phase noise and output power of a VCO fabricated on several wafer splits allows the relative performance of the HBTs to be deduced. In this fashion, the profile of the HBT can be optimized for mm-wave performance.

This paper presents a Colpitts oscillator topology with compact layout, suitable for low-voltage, low-phase noise applications in the W-band, and explores the impact of technology scaling on VCO performance. Also presented is a low-voltage SiGe BiCMOS output buffer using 0.13µm MOSFETs, suitable for W-Band applications.

II. VCO AND OUTPUT BUFFER TOPOLOGY

The differential Colpitts topology [7] is a common choice for low-phase noise, mm-wave VCOs [8]-[11], [13, [14]. Fig. 2 reproduces the schematic of our SiGe BiCMOS implementation of this topology.



Fig. 2. Colpitts oscillator schematic.

In an effort to minimize the supply voltage and phase noise, and to simplify layout (layout is critical at 100GHz), a single transistor topology is employed. A MiM capacitor (C_1) in parallel with c_{π} improves negative resistance and reduces phase noise by shunting the base resistance, as illustrated in Fig. 2 (c). Negative Miller capacitors (C_M) are placed at the BC junctions to cancel the effect of C_{BC} (see Fig. 2 (a)). Finally, fully differential tuning with MOS varactors is used for better supply noise rejection. Differential tuning also reduces the modulation of the varactor capacitance (C_{VAR}) by the tank voltage, which helps to suppress the maximum in phase noise at the center of the tuning range seen in some other VCOs [13]. The varactor layouts are optimized for high-Q as in [13]. Where appropriate, spiral inductors are used in place of transmission lines to achieve a compact layout. When

MOSFETs are not available, HBT varactors, shown in Fig. 2 (b), can be used instead, with a performance penalty.

To obtain yet larger output power, and further isolate the VCO tank from external noise sources, an output buffer can be added to the VCO. The most common circuit topology for a powerful output buffer is the HBT cascode, shown in Fig 3 [8]. While +19dBm output power at 77GHz has been achieved using the HBT cascode, the topology has significant DC power consumption. The high input time constant of the buffer HBT [14] requires that it be driven by an emitter follower. DC power is thus wasted in the intermediate emitter follower stage. Furthermore, the topology requires a high supply voltage, further increasing power consumption. The power consumption problem becomes particularly apparent in mm-wave imaging applications, where multiple transceivers are required [16].



Fig 3. HBT cascode output buffer for W-band VCOs [8].

To reduce the supply voltage of the VCO output buffer, the input HBTs are replaced with 130nm MOSFETs, forming the MOS-HBT cascode shown in Fig 4. The 130nm MOSFETs have better linearity at high input voltage swings, and a lower input time constant, and can thus be driven by the VCO directly [14]. The tail current source in [8] is eliminated, and the MOSFETs require less voltage headroom, allowing the supply voltage of the buffer to be reduced from 5.5V to 2.5V.



Fig 4. MOS-HBT cascode output buffer for W-band VCOs.

III. CIRCUIT DESIGN METHODOLOGY

Voltage Controlled Oscillator

The oscillation frequency (f_{osc}) of the VCO is given by (1). Two VCOs were designed at 100GHz and 87GHz. In line with the VCO design methodology outlined in [13], the tank inductance (L_B) is chosen as the smallest realizable inductance with acceptable Q, or about 25pH given the technology back-end (the inductor design methodology is described in [23]). Thus, C_{EFF} is fixed by the desired oscillation frequency. In reality, c_{π} is much greater than C_{VAR} , and consequently, $C_{EFF} \approx C_{VAR}$ for initial design purposes.

$$f_{osc} = \frac{1}{2\pi\sqrt{L_B C_{EFF}}} \quad \text{where} \quad C_{EFF} = \frac{C_{VAR}(C_1 + C_{\pi})}{C_{VAR} + C_1 + C_{\pi}} \tag{1}$$

The negative resistance provided by Q_1 , given by (2), must be large enough to overcome the base resistance and other tank losses. In the W-band, the finite Q of the varactor (C_{VAR}) and base inductance (L_B) add substantial losses to the tank. Alternatively, (2) can be recast as (3), where τ_F is the transit time through the base and collector. From (3), biasing at peak f_T current density maximizes R_{NEG} , and therefore allows the largest values of C_1 and C_{VAR} , given ω_{osc} .

$$R_{NEG} = R_B + \frac{\omega_{osc} L_B}{Q_{LB}} + \frac{1}{\omega_{osc} Q_{CVAR} C_{VAR}} - \frac{g_m}{\omega_{osc}^2 (C_\pi + C_1) C_{VAR}}$$
(2)

$$R_{NEG} = (Tank \ losses) - \frac{I_C/V_T}{\omega_{osc}^2(\tau_F I_C/V_T + C_1)C_{VAR}}$$
(3)

Capacitor C_1 is important in minimizing the oscillator phase noise, vital in radar applications [9]. The phase noise of the Colpitts oscillator is given by (4), where I_n represents the noise contribution of the transistor, and $|V_{tank}|$ is the tank swing [18].

$$S_{\Delta out} = 2 \frac{\left\langle \left| I_n \right|^2 \right\rangle}{\left| V_{\text{tank}} \right|^2} \frac{1}{\left(C_1 + C_\pi \right)^2 \left(\frac{C_1 + C_\pi}{C_{\text{var}}} + 1 \right)} \frac{1}{\Delta \omega^2}$$
(4)

To minimize phase noise in 40GHz VCOs, in [13,14], it was shown that Q_1 should be biased at the NF_{MIN} current density, which minimizes I_n. In the W-band, the correlation between base and collector noise currents (illustrated in Fig 5) pushes the optimum NF_{MIN} current density closer to the peak f_T current density [15]. Furthermore, biasing at peak f_T current density increases the tank swing, and enables larger values of C₁ and C_{VAR} to meet the oscillation condition in (2). Because $|V_{tank}|$, C₁, and C_{VAR} all appear in the denominator of (3), the optimum phase noise bias current density of W-band VCOs shifts toward peak f_T current density.

Table 1 summarizes the design parameters for the 87GHz and 100GHz VCOs designed for lowphase noise and biased at the peak f_T current density. The different emitter sizes will be discussed in section 4, Fabrication and Layout.



Fig 5. Correlation of base and collector shot noise currents where τ_n is the noise transit time.

fosc	87GHz	100GHz
LB	28pH	23pH
L _C	35pH	35pH
L _{EE}	200pH	200pH
C _{VAR}	$2 \times 24 \times 1 \mu m \times 130 nm$	2×18×1µm×130nm
	NMOS varactor	NMOS varactor
C1	100fF	80fF
I _C	24mA	24mA
A _E	4×5×0.17µm or	4×5×0.17µm or
	4×5×0.13µm	4×5×0.13µm

TABLE 1. VCO DESIGN PARAMETERS

MOS-HBT Cascode Output Buffer

All transistors in the output buffer are biased at peak f_T current density for maximum speed and linearity [17]. The transistor sizes and bias currents are chosen such that the buffer delivers +10dBm simulated output power per side into a 50 Ω load. The cascode bias voltage (1.8V-1.9V) is chosen to set the drain-source voltage of Q_1 equal to 0.9V when the supply voltage is 2.5V.

Components C_G , T_G , and L_G perform DC blocking, and impedance match the VCO to the buffer. In fact, the parallel gate inductance L_G in Fig 4 is chosen to resonate with C_{GS1} , maximizing the buffer input impedance, which is otherwise very low because of the large transistor sizes needed to carry the bias current. T_M is added to maximize the f_T of the cascode [19], whereas L_S improves linearity and stability, and increases the buffer input impedance.

Table 2 summarizes the design parameters for output buffer.

f _{center}	87GHz
L _C	35pH
T _M	20µm of 50Ω t-line
I _C	40mA
M ₁	66×2µm×130nm
Q ₂	4×8×0.17μm

TABLE 2: OUTPUT BUFFER DESIGN PARAMETERS.

IV. FABRICATION AND LAYOUT

The 100GHz VCO, with the architecture shown in Fig. 2, was designed and fabricated in a SiGe BiCMOS process with f_T/f_{MAX} of 150GHz/160GHz, (referred to as "BiC9" [1]), and two SiGe HBT process splits with f_T/f_{MAX} of 230/300GHz and 260GHz/270GHz, referred to as BipX1 and BipX2 respectively [2]. The measured f_T/f_{MAX} of the HBTs in the three technologies are illustrated in Fig 6 and summarized in Table 3. The three technologies are identical except for the HBTs (also MOSFETs are not available in BipX), which allows investigation of the impact of SiGe HBT scaling on mm-wave VCO performance. Furthermore, the different HBTs are directly substitutable in the layout view, and therefore the VCO layout need not be modified when porting between the technologies. Consequently, measurement results from all three VCOs can be compared directly.



Fig 6. Characteristics of two generations of SiGe technology.

Technology	f_{T}	f _{MAX}	Emitter
Name	(GHz)	(GHz)	width (µm)
BiC9	150	160	0.17
BipX1	230	300	0.13
BipX2	260	270	0.13

TABLE 3. SIGE TECHNOLOGY F_T and F_{MAX} .

Because MOSFETs are not yet available in BipX1 and BipX2, two versions of the 100GHz VCO were designed, one with the differential MOS varactor tuning illustrated in Fig. 2 (a), and another with single-ended HBT varactors, as illustrated in Fig. 2 (b). Because MOSFETs are required, the 87GHz

VCO with output buffer was fabricated in BiC9 only. A separate structure of only the 87GHz VCO was also fabricated to allow determination of the buffer gain. A microphotograph of the 100GHz VCO layout is shown in Fig. 7, and the 87GHz VCO with buffer is illustrated in Fig. 8. Each VCO occupies $300\mu m \times 400\mu m$ each including all DC pads (not shown), while the VCO core is only $100\mu m \times 100\mu m$. The VCO with output buffer occupies $550\mu m \times 500\mu m$ including all DC pads (not shown). The die areas are smaller than other W-band SiGe VCOs [8], [9], [11] because inductors are used in place of transmission lines.



Fig. 7. 100GHz VCO microphotograph.



Fig. 8. 87GHz VCO with output buffer.

V. EXPERIMENTAL RESULTS

VCO Performance

The 87GHz and 100GHz VCOs each consume 135mW from a 2.5V supply, which to the authors' knowledge is the lowest supply voltage published for W-band VCOs in SiGe BiCMOS technology. Table 4 and Table 5 summarize the measurement results (probe and cable losses de-embedded) for the 100GHz and 87GHz VCOs, respectively. Note that the measured center frequencies of the VCOs designed at 100GHz vary from 96GHz to 106GHz. Consequently, the tables provide post-layout simulation data for comparison.

	BiC9	BiC9	BipX1	BipX2
	MOS var.	HBT var.	HBT var.	HBT var.
Process f_T/f_{MAX} (GHz)	150/160	150/160	230/300	260/270
Differential Output Power	+0.5	-3.5	+2.7	+2.5
(dBm)	sim. +5.5	sim1.15	sim. +6.5	
SSB Phase Noise @ 1MHz	-98	-80	-99.0	-101.3
offset (dBc/Hz)				
Center Frequency (GHz)	96	100	106	104
	sim. 96	sim. 100	sim. 108	Not simulated

TABLE 4: SUMMARY OF 100GHZ VCO PERFORMANCE

	BiC9,	BiC9
	MOS var., w/o buffer	HBT var. w buffer
Process f_T/f_{MAX} (GHz)	150/160	150/160
Differential Output Power	+0.5 (2.5V)	+7 (2.5V)
(dBm)		+10.5 (3.3V)
	sim. +5 (2.5V)	sim. +10 (2.5V)
SSB Phase Noise @	-101	not measured
1MHz offset (dBc/Hz)		
Center Frequency (GHz)	87	87
	sim. 87	sim.87

TABLE 5: SUMMARY OF 87GHZ VCO PERFORMANCE

Fig. 9 illustrates averaged spectral plots of phase noise at 1MHz offset for the 87GHz BiCMOS9 VCO and 105GHz BipX VCO, and Fig. 10 shows the output power and phase noise of three 100GHz VCOs over the tuning range. The measured phase noise of -94.2dBc/Hz at 1MHz offset for the 96GHz BiCMOS9 VCO with MOS varactor, -101dBc/Hz for the 87GHz BiCMOS9 VCO, and -101.3dBc/Hz for the 105GHz BipX2 VCO with HBT varactor are records for SiGe VCOs above 80GHz. All phase noise measurements are averaged over 100 sweeps to ensure that the record results have not occurred by chance. The measurements were performed using a low noise power supply capable of providing 62mA, and a voltage regulator powered using standard 9V batteries was employed to adjust the tuning voltage inputs. The phase noise of the BiC9 VCO with output buffer could not be measured accurately because the low noise power supply cannot provide the DC current necessary for both the VCO and output buffer.



Fig. 9. Averaged spectral plots of phase noise in (a) the 105GHz VCO with HBT varactor (BipX2), and (b) the 87GHz VCO with MOS varactor (BiC9).



Fig. 10. Phase noise versus oscillation frequency.

The measurements in Fig. 10 indicate that phase noise improves by 5dB and output power by 2.2dBm when the 94GHz BiCMOS9 VCO with MOS varactors is compared to the 105GHz BipX1

VCO. However, if BiC9 and BipX VCOs with MOS varactors are compared, the improvements are 20dB and 6dB, respectively. Furthermore, in the 150GHz BiCMOS technology, the BiC9 VCO with MOS varactors achieves 14dB lower phase noise than the same VCO with junction varactor, demonstrating that BiCMOS, not just HBT, technology is required to optimize the phase noise of W-band SiGe VCOs.

The VCO center frequency is practically immune to the change in technology. Although the transistor f_T improves by 40%, the VCO center frequency changes by only 6%. Clearly, accurate design and modeling of passive components has a greater effect on the center frequency than the transistor itself. So long as the back-end-of-line (BEOL) remains unchanged, mm-wave circuits can be ported between successive generations of SiGe technology, mitigating some of the cost of moving to the next node.

Shown in Fig. 11 are simulated and measured tuning characteristics of the VCOs with HBT varactors. The BipX1 VCO displays 2.5GHz of tuning range up to 125°C.



Fig. 11. Tuning characteristics across temperature for HBT varactor VCOs.

The tuning is linear enough to allow frequency modulation of the VCO output by applying a triangular wave to the tuning input – a modulation technique commonly employed in FMCW radar systems. The resulting spectrum obtained at 100°C using the BipX1 HBT varactor VCO, is shown in Fig. 12.



Fig. 12. Frequency modulation of 105GHz BipX1 VCO.

Fig. 13 compiles the measured output power across the tuning range at 25°C, 70°C, and 125°C. The BiC9 VCO with MOS varactor oscillates up to 70°C and the BiC9 VCO with HBT varactor operates up to 50°C. In contrast, the BipX1 oscillator functions up to at least 125°C.



Fig. 13. Output power versus f_{osc} at 25°C, 70°C, and 125°C.

The lumped inductors of the 100GHz and 87GHz VCOs were both designed to be 23pH and 28pH, respectively, as described in section 3. To demonstrate the accuracy of the inductor designs, in Fig. 14 we show the inductance measurements of the base inductance used in the 87GHz VCO. The quality factor of the inductor is also shown.



Fig. 14. Measurements of the base inductance used in the 87GHz VCO.

Output Buffer Performance

The output power of the 87GHz BiCMOS9 VCO with and without the MOS-HBT output buffer is shown in Fig. 15, for a 2.5V supply. The output buffer has a gain of 6dB across the 4GHz tuning range of the VCO, and achieves +7dBm differential output power from a 2.5V supply. If the output buffer supply voltage is increased to 3.3V, +10.5dBm differential output power is obtained, also illustrated in Fig. 15. Though higher output power at 87GHz has been obtained in SiGe HBT technologies with f_T/f_{MAX} greater than 200GHz ([8] and [21]), the output buffer performance demonstrates that when SiGe HBTs with f_T/f_{MAX} of 155GHz are combined with 130nm MOSFETs, substantial output power can be obtained at 87GHz. The MOS-HBT cascode will become even more competitive when the next generation SiGe BiCMOS processes are developed [22].



Fig. 15. 87GHz BiC9 VCO and output buffer measurements (differential output power).

Figures of Merit

Shown in Fig. 16 are the ITRS VCO FoMs for numerous state-of-the-art VCOs, alongside the FoMs of the VCOs that constitute this work. The VCO FoM used by ITRS is given by (5). The fact that the ITRS FoM excludes output power explains why CMOS VCOs rate very highly using this figure of merit. However, in many applications, a mm-wave VCO with low output power would require amplification before becoming useful. This increases the P_{DC} term in the denominator of (5), effectively decreasing the figure of merit. A better design strategy is to dissipate greater power in the VCO core, which reduces the overall VCO complexity by eliminating amplifier stages. Furthermore, increased core power dissipation can ultimately improve phase noise, whereas amplifying stages do nothing to improve phase noise. As shown in Fig. 17, when the same state-of-the-art VCOs are compared on the basis of the FoM in (6), SiGe VCOs consistently rate higher.

$$FoM_1 = \left(\frac{f_{osc}}{\Delta f}\right)^2 \left(\frac{1}{L[\Delta f]P_{DC}}\right)$$
(5)

$$FoM_2 = \left(\frac{f_{osc}}{\Delta f}\right)^2 \left(\frac{P_{out}}{L[\Delta f]P_{DC}}\right)$$
(6)



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Fig. 16. VCO figure of merit excluding output power.



Fig. 17. VCO figure of merit including output power.

Biasing for Minimum Phase Noise

To experimentally investigate the optimum bias current density for minimum phase noise in Wband VCOs, the bias current in the 87GHz BiCMOS9 and 105GHz BipX1 VCOs was varied, and the phase noise at 1MHz offset was recorded at each current density. The results, shown in Fig. 18, show that the 87GHz BiCMOS9 VCO reaches a minimum phase noise at $J_C = 5mA/um^2$, whereas the 105GHz BipX VCO reaches minimum phase noise at $J_C = 15mA/um^2$.



Fig. 18. Phase noise and output power as functions of bias current density in 87GHz (BiC9) and 105GHz (BipX1) VCOs.

Next, the S-parameters of the BiC9, BipX1, and BipX2 HBTs were measured, and their f_T , f_{MAX} , and NF_{min} were extracted using de-embedded Y-parameters up to 65GHz. The NF_{min} extraction was performed using the techniques in [15], with a noise transit time (τ_n) of 0.4ps and 0.3ps, respectively. The results, shown in Fig. 19, indicate that the peak f_T/f_{MAX} and minimum NF_{min} current densities of the BipX1 and BipX2 HBTs are double those of the BiC9 HBTs. The peak f_T current densities of the BiC9 and BipX1/BipX2 HBTs are, respectively, $J_C = 7mA/um^2$, and $J_C = 14mA/um^2$. The NF_{min} current densities at 65GHz are $J_C = 3.5mA/um^2$ and $J_C = 7mA/um^2$, respectively. Note that NF_{min} @ 65GHz is only 1.7dB, the lowest reported for a SiGe HBT at this frequency. As indicated by the minimum values of the 5GHz and 65GHz noise figure data, as expected the NF_{min} current density varies with frequency.



Fig. 19. Peak f_T and NF_{min} as functions of bias current density in SiGe HBTs.

Comparing the peak f_T current densities in Fig. 19 to the minimum phase noise current densities in Fig. 18, clearly the minimum phase noise is obtained near peak f_T current density. Also shown is output power as a function of current density. The results indicate that high tank swing is vital in low noise W-band VCOs.

Process Monitoring

To gauge the impact of process variations on VCO performance, the mm-wave and DC characteristics of both BiC9 VCOs were collected from 60 dice from 4 different wafers. Tables 5 and 6 summarize the results for the MOS varactor and HBT varactor VCOs, respectively. Of the 120 VCOs tested, 4 had significantly below average performance, and another 2 VCOs failed to oscillate. The 6 outlier VCOs are not included in the averages given.

Wafer	1	2	3	4
Center freq.	94.7	94.9	94.9	95.0
(GHz)				
Tuning range	4.6	4.6	4.6	4.6
(GHz)				
Output	0.2	0.7	0.6	0.8
power (dBm)				
DC power	133.8	133.2	137.3	132.6
(mW)				

 TABLE 6: PERFORMANCE OF MOS VAR. VCOS.

TABLE 7: PERFORMANCE OF HBT V.	AR. VCOS.
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Wafer	1	2	3	4
Center freq.	99.6	100.5	100.1	100.5
(GHz)				
Tuning range	3.4	3.6	3.6	3.7
(GHz)				
Output	-1.1	-1	-1.4	0.9
power (dBm)				
DC power	133.0	133.0	136.2	132.8
(mW)				

To further characterize the VCOs over process variations, in Fig. 20 output power is plotted versus oscillation frequency for 1 die on each of the 4 wafers, alongside simulation results. A 2dB variation in output power between BiCMOS9 VCOs on different wafers is illustrated. Note however that the center frequency remains constant over the wafers.



Fig. 20. Output power versus center frequency for BiCMOS9 VCOs on different wafers.

Fig. 21 reproduces wafer maps of oscillation frequency and phase noise as functions of location for BipX1 VCOs. Both plots show that dice at the center of the wafer perform better than dice on the edges.



Fig. 21. BipX1 wafer maps of oscillation frequency (left) and phase noise at 1MHz (right).

VI. CONCLUSIONS

W-band low-voltage VCOs have been presented with record phase noise for SiGe VCOs above 80GHz. Experimental results indicate that transistors in W-band VCOs should be biased at peak f_T current density to minimize phase noise because NF_{min} current density approaches peak f_T current density as frequency increases. Additionally, MOS varactors are shown to be superior to HBT varactors for achieving low phase noise. Furthermore, while VCO performance improves when SiGe

technology is scaled, the oscillation frequency – determined by passive components – is insensitive to scaling. Wafer mapping and temperature data show that SiGe HBTs with over 200GHz f_T are required to obtain production-quality W-band VCOs.

ACKNOWLEDGEMENTS

The authors thank CMC, the University of Toronto, and especially Jaro Pristupa for CAD

support, CMC and STMicroelectronics for fabrication, and CITO and STMicroelectronics for funding.

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