Design of Silicon W-Band Low Noise Amplifiers

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1. Introduction

What is a Low-Noise Amplifier?

Digital signal processing (DSP) systems require interfaces to the analog world. The first amplification stage in a radio receiver is typically the tuned low-noise amplifier (LNA), which provides enough amplification to the input signal to make further signal processing insensitive to noise. Although the primary goal in LNA design is to minimize the system noise figure, the LNA must also meet other equally important specifications in gain, linearity, power consumption, input and output impedance matching, and bandwidth. This chapter provides a systematic method for achieving these design goals in V-band and W-band LNAs, based on an existing gigahertz-range simultaneous noise and impedance matching technique.

LNA Design in the V-Band and W-Band

With the measured f_{MAX} of the latest SiGe HBT and 65nm CMOS technologies at 300GHz and with noise figure values as low as 1 dB at 40 GHz [1], as illustrated in **Figure 1**, V-band (50-75GHz) and W-band (75-110 GHz) radios are now possible in silicon. Several SiGe HBT V-band and W-band LNAs have been reported [2]-[7]. Although 60-GHz CMOS LNAs have been developed almost at the same time [8],[9] it is only at the 90nn node that their power dissipation and noise figure [10],[11] have become competitive and that W-band operation has been demonstrated [12]. LNA design for the W-Band is particularly challenging for several reasons. First, the performance of silicon devices in the W-Band is poor, and in the case of MOSFETs, highly layout dependent. Second, passive devices are lossy, and obtaining a low impedance "analog ground" is difficult, particularly with the strict metal density and "slotting" rules found

in state-of-the-art silicon processes. Perhaps most importantly, existing gigahertz range techniques for simultaneous noise and input-impedance matching need adjustments in the W-Band.

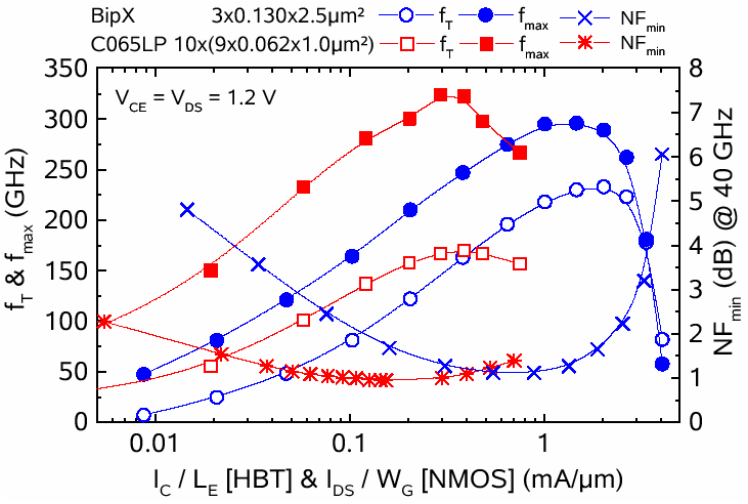


Figure 1. f_T/f_{MAX} versus drain or collector current density, for the latest CMOS and SiGe processes [1].

A Brief History of LNA Design Philosophy

Traditional LNA design employed lossless reactive components to transform the signal source impedance to the optimum noise impedance of a transistor biased at optimum NF_{min} current density [13]. Because the real part of the optimum noise impedance and the real part of the input impedance of transistors are in general different, this approach compromises the input reflection coefficient (and hence gain) to improve noise performance. When the designer has no control over the relationship between the real parts of the input impedance and optimal noise impedance, as in LNA designs involving discrete off-the-shelf components, this simple design methodology yields a unique and optimal solution which minimizes the amplifier noise factor.

In integrated circuit LNAs however, the designer can control the optimum noise impedance and bias current of the input transistor by adjusting its emitter length (or gate width). Thus, by choosing the correct transistor size, it is possible to obtain simultaneous noise and impedance match at the input of a SiGe or CMOS *integrated circuit* LNA. The method employed to achieve simultaneous noise and input-impedance match was first presented in [14],[15], and will be

reviewed in section 2. Unfortunately, like all other LNA design methodologies to date, it suffers from several limitations that arise at mm-waves.

The first limitation is caused by the pad capacitance at the LNA input, which appears in parallel with the signal source impedance. The pad capacitance, which might be as large as 50 fF, is a negligible 530 Ω at 6 GHz, but only 53 Ω at 60 GHz. A second limitation arises because bond wires are often used to connect an LNA to an off-chip antenna, and the original technique does not describe how the bond wire inductance can be incorporated into the low-noise design methodology. Finally, the methodology does not explain how to optimize the transistor layout to minimize transistor noise, other than ensuring the real parts of the optimal noise and input impedances are equal.

In this chapter, we review the original simultaneous noise and impedance matching methodology of [14], and present a new methodology that addresses its limitations through design and layout techniques. Finally, we present experimental results of 77GHz and 94GHz LNAs fabricated in 90nm and 65nm CMOS.

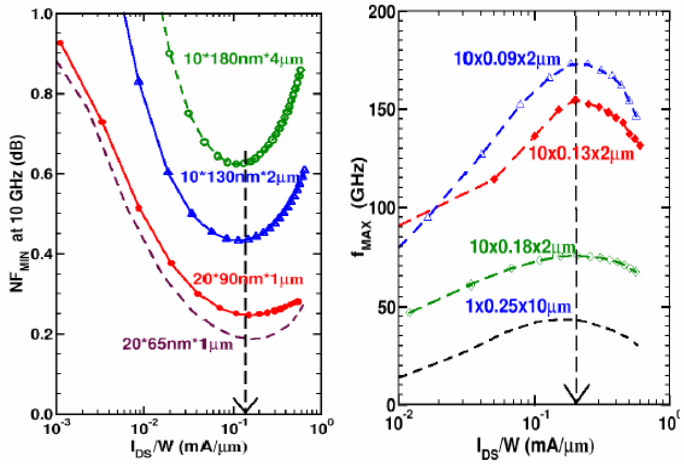
2. Original Methodology for Simultaneous Noise and Input Impedance Matching

The original methodology for achieving simultaneous noise and input impedance match in integrated LNAs can be summarized neatly in 5 steps. References [14] and [15] provide many details omitted here for brevity. For the interested reader, there are two alternate design approaches for sub 10-GHz CMOS LNAs which focus on meeting power dissipation constraints [16],[17]. To save power, they sacrifice the noise figure [16],[17], the gain, and noise resistance of the LNA [17]. However, the power dissipation is quite low at mm-wave frequencies because the device sizes and currents required for simultaneous noise matching are smaller than 40μm and 6 mA respectively [10]-[12].

STEP 1: Optimum Biasing

At a given frequency, SiGe HBTs and MOSFETs feature at optimum current density J_{OPT} that minimizes the transistor noise figure [13]-[15]. The LNA transistors should be biased at this

current density. In n-MOS LNAs, J_{OPT} is 0.15mA/μm, and has been independent of technology since the application of constant-field scaling rules beginning at the 0.5μm node [18]. **Figure 2** (a) shows the trend from the 0.18μm node to the 65nm node. To maximize gain with minimal increase in noise figure, the amplifier can be biased instead at peak f_{MAX} current density J_{pfMAX}, which is 0.2mA/μm in CMOS, as illustrated in **Figure 2** (b). In addition to being independent of CMOS technology, J_{OPT} is also independent of frequency, as illustrated in **Figure 3** [19].



(a) (b)

Figure 2: J_{OPT} and J_{pfMAX} are independent of CMOS technology [19].

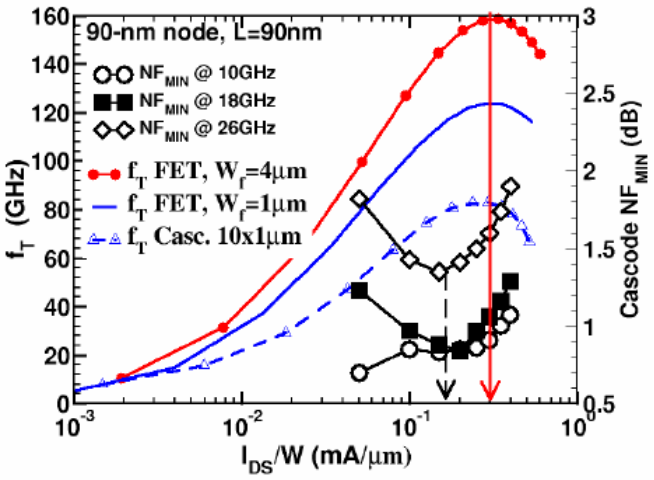


Figure 3: NF_{min} versus design frequency and f_T versus finger width in 90nm n-channel MOSFETs [10].

In contrast, the optimum noise figure and peak f_{MAX} current densities of SiGe technologies depend on the technology and the design frequency, as shown in Figure 4. Furthermore, In SiGe,

J_{OPT} is higher for cascode amplifiers than for single transistor amplifiers. Regardless, the optimal noise figure current density can be found by performing s-parameter simulations at a variety of bias current densities for the particular LNA topology (CS/CE transistor or cascode).

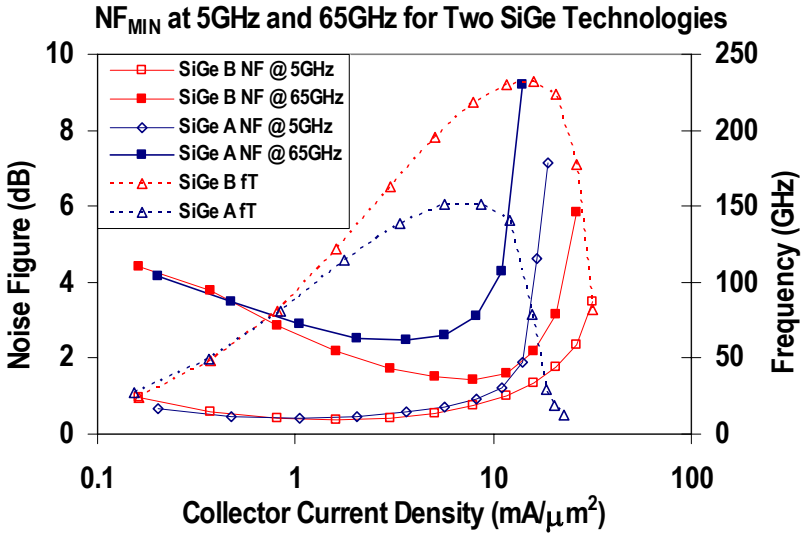


Figure 4: In SiGe, J_{OPT} depends on the technology and frequency.

STEP 2: Device Size

In CMOS LNAs, the total gate width (W_G) is controlled by connecting a number of fingers N_f in parallel, each with a fixed finger width W_f. In this case, the noise parameters of a MOSFET can be expressed in terms of the total gate width $W_G = N_f W_f$, as shown in (1) through (4) where parameters R_{NMOS}, $G_{u,NMOS}$, $G_{cor,NMOS}$ and $B_{cor,NMOS}$ are bias-dependent technology parameters

$$R_n = \frac{R_{NMOS}}{N_f W_f} \tag{1}$$

$$G_u = G_{u,NMOS}\,\omega^2 N_f W_f \tag{2}$$

$$G_{cor} = G_{cor,NMOS}\,\omega^2 N_f W_f \tag{3}$$

$$B_{cor} = B_{cor,NMOS}\,\omega^2 N_f W_f \tag{4}$$

The total gate width is chosen such that the real part of the optimum noise impedance (5), is equal to the source impedance at the design frequency [14]. Note that this design methodology places no constraints on N_f or W_f individually, only on W_G. However, as illustrated by the solid

f_T curves in Figure 3, W_f plays an important role in the MOSFET f_T and hence is critical to LNA performance. Also note that because G_{cor}, B_{cor}, and G_u all increase with frequency, lower frequency LNAs require larger devices and counter-intuitively, have higher power dissipation [15]. In HBT LNAs, the emitter length (l_E) is substituted for W_G in (1) through (4), and exactly the same design procedure applies.

$$\frac{1}{Z_{sopt}} = \sqrt{G_{cor}^2 + \frac{G_u}{R_n}} - jB_{cor} \tag{5}$$

STEP 3: Input Impedance matching

The input impedance (Z_{IN}) of the source-degenerated amplifier, given by (6), is now tuned to the source impedance (Z_0) using two inductors L_S and L_G, as illustrated in **Figure 5** [14,20]. Decomposing (6) into its real and imaginary parts yields the required values of L_S (7) and L_G (8). If a pad is now added at the LNA input the amplifier is no longer matched correctly. Note that L_S changes the real part of the input impedance, but not the real part of the optimum noise impedance [14], [15], [21].

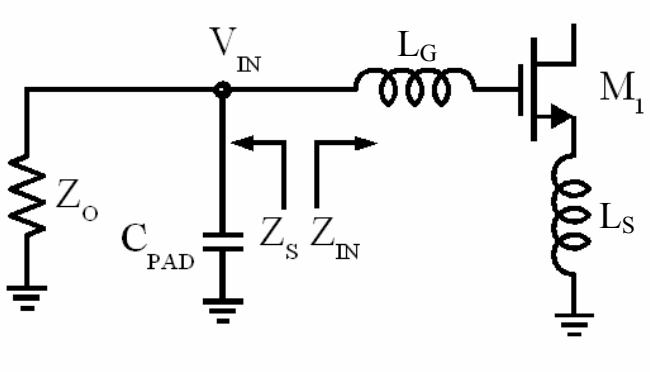


Figure 5: Schematic of LNA input.

$$Z_{IN} = \omega_T L_S + j\left(\omega L_S + \omega L_G - \frac{\omega_T}{\omega g_m}\right) \tag{6}$$

$$L_S = \frac{Z_0}{\omega_T} \tag{7}$$

$$L_G = \frac{\omega_T}{\omega^2 g_m} - L_S \tag{8}$$

STEP 4: Gain Optimization

Finally, an inductive load is employed to maximize amplifier gain and linearity. When the LNA is matched at *input and output,* the power gain is given by (9), where R_P is the output impedance of an inductively loaded LNA *at resonance*. Note that although the source degeneration inductance (L_S) is independent of the design frequency, the impedance of L_S increases with the design frequency. Therefore, in W-Band SiGe LNAs, the large degeneration impedance and the large transconductance of the HBT can cause the series feedback to be quite strong. In these cases the gain can be simplified as shown.

$$|G| = \frac{1}{2} R_P Z_0 \left| \frac{g_m}{1 + j(\omega/\omega_T) Z_0 g_m} \right|^2 \approx \frac{1}{2} \left(\frac{\omega_T}{\omega} \right)^2 \frac{R_P}{Z_0} \tag{9}$$

Given that g_m was fixed in steps 1 and 2 when we fixed bias current density and total gate width, and Z_0 is normally 50 Ω, the only means of increasing the amplifier gain is to increase R_P using a higher-Q inductive load, in turn reducing the amplifier bandwidth. Ultimately, the gain is limited by the device output resistance.

STEP 5: Extension to Multi-Stage Designs

In a single stage amplifier, all design parameters are either beyond the designer's control (Z_0, ω) or optimized to minimize the amplifier noise figure (W_G, I_{DS}, ω_T), or gain (R_P). In a multi-stage amplifier, the noise contribution of the second stage to the overall amplifier noise figure is reduced by the gain of the first stage, as given in (10), where A_1 is the first stage gain, and F_n is the n^{th} stage noise factor.

$$F_{overall} = F_1 + \frac{F_2 - 1}{A_1} \tag{10}$$

Therefore, the second stage can be optimized for bandwidth, gain, and/or linearity with reduced impact on the overall amplifier noise figure. For example, the second stage need not be biased at the optimum noise figure current density, but instead at a higher current density to improve gain and linearity. Alternatively, to increase the amplifier bandwidth, the second stage can be tuned to a slightly different frequency to produce a wider, flatter gain response, as shown in Figure 6. Finally, the output impedance of the first stage and input impedance of the second stage are no longer part of the 50Ω environment, and can be adjusted to meet gain and linearity specifications, albeit at the expense of increased noise if the stages are not noise matched.

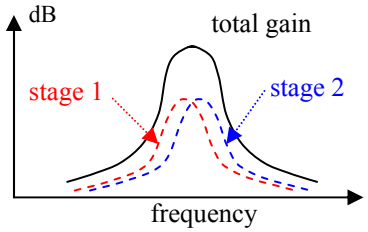


Figure 6: Stagger-tuned stages increase amplifier bandwidth.

3. Matching Methodology for W-Band LNAs

In the W-band, the pad capacitance C_{PAD} (see Figure 5) cannot be neglected in the matching process. The optimum noise impedance of the transistor must now be matched to the real part of Z_S, and the amplifier input impedance Z_{IN} must be conjugately matched to Z_S. Accounting for C_{PAD}, Z_S is now given by (11), and has a real part which is a factor of k, given by (12), smaller than Z_0. Intuitively, Z_S decreases because the amplifier now sees admittance through C_{PAD}, in addition to admittance through the original 50Ω source.

$$Z_S = \frac{Z_0}{1+\omega^2 C_{PAD}^2 Z_0^2} - j\frac{\omega C_{PAD} Z_0^2}{1+\omega^2 C_{PAD}^2 Z_0^2} \tag{11}$$

$$k = 1+\omega^2 C_{PAD}^2 Z_0^2 \tag{12}$$

The new emitter length ($l_{EM(new)}$) or gate width ($W_{G(new)}$) required for optimum noise match increase by the same factor of k, as shown in (13). The larger device size leads to increased transconductance (14) and bias current (15), again by a factor of k, as well as a larger output 1dB compression point.

$$W_{G(new)} \text{ or } L_{E(new)} = kW_G \text{ or } kl_{EM} \tag{13}$$

$$g_{m(new)} = kg_m \tag{14}$$

$$I_{DS(new)} = kI_{DS} \tag{15}$$

To find the the new values of L_S and L_G, consider that (16) must be satisfied for optimal impedance match. Substituting (11) into (16) and solving, the new values for L_S and L_G are

given by (17) and (18) respectively.

$$Z_S^* = \omega_T L_{S(new)} + j\left(\omega L_{S(new)} + \omega L_{G(new)} - \frac{\omega_T}{\omega g_{m(new)}}\right) \tag{16}$$

$$L_{S(new)} = \frac{Z_0}{k\omega_T} \tag{17}$$

$$L_{G(new)} = \frac{Z_0^2 C_{PAD}}{k} - L_{S(new)} + \frac{\omega_T}{\omega^2 g_{m(new)}} \tag{18}$$

With this new methodology, L_S is decreased by a factor of k, resulting in weaker feedback, and correspondingly higher gain (helped further by increased g_m). To determine the conditions under which L_G is also reduced by the addition of C_{PAD}, consider solving (19), the inequality $L_{G(new)} < L_G$, using (8) and (18). The inequality can be simplified as shown in (20), by substitution of (7) for L_S, (17) for $L_{S(new)}$, and finally (12) for k. The resulting constraint on C_{PAD} which ensures $L_{G(new)} < L_G$ is given by (21). Because C_{PAD} can be augmented using on-chip capacitors, L_G can be easily reduced by the appropriate selection of C_{PAD}.

$$\frac{Z_0^2 C_{PAD}}{k} - L_{S(new)} + \frac{\omega_T}{\omega^2 g_{m(new)}} < \frac{\omega_T}{\omega^2 g_m} - L_S \tag{19}$$

$$\frac{Z_0^2 C_{PAD}}{k} - \frac{Z_0}{k\omega_T} + \frac{\omega_T}{\omega^2 k g_m} < \frac{\omega_T}{\omega^2 g_m} - \frac{Z_0}{\omega_T} \tag{20}$$

$$C_{PAD} > \left(\frac{\omega_T}{g_m} - Z_0 \frac{\omega^2}{\omega_T}\right)^{-1} \tag{21}$$

The reduction in L_S and L_G result in lower series resistance and higher self-resonance frequency for these passives, and correspondingly less noise figure degradation. *Table 1* provides numerical examples of the new design technique, applied to SiGe and CMOS mm-wave LNAs at 60 GHz, 77 GHz, and 94 GHz. The CMOS examples are based on simulations that show W_G = 30 μm is required for simultaneous noise and impedance match to 50 Ω at 60 GHz, without C_{PAD}.

Table 1: Numerical design examples of LNAs from 60GHz to 94GHz.

Parameter	65GHz cascode 0.18μm SiGe HBT [6]	60GHz cascode 90nm CMOS [10]	77GHz cascode 90nm CMOS [12]	94GHz cascode 90nm CMOS [12]
f_T device/cascode	125GHz/110GHz	128GHz/80GHz	128GHz/80GHz	128GHz/80GHz
device size	9μm by 0.18μm	34μm	30μm	26μm
C_{PAD}	12fF	20fF	20fF	20fF
k	1.166	1.142	1.234	1.349
J_{DS} (J_{CE})	2.4mA/μm^2	0.2mA/μm	0.3mA/μm	0.3mA/μm
I_{DS} (I_{CE}) and g_m	3.9mA & 30mS	6.9mA & 34mS	8.7mA & 30mS	7.8mA & 26mS
$L_{S/E}$, $L_{G/B}$	60pH, 90pH	55pH, 155pH	50pH, 110pH	45pH, 80pH

4. Accounting for Bond Wire Inductance

Often, a bond wire is used to connect the LNA input to an off-chip antenna. At mm-waves, the bondwire impedance must be accounted for to achieve simultaneous noise and impedance matching. The bondwire and bondpad are represented by the T-network shown in Figure 7, which can be thought of as an impedance transformer. Repeating the analysis of section 3, this time including L_W yields (22) for k, and (23) for Z_S. The values of L_S and L_G can now be recalculated using (16) and (23), where k is given by (22) in place of (12).

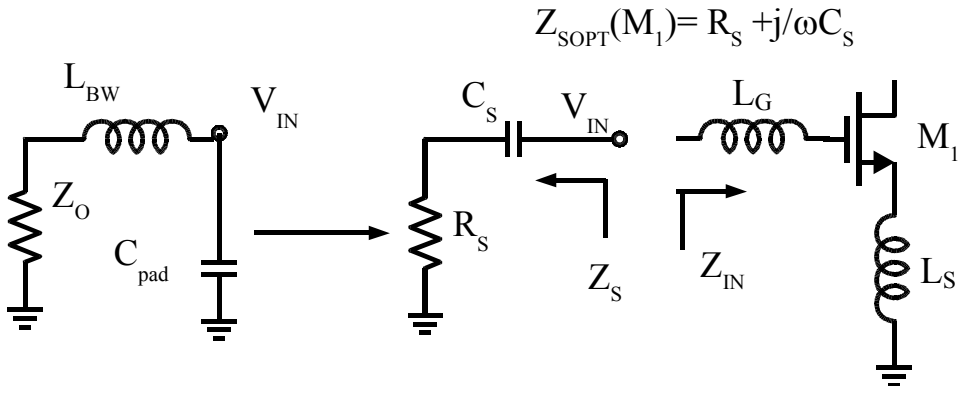


Figure 7: Noise matching with bondwire and pad

$$k = \left(1 - \omega^2 L_{BW} C_{PAD}\right)^2 + \omega^2 Z_0^2 C_{PAD}^2 \tag{22}$$

$$Z_S = \frac{Z_0}{k} + j\omega \frac{\left[L_{BW}\left(1-\omega^2 L_{BW} C_{PAD}\right) - Z_0^2 C_{PAD}\right]}{k} \tag{23}$$

To minimize the sensitivity of the match to variations in L_W that may arise in the packaging process, components L_W and C_{PAD} should be chosen to resonate at the design frequency. This causes k to become independent of L_W, which also makes L_E, g_m, and therefore the transistor size and bias current, independent of L_W.

When C_{PAD} and L_W resonate, they transform Re(Z_S) to another real impedance $n \times Z_0$ at the design frequency, where n is given by (24). The input transistor size and bias current must thus be modified to match to $n \times Z_0$. The new LNA parameters are given in Table 2, in terms of the original parameters, derived in section 2. The gain of the new LNA is given by (25). Note that n is just a simplification of k under the condition that L_W and C_{PAD} resonate.

$$n = \left(\frac{1}{\omega^2 Z_0^2 C_{PAD}^2} \right) \tag{24}$$

Table 2: LNA parameters when noise and imedance matched to $n \times Z_0$.

Parameter	*transformation*
device size	$W_{G(new)} = W_G / n$
g_m	$g_{m(new)} = g_m / n$
I_{DS}	
L_S	
L_G	$L_{G(new)} = nL_G$

$$|G|_{(new)} = \frac{1}{2n} R_P Z_0 \left| \frac{g_m}{1 + j(\omega/\omega_T) Z_0 g_m} \right|^2 \approx \frac{1}{2n} \left(\frac{\omega_T}{\omega} \right)^2 \frac{R_P}{Z_0} \tag{25}$$

For greater gain, we would like to select n < 1. However, selecting n < 1 places the constraint given by (26) on L_W, if C_{PAD} and L_W are assumed to resonate. For W-Band LNAs in a 50Ω environment, this places L_W in the range of 70pH to 105pH, maximum. To perform matching with larger, more realistic bondwire inductances requires n > 1, and a correspondingly, decreased gain.

$$L_W \leq \frac{Z_0}{\omega} \tag{26}$$

Alternatively, if greater dependence on manufacturing variation in L_W can be tolerated, then the

constraint that L_W and C_{PAD} resonate can be relaxed. In this case $k < 1$ can be obtained for larger values of L_W. For example, for a 77GHz automotive radar LNA in a 50Ω environment with 30fF pad capacitance, $k = 3$ can be obtained for $L_W = 370$ pH.

5. Intra-Stage Matching for Cascode Amplifiers

In sub-100nm n-channel MOSFETs, because C_{GD} is 50% of C_{GS}, the f_T of the cascode is at least 33% smaller that that of the transistor. Consequently, the middle pole degrades the cascode frequency response and therefore CMOS cascode amplifiers require bandwidth extension techniques [22-24] in order to achieve acceptable gain at mm-waves. One approach is to create a parallel resonance at the middle node between the common-source (CS) and common-gate (CG) transistors [6]. However, this resonance is narrowband. Another technique is to form an artificial transmission line by inserting a series inductor between the drain of the CS FET and the source of the CG FET, as illustrated in Figure 8. Besides recovering some of the loss in f_T, this technique has the added benefit of improving the noise figure of the cascode stage. As shown in Figure 9 for two 90nm CMOS cascode stages, the optimum value of L_M required to maximize the available gain of the cascode is inversely proportional to the transistor size and is a strong function of the layout parasitics of the transistor. Thus, the LNA design methodology described earlier must be refined to include the maximization of the f_T of the cascode just before Step 2. Note that during Step 2 the size of L_M scaled with that of the MOSFETs.

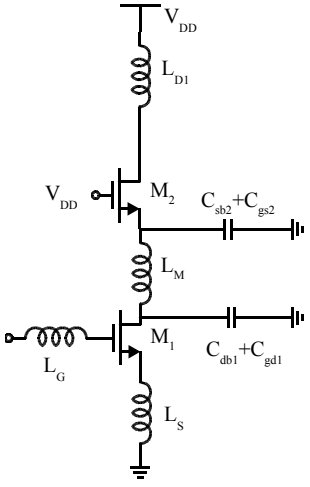
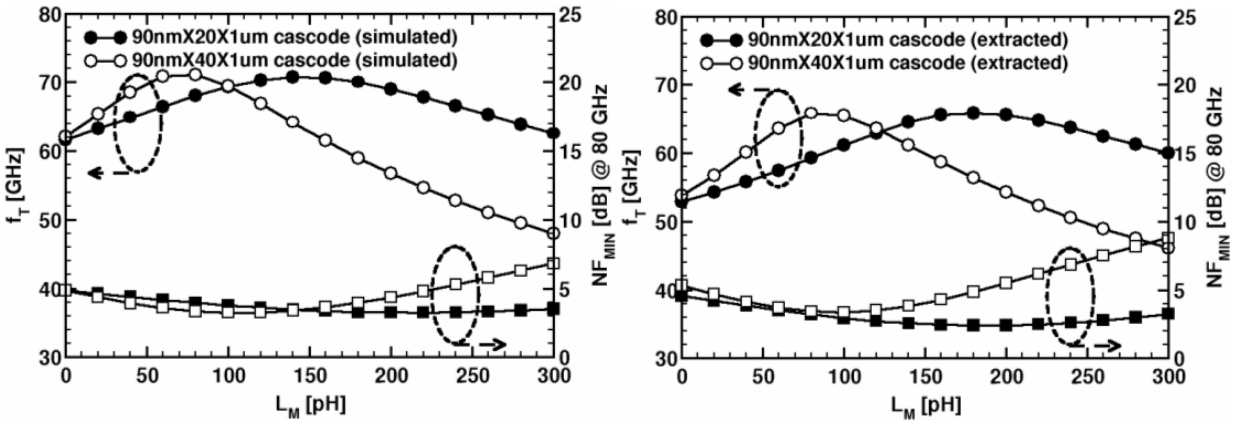


Figure 8. Adding L_M to the middle node of a CMOS cascode.



(a) (b)

Figure 9. The simulated f_T and NF_{MIN} of a 90nm CMOS cascode amplifier when L_M is swept from 0 to 250pH a) before and b) after transistor layout parasitics extraction.

6. Layout Techniques for Millimeter-Wave CMOS

Unlike SiGe HBTs, MOSFET performance is extremely sensitive to device layout. The f_T and f_{MAX} of MOSFETs depend upon finger width, drain and source metallization, gate finger spacing, and gate and substrate contact arrangement [21]. In W-Band CMOS circuits, finding the optimal layout for the MOSFET is critical to achieving the best possible circuit performance. Here we discuss strategies for obtaining the highest f_T and f_{MAX} possible in a given technology. In general, the layout geometry with the highest f_{MAX} coincides with that for the minimum noise figure. We also note that in the expressions for f_{MAX}, NF_{MIN} and noise resistance R_n, R_{gate} and R_S always appear as a sum R_S+R_{gate}. Unlike R_{gate}, R_S only depends on the total gate width of the device, and not on contact arrangements or finger width. It is typically 200-300 Ωμm in 130nm, 90nm, and 65nm CMOS. Therefore, once R_{gate} becomes much smaller than R_S, no further improvement in f_{MAX} or NF_{MIN} can be achieved.

Gate Contact Arrangements

Shown in Figure 10 are three MOSFET layouts, with one single-sided contact per gate (a) two single-sided contacts per gate (b) and double-sided gate contacts (c). Double-sided gate contacts have the advantage that the gate finger is treated as a transmission line driven from *both* ends, however because the drain and gate are overlapped the layout suffers from increased C_{GD}.

Generally speaking, the more gate contacts that are added, the more reliable the layout and the lower the gate resistance. These benefits come at the expense of increased parasitic capacitance. The gate resistances for single-sided and double-sided contacts are given by (16) and (17), respectively, where R_{cont} is the contact resistance, N_{cont} is the number of contacts per gate finger, R_{sq} is the gate poly sheet resistance per square, W_{ext} is the gate extension beyond the active region, W_f is the finger width, N_f is the number of gate fingers connected in parallel, and l_{phys} is the physical channel length.

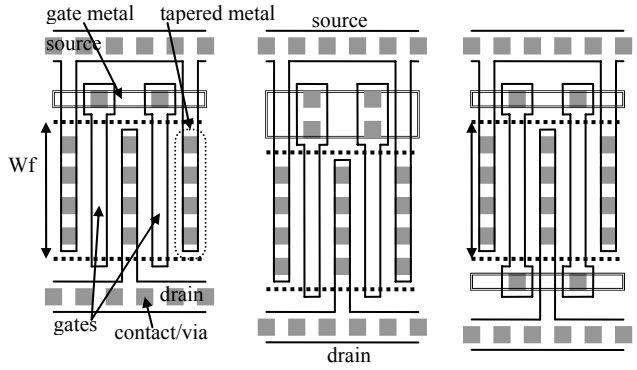


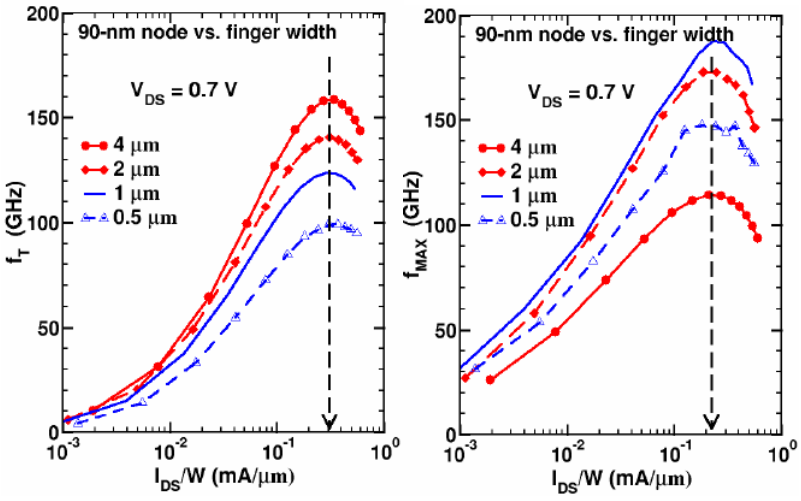
Figure 10: MOSFETs with different gate connections.

$$R_G = \frac{\frac{R_{CON}}{N_{CON}} + \frac{R_{sq}}{L}\left[W_{ext} + \frac{W_f}{3}\right]}{N_f} \tag{27}$$

$$R_G = \frac{\frac{R_{CON}}{N_{CON}} + \frac{R_{sq}}{L}\left[W_{ext} + \frac{W_f}{6}\right]}{2N_f} \tag{28}$$

Finger Width

Finger width also affects MOSFET performance. Longer fingers result in higher f_T, and shorter fingers initially result in higher f_{MAX} until the degradation of f_T offsets the reduction in gate resistance, as illustrated for 90nm CMOS in Fig. 11 (a) and (b), respectively. For finger widths of 1 μm to 2 μm in 90nm CMOS, f_{MAX} and f_T are both reasonably large, demonstrating that there is probably an optimum finger width between 1 μm and 2 μm for the best LNA performance.



(a) (b)

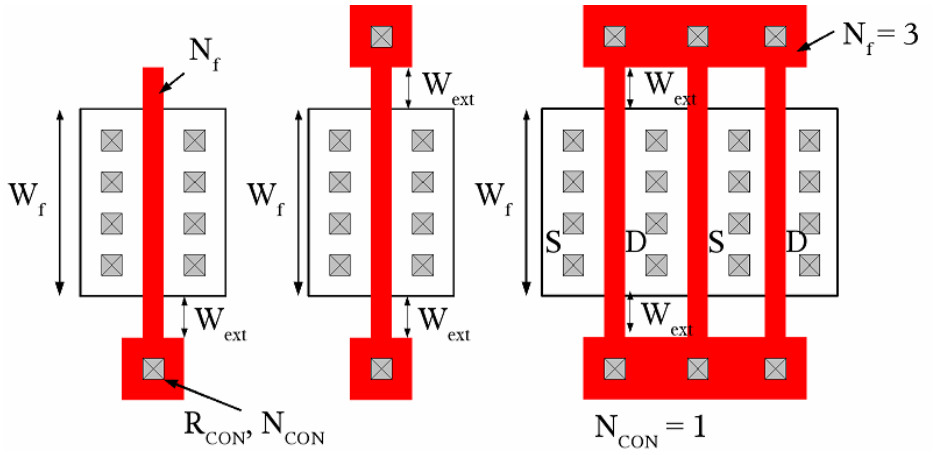
Figure 11. f_T and f_{MAX} versus finger width for 90nm CMOS.

Optimizing Finger Width and Gate Contacts

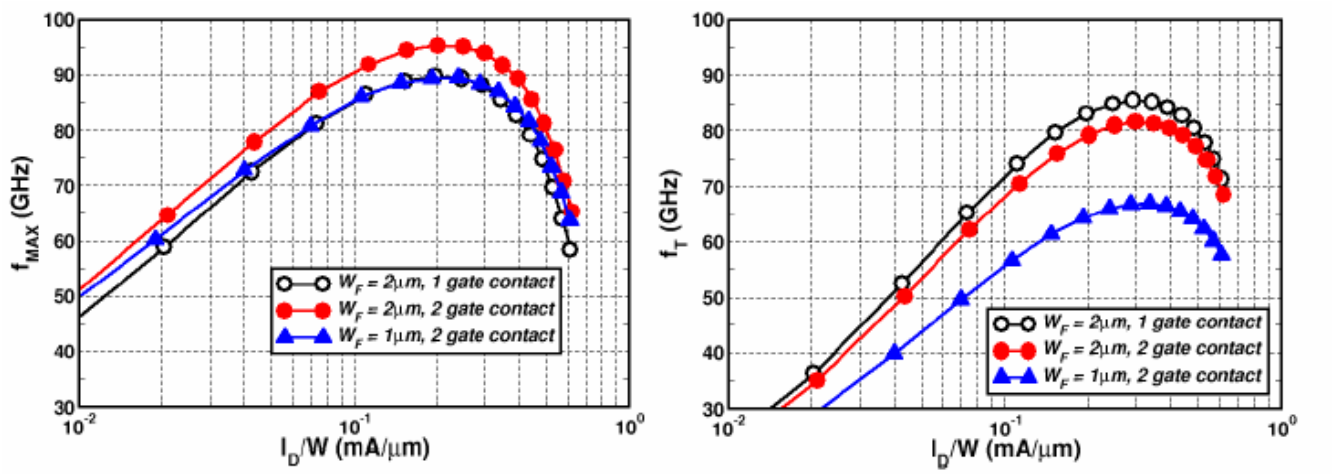
Shown in Fig.12 are measured f_T and f_{MAX} for three different MOSFET layouts in 130nm CMOS. The layout with 2µm fingers and single gate contacts has f_T and f_{MAX} of about 85 GHz. The other two layouts suffer degradation in either f_T or f_{MAX} for an improvement in the other. Such degradation is unacceptable in a millimeter-wave LNA tuned near f_T/f_{MAX}. In a technology with higher f_T/f_{MAX}, a greater number of gate contacts could be used for improved yield and reliability, however 130nm CMOS does not have enough performance at mm-wave frequencies for such considerations.

If W_f is held constant as the CMOS gate length is scaled by $\sqrt{2}$ to the next technology node, the capacitance of the gate finger is scaled down by $\sqrt{2}$, and the resistance of the gate finger is scaled up by $\sqrt{2}$. However, the contact resistance is scaled by a factor of 2 because the contact size is scaled in both dimensions. The longer finger width relative to the new gate length, combined with greater contact resistance per finger will cause f_T to increase relative to f_{MAX}. Therefore, the starting point for finding the optimum MOSFET layout in a new technology is to scale W_f by $\sqrt{2}$ along whith the length. This strategy should yield optimum finger widths of 1.4 µm in 90 nm CMOS and 1 µm in 65nm CMOS (*Table 3*) based on the 2µm finger width in 130nm CMOS. In subsequent sections we demonstrate that this scaling strategy is reasonably

accurate. Regardless, it is important to note that the contact resistance becomes an ever larger proportion of the gate resistance as CMOS technology is scaled.



(a)



(b) (b)

Figure 12. a) Gate contact arrangement and measured b) f_{MAX} and c) f_T of 130nm MOSFETs with different layout styles [25].

Table 3: Typical parameters for 65nm n-MOS GP and LP devices

Parameter	***GP***	***LP***
Physical L (nm)	45	57
EOT (nm)	1.3	1.8
W_f (μm)	1	1
N_{CON}	1	1
Contact on both sides	N	N
R_{CON} (Ω)	40	40
R_{sq} (Ω/sq)	20	20
W_{ext} (nm)	200	200
N_f	1	1
R_{gate} (Ω)	198	160
R_S (Ω)	300	300

Example 1: 10μmx90nm device contacted on one side:

R_{sq} = 10 Ω, l_{phys} = 65 nm, N_{CON} = 1, R_{CON} =20, W_{ext} = 200 nm; $R_S = R_D = (1/W_G)*300$ Ω/μm = 30 Ω

a) W_f =1 μm; N_f = 10, R_{gate} = 10.2 Ω, $R_{gate} + R_S$ = 40.2 Ω

b) W_f = 2 μm; N_f = 5, R_{gate} = 30.66 Ω, $R_{gate} + R_S$ = 60.66 Ω

Example2: 10μmx90nm device contacted on both sides:

R_{sq} = 10 Ω, l_{phy} = 65nm, N_{CON} = 1, R_{CON} = 20, W_{ext} = 200 nm; $R_S = R_D = (1/W_G)*300$ Ω/μm = 30 Ω

a) W_f =1 μm; N_f = 10, R_{gate} = 3.82 Ω, $R_{gate} + R_S$ = 33.82 Ω

b) W_f =2 μm; N_f = 5, R_{gate} = 10.2 Ω, $R_{gate} + R_S$ = 40.2 Ω

Drain and Source Metallization and Gate Pitch

To meet electromigration rules at 100ºC, and to minimize parasitic C_{DS} caused by the closely spaced, vertically stacked metals on the drain and source fingers, the drain and source metallization should be tapered as shown in Figure 13.

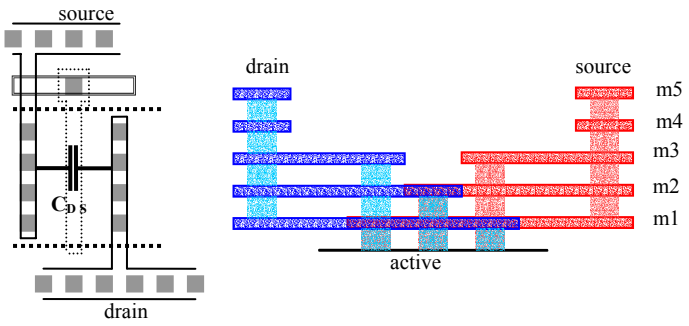


Figure 13. Tapered metallization on the drain and source minimize parasitic CDS while meeting electromigration rules.

7. CMOS LNA Design in the W-Band

To verify the new noise and impedance matching methodology, and to evaluate CMOS for W-band applications, 77 and 94GHz LNAs were designed and fabricated in STM's 90nm CMOS technology. The schematics of the LNAs are shown in Figure 14, and consist of three topologies: a 1-stage cascode, a 2-stage cascode, and a 2-stage transformer-coupled cascode. The designs employ a combination of lumped inductors over substrate, allowing compact layout, and transmission lines over metal, allowing easy routing of power and ground planes.

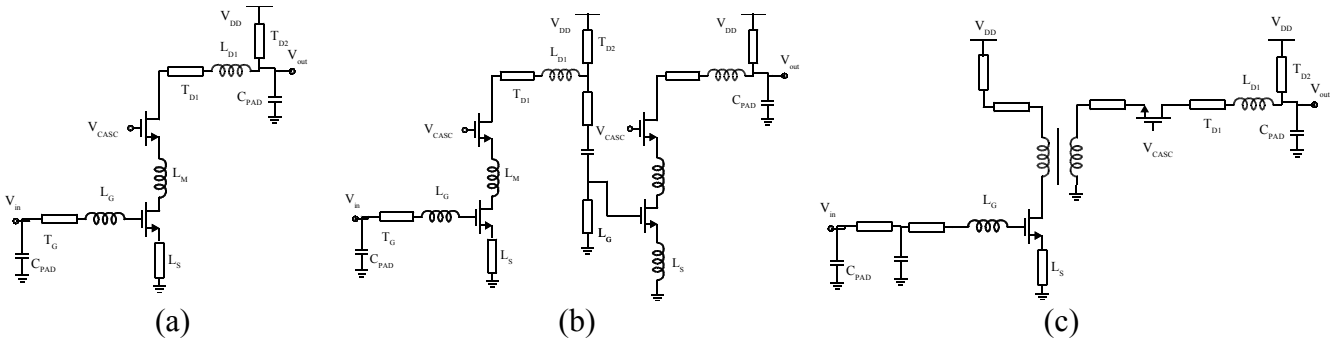


Figure 14: a) 1-stage, b) 2-stage cascode and c) transformer-coupled LNA schematics

To investigate the effects of the layout issues discussed in section 6 upon LNA performance, three single stage cascode LNAs were designed, each with a different device layout but identical gate width. Based upon simulation results with extracted RC parasitics, the layout that yielded the best performing single stage cascode was chosen to design the remaining two LNAs. Note that although the variation of f_{MAX} with finger width is captured in simulation, the variation of f_T seen in measurements of 90nm MOSFETs is not captured in simulation [19], [21]. The three MOSFET layouts are described in Table 4. Because only digital MOSFET models were available, the gate resistances of the MOSFET layouts summarized in Table 4 were calculated and manually added to post-layout extracted netlists of the MOSFETs. The post-layout simulation results for the three LNAs are summarized in Table 4, and indicate that layout C, with single-sided gate contacts and 1.5μm fingers is superior. This result offers some supporting evidence to our theory of CMOS layout scaling in section 6.

Table 4: Description of MOSFET layouts.

	W_{finger} (μm)	W_G (μm)	*Contacts*
A	1	36	One, single-sided
B	2	36	One, double-sided
C	1.5	36	One, single-sided

Table 5: LNA performance summary (simulations).

	S21 (dB)	*NF (dB)*
A	3.63	4.78
B	4.36	4.88
C	5.04	4.63

8. Measurement Results

Shown in Figure 15 are the S-parameter measurements for the fabricated LNAs [12]. The S-parameters and DC performance of the LNAs are summarized in Table 6. Due to lack of equipment, we cannot measure the LNA noise figure above 65 GHz. However, good agreement between simulations and receiver noise figure measurements was found in a 60GHz radio receiver fabricated in the same process [11]. The LNA die photo micrographs are shown in

Figure 16.

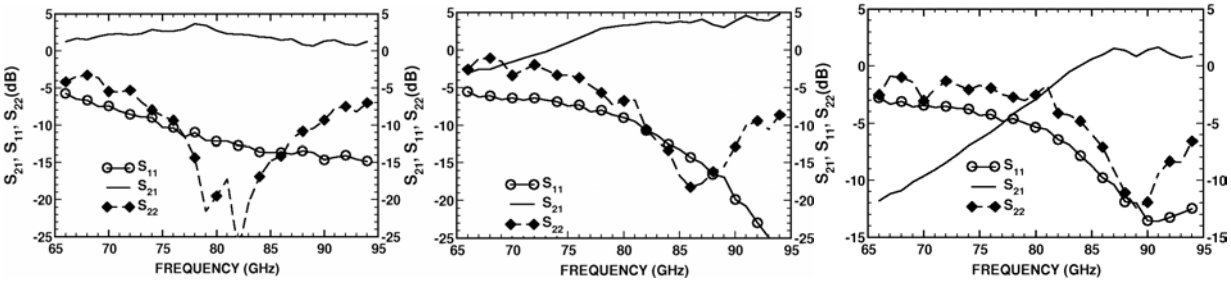


Figure 15: LNA S-parameter measurements (a) single stage cascode, (b) two-stage cascode, (c) transformer coupled cascade [12].

Table 6: LNA performance summary (measurements).

LNA	*S21 (dB)*	*frequency (GHz)*	*Power supply (V)*	*Current (mA)*
1-stage	3.8	78	1.8	8
2-stage	4.8	94	1.8	16
xfmr	1.65	92	1.5	23

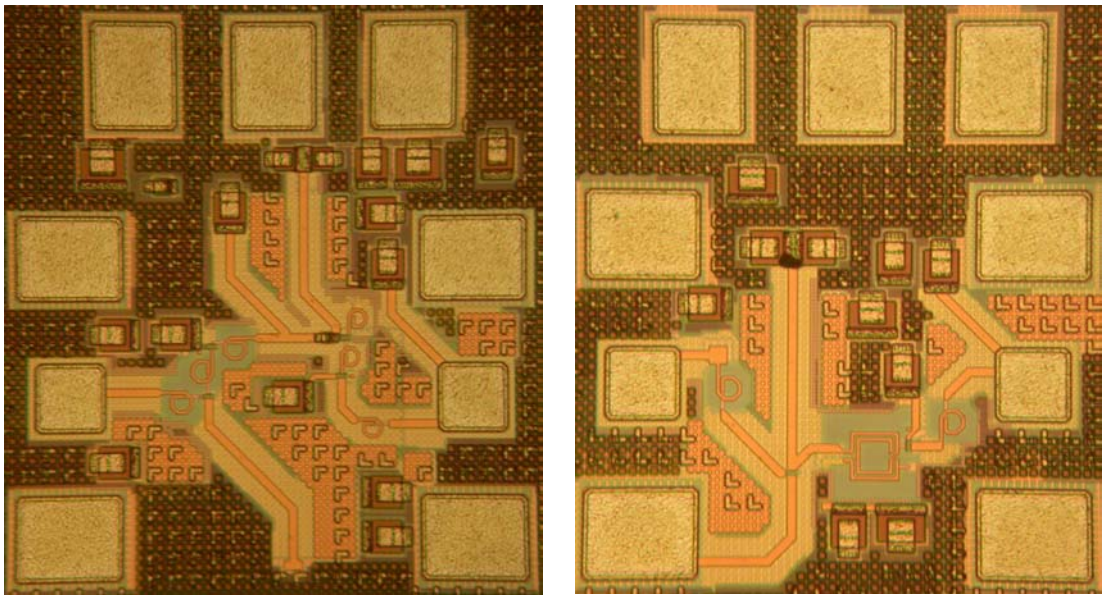


Figure 16: Die photos of a) 2-stage cascode and b) transformer-coupled CS-CG LNA [12].

9. Conclusion

An algorithmic design methodology for simultaneous noise and input impedance matching in mm-wave LNAs has been presented and verified using design examples and measurement results. It directly accounts for the pad capacitance and bond wire inductance without requiring iteration. Finally, the first CMOS W-band LNAs at 77 GHz and 94 GHz have been experimentally demonstrated.

Acknowledgements

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