Ultralow-Power Radar Sensors for Ambient Sensing in the *V*-Band

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***Abstract*— The design considerations and circuit topologies of a family of ultralow-power fundamental-frequency and second-harmonic 60-GHz radar sensors are described. The single-chip sensor architecture features four low-noise-matched receivers, either a fundamental-frequency 60-GHz voltage-controlled oscillator (VCO) or 30-GHz VCO + doubler, and a static divide-by-8192 chain which is turned OFF 95% of the time to save DC power. On-die measurements show a power consumption of 42 mW from a single 1.2-V supply, 10% frequency tuning range, −104 to −108 dBc/Hz phase noise at 10-MHz offset, 10-dB conversion gain per receiver, and −7-dBm transmitter output power at the antenna pads. Several 45-nm SOI-CMOS sensor dies were flip-chip mounted on a 7 × 7 mm^2 flexible interposer which also includes four receive- and two transmit antennas. Doppler and direction of arrival tests were conducted over distances of several tens of centimeters.**

***Index Terms*— Ambient sensing, CMOS, doppler sensor, Internet of Things (IoT), millimeter wave (mm-wave) radar, multichannel transceiver, SOI.**

I. Introduction

THE proliferation of drones, autonomous vehicles, and the expected introduction of billions of miniature Internet of Things (IoT) devices have created the demand for ambient sensing. Low-power millimeter wave (mm-wave) sensors for precise distance and velocity measurements can potentially fill this gap [1], [2]. Moreover, in small size gadgets [3], [4], mm-wave multichannel radar sensors [4] could provide an alternative gesture-based touchless user interface to the touch screen. Unfortunately, current mm-wave sensor implementations suffer from high power consumption or large form factors. At the same time, developing a multitransmitter, multireceiver sensor at 60 GHz or higher frequencies, needed for a small antenna footprint, with less than 100-mW power consumption, has proven to be a challenge [5], [6]. A multireceiver, multiantenna architecture, as opposed to a single-channel one [7], is needed to enable robust direction of arrival detection (DOA).

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Such a 60-GHz multichannel SOI-CMOS sensor transceiver with six antennas integrated on a thin 7 × 7 mm^2 flexible interposer and which consumes 40 times less power than previously published work was presented recently [8]. In this paper, we expand on the low-power circuit design methodology and provide additional measurement results. We also suggest that such low-power performance is not specific to SOI CMOS. By employing 1.2-V SiGe HBT VCO and local oscillator (LO) tree amplifier topologies, an identical sensor architecture with similar power consumption and performance can also be realized in a 55-nm SiGe BiCMOS process.

II. Sensor Architecture

The sensor architecture and its circuit topologies were specifically tailored to minimize power consumption while still achieving an output power of −7 dBm at the transmitter output pads, as needed for distance, velocity, and angle of arrival measurement over several tens of centimeter. Given the Doppler-mode operation and the short distances travelled by the mm-wave radiation to and from the target, phase-noise cancellation in the receiver is sufficiently strong to relax the VCO phase noise and output power requirements and thus allow for the lowest power VCO and transceiver implementation. Power consumption is further reduced by turning OFF the divider chain under normal operation conditions.

The block diagram of the proposed sensor is illustrated in Fig. 1. It consists of four identical receivers, a differential transmitter, a 60-GHz signal source, an LO tree, and a static divide-by-8192 chain. The signal source is implemented either as a fundamental-frequency VCO or to relax the divider specification and reduce its power consumption, as a 30-GHz VCO followed by a doubler. The divider output at 4-8 MHz is directly read by an off-chip microprocessor, which also provides the differential control voltage to modulate and lock the VCO. This allows for a variety of modulation schemes, including FMCW. While, for correct operation, the VCO, LO tree, transmitter, and all the receivers must be always turned ON; the divider chain, which consumes the most power, is OFF 95% of the time. It is only turned ON to periodically verify that the transmit frequency remains in the desired range.

III. Technology

The circuits were manufactured in GlobalFoundry's 45-nm partially depleted SOI-CMOS process with 11 metal layers in the back-end-of-line (BEOL). The top metal is 2.2 μm thick. The measured f_T/f_{MAX} values of the fully wired thin oxide MOSFETs used in this circuit are 250/250 GHz and

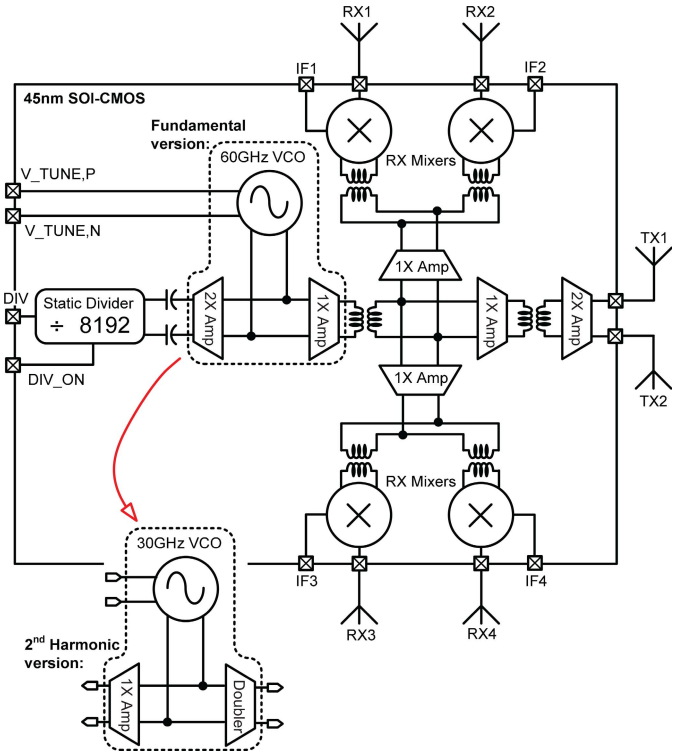


Fig. 1. Block diagram of the fundamental-frequency version of the 60-GHz sensor. Inset: changes made in the second-harmonic version.

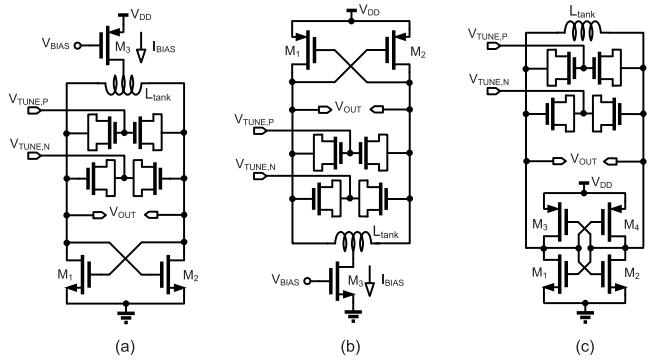


Fig. 2. Schematics of (a) nMOS, (b) pMOS, and (c) CMOS cross-coupled VCO topologies. All MOSFETs have a physical gate length of 40 nm.

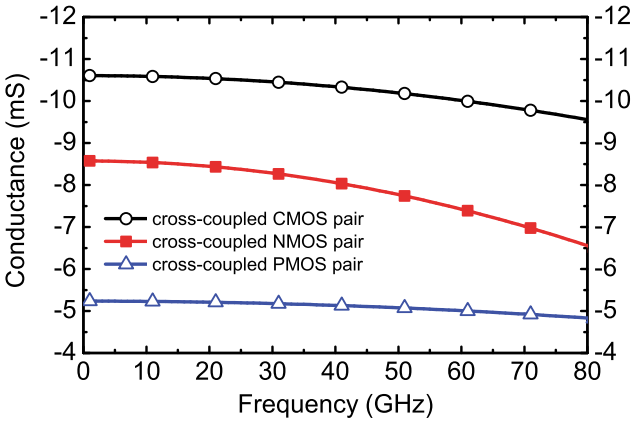


Fig. 3. Simulated small-signal negative conductance of cross-coupled transistor pairs.

180/250 GHz for n- and p-MOSFETs, respectively [9]. Although both thin and thick oxide varactors are available in the technology, thin-oxide n-MOSFETs with minimum gate length were preferred as varactors in the VCOs because of their higher quality factor at 60 GHz.

IV. Circuit Design

The main goal in the design of each circuit block was to minimize power consumption while still achieving the desired performance level. Only topologies capable of operation from 1.1 V or lower supplies were selected. With the exception of the CMOS cross-coupled VCO, n-channel MOSFETs were preferred in all 60-GHz circuits due to their higher f_T compared to p-MOSFETs. All MOSFETs in the 60-GHz path are biased at the peak f_{MAX} current density of 0.3 mA/μm, have the minimum physical gate length (40 nm), and a gate finger width of 0.78 μm for maximum power gain, low noise figure, and low phase noise. To minimize power consumption, in each circuit block, the smallest possible MOSFET gate width was employed that still allowed for matching networks which are realizable at 60 GHz in the technology BEOL. If the gate width and bias currents per stage are smaller than 1 mA, the input and output impedances of amplifier stages become too large for the realizable quality factor, leading to significant power gain degradation.

A. 60-GHz VCO

Because of the 250-GHz f_{MAX}, both the n-channel and p-channel MOSFETs have ample gain at 60 GHz. Therefore, nMOS, pMOS, and CMOS cross-coupled VCO topologies were considered. The schematics of three VCO topologies are reproduced in Fig. 2. The voltage control is realized through differentially driven AMOS varactor pairs in all three cases. To ensure that the full control range remains within the limits of the supply and that for reliability reasons, the peak-to-peak VCO swing does not exceed the supply, the mid-range of the control voltage should be set at $V_{DD}/2$. For the nMOS and pMOS versions, this is accomplished by placing the current-mirroring transistor (M_3) at the center tap of the tank inductor, instead of placing it at the common source node of M_1 and M_2. For the CMOS VCO topology, the control voltage is centered by adjusting the gate-width ratio of the n-MOSFET to the p-MOSFET (e.g., $W_p \approx 1.25\ W_n$). This also maximizes the voltage swing of the CMOS cross-coupled VCO.

The small-signal negative conductances were simulated as the function of frequency and are shown in Fig. 3. In these simulations, all three VCOs are biased at 4.5 mA from 1.2 V featuring the same $2 \times 12 \times 0.78$ μm $\times$40 nm n-MOSFETs and $2 \times 16 \times 0.78$ μm $\times$40 nm p-MOSFETs. For the same transistor sizes and bias current, the CMOS cross-coupled VCO shows the highest negative conductance since both n- and p-MOSFETs contribute to the negative conductance. In other words, the CMOS topology will oscillate at the lowest bias current and consume the least power.

Next, the large-signal performance of the two best candidates, the nMOS cross-coupled VCO and the CMOS cross-coupled VCO, is compared in Fig. 4, where the voltage swing

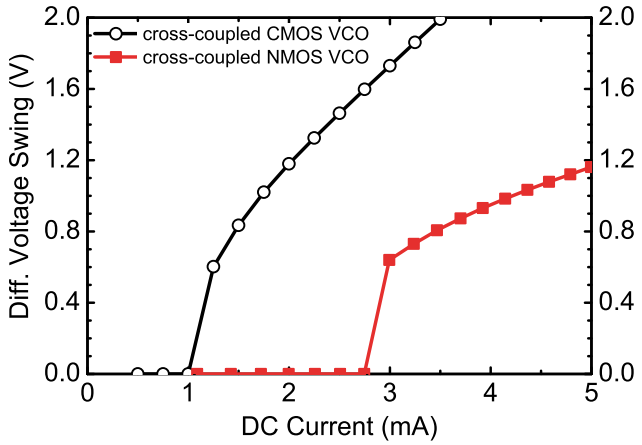


Fig. 4. Simulated large-signal output swing at 65 GHz of the nMOS and CMOS cross-coupled VCOs.

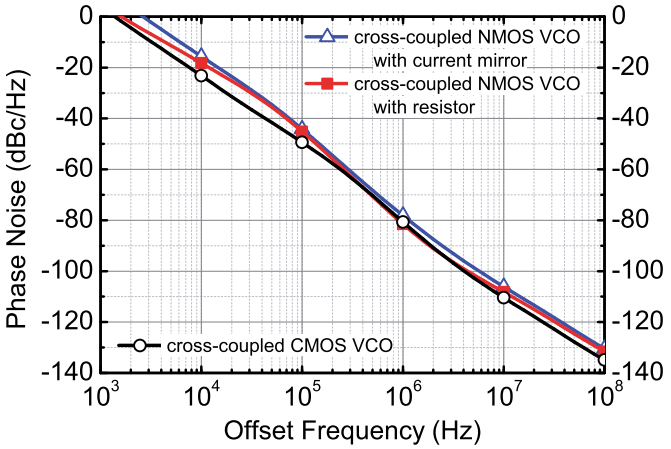
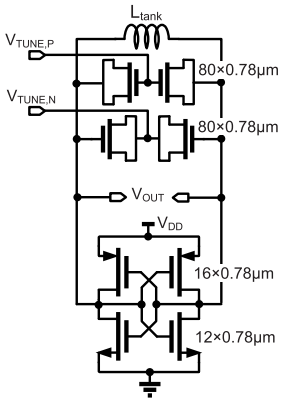


Fig. 5. Simulated phase noise at 65 GHz for the nMOS and CMOS cross-coupled VCOs, both biased at 4.5 mA.

was simulated as a function of bias current. The simulation results include full R-C extraction and electromagnetic (EM)-simulated tank inductors. Due to the larger negative conductance, the CMOS version starts to oscillate at a bias current of 1.25 mA, while the nMOS version needs at least 2.75 mA for the onset of oscillations. The CMOS version swings rail-to-rail, which also improves the phase noise. The phase noise was simulated for both VCOs at 65 GHz and is shown in Fig. 5.

Two different bias arrangements are compared for the nMOS version: one with current mirror (M_3) as in Fig. 2(a) and one with M_3 replaced by a resistor. Although the bias arrangement with resistor improves the phase noise for the nMOS version, the CMOS cross-coupled VCO has superior phase noise performance at almost all offsets, with 2.3 dB better phase noise at 10-MHz offset.

Due to the lower power consumption, larger output swing, and better phase noise performance, the CMOS cross-coupled VCO topology was selected for the sensor. The final schematic of the VCOs used for the fundamental and second-harmonic sensors is shown in Fig. 6. The different VCO versions were realized by varying the tank inductance. The exact inductor values are included in Fig. 6.



L_{tank} Fundamental	L_{tank} 2nd Harmonic
LF: 81pH	LF: 292pH
MF: 71pH	HF: 256pH
HF: 67pH	

Fig. 6. Schematic of the CMOS cross-coupled VCO used in the fundamental and second-harmonic 60-GHz sensors.

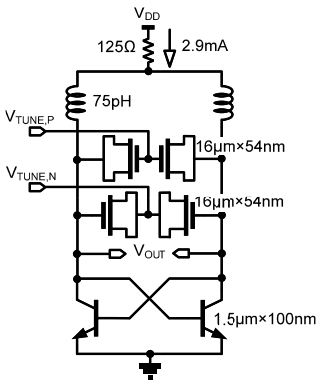


Fig. 7. Schematic of a 60-GHz SiGe HBT cross-coupled VCO used in a 55-nm SiGe BiCMOS version of the proposed 60-GHz sensor architecture [10].

For comparison, a 55-nm SiGe BiCMOS VCO topology [10], which is also capable of operation from 1 to 1.2-V supply with slightly lower power consumption and 2-3 dB lower phase noise at 1-MHz offset is shown Fig. 7.

B. 30-to-60-GHz Doubler

Two different balanced doubler topologies were considered for the second-harmonic versions of the 60-GHz sensor. Unbalanced topologies were not considered since they inherently have fundamental leakage. Harmonic resonators were avoided due to their large size at the frequency of operation. The first topology, shown in Fig. 8(a) [11], consists of a common-source n-MOSFET pair with a series-stacked common-gate n-MOSFET (M_3) added at their common drain node to amplify the $2f_0$ signal. The second topology, shown in Fig. 8(b), is an n-MOSFET cascode pair where the $2f_0$ signal is collected at the common drain of the common-gate MOSFETs, M_3 and M_4. In both designs, the input and output matching networks were optimized through the use of load-pull and harmonic-balance simulations. Fig. 9(a) compares the transfer characteristics, while Fig. 9(b) compares the output power and drain efficiency as a function of doubler bias for the two topologies. The common-source doubler with series-stacked common-gate amplifier topology in Fig. 8(a) proved to be better suited for the 60-GHz sensor due to the

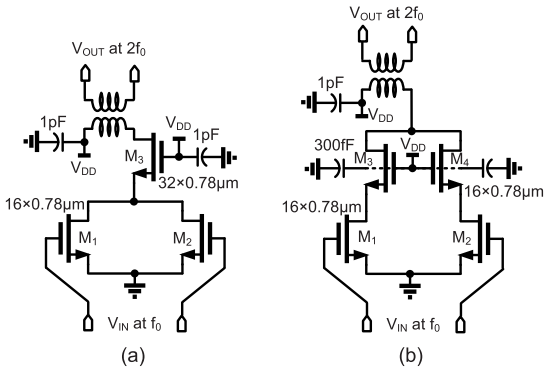


Fig. 8. Schematic of (a) 60-GHz common-source doubler with series-stacked common-gate device, and (b) 60-GHz cascode doubler.

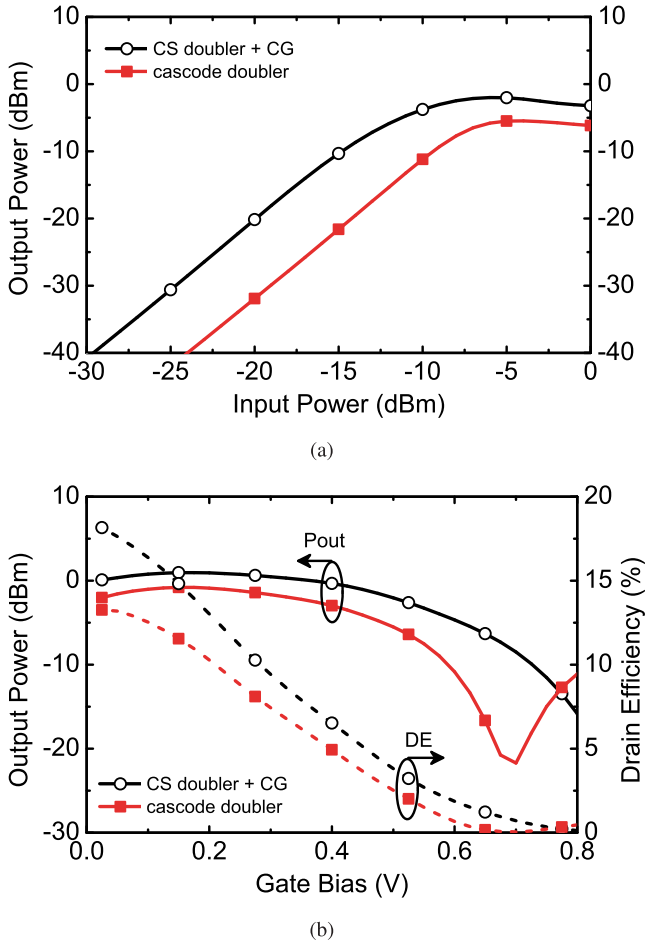


Fig. 9. (a) Simulated doubler transfer characteristics with V_{GS} = 0.5 V and (b) simulated doubler output power and drain efficiency as a function of the differential-pair gate-source bias voltage at 60 GHz ($P_{in} = -5$ dBm).

additional gain from common-gate device (M_3). It has 6 dB of conversion gain and 1 dBm of output power compared to 4.2 dB and −0.8 dBm, respectively, simulated for the cascode-doubler topology.

C. 60-GHz LO Tree

The 60-GHz LO tree and the transmitter output stage feature transformer-coupled differential cascode amplifiers. Only two different LO amplifier sizes (1× and 2×) are used in the

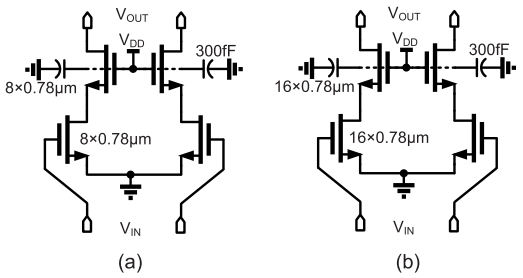


Fig. 10. Schematic of (a) 1× cascode LO amplifier and (b) 2× cascode LO amplifier.

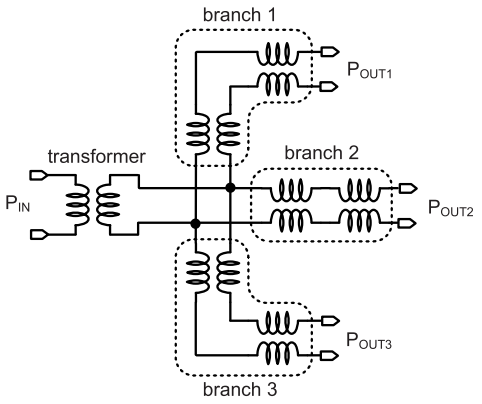
LO tree. Their schematics are reproduced in Fig. 10. Since the LO signal is generated on-die, the common-mode rejection of the transformers was sufficient and no explicit common-mode resistors were needed. The transmitter output stage and the LO stage driving the divider in the fundamental version of the sensor employ the 2× amplifier stage to maximize the output power and to boost the signal driving the 60-GHz divider. A maximum fan-out of three is used between the stages in the LO tree. Because of the large MAG of the cascodes (≈15 dB at 60–70 GHz), this fan-out proved sufficiently small to saturate the signal power in the LO tree. It also provides convenient transformer ratios for the 60-GHz frequency range.

A key goal in the LO tree design was to minimize the capacitive loading on the VCO to maximize its tuning range. It was accomplished by DC-coupling the VCO to the first stage of the LO tree, thus avoiding the use of series capacitors, interstage transformers, and long interconnects. The downside is that it prevents the directly coupled stages from being independently biased, which does impact their performance.

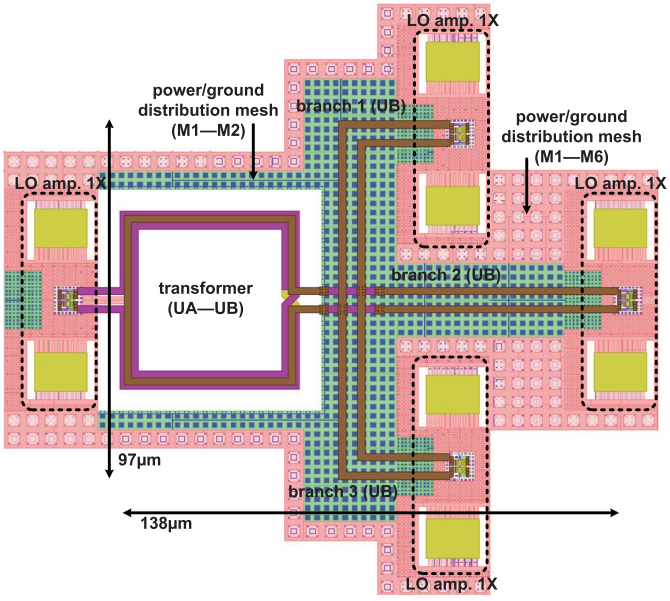
Another key element in the LO distribution network is the small-size, lumped-element, three-way power splitter. Unlike the 60-GHz sensor implementation in [4], where power splitting is done with a bulky three-way Wilkinson divider followed by three baluns for single-ended to differential conversion, the lumped approach, shown in Fig. 11, eliminates the unnecessary transformations to and from 50 Ω and takes advantage of the line inductances for interstage matching. The total area of the power splitter is 0.013 mm^2 compared to an estimated 0.45 mm^2 for the distributed approach in [4].

The following outlines the design steps for the three-way power splitter.

1) The outside branches of the splitter (branch 1 and branch 3) were drawn first, with the minimum possible span that allowed fitting the layouts of the following amplifier stages. All branches use narrow, inductive, and lines implemented with the top metal layers.
2) The central branch (branch 2) is drawn next and its physical length is optimized with an EM simulator [12] until it has the same electrical length as the outside branches. Fig. 12 shows the simulated phase for the three branches after optimization. The maximum phase difference is 0.4°.
3) The power splitter outputs are loaded with the three amplifier stages whose outputs are connected together to a single output port. The input port is placed at the



(a)



(b)

Fig. 11. (a) Schematic and (b) layout of the three-way power splitter.

three-way junction (i.e., where the output terminals of the transformer would be placed). This allows for a two-port simulation test bench instead of a four-port test bench.

4) The impedance seen at the input port at the frequency of interest is recorded and a transformer-based matching network to the preceding LO amplifier stage is designed.

The EM-simulated insertion loss, including the transformer losses and losses along the lines, is 1.1–1.2 dB at 60–70 GHz, as shown in Fig. 12. The advantage of this procedure is that maximum power transfer can be achieved without resorting to complex EM optimization of the four-port network.

D. 60-GHz Receivers

Like the VCO and LO tree, the four receivers are ON all the time during the operation of the sensor. Their power consumption must be minimized without significantly degrading receiver noise figure and gain. This can be achieved by combining the mixer, the LNA and IF amplifier in a single stage, and sharing the bias current. Each receiver, whose

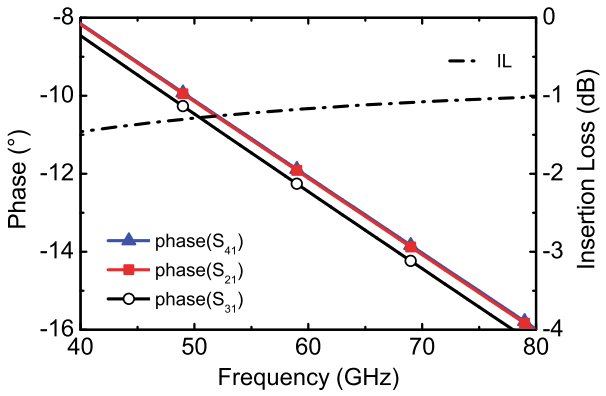


Fig. 12. Simulated phase and insertion loss of the three branches of the power splitter.

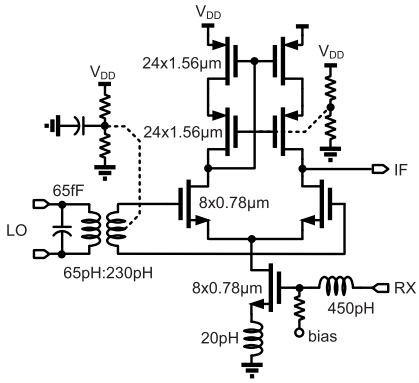


Fig. 13. Schematic of the CMOS single-balanced mixer. All MOSFETs have 40-nm physical gate length.

transistor-level schematic is shown in Fig. 13, consists of a low-noise, single-balanced mixer with large-swing current mirror load to maximize the conversion gain while minimizing the bias current and capacitive load seen by the LO tree. The transconductor is biased at 1 mA, at the minimum noise figure current density of 0.15 mA/μm, and is sized such that the real part of its input impedance is close to 50 Ω, thus simplifying the input matching network. The simulated single-sideband noise figure as a function of the IF frequency is reproduced in Fig. 14. The noise figure is 13.2 dB with a flicker noise corner at 40 MHz. With a simulated conversion gain of 10 dB per channel, the four receivers consume a total of 4.6 mW from 1.1 V.

Fig. 14 also includes the noise figure of a single-balanced mixer implemented in 55-nm SiGe BiCMOS [10]. Despite the higher noise figure at large offsets, beyond 10 MHz, the SiGe version has two orders of magnitude lower noise figure at low frequency offsets below 1 kHz.

E. 60-GHz Static Divider

The block diagram of the static 60-GHz divider chain is illustrated in Fig. 15(a) along with the current consumed by each stage from the 1.2-V supply. It consists of three CML D-type flip-flop divide-by-two stages followed by a CMOS-to-CML converter and 10 standard CMOS logic divide-by-two stages operating at frequencies below 9 GHz.

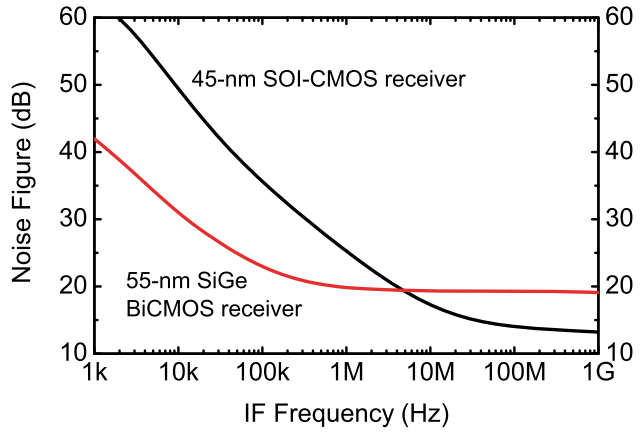


Fig. 14. Simulated single-sideband noise figure of the 45-nm SOI-CMOS single-balanced mixer compared to that of a 55-nm SiGe BiCMOS single-balanced mixer [10].

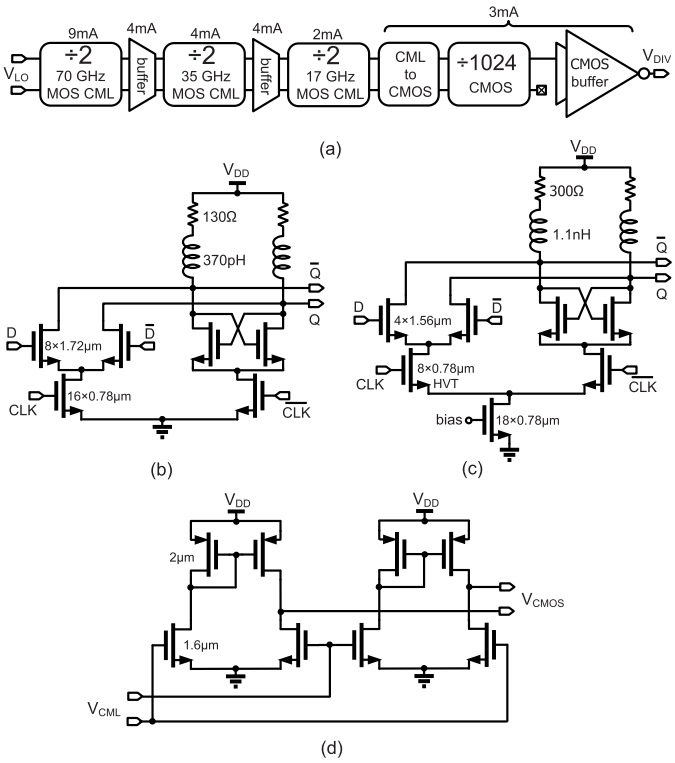


Fig. 15. (a) Block diagram of the 60-GHz divide-by-8192. (b) Schematic of the MOS quasi-CML latch in the 60-GHz divider stage. (c) Schematic of the MOS CML latch in the 30-GHz divider stage. (d) Schematic of the CML to CMOS converter. All MOSFETs have 40-nm physical gate length.

The schematics of the quasi-CML 60-GHz and CML 30-GHz divider stages are shown in Fig. 15(b) and (c), respectively. To save power, the 15-GHz divider uses a scaled version of the topology, as shown in Fig. 15(c). CML buffer stages were required after the 60-GHz and 30-GHz stages to amplify and filter the divided-down signals. The simulation results show that the divider requires 1.2 V or higher supply to divide correctly up to 70 GHz. However, for input signals below 40 GHz, as in the second-harmonic version of the sensor, 0.9-V supply is sufficient for correct operation, thus saving more than half of the nominal power consumption. This is important especially

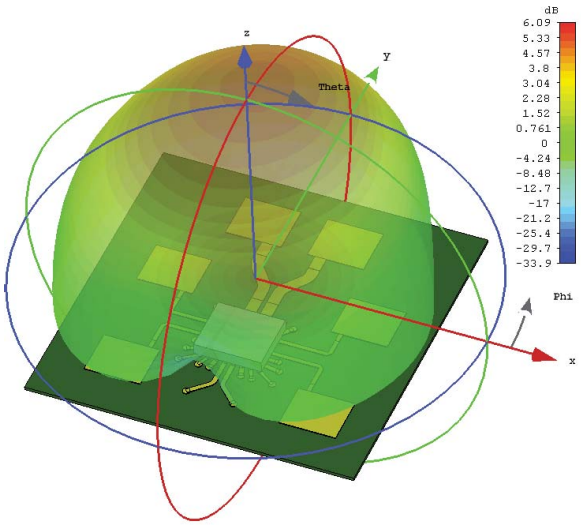


Fig. 16. Simulated realized gain pattern in transmit mode.

in short-distance (< 50 cm) ambient sensing, such as in gesture control of wearable gadgets, where the transmit power can be reduced below -30 dBm and the sensor can be operated from 0.9 V consuming only 18/27 mW with the divider OFF/ON.

F. Antennas

The four single-ended receive patch antennas and the differential transmit antennas were designed on an interposer. The transmit and receive antennas are polarized in the x-axis direction. The two transmit patches are fed differentially and placed at a distance of $< \lambda/2$ to each other. The CAD model and transmit realized gain pattern are shown in Fig. 16. The simulated realized gain (i.e., including losses and mismatch) at 62.5 GHz is 6.09 dBi with a radiation efficiency of 80%.

V. Experimental Results

Three variants of the fundamental-frequency sensor, centered on 63, 65, and 67 GHz, and two variants of the second-harmonic sensor, centered on 64 and 67 GHz, were designed and manufactured in the 45-nm SOI CMOS process mentioned earlier. In all cases, the center frequency of the LO tree was 67-68 GHz. All sensor variants worked within 2% of the targeted frequency range. Some of the flip-chip dies were post-processed by GlobalFoundries to remove the solder bumps and were tested with on-die probing. Several 67-GHz second-harmonic sensor dies were flip-chip mounted on an ultrathin 7×7 mm^2 interposer which includes the two transmit and four receive antennas, also centered on 67 GHz. The die micrograph and the interposer are reproduced in Fig. 17. Measurements such as output power and phase noise were conducted on die, while through-the-air Doppler and DOA tests were performed with the interposer and chip mounted on a PCB.

The versions with fundamental VCOs start to oscillate at 0.9-V supply and work reliably up to 1.4 V, while the second-harmonic versions oscillate with a supply voltage as low as 0.65 V. As shown in Fig. 18, the DC power consumption is about the same for all five variants. The measured

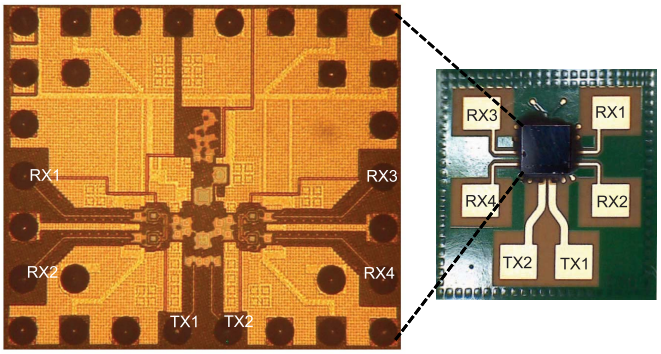


Fig. 17. Die microphotograph (1.18×1.36 mm^2) and flip-chipped mounted die on a 7×7 mm^2 interposer with four receive antennas and two transmit antennas.

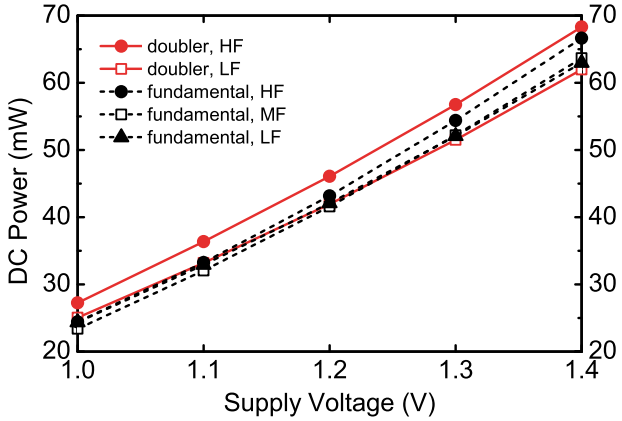
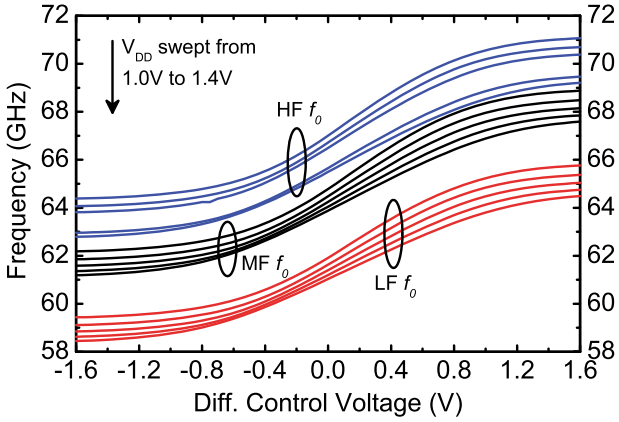
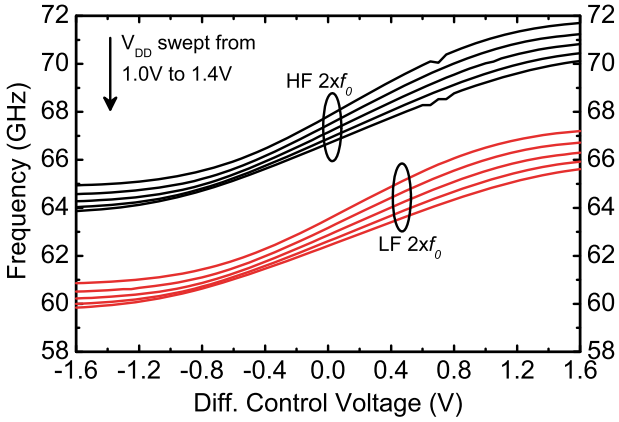


Fig. 18. Measured DC power consumption of the VCO and LO tree for the five sensor variants.



(a)



(b)

Fig. 19. Measured frequency tuning curve as a function of the differential control voltage for (a) three fundamental-frequency and (b) two second-harmonic versions of the 60-GHz sensor.

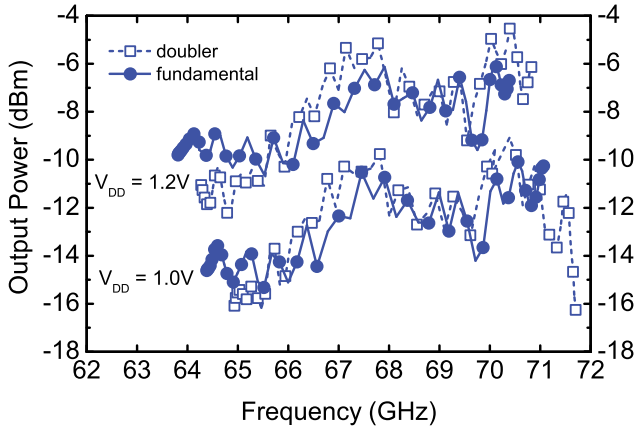
frequency tuning curves are summarized in Fig. 19 for all sensors at different supply voltages. The three fundamental variants of the sensor cover 58.5–65.8 GHz, 61.2–68.9 GHz, and 62.8–71.1 GHz, respectively, while the two second-harmonic variants cover 59.9–67.2 GHz and 63.9–71.7 GHz, respectively. The individual tuning range is greater than 11.6%. Together, an LF and HF fundamental or second-harmonic sensor pair covers the entire 59-71 GHz frequency range.

Fig. 20(a) depicts the measured output power versus frequency for the fundamental and second-harmonic 67-GHz versions at the antenna pads. A peak output power greater than -6 dBm was achieved with both fundamental and second-harmonic architectures. Also, less than 0.9-dB variation in the peak power can be observed across five randomly chosen dies [Fig. 20(b)]. The output power increases by about 1.5 dB per 0.1 V and shows signs of saturation at -4 dBm when the supply reaches 1.4 V. The tuning range remains approximately 10% for each value of the supply voltage. More importantly, the transmitter frequency changes by less than 80 MHz when the divider is turned ON and OFF, as shown in Fig. 21. This allows for the VCO to operate in open loop, with the divider turned OFF for more than 95% of the time. Fig. 20(a) depicts the measured output power versus frequency for the fundamental and second-harmonic 67-GHz versions at the antenna pads.

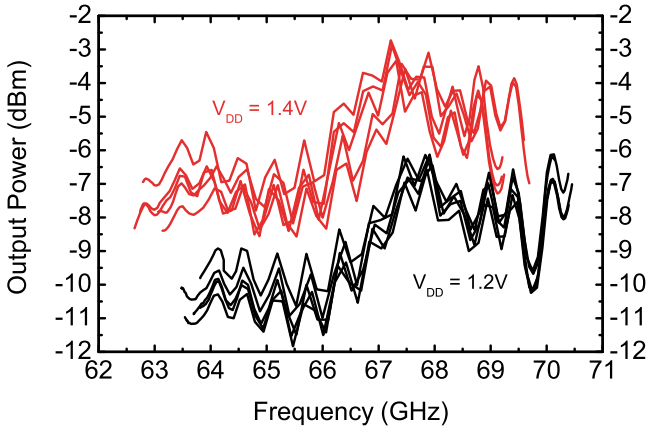
The phase noise was measured on die at one of the 60-GHz transmit antenna pads for all five sensor variants and also above the interposer with sensor and antennas mounted on the PCB. As shown in Fig. 23, the phase noise at 10-MHz offset increases with frequency and varies from -103.5 to -108 dBc/Hz. The fundamental-frequency sensors show 1-dB lower phase noise than the corresponding second-harmonic versions operating at the same output frequency. The power consumption is also lower by a few milliwatts in the fundamental sensor. At 1.2 V, the power consumption of the fundamental sensor is 42 mW with a corresponding transmitter output power of -7 to -6 dBm.

Finally, the experimental setup used to demonstrate short-range ambient sensing is shown in Fig. 24. Fig. 25 depicts the signals recorded at the four receiver baseband outputs during the Doppler test in which the moving target is asymmetrically positioned away to one side of the packaged chip on the PCB.

FMCW tests were also conducted up to a distance of 1 m using a 10-15 dB lens positioned above the PCB. The sweep bandwidth was approximately 1 GHz with a sweep time of 20 ms and was done using a digital-to-analog converter to modulate the VCO tuning input. The corner reflector, used in the experiments, had an RCS of 6.5 m^2 at a distance of 1 m and resulted in a received IF beat frequency signal with an amplitude of 10 mV$_{pp}$.



(a)



(b)

Fig. 20. (a) Comparison of the measured output power versus frequency characteristics for the 67-GHz fundamental and second-harmonic sensors. (b) Measured output power versus frequency for the 67-GHz fundamental sensor across five dies.

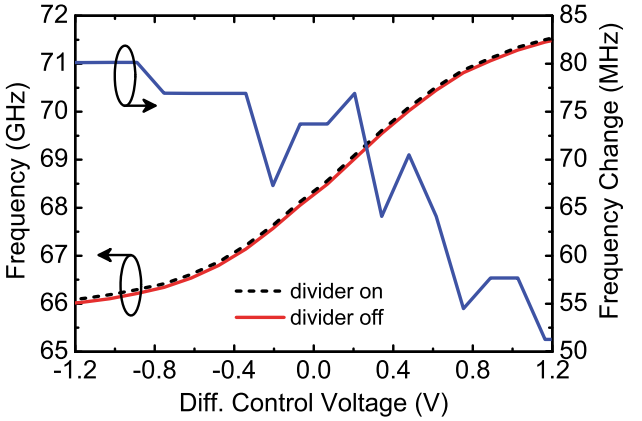


Fig. 21. Output frequency versus differential control voltage when the divider is turned ON and OFF.

All these experiments demonstrate that the output power and the phase noise are sufficient for a variety of ultralow-power applications such as touchless gesture control of wearable and IoT devices, and for short-range collision avoidance and autonomous navigation of miniature objects, robots, and drones.

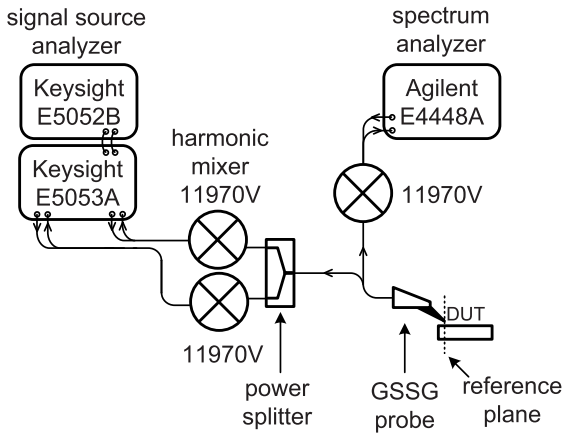


Fig. 22. Setup for the phase noise measurements at 50–75 GHz.

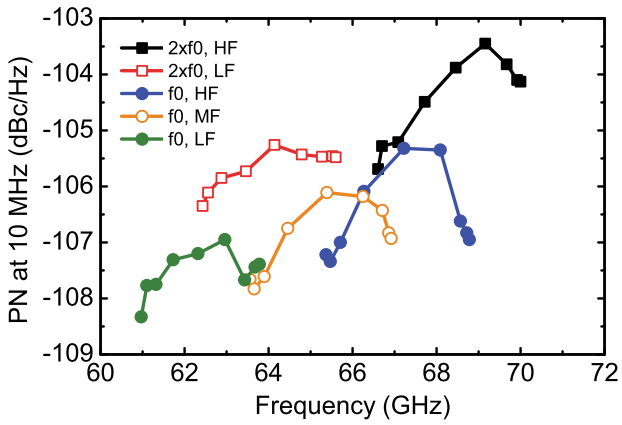


Fig. 23. Measured phase noise versus frequency for the five sensor versions.

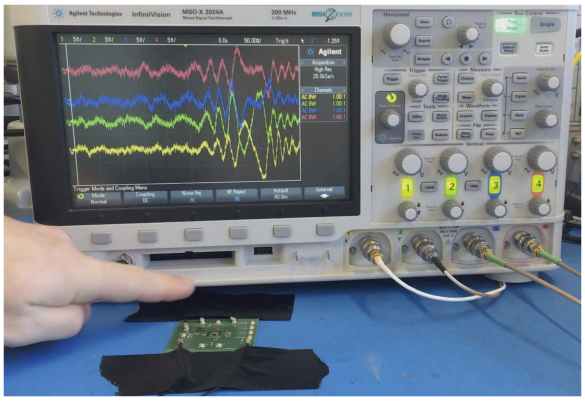


Fig. 24. Experimental setup and demonstration of ambient movement sensing.

Table I summarizes the performance of the fundamental and second-harmonic SOI-CMOS sensors and compares it to the state-of-the-art. An unpublished, low-power 55-nm SiGe BiCMOS implementation of the same fundamental-frequency sensor architecture [10] is also included in the table. The proposed sensor architecture has the same number of receive channels as the SiGe-HBT one in [4], consumes the lowest power and has the smallest footprint. The 20 times lower power consumption comes at the cost of 6–7 dB lower output

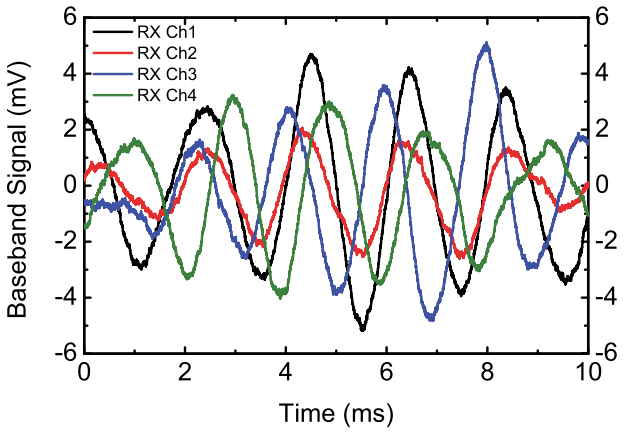


Fig. 25. Measured signals at the baseband outputs of the four received channels during the Doppler test.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO STATE-OF-THE-ART

Ref.	Tech.	Architecture	Freq. (GHz)	NF per RX (dB)	G_{RX} per RX (dB)	P_{out} (dBm)	PN (dBc/Hz)	P_{DC} (mW)	Area (mm^2)
This work f_0	45nm CMOS	TX, 4RX	63.8-70.2	13.2*	10*	-7	-105.5 to -107.5 (at 10MHz)	42 (V_{DD} = 1.2V)	1.60
This work $2\times f_0$	45nm CMOS	TX, 4RX	64-70.9	13.2*	10*	-6	-103.5 to -106 (at 10MHz)	54 (V_{DD} = 1.2V)	1.60
[10]	100nm SiGe BiCMOS	TX, 4RX	64.5-70.5	--	0*	-7	-104 to -106* (at 10MHz)	38	1.60
[4]	350nm SiGe BiCMOS	2TX, 4RX	57-64	10	19	4-5	-80 (at 100kHz)	990 (V_{DD} = 3.3V)	20.25
[1]	130nm SiGe BiCMOS	1TX, 1RX	120	8.5	12-36	0	-96 (at 1MHz)	350	3.96
[7]	90nm CMOS	1TX, 1RX	51-58	--	36	1.5	--	377 (V_{DD} = 1.2V)	2.26

*Simulation

power and 15-dB larger phase noise, none of which impede the correct operation for the intended applications.

As can be seen in the table, when the same sensor architecture with identical performance specification is realized in 55-nm SiGe BiCMOS using low-voltage, low-power SiGe HBT, and MOSFET circuit topologies, somewhat lower power consumption can be achieved. In fact, the power consumption in [10] could be reduced by another 11 mW if its 2.5-V, SiGe-HBT single-balanced mixer with 100-Ω resistive loads were replaced by a 1.2-V 55-nm n-MOSFET version of the mixer topology in Fig. 13.

VI. CONCLUSION

A comprehensive analysis of the system architecture and circuit topologies for ultralow-power multichannel Doppler radar transceivers was presented for a variety of short-range distance, velocity, and gesture sensing. Three fundamental- and two second-harmonic, ultralow-power multireceiver 45-nm SOI CMOS transceivers were designed, fabricated, and tested in the 59–71 GHz range. The fundamental-frequency sensor consumes a record low power of only 42 mW, at least 20 times less than a similar four-receive channels sensor reported recently [4]. The low power performance was made possible by the choice of CMOS inverter and n-MOSFET cascode circuit topologies, by the minimalist system architecture and by the reduced output power and phase noise requirements for the intended short-range applications. Although the reported results were obtained in a 45-nm SOI CMOS technology, we have shown that similar or lower power consumption is achievable in 55-nm SiGe BiCMOS, with slightly improved phase noise, if 1.2-V cross-coupled SiGe HBT VCO and LO-amplifier topologies are used.

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