Ultra-Broadband I/Q RF-DAC Transmitters

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***Abstract*— An ultra-broadband I/Q RF-DAC digital wireless transmitter architecture is proposed for 5G terminals and base stations. Broadband 1–32-GHz and tuned 20–32-GHz 2×6-bit versions of the transmitter were designed and manufactured in a production 45-nm SOI CMOS technology. They feature a process-and-temperature invariant quadrature phase generator with less than 1.4° phase error from 1 to 32 GHz, and a series-stacked, gate-segmented 2×6-bit I/Q RF-DAC. The transistor-level schematics of each block, and novel series-differential inductors for broadband common-mode rejection and differential-mode bandwidth extension are described in detail. The tuned transmitter prototype with transformer-coupled output stage achieved 19.9-dBm output power with record data rates of up to 30 Gbit/s and 24.6-pJ/bit efficiency in the 20–32-GHz range using QPSK, 16-QAM, 32-QAM, and 64-QAM modulation formats. The measured output power of the broadband transmitter is 18.4 dBm and remains larger than 13 dBm from 1 to 32 GHz. On-die generation of 16-QAM, 32-QAM, and 64-QAM modulated carriers at data rates of up to 20, 15, and 6 Gbit/s, respectively, was demonstrated.**

***Index Terms*— Digital power amplifier, digital transmitter, 5G, RF-DAC, 64-QAM, SOI CMOS.**

I. Introduction

THE next generation of 5G wireless terminals and base stations must be capable of operation at tens of gigabits per second, cover the newly proposed bands up to 30 GHz, and be backward-compatible with existing infrastructure. The traditional transmitter architecture with I and Q baseband DACs, linear up-convert mixers, and linear PA may no longer be the most energy-efficient and cost-effective solution to satisfy all of those requirements. A multioctave fully digital I/Q RF-DAC is an attractive candidate as it can provide a single-chip, low-cost, and small form-factor alternative. An RF power-DAC with 20-dBm output power, feasible in today's nanoscale SOI CMOS and SiGe BiCMOS technologies, can directly drive the antenna switches. If more output power is needed, for example in basestations, it can be followed up by a high-efficiency III–V power amplifier, similar to the one in [1].

During the past ten years, a large number of RF-DACs have been proposed, covering the 0.9 GHz [2] to 140 GHz [3], [4] spectrum. Most of them operate in the 0.9–5 GHz range at sub-gigahertz sampling rates [2], [5]–[7], and would not satisfy the 5G requirements mentioned earlier. However, more recently, millimeter-wave frequencies and multigigabit per second sampling rates have been demonstrated [8]–[15]. A more comprehensive discussion and survey of millimeter-wave RF-DAC concepts can be found in [16].

Some of the proposed millimeter-wave digital transmitter architectures describe I/Q RF power-DACs, where the output stage also acts as a high-efficiency power amplifier operating either in saturation or being shut off [8], [10], [14], and the I/Q signal summation and constellation formation is performed in free space.

In this paper, we build on the tuned, narrowband, multi-bit RF power-DAC concept with segmented-gate Gilbert-cell topology introduced in [11] to propose a new broadband I/Q RF-DAC transmitter architecture, in which, unlike [4], where the the I/Q signal summation and constellation formation was performed in free space above the on-chip antennas, the I/Q signal summation and constellation formation are realized on chip. In addition to the material discussed in [17], the modeling and design of the differential series-peaking inductors for broadband common-mode rejection are presented, and the experimental characterization of the broadband 1-to-32-GHz I/Q RF-DAC transmitter version with active series-stacked cascode load is covered for the first time and contrasted with that of the tuned 20–32-GHz transmitter.

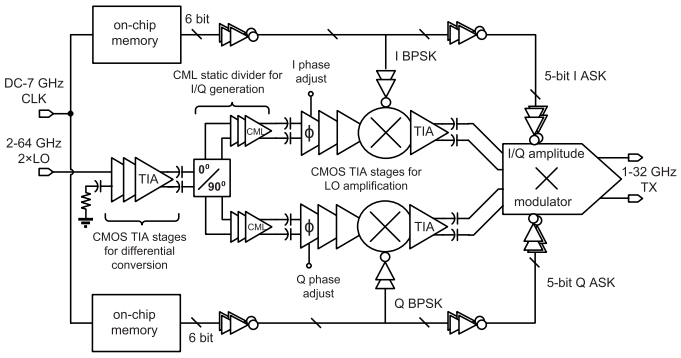

Fig. 1. Block diagram of the proposed 2×6-bit I/Q RF-DAC transmitters.

II. Broadband I/Q RF-DAC Transmitter Architecture

The block diagram of the proposed 2×6-bit I/Q RF-DAC transmitters is shown in Fig. 1. It consists of a dc–64-GHz input amplifier chain feeding a high-precision, process-and-temperature independent 1–32-GHz quadrature signal generator, I- and Q-path CMOS inverter chains, each followed by a BPSK modulator, and a large-power 2×5-bit I/Q amplitude modulator output stage. The 1–32-GHz quadrature (I/Q) carrier signals are generated by applying

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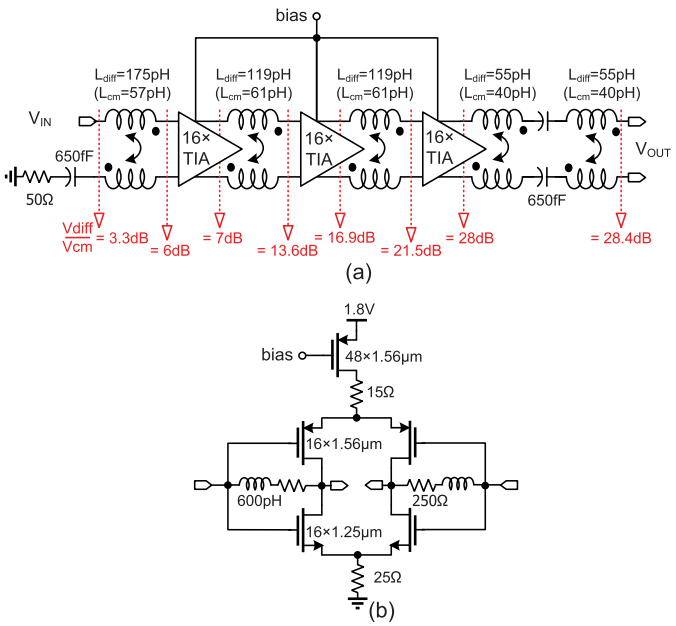


Fig. 2. Schematic of (a) 64-GHz bandwidth amplifier and (b) 64-GHz differential CMOS TIA stage. The half-circuit values of the differential series inductors are shown. $V_{\rm diff}/V_{\rm cm}$ represents the ratio between the differential-mode and common-mode signals at each node. All transistors have a physical gate length of 40 nm.

an external 2–64-GHz sinewave at the analog input of the transmitter. The 12-bit streams are stored through a clocked serial interface in two on-chip memories and then sent to the two BPSK modulators and 2×5-bit I/Q amplitude modulator output stage through 12 parallel CMOS inverter chains at up to 7-GHz clock frequency. The dc-7-GHz sampling clock is applied externally and is independent of and unrelated to the local oscillator (LO) carrier signal. The only difference between the broadband and tuned transmitters is the nature of the load used in the output stage.

Instead of applying an external signal for I/Q carrier generation, it is also possible to include a bank of phase-locked fundamental frequency voltage-controlled oscillators (VCOs) on chip, covering the second harmonic of the desired frequency bands. Fundamental VCOs driving static divider chains in 59–71-GHz frequency range have been demonstrated in the same 45-nm SOI CMOS technology used in this paper [18].

III. Circuit Design

A. Broadband 64-GHz Bandwidth Amplifier

Because only single-ended dc–64-GHz signal sources are available for testing the transmitter prototypes, a 2–64-GHz transimpedance amplifier (TIA) chain, shown in Fig. 2(a), with very good common-mode rejection up to 64 GHz must be included on chip for single-ended-to-differential conversion. Common-mode and power-supply rejection are achieved at low and moderate frequencies by adding common-mode resistors to ground and a p-MOSFET current source to the 1.8-V supply in each TIA stage, as illustrated in Fig. 2(b). At high frequencies, in the millimeter-wave regime, additional (passive) common-mode rejection is introduced by placing novel differential series peaking inductors between stages.

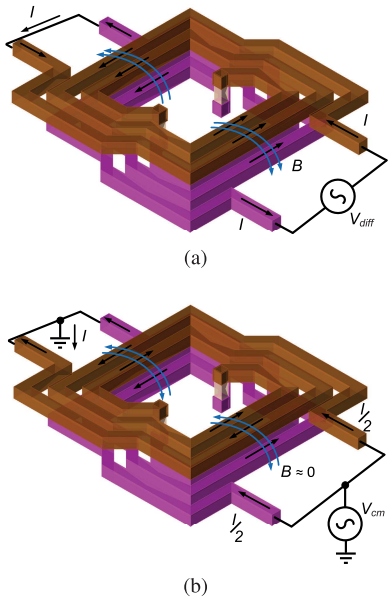


Fig. 3. Magnetic fields for a series differential inductor excited in (a) differential mode and (b) common mode.

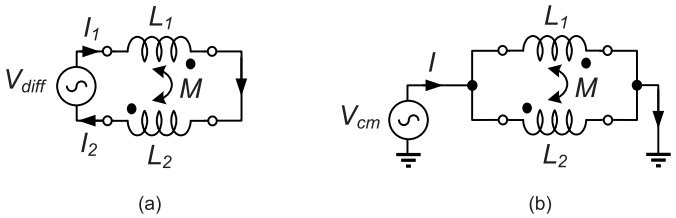


Fig. 4. Equivalent circuit representation for a series differential inductor excited in (a) differential mode and in (b) common mode.

The differential series inductors consist of two magnetically coupled coils with a specific direction of the windings such that the mutual inductance enhances the differential-mode peaking, while simultaneously minimizing the common-mode peaking. This is illustrated in Fig. 3 where the magnetic field B is strengthened during differential-mode excitation and diminished during common-mode excitation.

Using the equivalent circuits in Fig. 4 of two series-fed magnetically coupled inductors, L_1 and L_2, and the analysis techniques described in [19], the differential-mode inductance $L_{\rm diff}$ and common-mode inductance $L_{\rm cm}$ can be found as

$$L_{\rm diff} = 2(L+M) = 2L(1+k) \tag{1}$$

$$L_{\rm cm} = \frac{L-M}{2} = \frac{L}{2}(1-k) \tag{2}$$

where k is the magnetic coupling factor and $M = kL$ for equal coil inductances (e.g., $L_1 = L_2 = L$).

From (1) and (2), the relationship between the differential-mode and common-mode half-circuit inductance can be derived as

$$L_{\rm cm,half\text{-}circuit} = \frac{1-k}{1+k} L_{\rm diff,half\text{-}circuit}. \tag{3}$$

$L_{\rm diff,half\text{-}circuit}$ is sized to introduce a differential-mode zero at $\omega_{z,\rm diff}$ with conventional series-peaking techniques, while

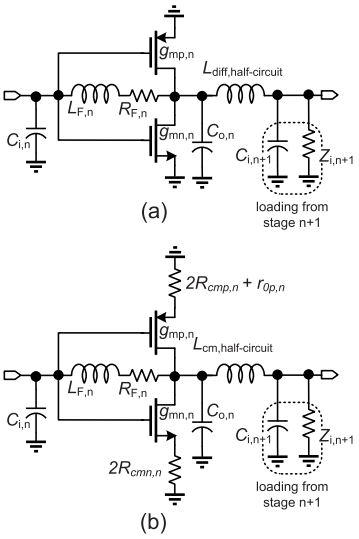


Fig. 5. Small-signal (a) differential- and (b) common-mode half-circuits of the differential CMOS TIA stage.

the associated zero produced by $L_{\text{cm,half-circuit}}$ appears at

$$\omega_{z,\text{cm}} \approx \frac{1+k}{1-k}\omega_{z,\text{diff}}. \tag{4}$$

When $k > 0.5$, the common-mode zero is at $\omega_{\text{cm,diff}} > 3\omega_{z,\text{diff}}$ and has little impact on the frequency response. This property is referred to as *selective peaking* of the differential-mode gain.

The resulting small-signal differential- and common-mode half-circuits for a single CMOS TIA stage are shown in Fig. 5. The expression for the differential-mode voltage gain (5), as shown at the bottom of this page, corresponds to that of a CMOS inverter with R–L shunt–shunt feedback and series peaking. For the common-mode voltage gain expression, the series peaking inductor contribution can be ignored when $L_{\text{cm,half - circuit}} \ll L_{\text{diff,half - circuit}}$, that is when k approaches 1. The gain expression reduces to that of a CMOS inverter with resistive degeneration and with R–L shunt-shunt feedback (6), as shown at the bottom of this page.

The impact of the differential series peaking inductors can be verified by comparing the voltage gain to the case when two uncoupled series peaking inductors are used in the interstage network. Fig. 6 shows the simulated differential- and common-mode voltage gains of a single TIA stage after layout parasitics extraction and electromagnetic (EM)-modeled inductors. In both cases, the circuits are optimized for differential-mode gain. When uncoupled series inductors are used, the common-mode gain peaks up to 4.7 dB at 107 GHz.

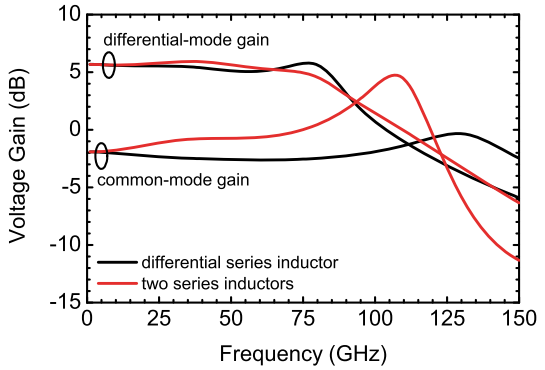


Fig. 6. Simulated differential- and common-mode voltage gain for a single LO amplifier stage when using differential series inductors compared to when using two separate series inductors.

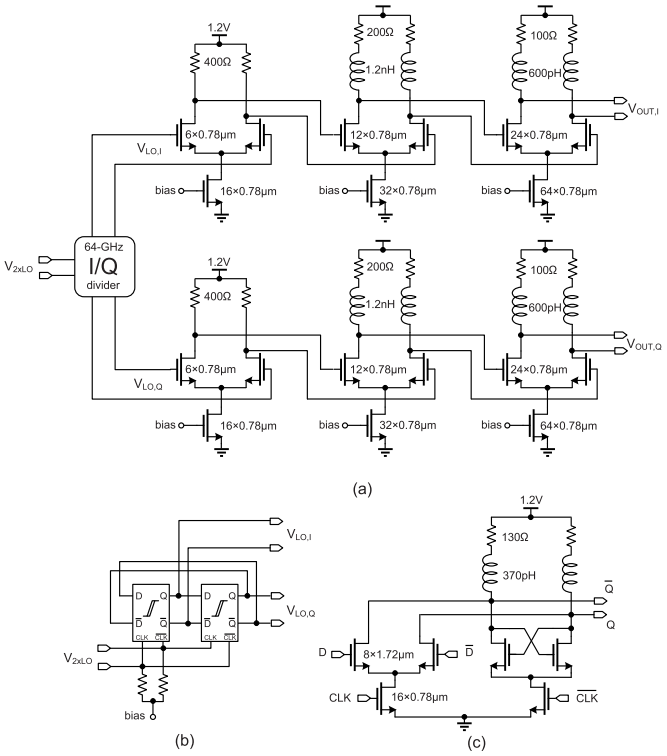


Fig. 7. Schematic of (a) 64-GHz I/Q divider with buffers, (b) 64-GHz I/Q divider, and (c) 64-GHz quasi-CML latch. All MOSFETs have 40-nm physical gate length.

In contrast, the proposed differential series inductor attenuates the common-mode signal at all frequencies and improves the common-mode amplifier stability of the circuit. As an additional advantage, the differential inductor occupies a 25% smaller footprint and contributes less capacitive parasitics.

$$A_{\text{diff},n}(s) = \frac{-(g_{\text{mn},n}+g_{\text{mp},n})\left(Z_{i,n+1}(s)\|\frac{1}{sC_{i,n+1}}\right)}{\left(g_{0n,n}+g_{0p,n}+sC_{o,n}+\frac{1}{R_{F,n}+sL_{F,n}}\right)\left(Z_{i,n+1}(s)\|\frac{1}{sC_{i,n+1}}+sL_{\text{diff,half - circuit}}\right)+1} \tag{5}$$

$$A_{\text{cm},n}(s) \approx \frac{-\frac{g_{\text{mn},n}}{1+2g_{\text{mn},n}R_{\text{cmn},n}}-\frac{g_{\text{mp},n}}{1+g_{\text{mn},n}(2R_{\text{cmp},n}+r_{0p,n})}}{sC_{o,n}+sC_{i,n+1}+\frac{1}{Z_{i,n+1}(s)}+\frac{1}{R_{F,n}+sL_{F,n}}} \tag{6}$$

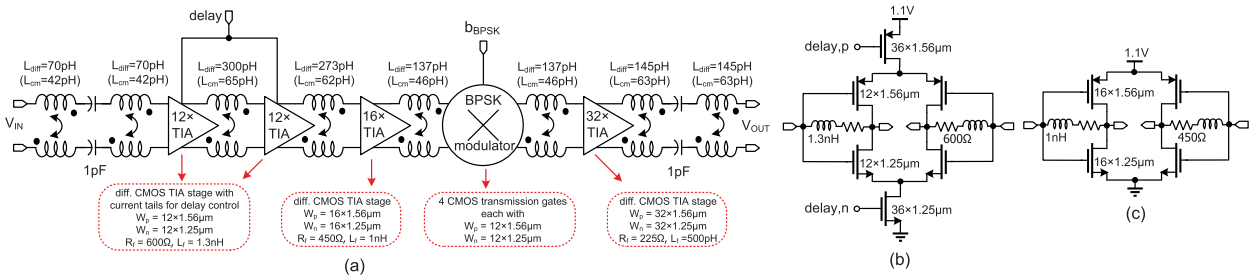


Fig. 8. Schematic of (a) 1–32-GHz amplifier with BPSK modulation used in the I and Q LO paths, (b) 32-GHz differential CMOS TIA stage with adjustable delay, and (c) 32-GHz differential CMOS TIA stage. The differential series inductances represent the half-circuit values. All MOSFETs have 40-nm physical gate length.

In the full 64-GHz amplifier circuit, the common-mode rejection can be verified by simulating with a single-ended 60-GHz 100-mV_{pp} input signal and observing the differential- and common-mode signals at different circuit nodes. The ratio of the differential-mode to common-mode signals is indicated at each node in Fig. 2. At 60 GHz, the differential series inductors provide 13 dB of additional common-mode rejection without consuming any dc power. Based on simulations of the 64-GHz amplifier and quadrature generator together, it was found that three CMOS-TIA stages with differential series inductors provide a sufficiently differential drive to the static divider for correct I/Q generation across frequency.

B. 1–32-GHz I/Q Divider

The I/Q generator is based on a static digital frequency divider as shown in Fig. 7. This scheme provides the broadest bandwidth with balanced I and Q digital outputs at half the input frequency and 90° phase difference which is insensitive to process, temperature, and supply variations. The static-divide-by-2 stage consists of a D-type flip-flop with quasi-CML latches to maximize the frequency of operation. The static divider is followed by a cascade of three CML inverters on each of the I and Q output branches. To minimize its footprint and allow placement in the close proximity of the divider, the first CML inverter (with 40-nm $\times 6 \times 0.78$-μm MOSFETs) has no inductive peaking. This proved to be critical in minimizing the capacitive loading of the divider, which stops dividing correctly for large loads. The divider and the CML inverters are biased from a 1.2-V supply. Series capacitors are used to separate the dc levels between the CML inverters and the following CMOS-TIA amplifier chain with BPSK modulator of the I and Q branches of the quadrature generator block. These capacitors limit the lower end of the I/Q generator bandwidth to 1 GHz.

C. 1–32-GHz Driver Amplifier and BPSK Modulator

The schematics of 1–32-GHz CMOS-TIA chain with BPSK (sign) modulation are shown in Fig. 8. As in the 64-GHz amplifier, differential CMOS inverters with R–L feedback and series inductive peaking are used, but without common-mode resistors. Removing the latter allows for a lower power supply of 1.1 V. To compensate for potential I/Q phase errors, the first two stages feature adjustable tail currents for delay control. Fig. 8(b) shows the schematic of the adjustable delay stage, while Fig. 9 depicts the simulated intrinsic phase error of the static divider and the phase adjustment range. Phase adjustment beyond this range begins to starve the CMOS TIA stages and prevents them from reaching full swing.

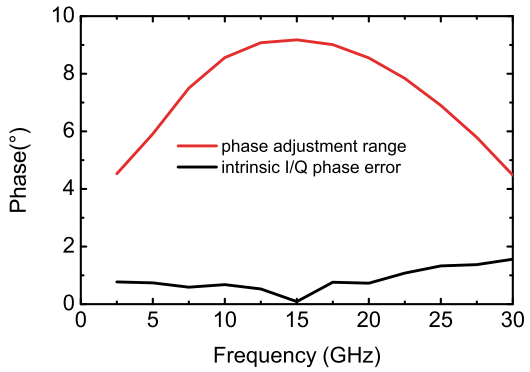


Fig. 9. Simulated I/Q phase error and phase adjustment range versus frequency.

The broadband BPSK modulator is implemented with four CMOS transmission gates similar to [20] and is placed as close as possible to the output stage to minimize the impact on the modulated signal. One extra CMOS TIA stage is added after the BPSK modulator to compensate for the loss and to ensure full rail-to-rail signal drive to the stacked output stage.

D. Broadband I/Q Amplitude Modulator Output Stage

The schematic of the single-quadrant 2×5-bit I/Q RF power-DAC used in the tuned 20–32-GHz version of the transmitter is shown in Fig. 10. Series-stacked common-gate devices [21] are placed after each I and Q 5-bit amplitude modulator to minimize mutual load pulling. Three more series-stacked common-gate n-MOSFETs are added after the I/Q summation node to amplify the complex-modulated LO-signal and increase the optimal load impedance without a matching network. The 20–32-GHz frequency range is set by the output transformer, the only tuned element in the entire I/Q RF-DAC transmitter.

The schematic of the 5-bit amplitude modulator at the core of the RF-DAC is shown in Fig. 10(b). It is implemented with a common-source version of the gate-segmented Gilbert

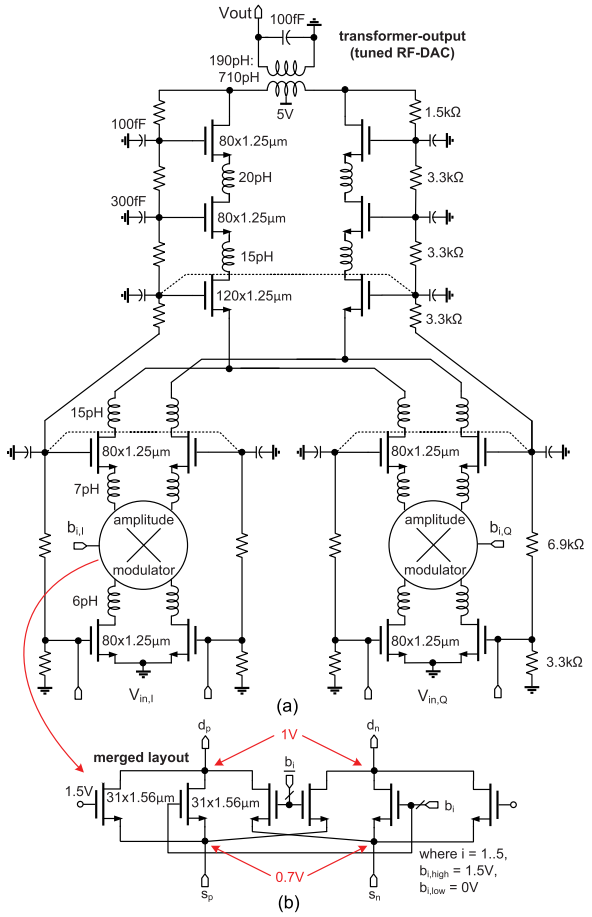


Fig. 10. Schematic of (a) series-stacked single-quadrant 2×5-bit RF-DAC with transformer output, and (b) Gilbert-cell-based 5-bit amplitude modulator. All MOSFETs have a gate length of 40 nm.

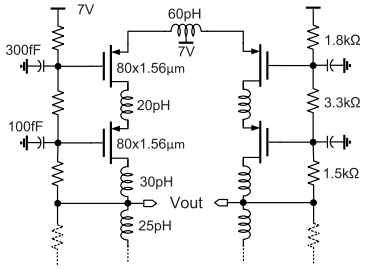


Fig. 11. Schematic of the series-stacked active load for the broadband I/Q RF-DAC. All p-MOSFETs have 40-nm physical gate length.

cell used at 138 GHz in [3]. The five binary-weighted gate-finger groupings of the Gilbert cell are driven with thick-oxide CMOS inverters, as in the 90-GHz RF power-DAC in [11].

To compensate for the delay experienced by the LO signal passing through the BPSK modulators, two extra inverters are included in the CMOS-inverter chains providing the 10 bits to the I/Q amplitude modulator output stage, compared to the number of inverters in the two CMOS-inverter chains driving the BPSK modulators.

In the 1–32-GHz broadband transmitter version, the transformer is replaced by the series-stacked p-MOSFET cascode active load shown in Fig. 11. The number of p-MOSFET

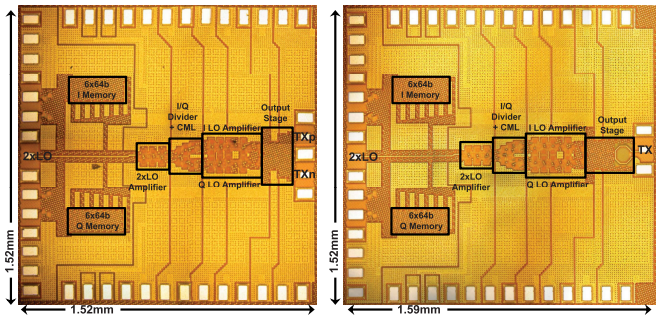


Fig. 12. Die micrographs of (a) 1–32-GHz I/Q RF-DAC and (b) 20–32-GHz I/Q RF-DAC transmitters.

devices in the active load is selected to accommodate the voltage swing per side

$$P_L \leq \frac{V_{\mathrm{pp}}^2}{8R_L} = \frac{(NV_{\mathrm{DS,MAX}})^2}{8R_L} \tag{7}$$

$$N \geq \frac{2\sqrt{2P_LR_L}}{V_{\mathrm{DS,MAX}}} \tag{8}$$

where N is the number of p-MOSFET devices, $V_{\mathrm{DS,MAX}}$ is the maximum instantaneous value of the drain–source voltage allowed per device (i.e., 2.2 V for 45-nm SOI CMOS), P_L is the output power per side, and R_L is the load per side. For a total output power of 17 dBm into a 100-Ω load (i.e., 14 dBm into a 50-Ω single-ended load) an active load with two devices is required. The capacitors at the gates of the active load devices evenly distribute the voltage swing and are sized with the same method as a regular stacked output stage [22].

IV. Experimental Results

The broadband and the tuned I/Q RF-DAC prototypes were designed and manufactured in GlobalFoundries' commercial 45-nm SOI CMOS process with 11 metal layers. The top metal is 2.2 μm thick. The measured f_T/f_{MAX} values of the fully wired thin oxide MOSFETs used in this circuit are 250/250 GHz and 180/250 GHz for n- and p-MOSFETs, respectively [23]. The die micrographs are shown in Fig 12. The total die areas, including on-chip memory and pads, are 1.52×1.52 and 1.52×1.59 mm^2, respectively.

A. Continuous-Wave Measurements

All measurements were conducted on die. The broadband and tuned variants of the I/Q RF-DAC transmitter were first characterized in continuous wave (CW)-mode by fixing the 12-bit input digital code word to the maximum amplitude setting and monitoring the output with a spectrum analyzer. This was needed to optimize the bias points of the 64-GHz divider and 64-GHz amplifier, and to measure the divider sensitivity which is reproduced in Fig. 13. It was found that an input signal of -1 dBm was sufficient for correct divider operation up to a 64-GHz input frequency. By turning off the input LO signal, the input-referred self-oscillation frequency of the static divider was found to be 43.95 GHz.

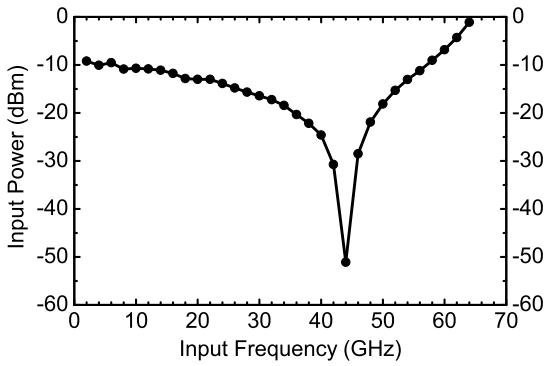
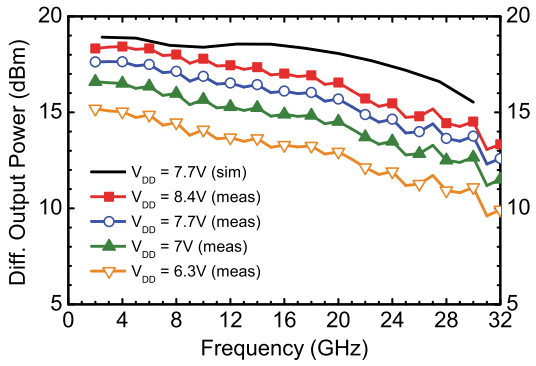
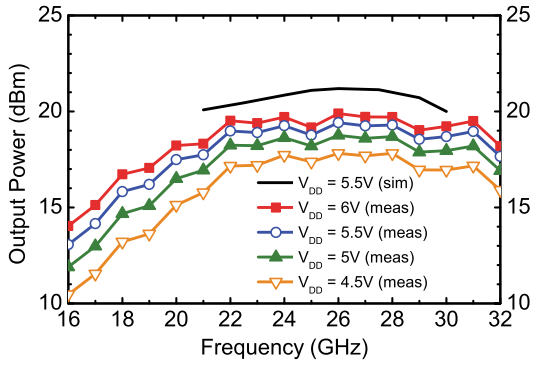


Fig. 13. Measured sensitivity of the I/Q divider.



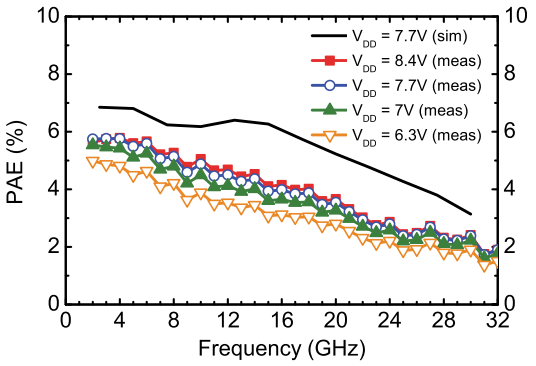
(a)



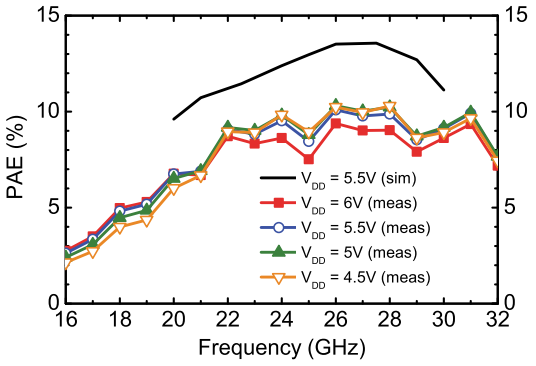
(b)

Fig. 14. Measured output power as a function of frequency for (a) broadband 1–32-GHz transmitter and (b) tuned 20–32-GHz transmitter.

The output power of the two transmitters was measured with a 50-GHz power sensor directly attached at the output probe to minimize the de-embedding errors. The setup losses were measured with a VNA using a two-tier calibration procedure. They were removed from the large signal measurement readings. Fig. 14(a) and (b) reproduces the output power as a function of frequency and output-stage supply voltage for both versions of the transmitter. The 4.5–6-V and 6.3–8.4-V supply voltages in Fig. 14(a) and (b) correspond to V_{DS} values of 0.9–1.2 V per series-stacked device. The maximum output power was 18.4 dBm at 4 GHz for the 1–32-GHz version, and 19.9 dBm at 26 GHz for the tuned version. The large-signal output 3-dB bandwidth of the broadband transmitter



(a)



(b)

Fig. 15. Measured power added efficiency as a function of frequency for (a) broadband 1–32-GHz transmitter and (b) tuned 20–32-GHz transmitter.

version was 24 GHz. In all measurements, the power of the fundamental tone remained at least 13 dB greater than the third harmonic. It should be noted that the broadband nature of the power sensor implies that the power of the third harmonic is included in the reported output power, especially at frequencies below 17 GHz; however, this error is at most 0.02 dB.

The PAE (Fig. 15) of the tuned and broadband transmitters was measured by accounting for all the power supplies, except the supply of the digital CMOS inverter chains, which does not consume power under static conditions. The peak PAE for the broadband version is 5.8% at 4 GHz and drops off at higher frequencies, as one would expect, while the peak PAE of the tuned version is 10.3% at 26 GHz and remains larger than 9% from 22–31 GHz. A maximum drain efficiency of 15.6% was observed at 26 GHz for a 4.5-V supply. The drain efficiency improved at lower supply voltages since the resistive ladder biasing the gates of the stacked output stage pushes the stage deeper into the class-AB mode of operation. Although PAE is important for RF-DACs which should operate as efficient power amplifiers in CW-mode, a more representative figure of merit is the energy efficiency, which was investigated next through a series of modulation experiments.

B. Modulated-Carrier Experiments

An 80-GSa/s real-time oscilloscope with 31.25-GHz bandwidth was used to measure the constellations, EVM, spectra, and to recover the I and Q eye diagrams synthesized at the

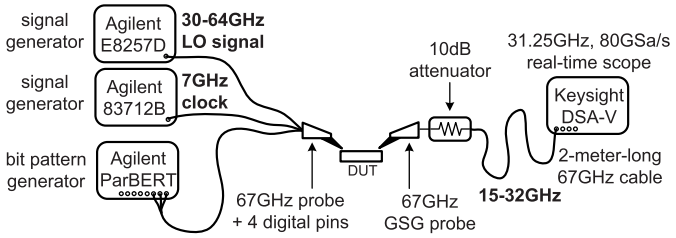


Fig. 16. Block diagram of the measurement setup used for the tuned 20–32-GHz transmitter.

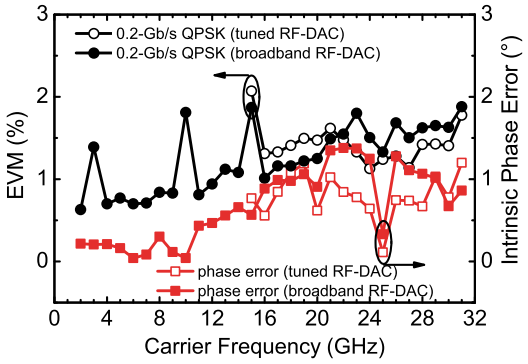


Fig. 17. Measured EVM of a QPSK signal without DPD, and corresponding intrinsic I/Q phase error versus frequency for the broadband 1–32-GHz and tuned 20–32-GHz transmitters.

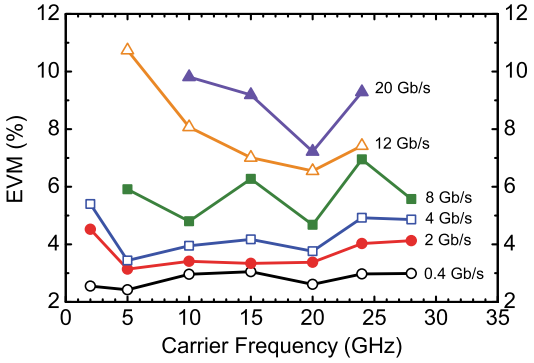


Fig. 18. Measured EVM of a 16-QAM modulated carrier versus carrier frequency and data rate for the broadband 1–32-GHz transmitter.

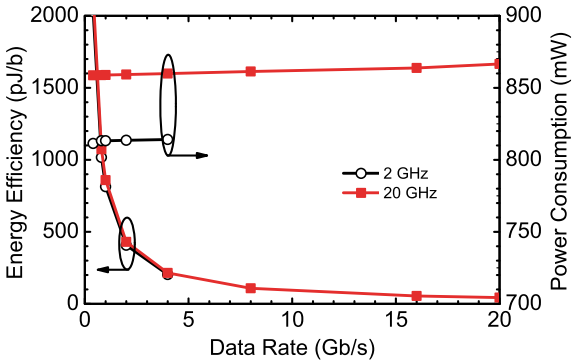


Fig. 19. Measured energy efficiency and dc power consumption for 16-QAM signals versus data rate at 2 and 20 GHz (broadband 1–32-GHz transmitter).

output of the I/Q RF-DAC transmitters from the 12 digital bit streams and the 2–64-GHz external LO signal. The block diagram of the test setup used to perform these measurements on the tuned transmitter variant is shown in Fig. 16. The same setup was used for the broadband version except for adding an external balun for differential to single-ended conversion. The external balun has a maximum gain imbalance of 1.2 dB and a maximum phase imbalance of 8.5°. Measurements were performed without equalization of the output probe and 2-m long cable connecting the probe and the oscilloscope.

DPD was applied to compensate for the code-dependent amplitude and phase nonlinearities of the RF-DACs, which were operated in saturated mode without backoff. It involved iteratively adapting the input digital code words at 20–100 Msymbols/s, where little memory and bandwidth effects are present. The iterative approach was necessary due to the presence of AM–PM distortion.

The accuracy of the quadrature generation was first verified by generating narrow-bandwidth (200 MHz) QPSK-modulated signals without DPD or phase correction. The measured EVM and corresponding intrinsic I/Q phase error of the QPSK-modulated signal are shown versus carrier frequency for the two transmitters in Fig. 17. The broadband version has an EVM and phase error better than 1.9% and 1.4°, respectively, over the 1–32-GHz frequency range. In the tuned version, they are better than 1.8% and 1.2°, respectively, from 16 to 32 GHz.

The EVM of the 16-QAM constellations generated at the output of the 1–32-GHz transmitter were measured as a function of the carrier frequency at different data rates and are summarized in Fig. 18. An EVM better than 10% was measured at a data rate of 20 Gbit/s with carrier frequencies ranging from 10 to 24 GHz. The highest modulation accuracy (7.2% EVM) was reached for a 20-GHz carrier. The EVM variations with frequency, especially at the higher data rates, are most likely due to gain and phase imbalances in the off-chip balun.

Next, the measurement results for 2- and 20-GHz carriers, where the external balun has the least amount of imbalance, are compared in detail. The energy efficiency and dc power consumption at the two carrier frequencies and for different data rates are reproduced in Fig. 19. The dc power consumption increases by 47 mW when the carrier frequency increases from 2 to 20 GHz, while there is less than 1% increase in the total power consumption when the symbol rate increases from 0.1 to 5 GBaud. The larger impact on power consumption observed when changing the carrier frequency is attributed to the 1–32-GHz I- and Q-path amplifiers, which are operated in switching mode. At the highest data rate of 20 Gbit/s, an energy efficiency of 43.3 pJ/b was measured.

For the tuned 20–32-GHz I/Q RF-DAC, the measured EVM versus data rate and modulation format is shown in Fig. 20. A 24-GHz carrier frequency was selected to ensure that the modulated signal remains within the bandwidth of the oscilloscope. The highest possible data rate is 30 Gbit/s for a 32-QAM modulation format with a corresponding energy efficiency of 24.6 pJ/bit. The measured 6-pulse-amplitude modulation I and Q eye diagrams of a 20-Gbit/s 32-QAM

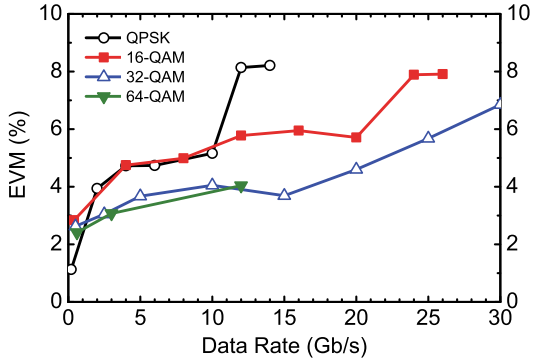


Fig. 20. Measured EVM versus data rate and modulation format at a 24-GHz carrier frequency for the tuned 20–32-GHz transmitter.

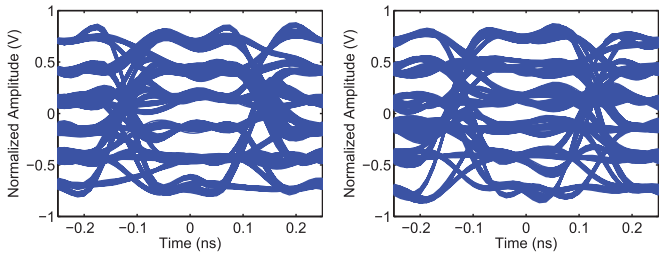


Fig. 21. Measured (a) I and (b) Q eye diagrams of a 24-GHz, 20-Gbit/s 32-QAM signal after carrier recovery by the oscilloscope.

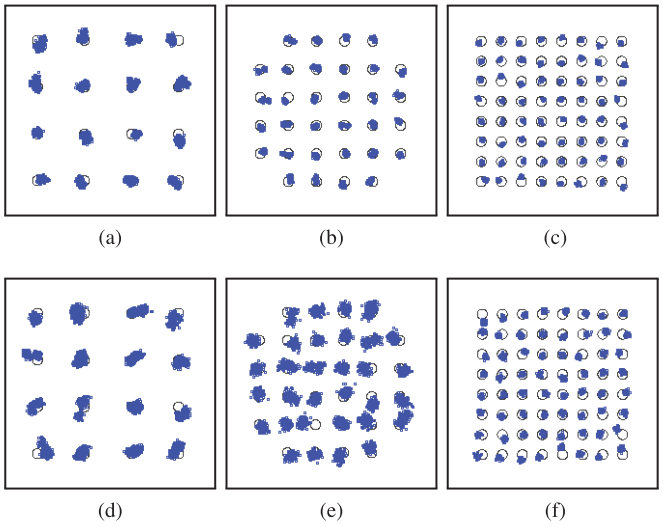
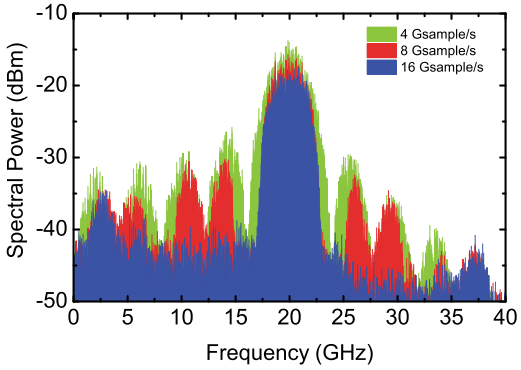


Fig. 22. Measured constellations at 24 GHz for various modulation formats and data rates (tuned 20–32-GHz transmitter). (a) 20 Gbit/s and 5.7% EVM. (b) 15 Gbit/s and 3.7% EVM. (c) 3 Gbit/s and 3.1% EVM. (d) 26 Gbit/s and 7.9% EVM. (e) 30 Gbit/s and 6.9% EVM. (f) 12 Gbit/s and 4.0% EVM.

signal after carrier recovery by the oscilloscope are shown in Fig. 21(a) and (b).

Constellations for the tuned 20–32-GHz transmitter are reproduced in Fig. 22.

Modulation formats with less out-of-band emissions, such as OFDM, are also possible with this transmitter architecture and have been demonstrated with the same number of bits at 138 GHz [4]. Since the on-chip memory depth of these prototypes was too low for the long OFDM symbols, they could not be demonstrated experimentally in this paper.



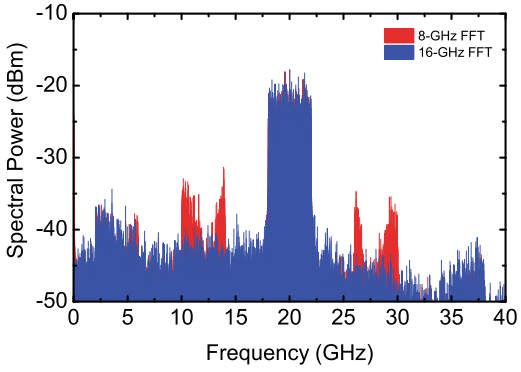


Fig. 23. Spectra of (a) 16-Gbit/s 16-QAM oversampled signals and (b) 24-Gbit/s 64-QAM OFDM signals at different sampling rates.

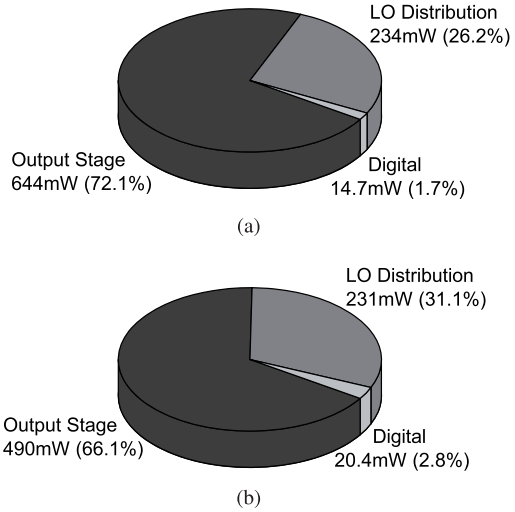


Fig. 24. DC power breakdown for (a) broadband 1–32-GHz transmitter operating at 20 Gbit/s and (b) tuned 20–32-GHz transmitter operating at 30 Gbit/s.

However, simulations with oversampling, as well as simulations with OFDM signals, were performed and the results are reproduced in Fig. 23. To further reduce the out-of-band emission to −40-dBc levels, an I/Q RF-DAC with several more bits, as well as DPD with memory, would have to be designed.

The power consumption breakdown of the two I/Q RF-DACs is shown in Fig. 24, while Table I summarizes their performance and compares it to state-of-the-art digital

TABLE I
COMPARISON TO STATE-OF-THE-ART DIGITAL TRANSMITTERS AT 10–60 GHz

Ref.	Tech.	Freq. (GHz)	3-dB BW (GHz)	Modulation Format	Data Rate (Gb/s)	EVM (%rms)	Energy Eff. (pJ/b)	Gain (dB)	Peak P_{SAT} (dBm)	Peak PAE (%)
This work	45nm SOI CMOS	15–32	18–32	16QAM 32QAM 64QAM	26 30 12	7.9 6.9 4	24.6 29.5 --	> 25	19.9	10.3
This work	45nm SOI CMOS	1–32	1–24	16QAM 32QAM 64QAM	20 15 6	7.2 6.6 4.4	44.6 59.3 150	> 25	18.4	5.8
[9]	45nm SOI CMOS	38–49	42–47	16QAM QPSK	0.04 1.25	8 5.5	675*	7.1	21.3	16
[10]	65nm CMOS	57–64	58–62*	16QAM QPSK	6 3.5	15.5 17.8	43.3 74.3	--	9.6**	17.4
[13]	40nm CMOS	50–67	50–67	16QAM QPSK	6.7 3.3	15 9.3	6.7 14.1	20.3	10.8	--

*Estimated from information available in the paper, **Peak EIRP is 22 dBm

transmitters. The lower modulation rate of the broadband version is likely due to the off-chip balun which was needed to combine the differential outputs of the 1–32-GHz RF-DAC. The proposed transmitters are the first to cover multioctave, 30-GHz bandwidth and operate with the highest data rate of 5G transmitters reported to date.

V. CONCLUSION

A new broadband I/Q RF-DAC transmitter has been proposed and demonstrated which is capable of covering all the 5G wireless bands from 1 to 30 GHz with a single silicon chip, radically simplifying portable terminal and basestation architectures. The key enablers of this architecture are: 1) the process-and-temperature insensitive digital quadrature signal generator covering the 1–32-GHz band; 2) the broadband, power-efficient class-D LO-distribution network based on CMOS inverters with shunt-shunt feedback and selective differential-mode inductive peaking; and 3) a novel series-stacked Gilbert-cell output stage with gate segmentation.

The transmitter is capable of generating QPSK, 16-QAM, 32-QAM, and 64-QAM single-carrier and OFDM signals from 1 to 32 GHz directly from digital bit streams and the LO signal. All circuit blocks operate in switching mode. The only analog signal is the 2–64-GHz LO, which, in this demonstration is external, but will normally be implemented on the same chip with a bank of VCOs and divider chains.

Tuned and ultra-broadband transmitter prototypes operating in the 20–32-GHz, and 1–32-GHz range, respectively, with record data rates were designed and manufactured in a commercial 45-nm SOI CMOS technology. The tuned 2×6-bit I/Q RF-DAC transmitter has an output power of 19.9 dBm, a peak PAE of 10.3%, and achieved a maximum data rate of 30 Gbit/s with 24.6-pJ/b energy efficiency. The second prototype covers the entire 1–32-GHz range with over 13-dBm output power and data rates up to 20 Gbit/s. Because all digital baseband lanes can operate with at least 16-GHz sampling clock, oversampling by a factor of 8 can be used to meet the spectral shaping requirements of future 5G systems, while still achieving transmitter data rates in excess of 10 Gbit/s.

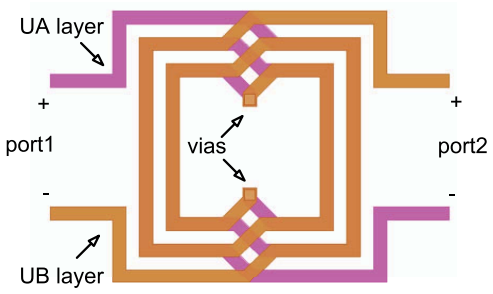


Fig. 25. Layout of a differential series inductor.

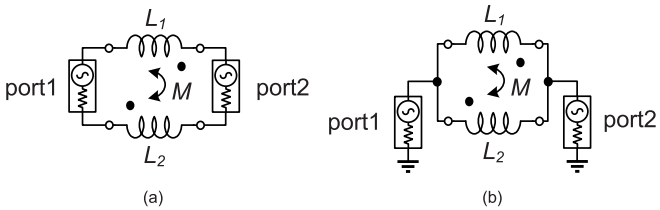
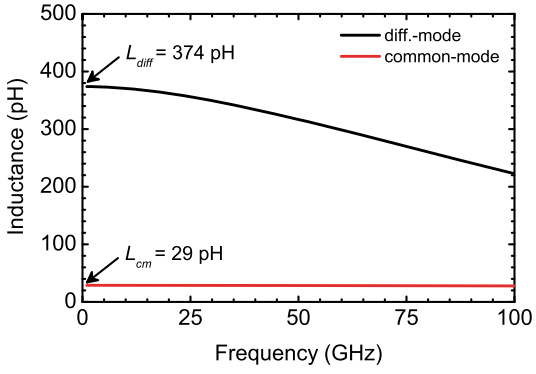
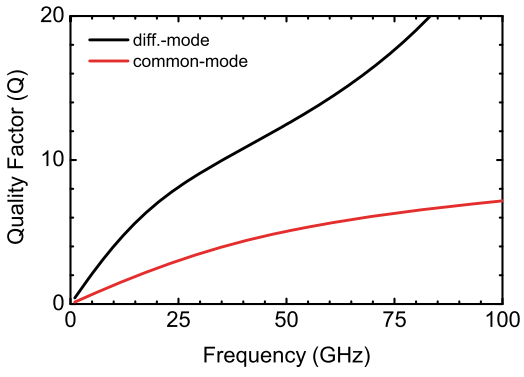


Fig. 26. Two-port test benches for (a) differential-mode and (b) common-mode parameter extraction.



(a)

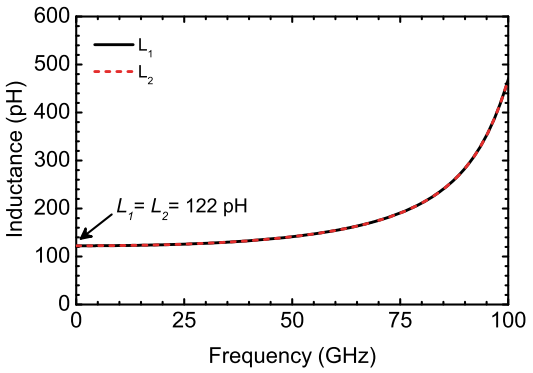


(b)

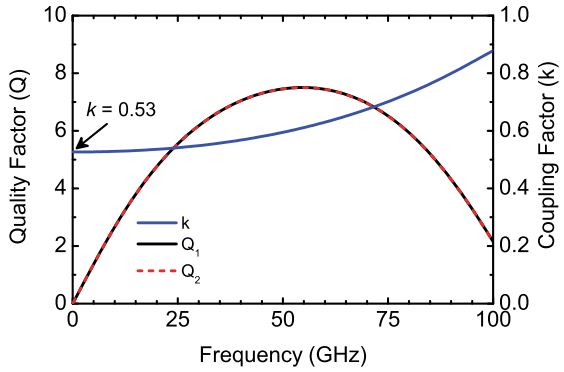
Fig. 27. Extracted series (a) inductances and (b) quality factors in differential- and common-mode.

APPENDIX

The purpose of this Appendix is to help the reader characterize differential series inductors. A layout example of a differential series inductor is shown in Fig. 25. The first step is to EM-simulate it as a four-port structure. Next, the



(a)



(b)

Fig. 28. Simulated (a) inductances, (b) quality factors, and magnetic coupling factor for the two coils characterized as a transformer.

differential- and common-mode inductances and corresponding quality factors are extracted by placing the EM-simulated network parameters of the differential inductor in the two test benches shown in Fig. 26(a) and (b), where the inductances and Qs can be obtained from the two-port Y-parameters using

$$L = \frac{\Im\left(-Y_{12}^{-1}\right)}{\omega} \tag{9}$$

$$Q = \frac{\Im\left(-Y_{12}\right)}{\Re\left(Y_{12}\right)}. \tag{10}$$

Fig. 27(a) and (b) reproduces the resulting differential- and common-mode series inductances and quality factors as a function of frequency. To verify the validity of (1) and (2), the structure is extracted as a regular transformer as in Fig. 28(a) and (b), where the transformer coil inductances and the magnetic coupling between coils are labeled. It can be noticed that at low frequencies the differential- and common-mode series inductances obtained from (9) are exactly the same as those given by (1) and (2). However, at higher frequencies, the distributed capacitance between coils C_C begins to reduce the differential inductance. It should be noted that C_C mainly impacts the differential-mode behavior since in common-mode there is no potential difference between the two coils.

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