A Circuit Designer's Perspective on Transistor Modelling Challenges for 6G, Fiberoptics, and Quantum Computing ICs

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***Abstract*—This paper reviews how HBT and FET compact models should be effectively used in the initial design of mm-wave 6G and fiberoptics circuits above 100 GHz and suggests which high frequency core model parameters and RCL parasitics require refinements. The latter are in part limited by on-die transistor *S*-parameter measurement and de-embedding inaccuracies at *J*-Band. Finally, we discuss the compact model research challenges that remain in capturing optimal noise figure current density and quantum phenomena at cryogenic temperatures, and the numerical convergence issues observed in existing commercial SiGe BiCMOS and CMOS process design kits below 20 K.**

Keywords—compact model, cryogenic low noise amplifier, D-Band, HBT, J-Band, MOSFET, modulator driver, power amplifier, quantum capacitance, tunneling capacitance, tunnel current.

I. Introduction

Transistor compact models [1] play a critical role in the initial design of millimetre-wave (mm-wave) circuits for 6G, fibreoptics and cryogenic quantum computing (QC) applications. If based on precise on-die measurements [2],[3], calibrations [4], and extraction methodologies beyond 300 GHz [2], they provide an efficient and accurate representation of transistor behaviour across the entire millimetre-wave (mm-wave) frequency spectrum, various operating conditions, process, and temperature variation [5,6]. They are being used efficiently to (i) identify potential issues in a proposed circuit topology, optimize its performance, and fine-tune component values, bias conditions, and layout; (ii) model increasingly significant high frequency (HF) non quasi-static (*NQS*) effects (distributed resistance, capacitance and inductance) and transistor stability problems at mm-wave frequencies [2]; (iii) for quick design exploration of various circuit topology alternatives before committing to a specific design topology [7], and (iv) in system-level analysis to evaluate the performance of an entire system, including the interactions between different circuit blocks and the effects of packaging and interconnects. Timely examples of the latter are in investigating the feasibility of integrated 250-GBaud transmitter and receiver analog front ends for 2-Tb/s fiberoptic systems, and *D*-band and *J*-band radio transceivers in scaled SiGe BiCMOS and InP HBT technologies.

Although there are no new compact modelling challenges for HBTs and FETs that are specific to 6G or >128-GBaud fibreoptic circuits, some HF model refinements/extensions are needed at *D*-band and beyond, where transistor, cascode, and emitter follower (EF) stability problems are exacerbated and must be accurately captured. The latter affect circuit topology choices, transistor sizing and biasing, often unnecessarily at the expense of scarce transistor HF performance margin.

In contrast, new compact modelling challenges arise for the design of cryogenic microwave and mm-wave circuits for readout and control of superconducting and semiconductor spin qubits, and for low-noise amplification of cryogenic photon counters in photonic quantum processors (QPs). New model development is also required to reproduce the behaviour of MOSFETs when used as qubits, single-hole (SHTs) and single-electron transistors (SETs), and even in classical computing circuits operated below 100 K. Simulator convergence, noise modelling, capturing the tunnelling effects in the *I-V* and *C-V* characteristics of both HBTs and FETs, and the linearity of circuits at low temperatures are important research problems that need addressing, despite the less appealing market pull of these cryogenic applications at the moment.

This paper reviews the transistor compact model refinements needed for the accurate design of high-yield fibreoptic and 6G integrated circuit (IC) products operating in the 100-300 GHz range, and the compact model research challenges which must be addressed to capture cryogenic and quantum behaviour in HBTs and MOSFETs across the entire frequency spectrum for emerging low-temperature applications. Several examples of how compact models are used in exploratory circuit design are discussed.

II. Compact Modelling Research Challenges

A. Model refinements

The bandwidth of fibreoptic system front-end circuits now exceeds 100 GHz [8],[9]. At the same time, radio and radar transceivers and phased arrays have already been demonstrated in silicon above 100 GHz [10]-[13], paving the road for future 6G systems and, using InP HBT [14] and HEMT [15] technologies, possibly up to 300 GHz. At these frequencies, accurately and efficiently (in terms of simulation speed) modelling a) the distributed small signal equivalent circuit and b) correlation of noise sources of HBTs and FETs becomes increasingly complex.

Due to reduced transistor breakdown voltages, these small signal parameters are also affected by non-linearities [16] and nonlinear self-heating behaviour [17] which must be accounted for in transient noise simulations. The latter are needed to correctly predict the sensitivity and linearity of the low-noise, linear broadband transimpedance amplifiers in 250-GBaud fibreoptic systems, as well as in *W*-band automotive radar receivers which operate with large, reflected signals.

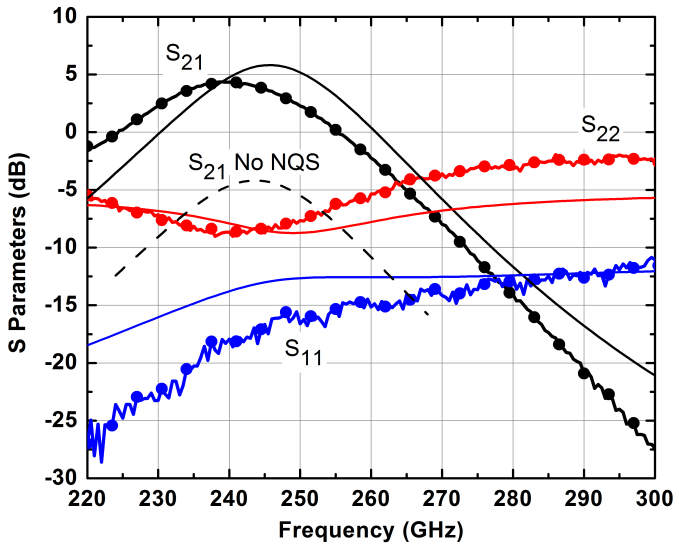


Fig. 1. Impact of including *NQS* model parameters from HBT measurements at *J*-band in HiCUM L2 on the simulated S_{21} of a 3-stage cascode amplifier [2] measurements (lines and symbols) simulations w/o *NQS* with solid/dashed lines. Copied from [2].

Fig. 1 illustrates a compelling example of the impact of activating the HiCUM L2 *NQS* parameters, extracted from *J*-band transistor *S*-parameter measurements, in explaining the measured gain in the 200-300 GHz range of a 3-stage cascode amplifier designed without transistor models in the development phase of a SiGe BiCMOS technology [2].

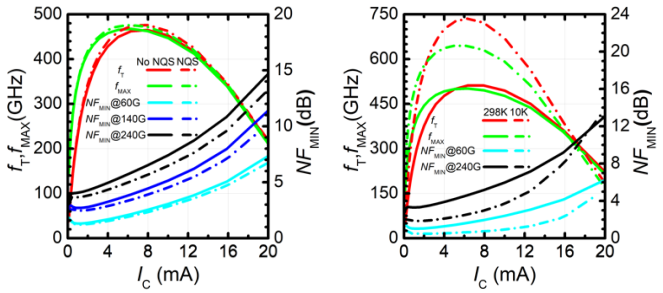


Fig. 2. a) Simulated impact of *NQS* effects (dash-dot lines) on the f_T, f_{MAX}, and NF_{MIN} at 60, 140, and 240 GHz vs. I_C characteristics at 338 K in a SiGe BiCMOS process. b) Temperature dependence of f_T. f_{MAX}, NF_{MIN} at 60 and 240 GHz.

The noise transit time, τ_n, is related to the transconductance delay and describes the correlation between the base and collector shot noise currents in HBTs. Its impact on all noise parameters and on the optimal noise figure current density, J_{opt}, needs to be accurately measured at frequencies above 100 GHz [18] and included in compact models. As can be observed in Fig. 2.a, it decreases the minimum noise figure, NF_{MIN}, and increases J_{opt}, especially at mm-wave frequencies above 100 GHz. However, as shown later, the temperature dependence of J_{opt}, which should decrease at cryogenic temperatures, is not captured correctly by the model in Fig. 2.b. Another question mark is that the simulated NF_{MIN} vs. I_C characteristics at 240 GHz does not exhibit a minimum like those at 60 GHz and 140 GHz, which have been validated experimentally. Until minimum noise figure measurements vs. current density are conducted at 240 GHz, it is impossible to confirm that the simulated $NF_{MIN@240GHz}$ vs. I_C characteristics are reliable. In SiGe HBT mm-wave amplifiers [7], [19], the measured J_{opt} has been shown to be close to the peak-f_{MAX} current density, J_{pfMAX}, in disagreement with design kit models which predict much lower values. Inaccuracy in J_{opt} is much more impactful for circuit design than the error in NF_{MIN}, because it leads to wrong transistor dimensions and bias current.

As discussed in [2] and [18], the key challenge for obtaining accurate *NQS* parameters and noise transit time is the precision of on-die *S*-parameter and noise measurements conducted at frequencies beyond $f_T/3$. Although TCAD can be used to determine the complexity and values of the distributed equivalent circuit components of the transistor, ultimately the *NQS* parameters and τ_n must be extracted from transistor measurements, or at least validated indirectly by measurements of circuits whose performance is sensitive to them.

B. New model features

While the rationale for 6G transceivers to operate above 100 GHz is questionable, fibreoptic systems continue to generate the "wave that raises all the technology boats". They demand "more Moore" CMOS device scaling [20] to 10-nm gate length and 23-nm metal pitch [21], needed for increasingly more complex error-correction digital signal processors (DSPs), concomitantly with HF figures of merit (FoM) scaling in terms of f_T, f_{MAX}, and NF_{MIN} of both SiGe [20],[22] and InP HBTs [9],[23],[24]. In turn, the smaller device dimensions, along with new applications at cryogenic temperatures in high performance classical computing, space exploration, and QC [25]-[27], also bring to the forefront quantum phenomena such as (i) tunnelling across the base in HBTs [28],[29], (ii) charge quantization and sequential tunnelling through the potential barriers formed below the gate-oxide spacers in MOSFETs [30], and (iii) frequency-dependent quantum and tunnel capacitance [31]. These phenomena are not captured in compact models.

III. How Are Models Used In Exploratory Circuit Design?

Mm-wave circuit design can be at least partly carried out by hand, in an algorithmic fashion [20],[22] and even in the absence of transistor models. However, accurate models are always needed for design verification and optimization. For example, using measured transistor data and room-temperature design-kit simulations, 22-nm FDSOI QPs with qubits and 60-200 GHz control and readout electronics were designed fabricated and tested for operation at 2 K even though the design kit does not simulate below 20 K due to convergence problems [32],[33] and the transistor models are not valid below 225 K. For any mm-wave circuit, the initial design starts from the measured or compact model (if available) simulated f_T, f_{MAX} and NF_{MIN} vs. current density characteristics. Figs. 3-5 compile such measured data over temperature for some of the most advanced production SiGe and InP HBT, FinFET and FDSOI CMOS technologies.

The collector base voltage, V_{CB}, dependence of these characteristics in SiGe HBTs is shown in Fig. 4. It is critical in

the design of linear mm-wave low noise (LNA) and power amplifiers (PA), like those illustrated in Fig. 6, linear optical modulator drivers, shown in Figs. 7 and 8b, and low noise transimpedance (TIA) and track-and-hold (THA) amplifiers, Fig.7. A linear current (density) axis is used in Figs. 4 and 5 to highlight the wide range of bias current values around the peak-f_T current density, J_{pfT}, where these characteristics are flat and relatively insensitive to bias current variation. Unlike in analog circuit design, tuned or broadband mm-wave circuits are biased in this region, facilitating robust circuit design with maximum possible gain and linearity. This choice of bias current density, imposed by gain and noise requirements, also makes the circuits less sensitive to compact model inaccuracy and process variation compared to a typical low-current-density analog circuit bias condition.

Fig. 4 emphasizes that the collector-base voltage, V_{CB}, (drain-source voltage, V_{DS}, in MOSFETs) has a significant impact on f_T, f_{MAX} and the associated optimal bias current densities. To first order, these characteristics are largely invariant with the FET number of gate fingers/fins and the HBT emitter length, and enable the designer to quickly select the transistor size, bias current and V_{CB}/V_{DS} values needed to meet the linearity, noise, bandwidth, output power or voltage swing specification for mm-wave radio, radar, and fibreoptic circuits.

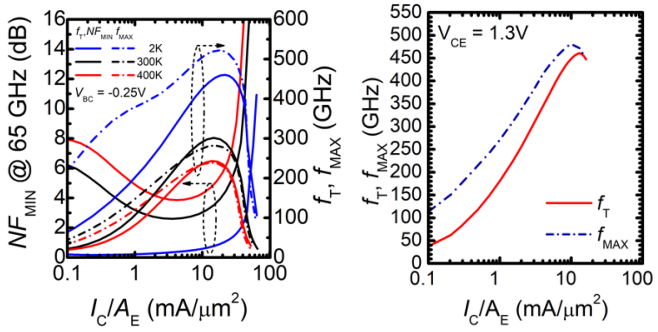


Fig. 3. Measured a) f_T, f_{MAX} and NF_{MIN} at 65 GHz vs. I_C/A_E and temperature at V_{BC} = -0.25 for a SiGe HBT. b) f_T and f_{MAX} vs. I_C/A_E of a 0.25μmx4μm InP HBT at 300 K [9].

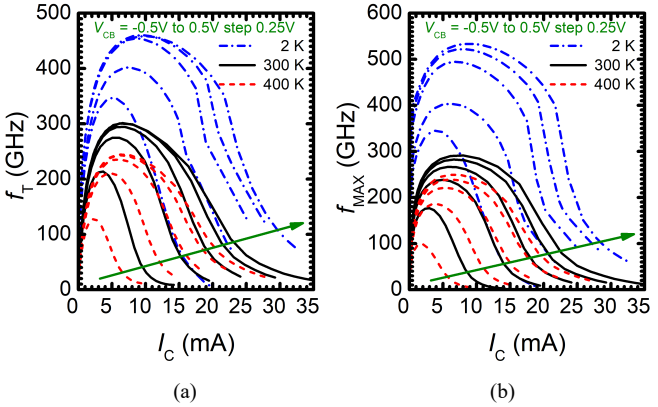


Fig. 4. Measured a) f_T and b) f_{MAX} for a 0.1μmx4.5μm SiGe HBT at 2, 300, and 400 K vs. I_C and V_{CB}.

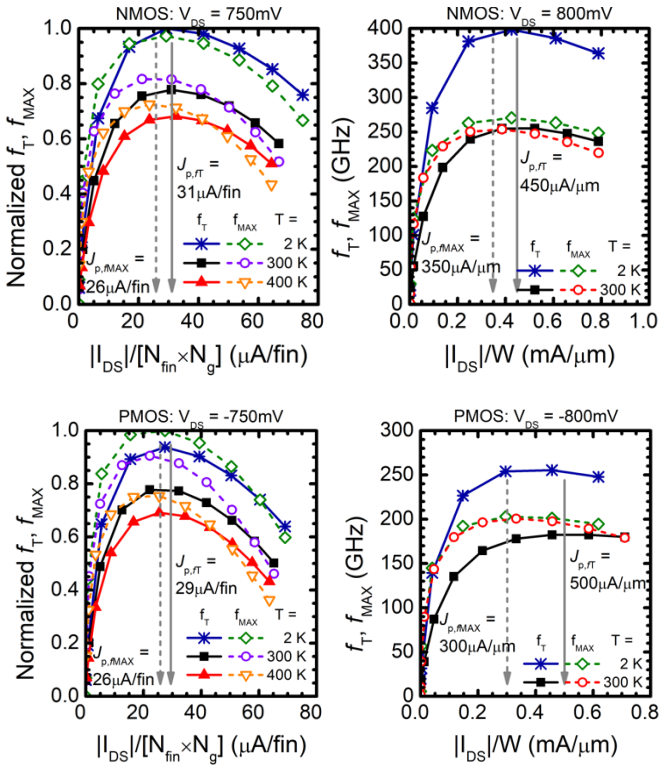
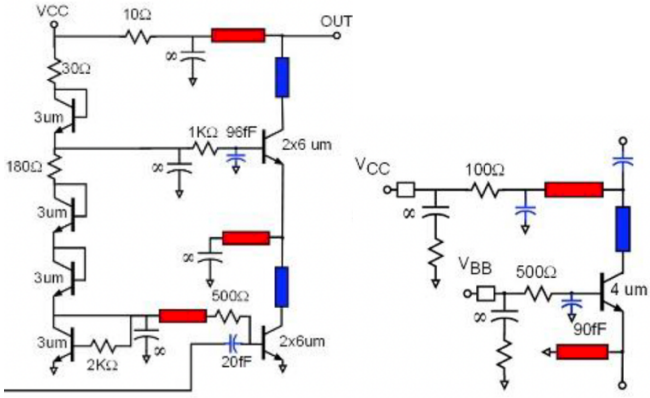


Fig. 5. Measured a) f_{MAX} of n- and p-FinFETs at 2, 300, and 400 K vs. I_{DS}/fin and gate finger and b) f_T and f_{MAX} vs. I_{DS}/W at 2 and 300 K for 22-nm FDSOI n- and p-MOSFETs biased at $|V_{DS}|$ = 0.8V.

Based on the f_T, f_{MAX}, and NF_{MIN} vs. I_C/I_{DS} and V_{CE}/V_{DS} characteristics at the smallest and largest emitter length, l_E, and gate (finger) width, $W_{(f)}$, feasible in the given technology (to assess impact of second order effects), transistor biasing (setting I_C/I_{DS}, V_{CE}/V_{DS}) and sizing (choosing l_E, W) is carried out by hand by (i) biasing the topology at J_{OPT} (in LNA, TIA, VCO) or peak f_T current density (maximum linearity in driver) to accommodate the desired input and output linear voltage/current ranges, and (ii) setting the DC voltage drops on the load and degeneration resistors in Figs. 7 and 8. The PA is an exception. Above 100 GHz, the PA transistor(s) may be biased in class *AB, B*, and maybe in class *D, E, F*, etc. in the lower *D*-band or for InP circuits. Good linearity can be achieved by proper termination of the first 1-2 harmonics, since higher harmonics reside at frequencies beyond the f_{MAX} of silicon transistors. V_{CE}/V_{DS} are typically set to $V_{MAX}/2$, where the V_{MAX} value is dependent on the transistor configuration: common emitter (CE), common-base (CB), or common-collector (CC). In the case of HBTs, it is typically <= BV_{CEO} (CE) or < BV_{CBO} (CB). This leads to V_{CE} values of ~1.2 V in CE SiGe HBTs, ~1.5 V in CE InP HBTs, and <~2 V in the CB configuration for both SiGe and InP HBTs. Transistor sizing is next done to achieve the desired current for noise impedance matching (LNA) or linearity and output power/voltage swing (PA/driver).

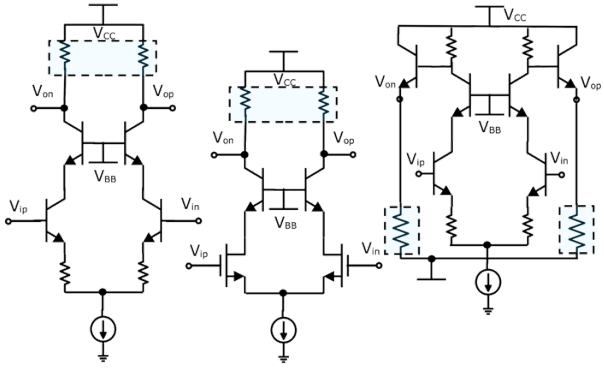
Considerations to maximize linearity, voltage swing and output power set the DC voltage drops on the resistors of the

circuit topologies in Figs. 7 and 8. Although this biasing design step involves no simulation, the need to maximize V_{CE}/V_{DS} points to the importance of modelling self-heating and avalanche breakdown and their impact on circuit linearity, gain, and noise. This precision is needed during the design verification stage which critically relies on simulation with accurate compact models. Stability issues can only be detected and solved using accurate compact models featuring *NQS* effects. Solving them often implies resizing or reducing the bias current density in emitter followers or adding resistors in common-base devices as in Fig. 6.b [24]. None of these circuit stability measures are desired and it is therefore important for the compact model to accurately predict the stability problems.



(a) (b)

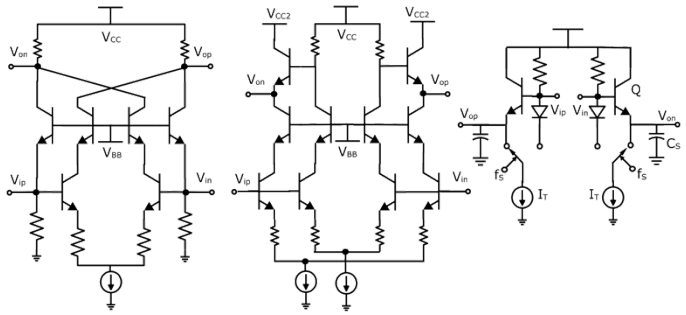
Fig. 6. a) Stacked cascode LO driver or PA output stage. Copied from [21]. b) Low noise CB amplifier stage. Copied from [24]. Filled rectangles represent transmission-line matching elements.



(a) (b) (c)

Fig. 7. Linear open collector: a) HBT cascode with emitter degeneration, b) MOS-HBT cascode [19], c) and open emitter [35] output stages for modulator drivers. The optical modulator is highlighted in light blue.

Several critical design steps cannot be completed without simulation with accurate models. These include: (i) finding the precise values of the peaking inductors in fibreoptic circuits, (ii) synthesizing the signal matching and noise impedance matching networks in tuned mm-wave circuits, and (iii) PA load-pull [23], [34], where the capability of the compact model to accurately predict circuit nonlinearity under large signal conditions is important in designing the output matching network. All these activities can only roughly be conducted by hand at low frequency, but not at *D* and *J* bands.



(a) (b) c)

Fig. 8. a) Linear regulated cascode TIA, b) linear modulator driver (adapted from [36]), and c) THA [8], [9] schematics. These topologies have been verified to be scalable beyond 250-GBaud operation.

As depicted in Fig. 5, in CMOS technologies, J_{pfT} and J_{pfMAX} are constant over temperature from 2 K to 400 K, simplifying circuit design. In contrast, Fig. 3 shows that in HBTs J_{pfT} and J_{pfMAX} remain constant between 300 K and 400 K but increase at 2 K [6],[27] by up to ~30% [6], commensurate with the increase in electron saturation velocity and mobility. The latter was also observed in FDSOI MOSFETs and FinFETs. This makes cryogenic SiGe HBT circuit design for superconducting qubit readout [26] a trial-and-error process, since, in the absence of HBT models verified on noise measurements at cryogenic temperature, J_{opt} is not known.

IV. Circuit Test Cases

An important aspect of transistor compact model development is its verification on representative circuits. In assessing the sensitivity of mm-wave circuits to compact model parameters, the circuit topologies should be chosen carefully, avoiding topologies with resistor-based negative feedback like the classical transimpedance-feedback amplifier [7],[20],[29]. The latter is not to be confused with transimpedance amplifiers (TIAs) in general, which can be implemented without negative feedback, e.g. with a transistor in CB topology. However, even in circuits with negative feedback, the gain-bandwidth product is sensitive to the transistor HF FoMs and the bandwidth is sensitive to RLC parasitics and *NQS* effects. For example, the bandwidth and noise figure of the topologies shown in Figs. 7-8, some of which use resistive degeneration, a form of series-series negative feedback, were verified to still scale with transistor f_T, f_{MAX} and NF_{MIN}, respectively, [20],[22] for two generations of SiGe HBT and two generation of InP HBT technologies.

The following circuit examples will be analyzed in detail in the presentation for sensitivity to HICUM L2 compact model parameters in two generations of SiGe BiCMOS technologies:

a) D-band PA [22]

b) 128GBaud linear optical modulator driver [36]

c) D-band common-base LNA and TIA

d) Current-Mode-Logic (CML) and emitter-coupled logic (ECL) library cells

e) cryogenic LNA for qubit state readout.

It should be noted that test cases (*b*) through (*d*) are also suitable for InP HBT model verification and circuit performance scaling across two technology nodes.

A. 6G Power Amplifier

As already mentioned, PA load-pull and output waveform optimization can only be carried out using accurate large signal transistor models. The negative output resistance observed in *S*-parameter measurements of SiGe HBTs and cascodes at *J*-Band is a big challenge in designing stable PAs, DACs, and optical modulator drivers based on HBTs, where large transistors and currents are needed. The typical approach to stabilize these stages is to place resistors [2],[21] and/or a small capacitor [11],[21] in series with the base at the expense of power gain. At these frequencies, and for this type of large power circuits, designers often rely on measured transistor- and cascode-stage *S*-parameters for design. For example, to design the 160-GHz PA of the radar transceiver in [10], the measured 110-170 GHz *S*-parameters of 3-stacked cascode stages with a measured MAG > 8 dB at 170 GHz were used. The MOSFET compact model, based on common-source (CS) transistor test structure layouts measured up to 110 GHz, and not representative of the layout in the common-gate (CG) configuration, predicted it would be impossible to get > 5 dB gain at 160 GHz. In PAs, the model must accurately capture non-quasi static effects, linearity to the 5th harmonic (few foundries measure transistors above 300 GHz and if they do, can those measurements be trusted for accuracy?), RLC parasitics, and the impact of self-heating and avalanche breakdown on these HF effects.

B. Optical modulator driver

In an optical modulator driver, where lumped topologies are preferred to save power, inductors are only used for bandwidth extension. All resistor vales, transistor sizes, bias currents and voltages, are determined by hand based on low-frequency, essentially DC, design considerations. The HF parasitics and *NQS* effects play only a minor role in the design itself, except in analyzing and accepting final design values without enforcing changes in the component values. The only situation where the model is critical and *NQS* parameters and HF RLC parasitics are absolutely needed, is in adjusting the emitter length and the bias current density in EFs to avoid too much peaking and oscillation, and in ensuring the stability of the cascode stage. Therefore, an accurate model of the parasitics in the CC and CB configurations (rarely measured or verified during compact model parameter extraction) is necessary. As can be observed in Figs. 7-8, all driver topologies consist of cascode and EF stages.

C. Common-base LNA and TIA

Using transistors in CB or CG configuration for LNAs and TIAs becomes very attractive above 100 GHz because it allows for simple input broadband matching to 50 Ω or provides a very low impedance to the photodiode in an optical receiver. At these frequencies, NF_{MIN} is almost the same in the CB and CE configurations. For example, the common-base *D*-band InP HBT LNA stage in Fig. 6.b [21] can be transformed in a DC- to-130-GHz bandwidth TIA by replacing the collector transmission line with a collector resistor, R_C, in series with a peaking inductor. To first order, the voltage gain, transimpedance gain and input resistance are given by g_mR_C, R_C, and $1/g_m$, respectively, and the maximum input linear current range is given by the collector current, I_C, which also affects g_m and the input impedance. As in the tuned *D*-band LNA, by biasing at J_{opt}, the equivalent input noise current of the TIA, i_{neq}, is minimized. The bandwidth of this circuit is easy to scale across technology nodes and is sensitive to transistor *NQS* and noise transit time model parameters, making it ideal for compact model verification. Another important benefit is that its input resistance can be reduced by increasing the HBT size and bias current to accommodate large capacitance photodiodes, or photodiodes whose capacitance does not scale as the symbol rate increases. There is little trade-off between linearity, input impedance, and bandwidth in this topology since increasing linearity requires larger bias current and transistor size (to keep the same current density for low noise). Better linearity thus leads to lower input resistance which further increases bandwidth. However, if the transimpedance gain needs to be preserved, the supply voltage and power consumption will also have to be increased. The regulated cascode TIA topology in Fig. 8.a also takes advantage of these properties, with slightly higher equivalent input noise current and bandwidth at the same transimpedance gain.

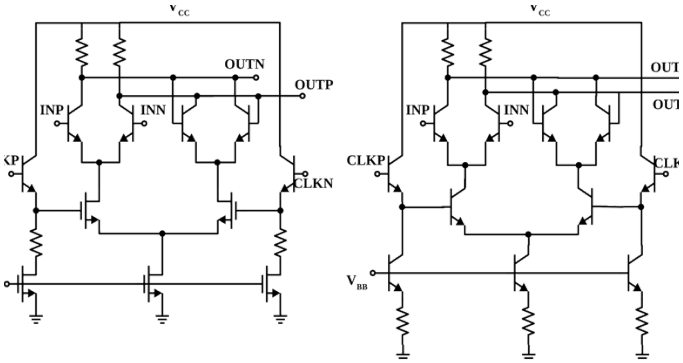
D. CML and ECL library cells

Despite the continued scaling of FinFETs [21], their HF and switching performance and even g_m scaling have saturated, as predicted in [20], due to surface scattering when the Si or SiGe fin width approaches 5 nm. This problem also applies to the next 2-nm CMOS technology node expected to use stacked nanosheet structures, a symbiosis between FDSOI MOSFETs and FinFETs. Barring the introduction of new types of high electron and high hole mobility and velocity materials to provide a spectacular speed improvement in CMOS logic, current-mode logic (CML) and emitter-coupled logic (ECL) circuits using SiGe or InP HBTs will have to be employed at least in the front-end circuits of 200-GBaud fibreoptic systems in the final 2:1 multiplexer (MUX). The MUX needs full-rate retiming with a 200-GHz clock to recondition the waveforms at the 200-GBaud selector output. It is therefore important to investigate the sensitivity of the ECL and CML cells to *NQS* model parameters and RLC parasitics. These logic cells, like the D-type flip-flop, are also important for the divider chain of the local oscillator (LO) generation blocks of 6G systems operating in the *D* and *J* bands and turn out to be more demanding in terms of transistor f_T and f_{MAX} than the analog front-end circuits such as TIAs, optical modulator drivers, or tuned LNAs and PAs.

Fig. 9 shows the schematics of a MOS-HBT CML latch, suitable for low voltage (<2.5 V) implementation in SiGe BiCMOS technology, and of a faster HBT-only latch which can be used in both SiGe BiCMOS and InP circuits. The HBT-only latch requires higher supply voltage and consumes more power but can operate with > 200 GHz clock signals. One of the HBT modelling challenges for these EF and cascode topologies is to accurately predict the negative resistance which appears at the base of the EF, causing signal distortion in the form of overshoot and undershoot in the digital waveforms, even in the absence of peaking inductors. Accurately accounting for the impact of 100-GHz and 200-GHz clock feedthrough on CML and ECL gate waveforms cannot be done by hand analysis and can only be simulated with a compact model whose *NQS* parameters were accurately extracted in this frequency range. The stability of cascode and EF stages in the CML and ECL gates can be

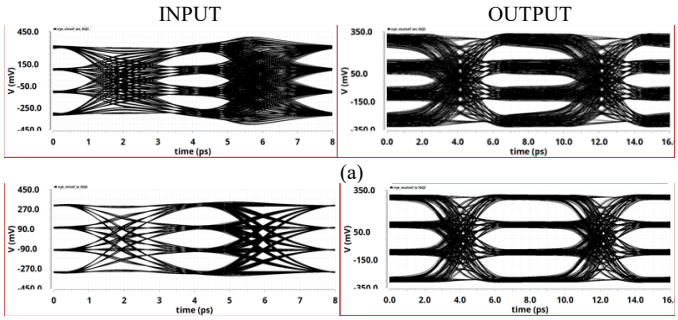
improved only by reducing the bias current density significantly below J_{pfT}, compromising bandwidth and switching speed, and/or by adding resistive degeneration at the expense of gain and larger voltage swing [9]. These measures alleviate signal overshoot and clock feedthrough.

Fig. 10 illustrates the impact of *NQS* effects on the transient noise simulated 250-GBaud and 125-GBaud PAM-4 eye diagrams at the input and the output, respectively, of one of the THAs (Fig. 7.c) in an analog demultiplexer using a half-rate clock of 125 GHz. As can be clearly seen, by correctly accounting for the *NQS* effects, the simulated bandwidth increases and the jitter of the output signal is reduced, resulting in larger SNR.



(a) (b)

Fig. 9. a) SiGe BiCMOS MOS-HBT CML and b) HBT-only SiGe or InP latch.



(a)

(b)

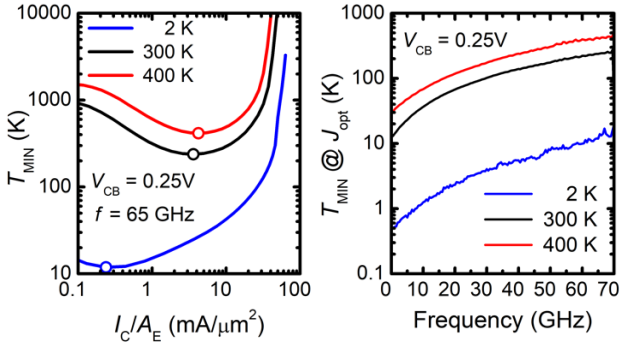
Fig. 10. Simulated input 250- and output 125-GBaud PAM-4 eye diagrams with self-heating and transient noise up to 300 GHz at the input and output of the THA in a SiGe HBT 1:2 Analog Demultiplexer: a) w/o *NQS* and b) with *NQS* effects.

E. Cryogenic Low Noise Amplifier

Currently, 20-mK superconducting Josephson-junction parametric amplifiers followed by cryogenic (4-K) *p*-HEMT or SiGe HBT LNAs are used for readout of superconducting qubits [26], while CMOS LNAs preceded by *p*-HEMT LNAs, both operated at 4 K, have been used for reflectometry readout of semiconductor spin qubits [37]. Low noise cryogenic amplifiers at a few K are also needed to amplify the signal from cryogenic photon counters in photonic QPs. Since noise current density, noise figure, and noise correlation vary with frequency and temperature, accurately modelling J_{opt} in CE/CS, CB/CG and cascode stages over frequency and temperature down to 1 K has become critical. This has been a challenge for FETs even at room temperature since dedicated noise measurements are needed to extract the drain noise temperature [38],[39]. Noise parameters are more difficult to measure above 100 GHz and are more sensitive to equipment dynamic range than the f_{MAX} of MOSFETs, a well-documented metrology challenge itself. For bipolar transistors, the noise parameters can be obtained from *S*-parameter measurements, without the need for direct noise measurements [6],[40]. This method was validated at 300 K with independent noise measurements [40] up to 170 GHz, including τ_n extraction [18], and yielding model/simulation-grade quality smooth curves. However, to our knowledge, at the time of writing there are no direct on-die cryogenic noise parameter measurement studies to confirm the validity of the minimum noise temperature, T_{MIN}, shown in Fig. 11, J_{opt}, depicted in Fig. 12.b, noise resistance (R_n) and optimal noise impedance (Z_{sopt}), Fig.13, behaviour obtained from cryogenic *S*-parameter measurements [6].

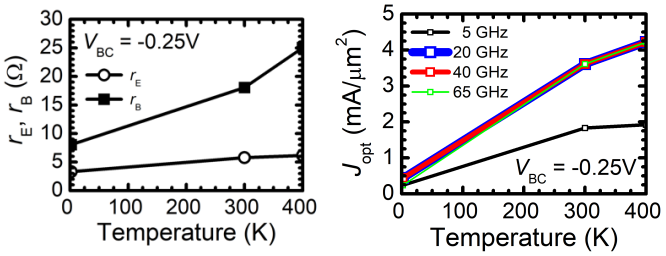
In principle, if τ_n, the small signal equivalent circuit parameters (Fig. 12), and the collector and base tunnel current components are included in the compact model and are accurately modelled as a function of temperature [28], and since no specific noise measurements are needed for bipolar transistor noise modelling, HBT compact models should be valid down to 2 K. However, experimental work with model verification is needed to validate the above statement.

Due to the temperature-dependent interplay between thermal noise (which decreases with temperature) and shot noise (largely independent of temperature), in SiGe HBTs J_{opt} becomes a strong function of temperature, decreasing by an order of magnitude between 300 K and 2 K, as shown in Figs. 11.a. and 12.b. This behaviour mandates radically different sizing and bias current densities for SiGe HBTs in an LNA designed for operation at cryogenic temperatures compared to one intended for room-temperature applications [6]. An LNA or TIA [38] designed for 300 K will work better at 2-4 K, as shown in Fig. 14, but its noise performance will be far from the best possible and its power consumption will be (significantly) larger than it needs to be. This is crucial because the power consumption in a QP is entirely due to the readout and control electronics and not due to qubits. It is the power consumption of the control and readout electronics that ultimately prevents the scaling of QPs to millions of qubits, irrespective of qubit technology and this fact is beginning to be recognized.



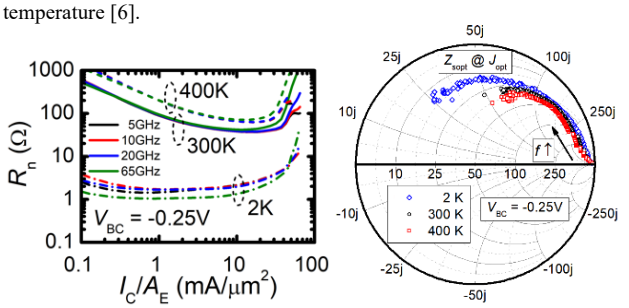
(a) (b)

Fig. 11. a) Measured T_{MIN} vs. I_C/A_E at 65 GHz and b) T_{MIN} at J_{opt} vs. frequency over temperature from 2 K to 400 K for a SiGe HBT [6].



(a) (b)

Fig. 12. Measured SiGe HBT a) external emitter and base resistance, b) J_{opt} vs. temperature [6].



(a) (b)

Fig. 13. Measured SiGe HBT a) R_n at 5, 10, 20 and 65 GHz and b) Z_{sopt} at J_{opt} vs. frequency up to 70 GHz vs. I_C/A_E at V_{BC} = -0.25 V [6].

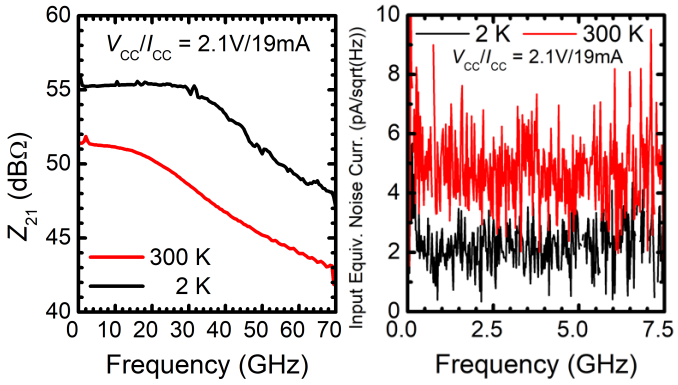


Fig. 14. Measured a) Z_{21} and b) the input equivalent noise current at 2 K and 300 K for a similar TIA as that in [38] but manufactured in an experimental SiGe BiCMOS technology. At the same bias, it shows significantly higher bandwidth with more gain and less noise at 2 K compared to 300 K.

The 20 times reduction in T_{MIN} at all frequencies, shown in Fig. 11, and the 10x reduction in J_{opt} at 2 K are not only due to the linear decrease of thermal noise with temperature, but also helped by the fact that both the base resistance (r_B) and the emitter resistance (r_E) decrease by factors of ~5 and ~2, respectively, over that temperature range, as illustrated in Fig. 12.a. They, too, were extracted from *S*-parameter measurements.

The exact variation and interplay between thermal noise and the drain noise current dominated by high energy carriers observed in p-HEMTs [39] has yet to be measured at cryogenic temperatures in MOSFETs. Even for p-HEMTs, it is only recently that a scalable small signal noise model, valid down to 10 K and up to 150 GHz, has been developed. It is based on noise measurements at different frequencies and different temperatures of LNAs with input attenuators, in which the channel noise temperature T_d was extracted described by an empirical polynomial function of physical temperature [40]. As in HEMTs, the MOSFET J_{opt} is expected to decrease significantly at 2 K compared to its value in the 300-400 K range, where it remains constant. Modelling J_{opt} and the noise parameters for FETs is more challenging than for HBTs since on-die noise measurements at cryogenic temperatures are necessary. Just like at 300 K, the noise parameters of MOSFETs cannot be extracted from *S*-parameter measurements alone. As pointed out by Pospieszalski first for p-HEMTs [39], the drain noise current, though thermal in nature, is determined by the elevated temperature of the carriers at the drain end of the channel and is not strongly dependent on temperature and can only be obtained from noise measurements [40]. This means that also the cryogenic CMOS TIAs [5] and LNAs [37] can be further improved in terms of noise and power consumption once the noise behaviour of 22-nm FDSOI and 3-nm FinFETs, both relevant for *D*-band and cryogenic applications, is characterized at low temperature and captured in compact models.

V. Conclusions

We have reported on the transistor compact model refinements, primarily *NQS* parameters, required to develop large volume 6G and fibreoptics circuits which operate in the *D*- and *J*-bands. The impact of the model accuracy on the design methodology of a large spectrum of relevant tuned and broadband circuits in SiGe and InP HBT technologies has been discussed in detail. More accurate instrumentation and on-die characterization, calibration, and de-embedding methods in the 110-GHz-to-330-GHz range are also needed to validate these compact model refinements.

For emerging quantum computing, high performance computing and space applications which operate in the 1-77 K range, compact model research must be conducted to capture quantum phenomena and noise contributors as a function of temperature, along with the development of on-die cryogenic characterization techniques for the HF and noise parameters of HBTs and FETs down to 2 K. But before that happens, the numerical code and compact models in circuit simulators will have to be adapted by normalizing it to kT to avoid the numerical overflow due to the large exponentials that appear in the diode and transfer characteristics of HBTs and FETs and which prevents most commercial design kits from converging at temperatures below 10 K.

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