Circuits Topologies and Design Methodologies for High Data Rate Radio in SOI and FDSOI CMOS

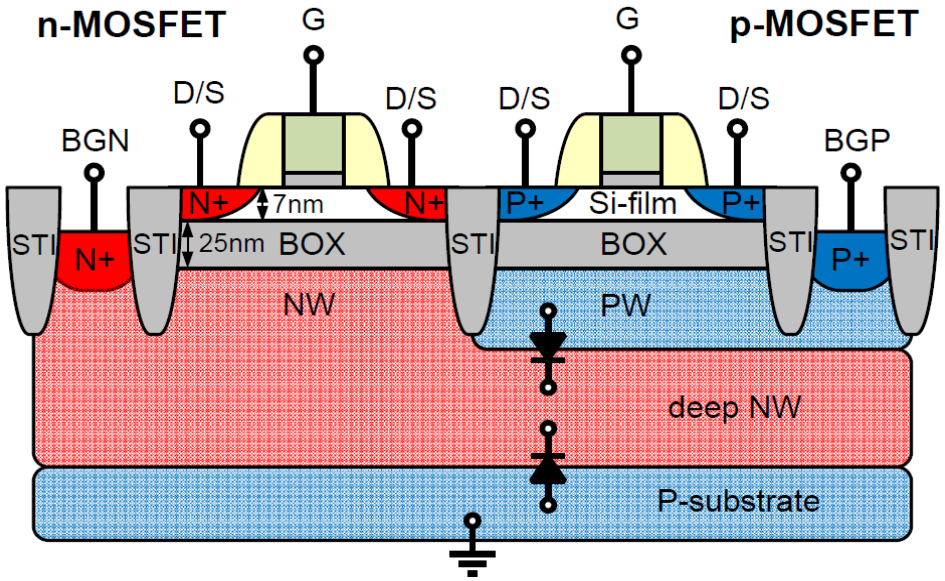
Sorin P. Voinigescu

University of Linz, December 12, 2018

Outline

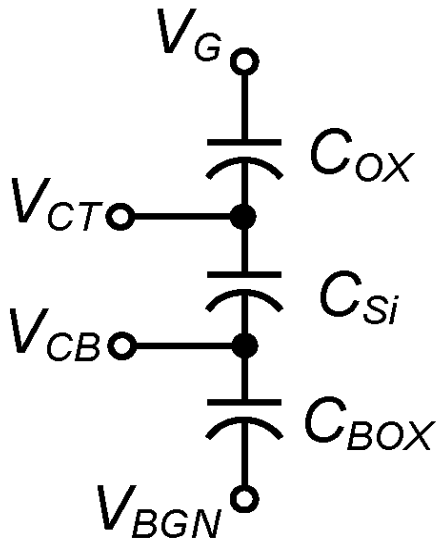
- **Unique Transistor Features and Performance**
- Design Fundamentals
- Specific mm-wave and high-speed circuit topologies
- Design Examples
- Conclusions

28nm, 22nm, 12nm FDSOI cross-section



$$V_{tp} \approx V_{tp0} + t_{OX}/t_{BOX} V_{BGP}$$

$$V_{tn} \approx V_{tn0} - t_{OX}/t_{BOX} V_{BGN}$$

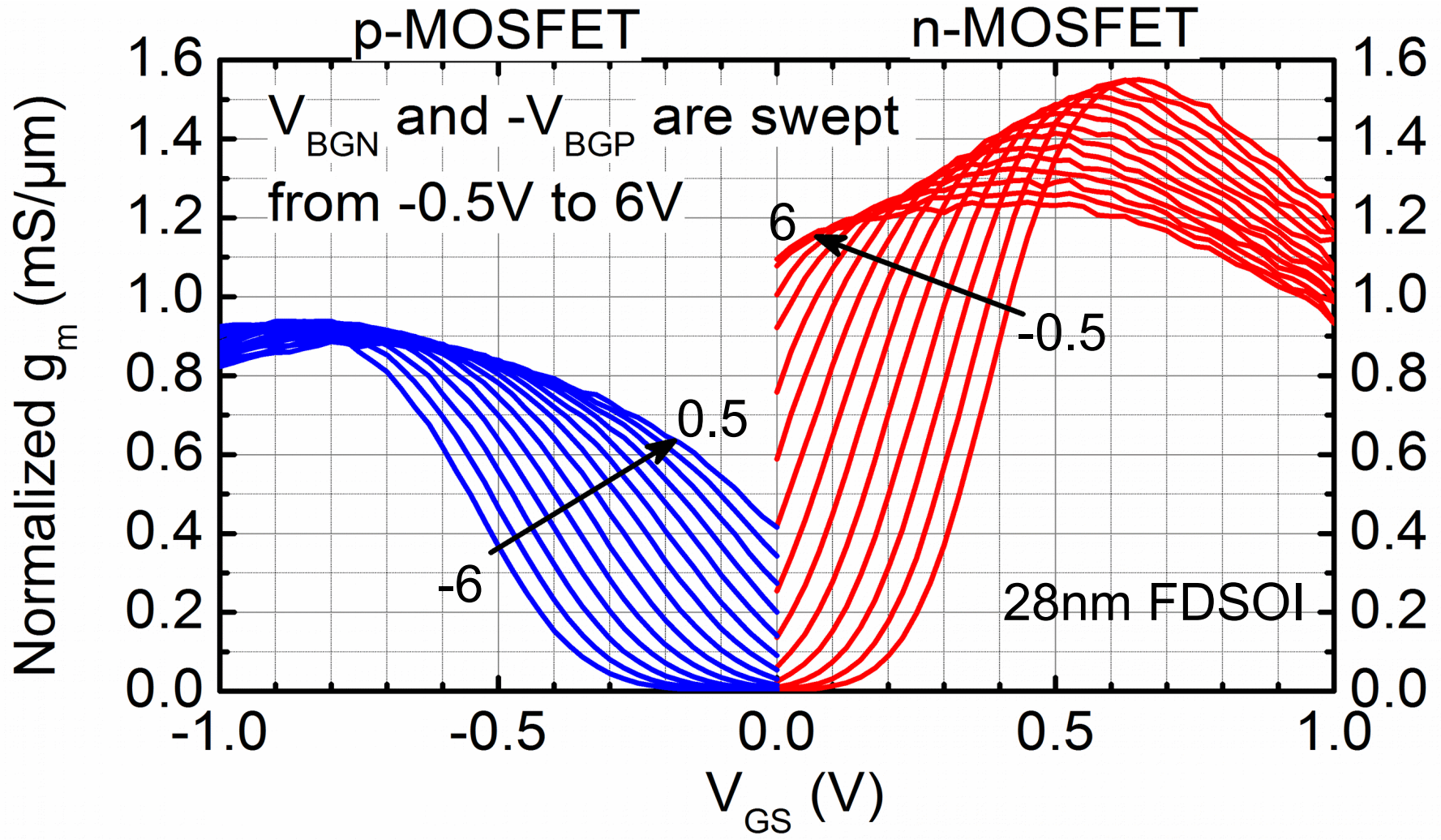


Unlike bulk planar and FinFET CMOS, the body is floating

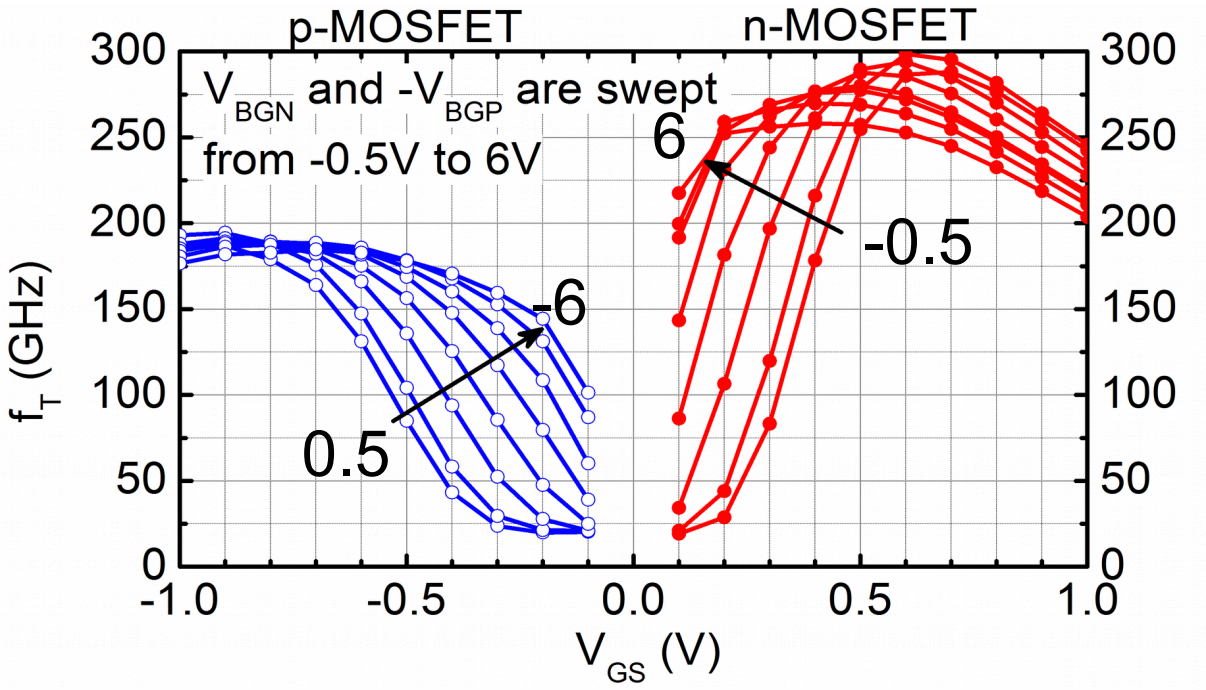
Can control V_t, I_{ON}, g_m, f_T and f_{MAX} characteristics

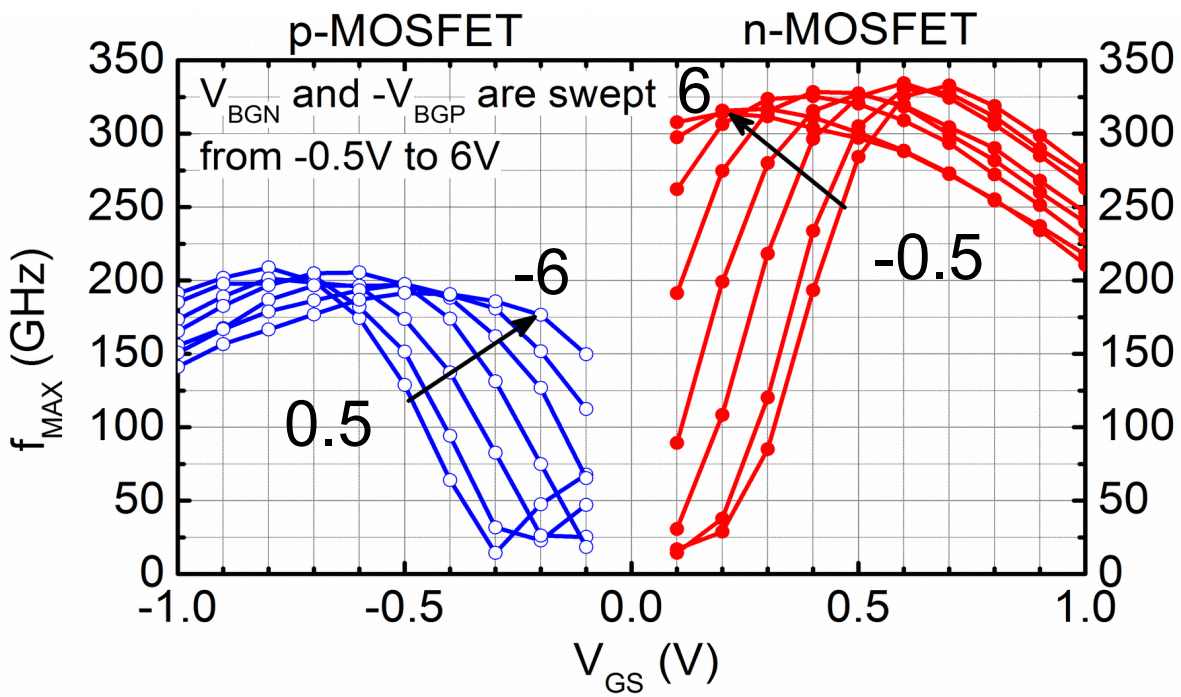
Si/Ge sheet channel scalable to 5nm physical gate length

Transconductance vs. V_{GS}, V_{BG}



f_T and f_{MAX} vs. V_{GS}, V_{BG}



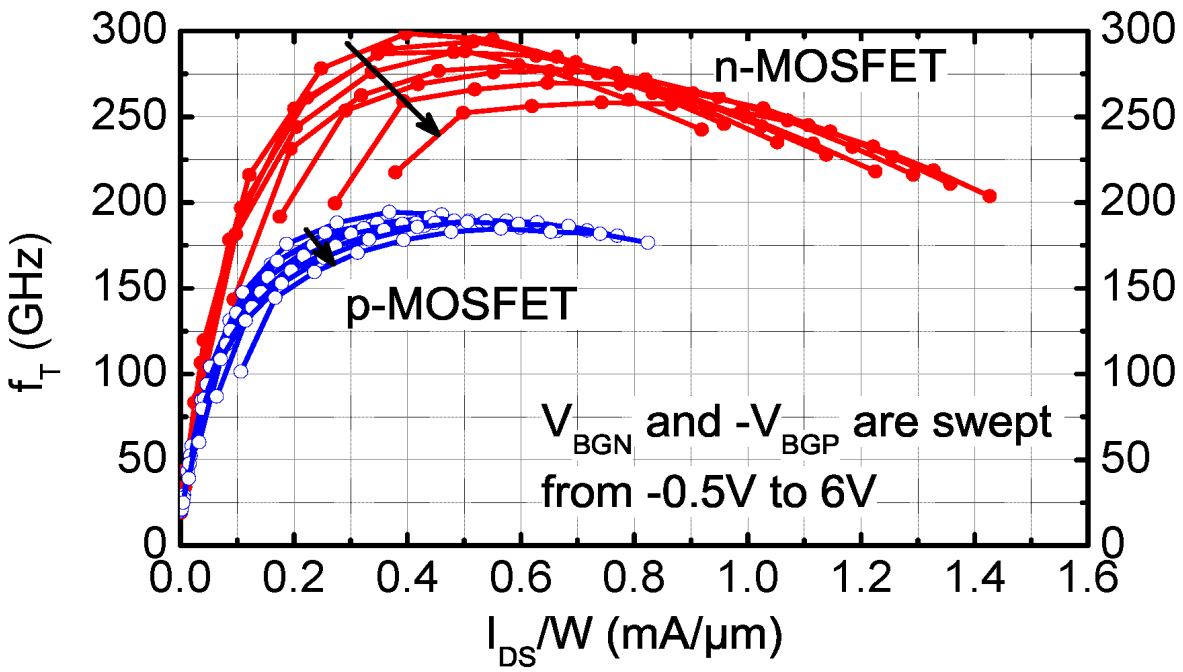


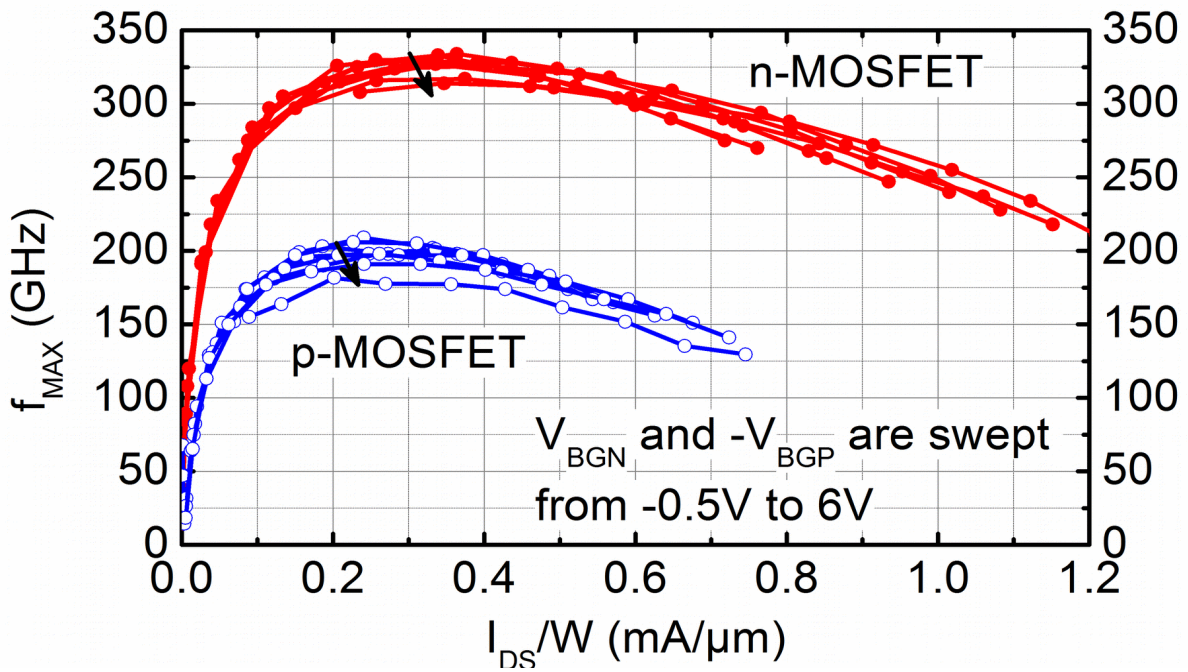
28nm FDSOI

Peak values occur at V_{BGN} =-0.5 V and V_{BGP}=0.5 V

When charge accummulates at top interface

Plot f_T and f_{MAX} vs. I_{DS}, V_{BG}

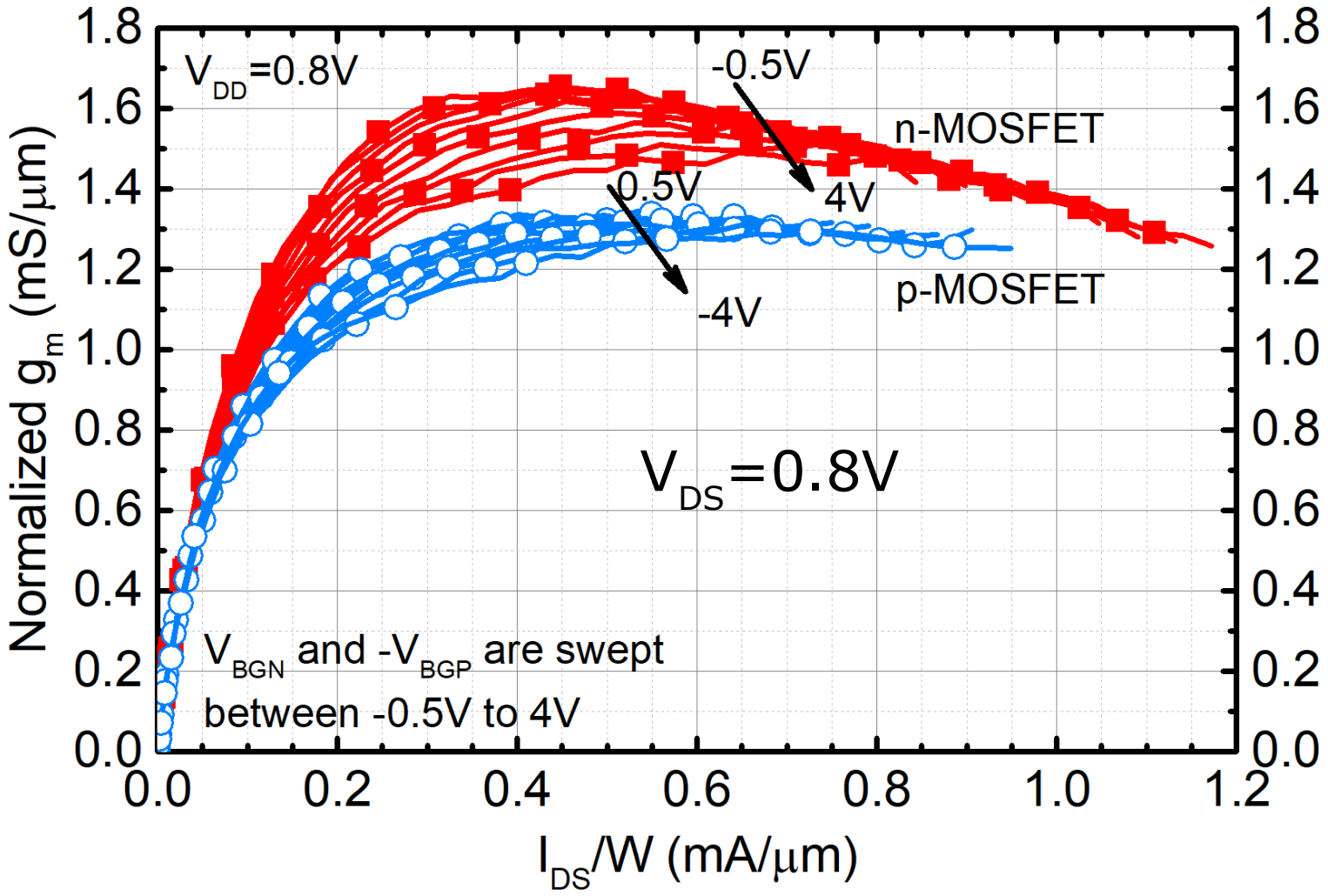




28nm FDSOI

[S. Shopov and S.P. Voinigescu, IEEE JSSC 2016]

g'_m vs. I_{DS}, V_{BG}



22nm FDSOI
40x20nmx590nm

$J_{peak\text{-}gm}$ tuneable from back gate

$J_{peak\text{-}gm} > J_{peak\text{-}fT}$

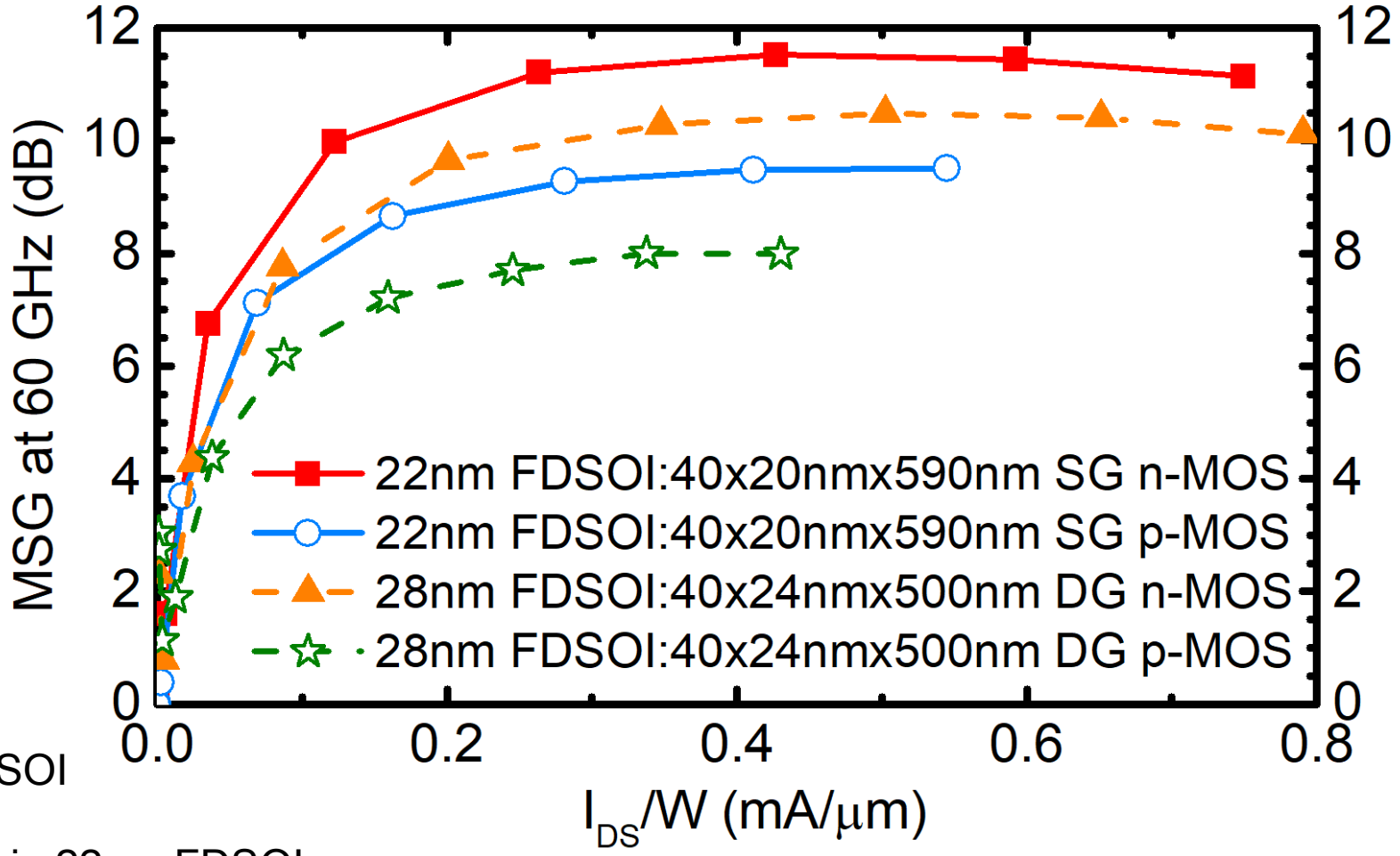
Same as $J_{peak\text{-}MAG}$

MAG in 28/22nm FDSOI with back-gate bias

g_m, f_T, *MAG* improve

but f_{MAX} saturated

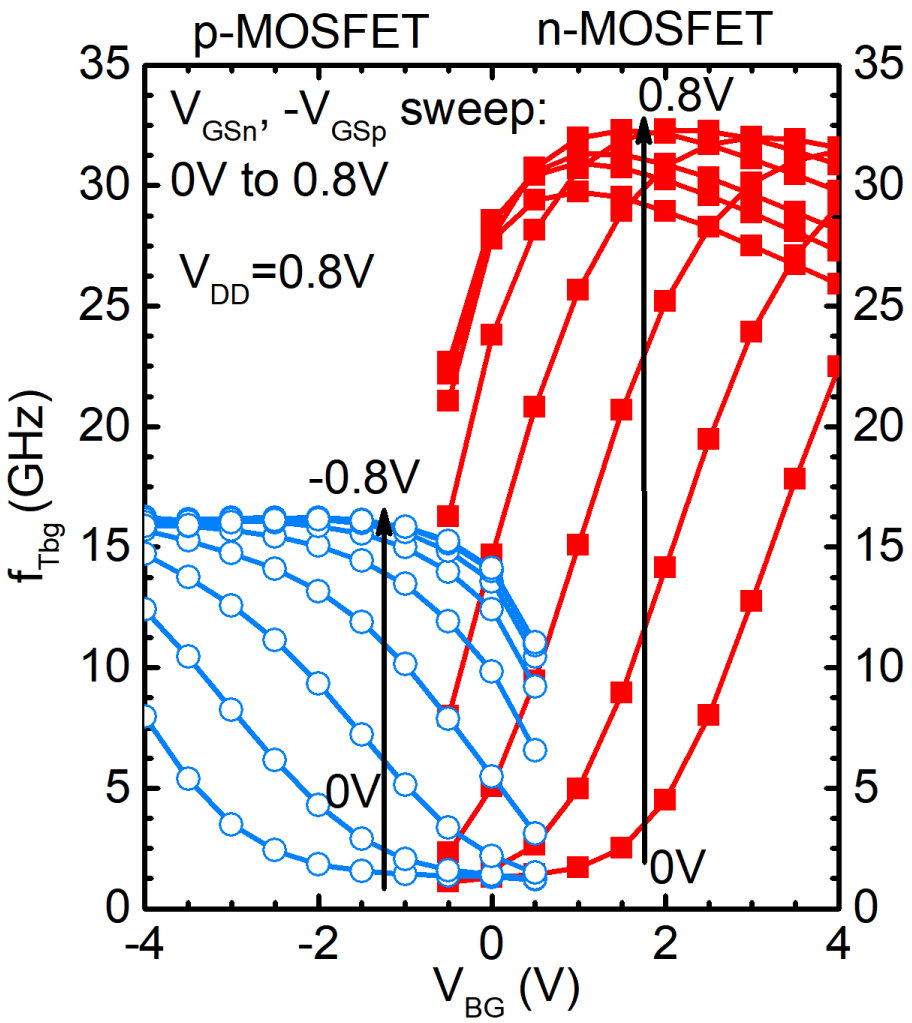
MAG small at 60 GHz

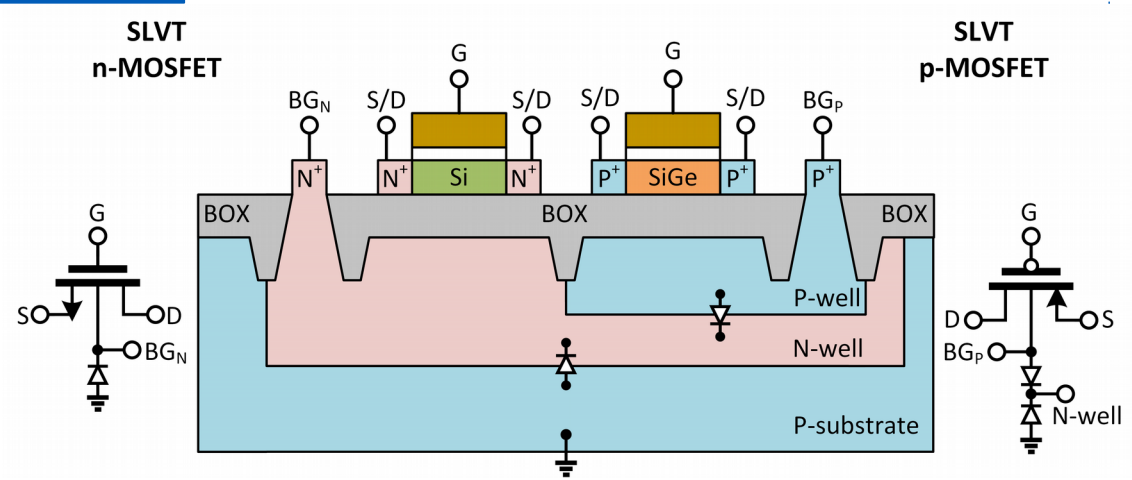


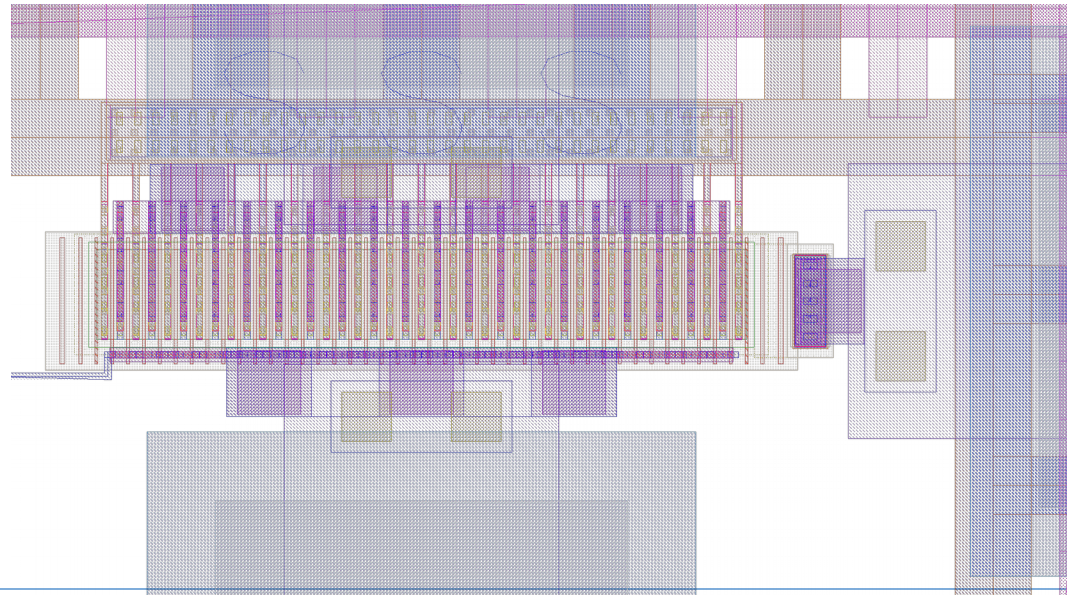
MAG increases from 28nm to 22nm FDSOI

V_{DS}= 1 V in 45nm PDSOI => V_{DS}= 0.8 V in 22nm FDSOI

f_{Tbg} for backgate input: 22nm FDSOI



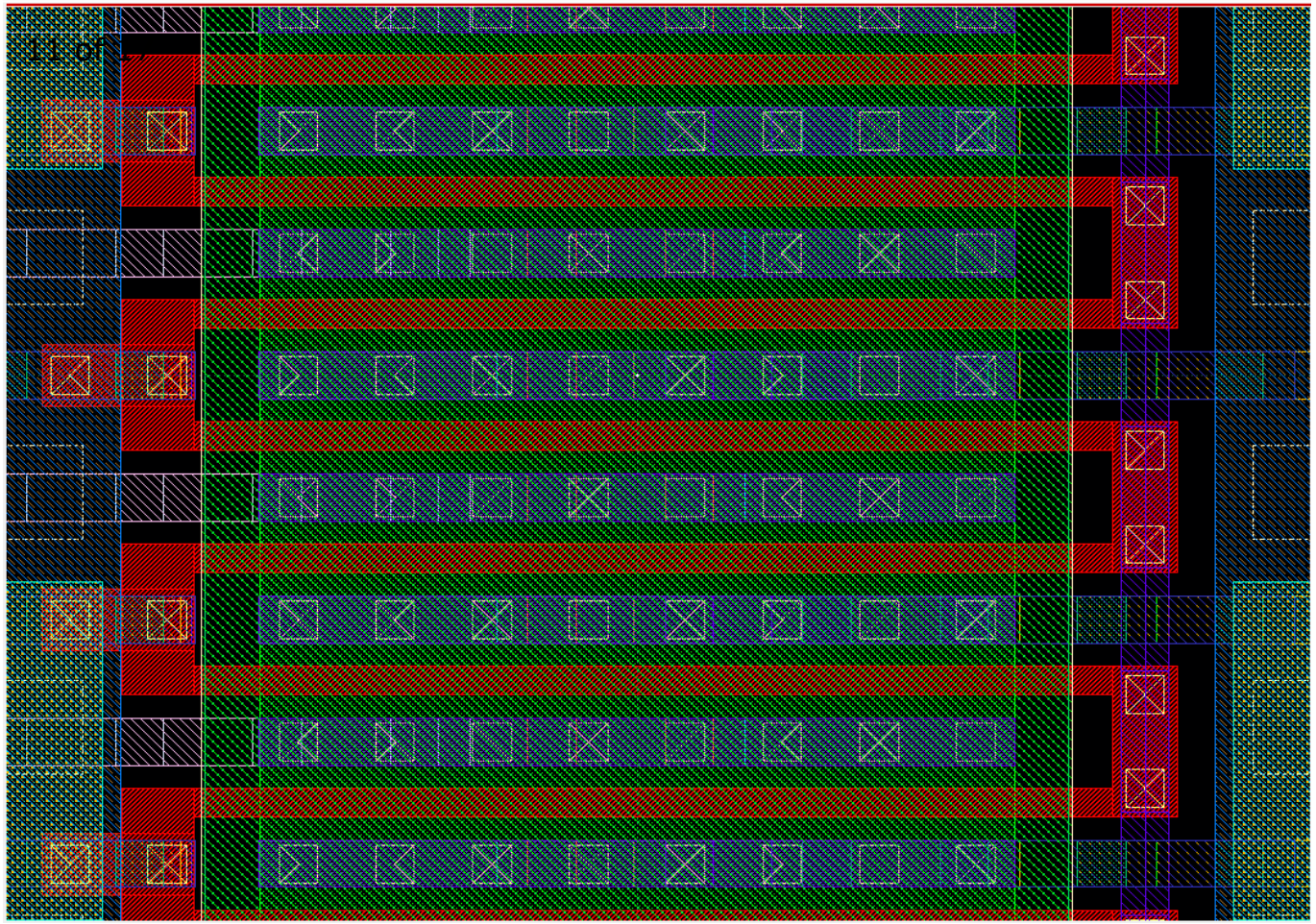




Outline

- Unique Transistor Features and Performance
- **Design Fundamentals**
- Specific mm-wave and high-speed circuit topologies
- Design Examples
- Conclusions

Mm-wave circuit design starts with layout!



n-MOSFET 40x28nmx780nm double-sided gate contact

Electromigration RULES!

Hard to bias at > 0.2mA/um

Enlarged gate pitch and S/D contact area

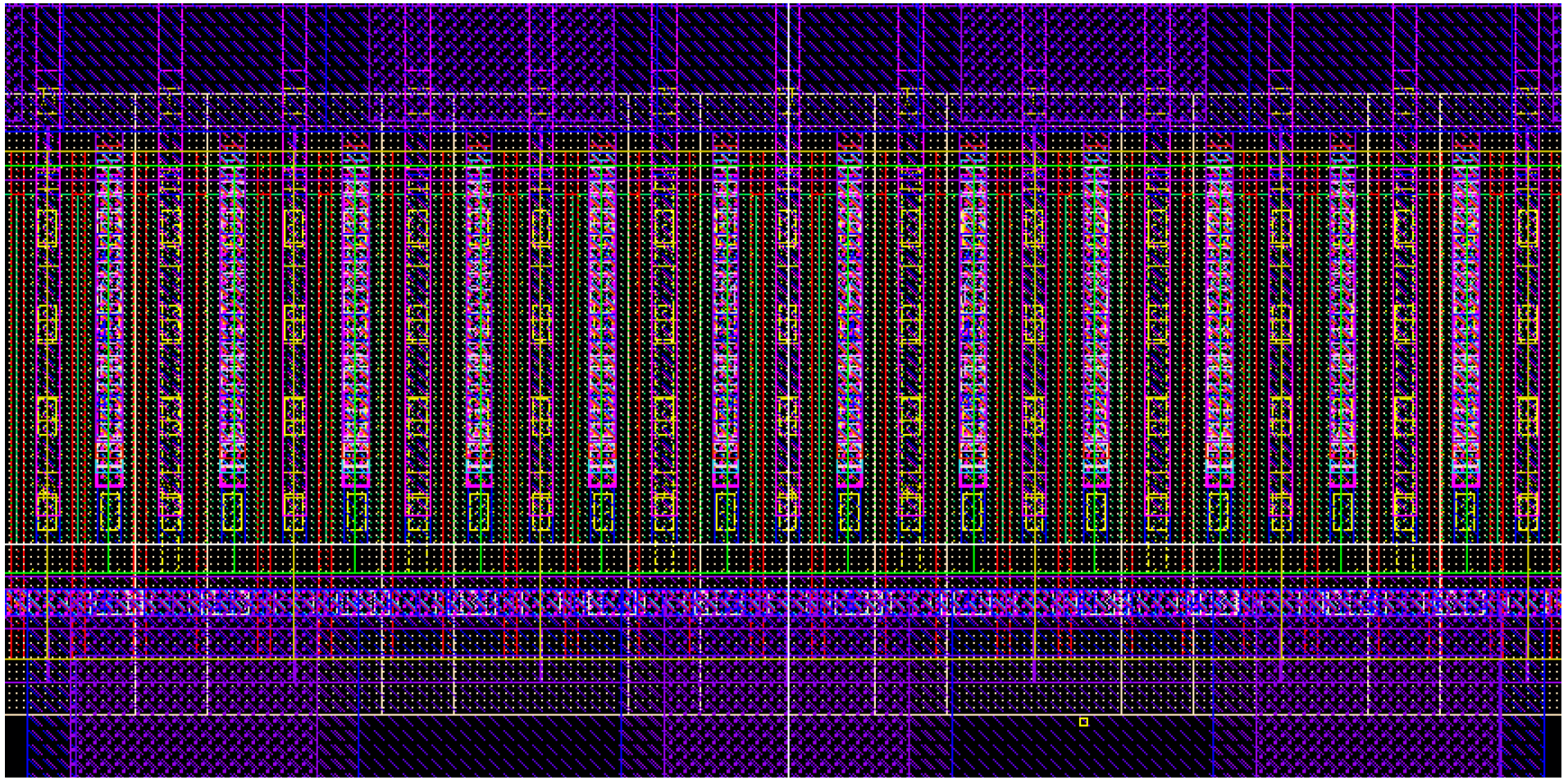
More flexibility than in FinFET

Impact of layout RC parasitics

higher than in older nodes

Optimal W_f = 0.3-0.6 μm

Most compact fine pitch layout in 22nm FDSOI



40x20nmx590nm single-sided gate contact, 1x pitch

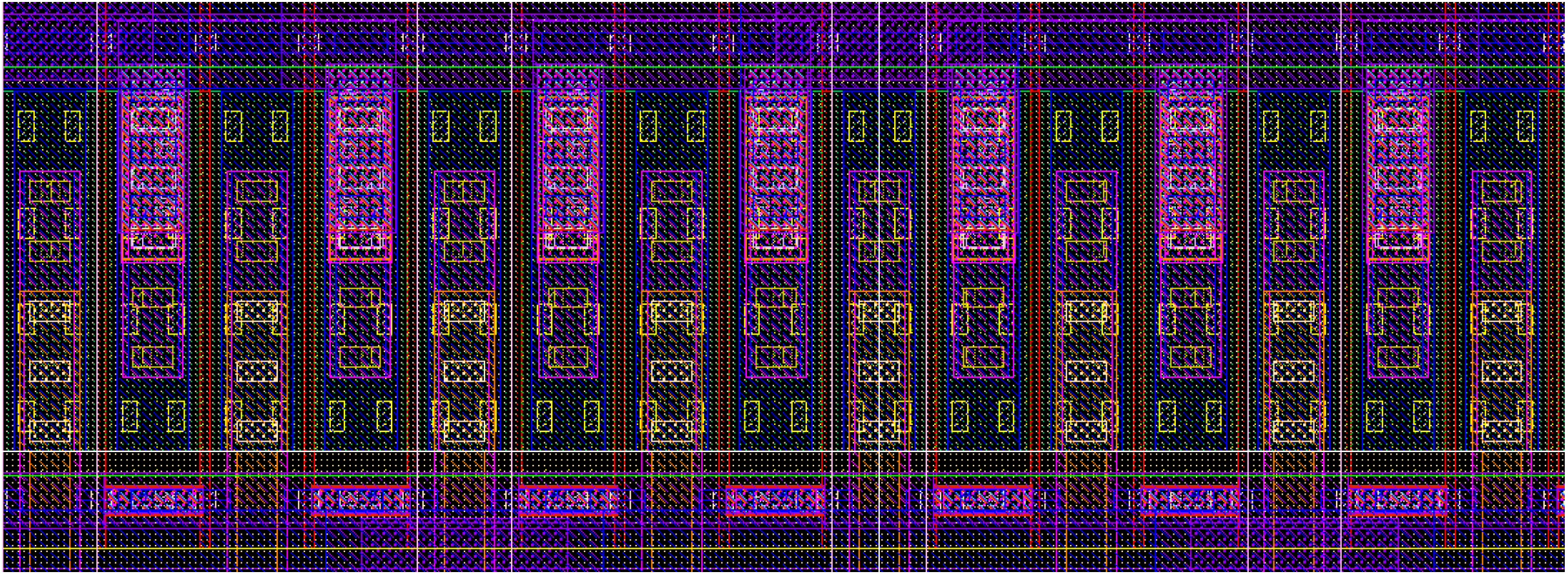
Double-sided gate contact not possible

Source and drain on the same side

High f_T, good f_{MAX}

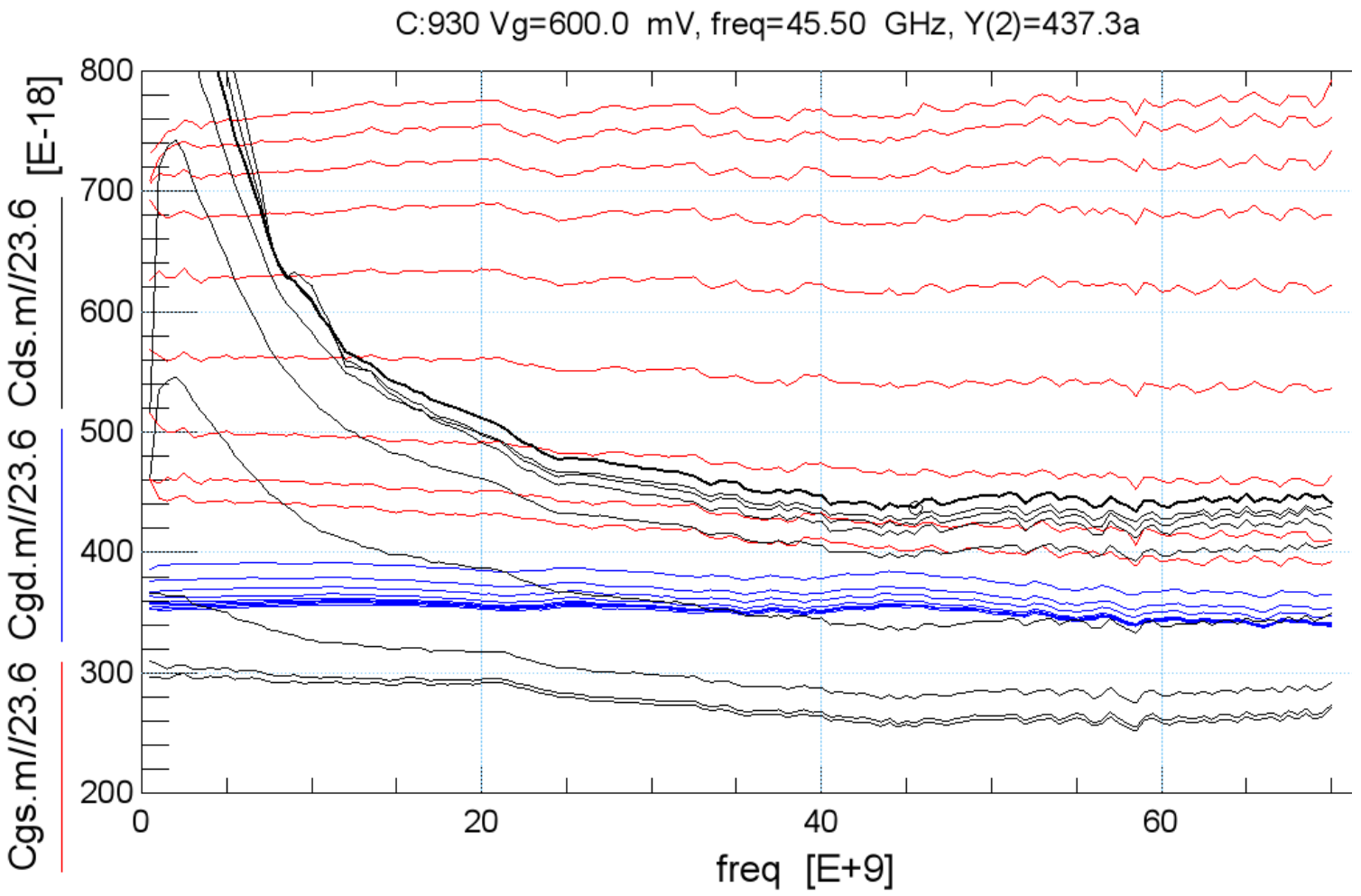
Optimal W_f = 0.4-0.6 μm

Using relaxed pitch in 22nm FDSOI



n-MOSFET 40x20nmx720nm double-sided gate contact 2x pitch

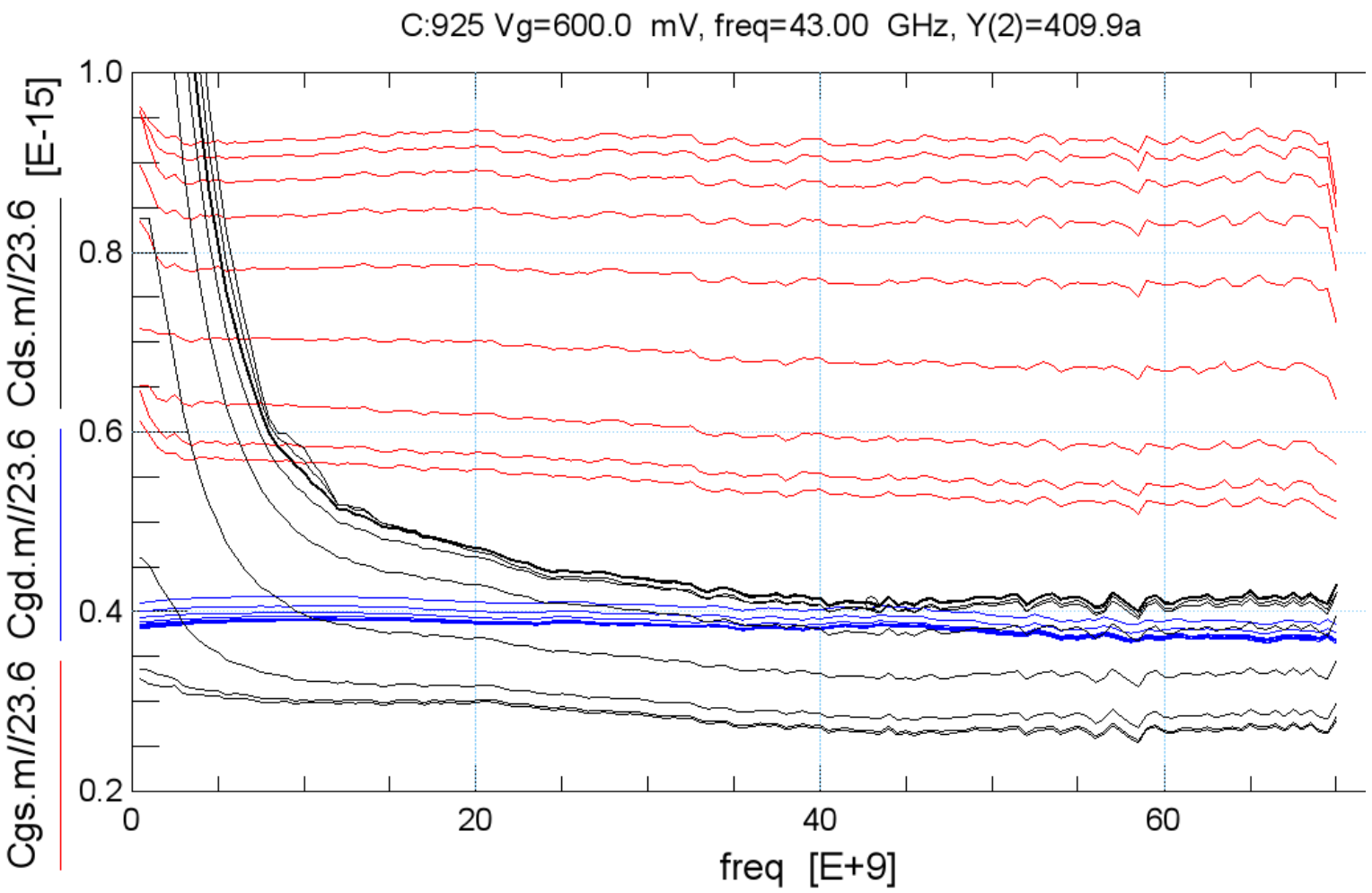
Extract C'_{gs}, C'_{gd}, C'_{db} : 1x pitch single-side gate



22nm FDSOI

N-MOSFET
40x20nmx590nm

Extract C'_{gs}, C'_{gd}, C'_{db}: 2x pitch, double-side gate

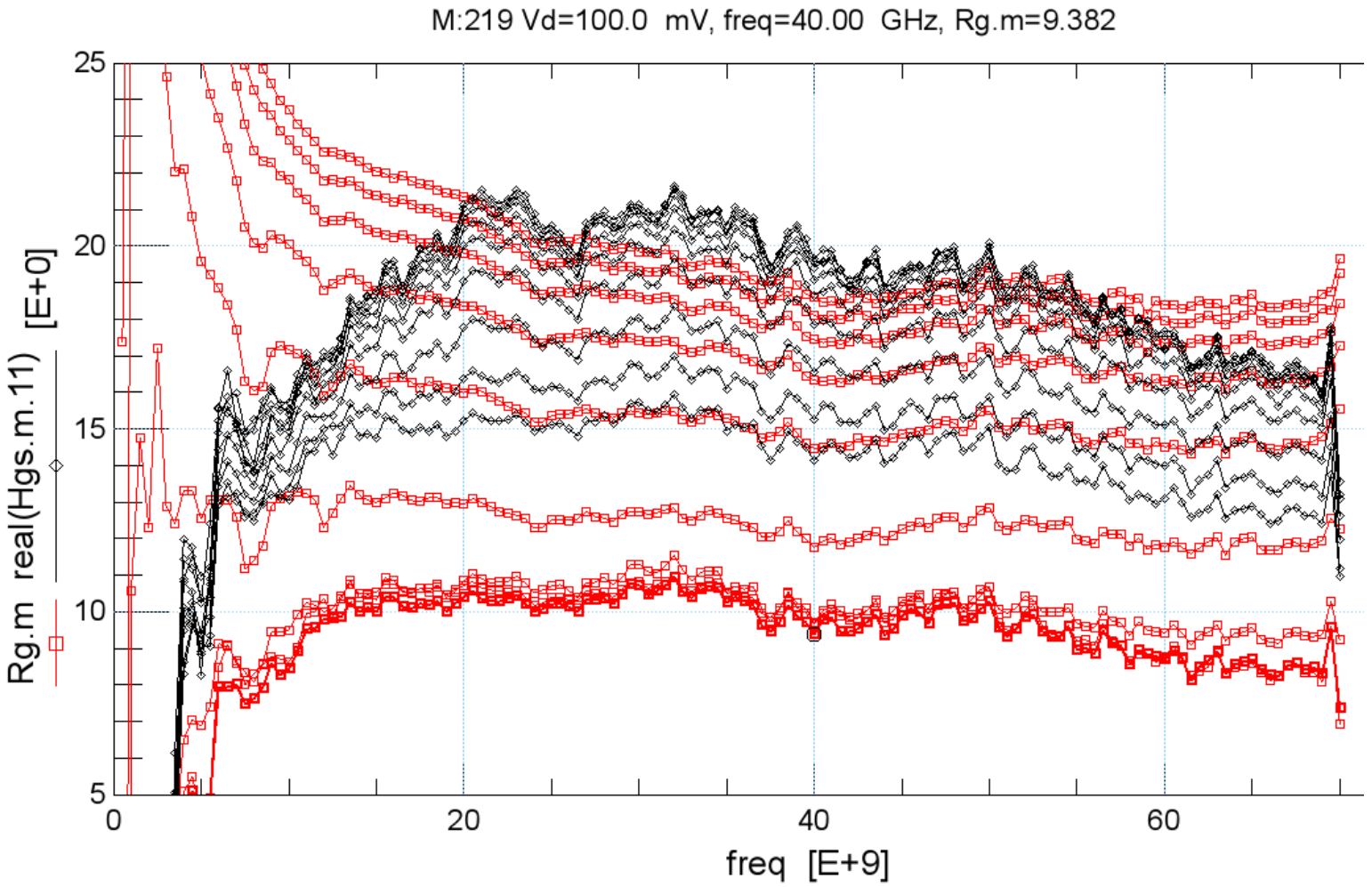


22nm FDSOI

N-MOSFET
40x20nmx590nm

C'_{gs} most affected

Extract R_g: single vs. double side gate contact



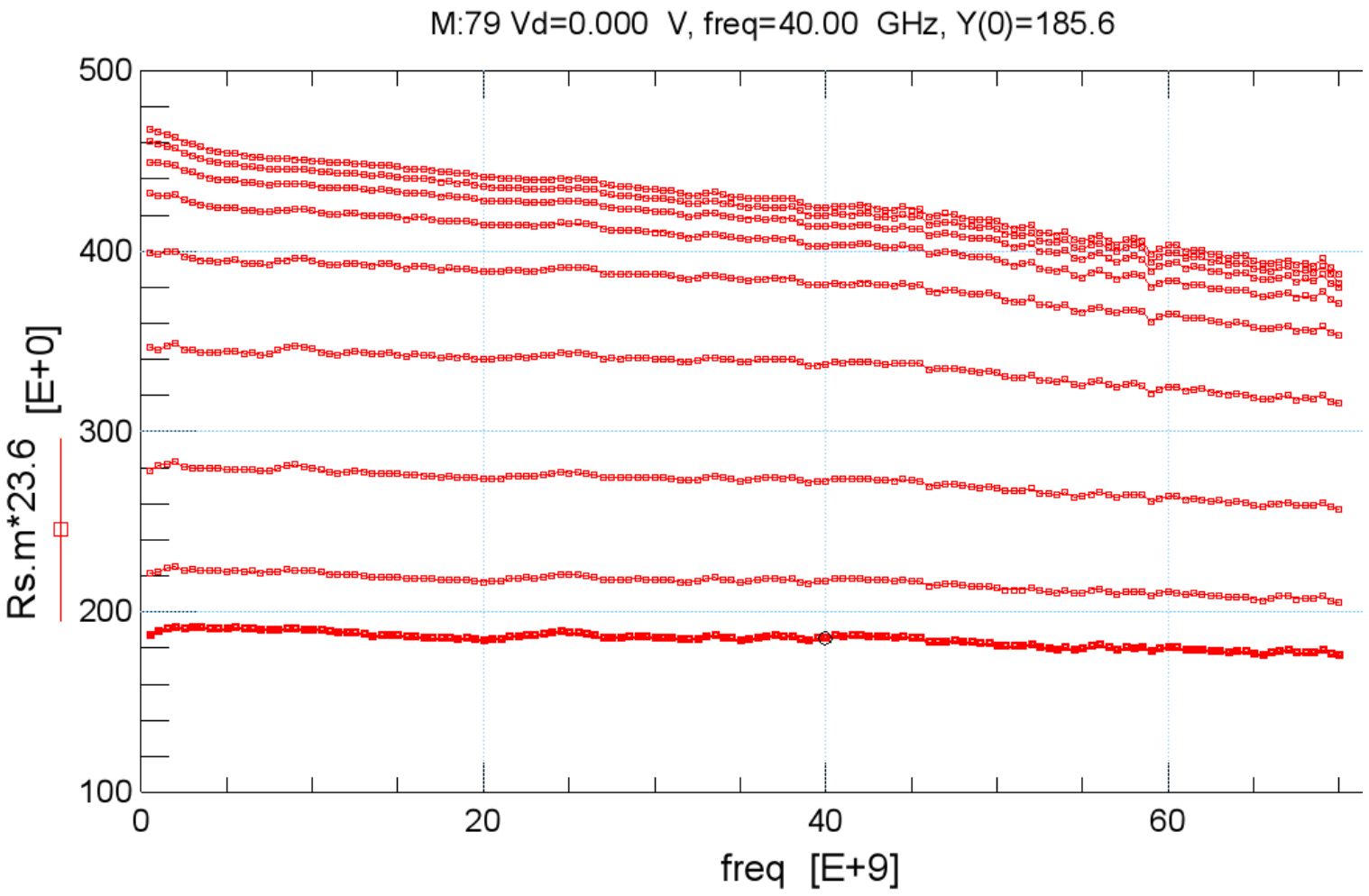
22nm FDSOI

N-MOSFET
40x20nmx590nm

2x pitch

Single Gate: R_g=15 Ω
Double Gate: R_g=9.4 Ω

Extract R'_s => source stripe width matters

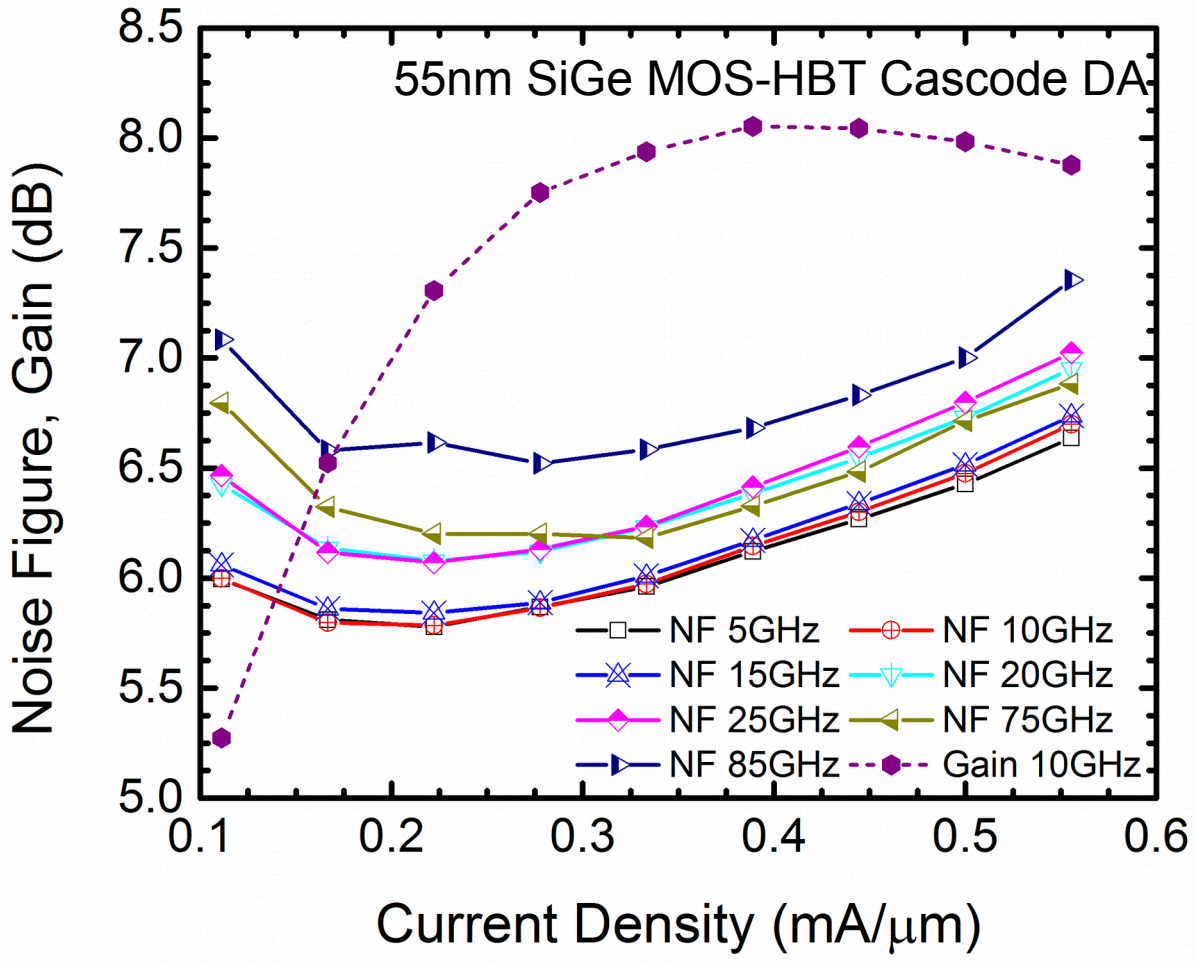


22nm FDSOI

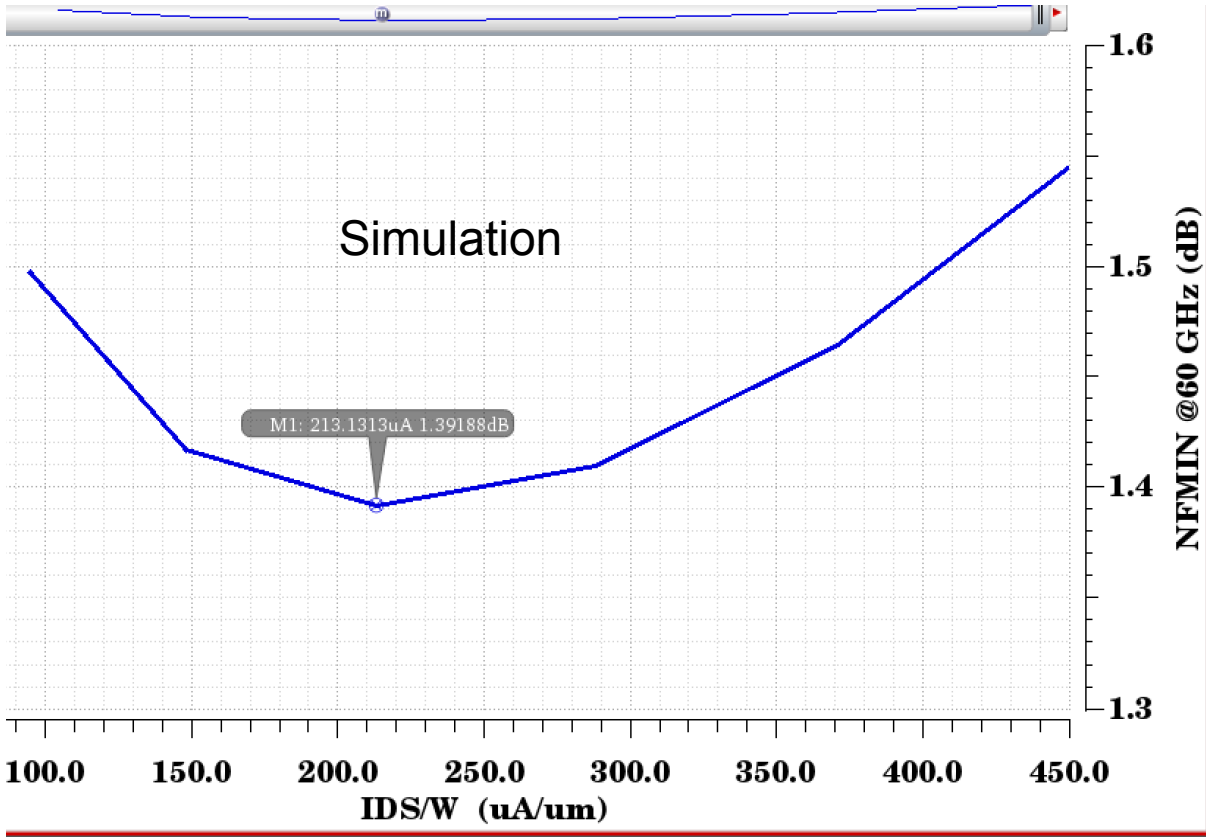
N-MOSFET
40x20nmx590nm

1x pitch: R'_s=209 Ω*µm
2x pitch: R'_s=185 Ω*µm

J_{opt}=0.2mA/μm: constant across nodes, frequency

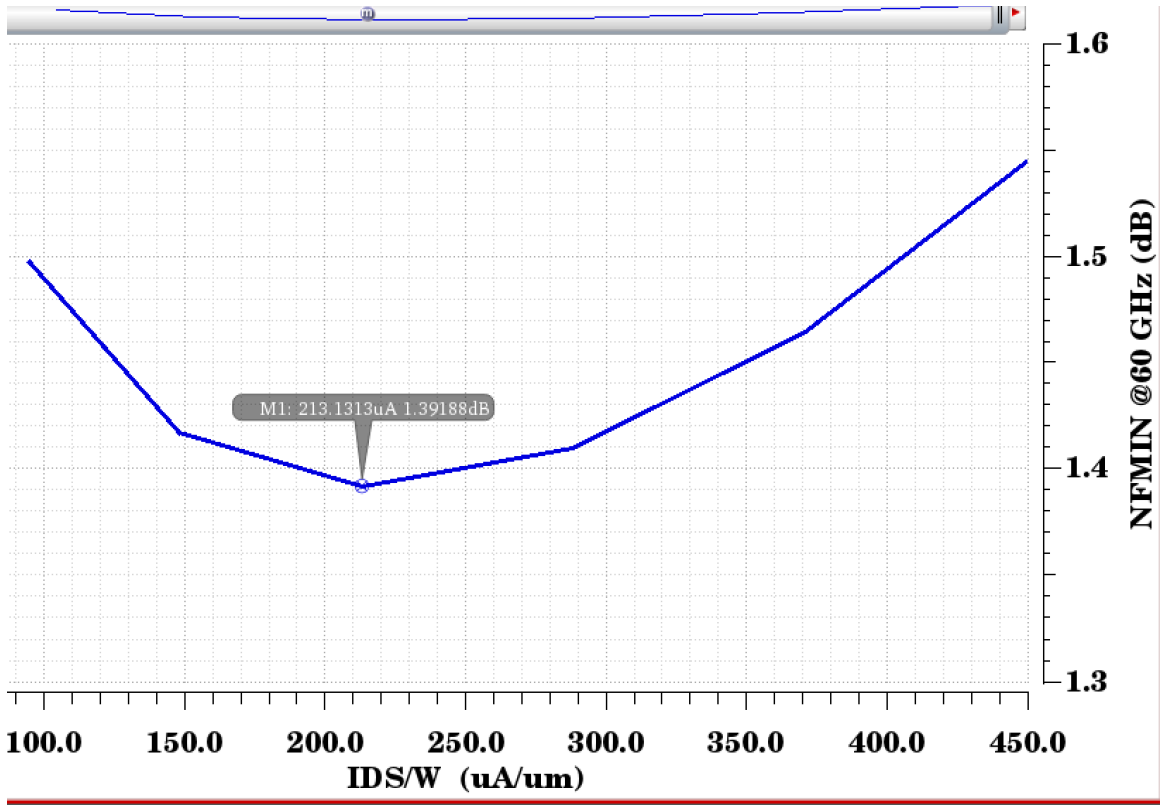


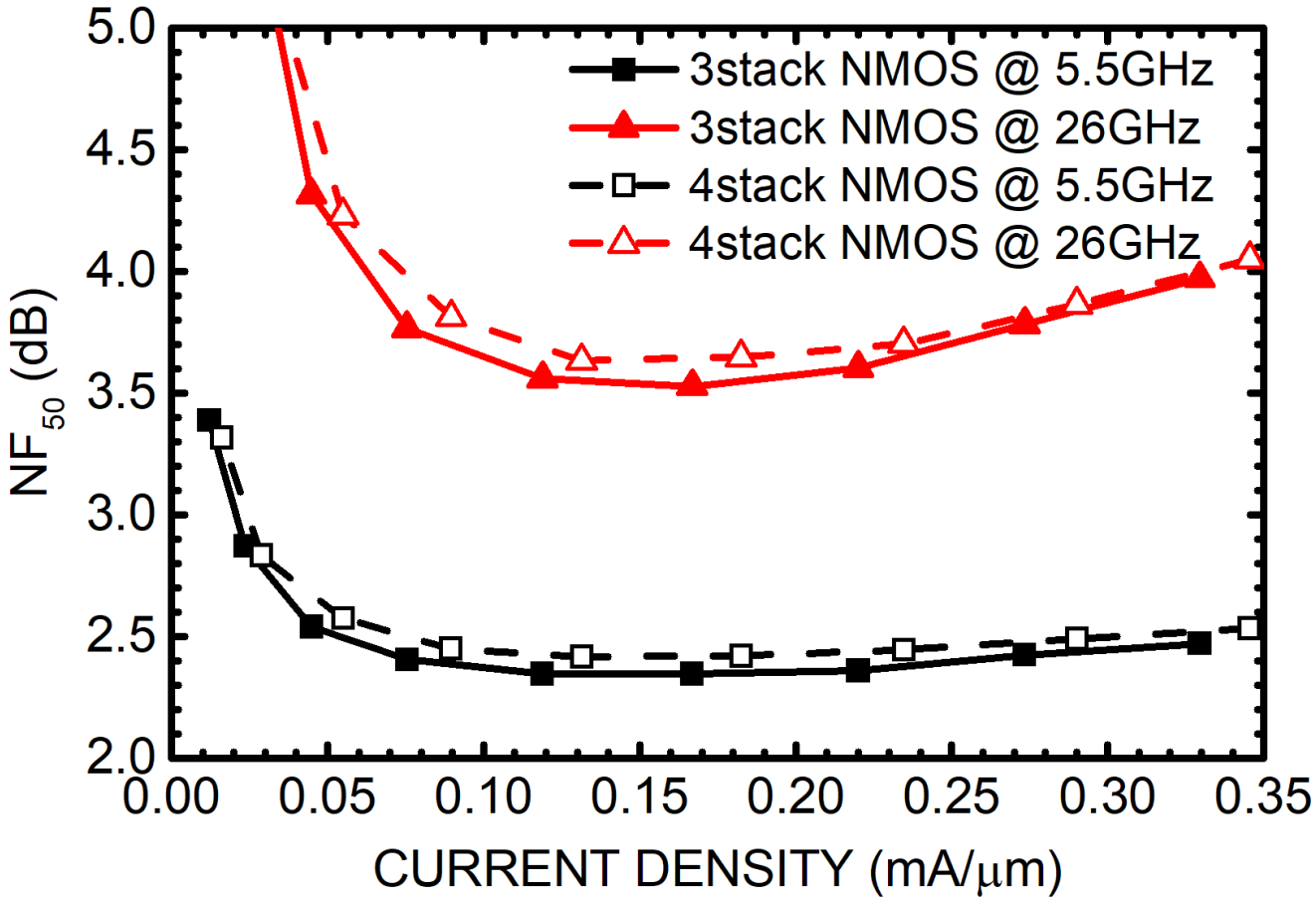
[J. Hoffman et al, IEEE JSSC Oct. 2016]



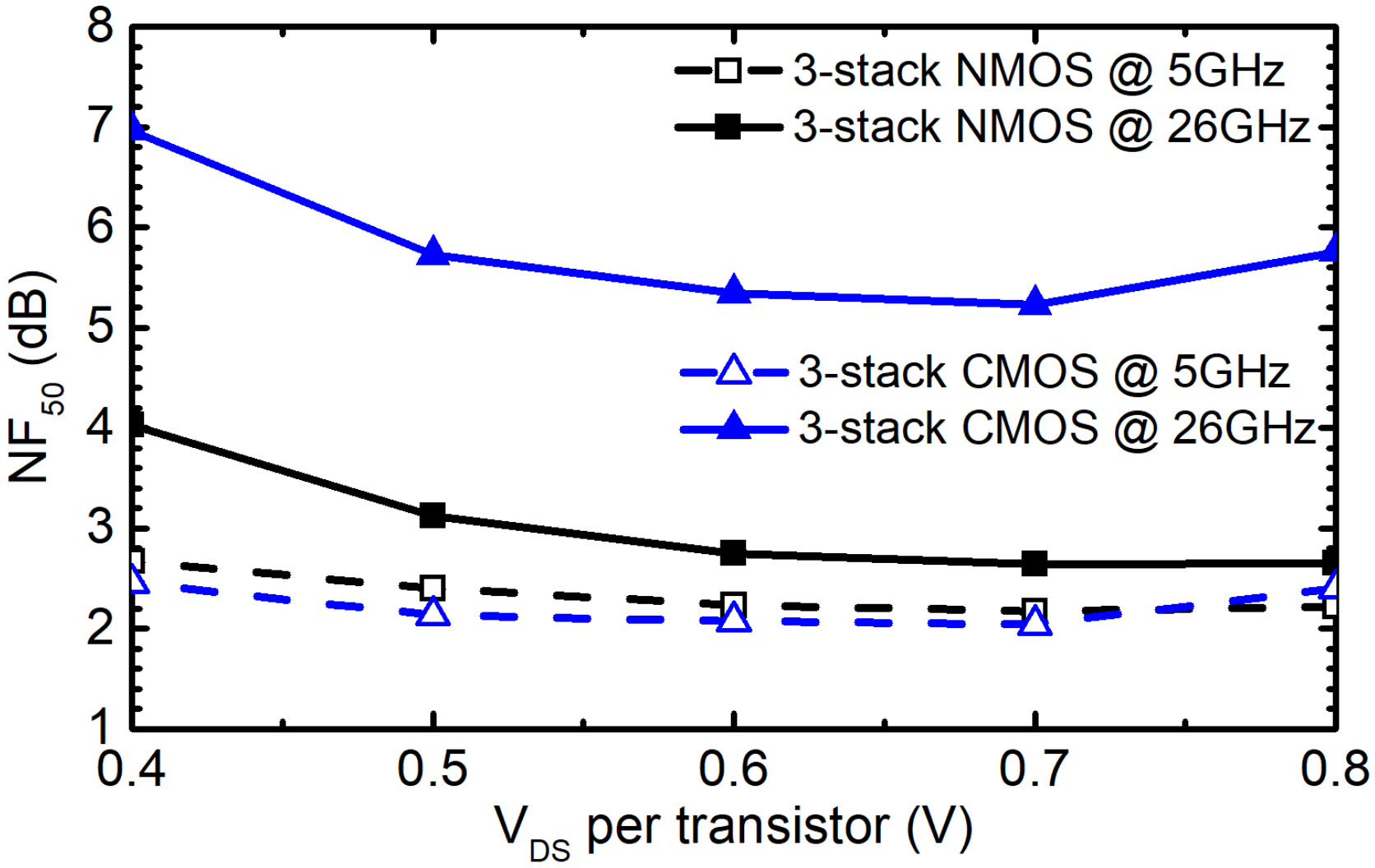
22nm FDSOI

J_{opt}=0.2mA/μm: constant across topologies



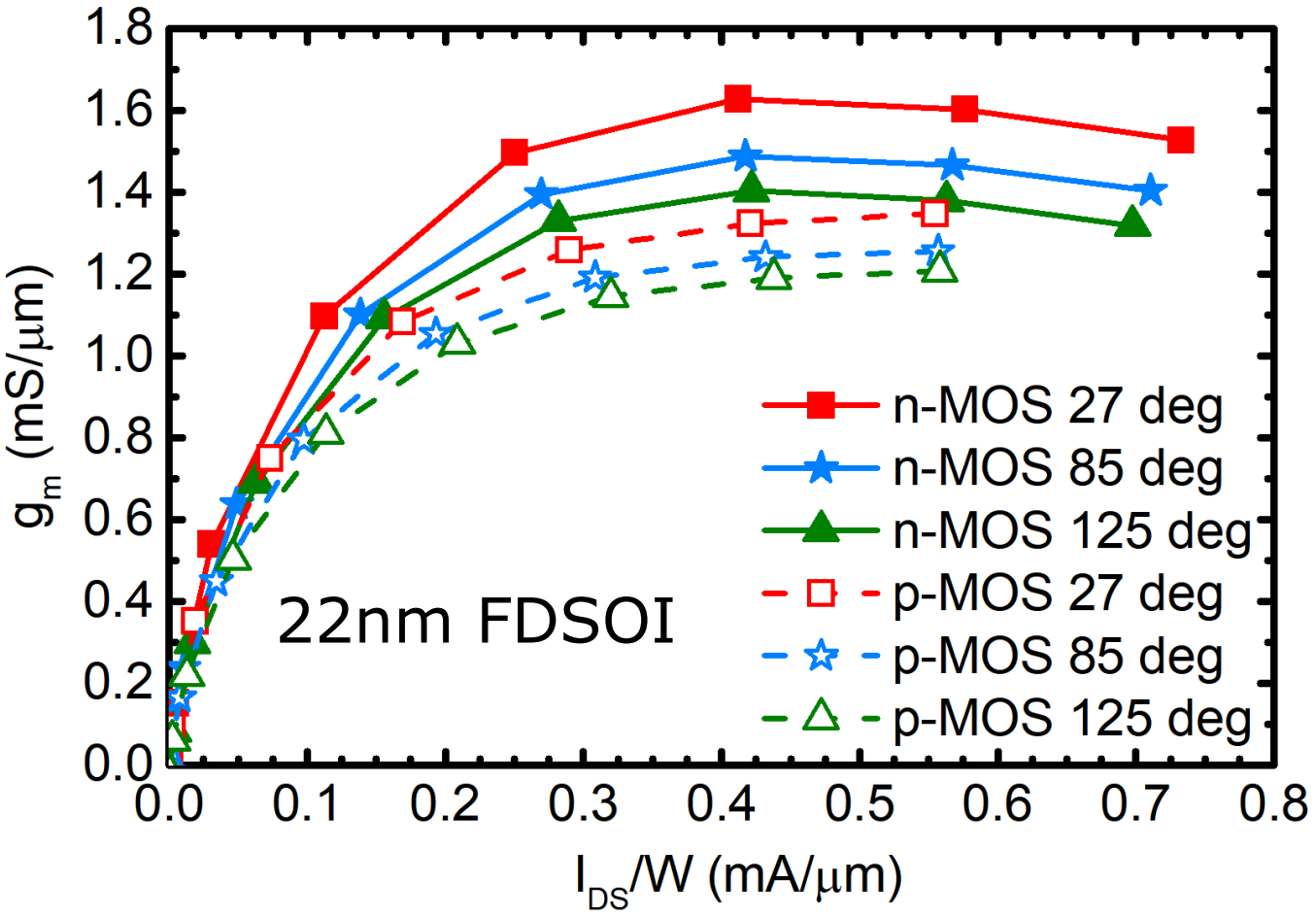


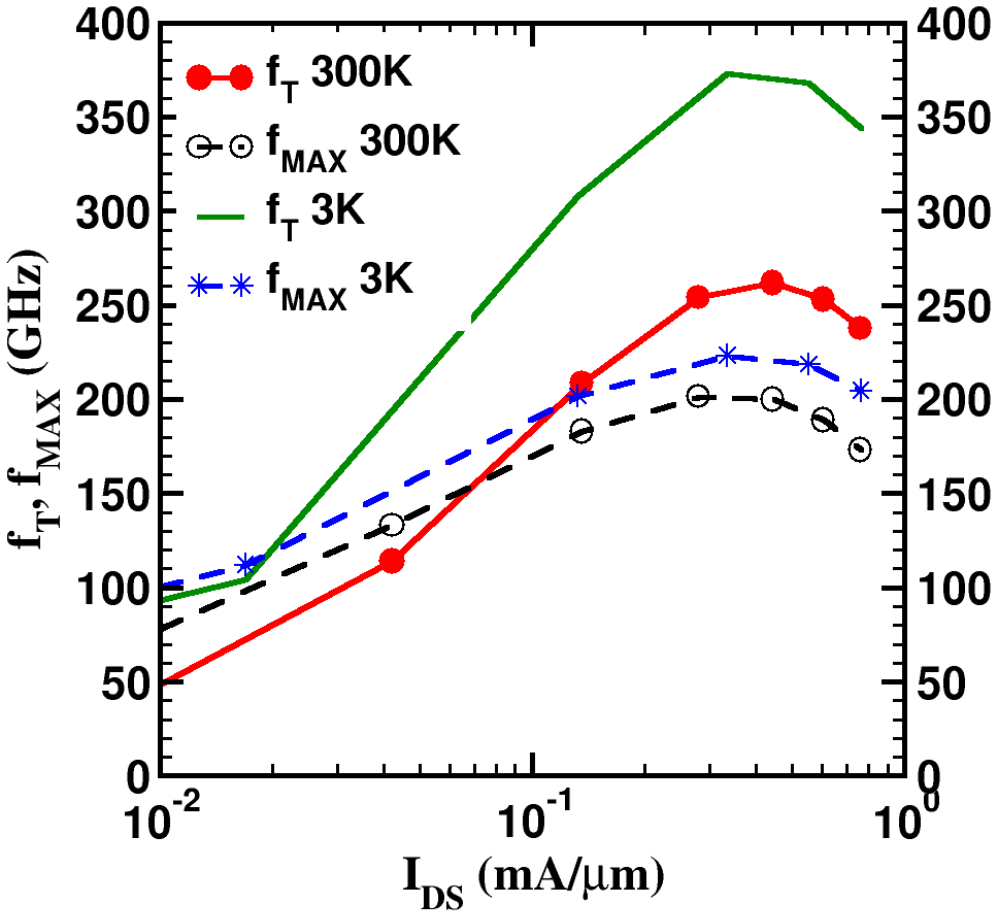
NF_{50} of series-stacked cascodes vs. V_{DS}



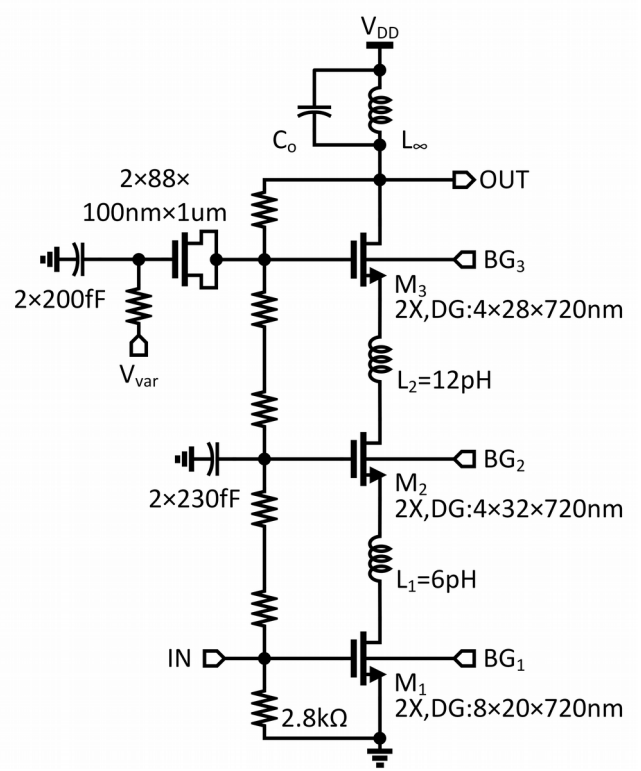
Neither input nor output matching networks used

Constant peak-g_m, f_T, f_{MAX}, J_{opt} vs. temperature

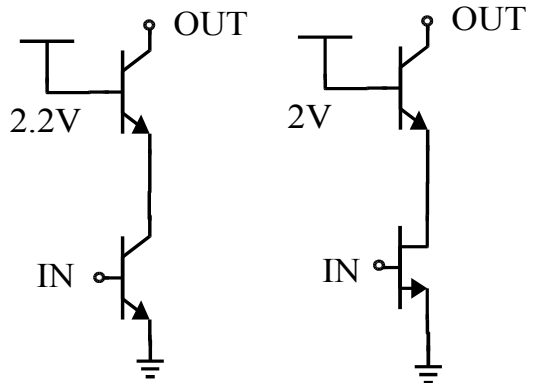




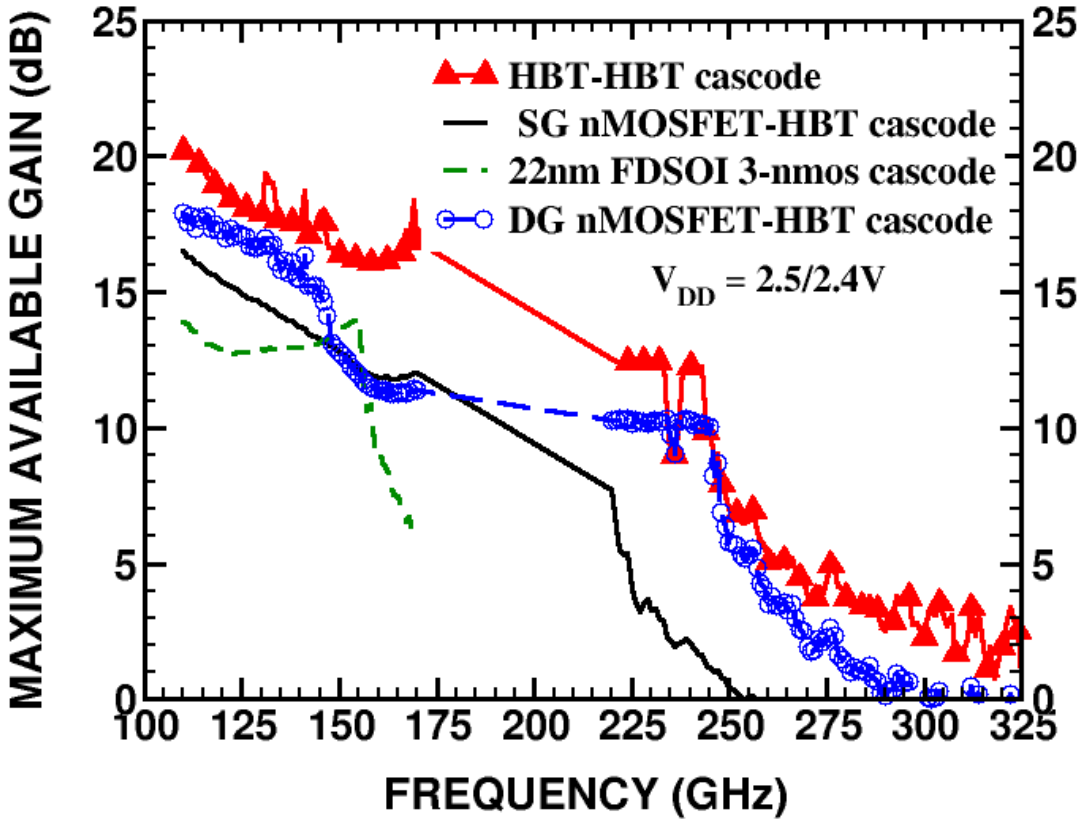
22nm FDSOI cascodes vs. 55nm MOS-HBT cascodes



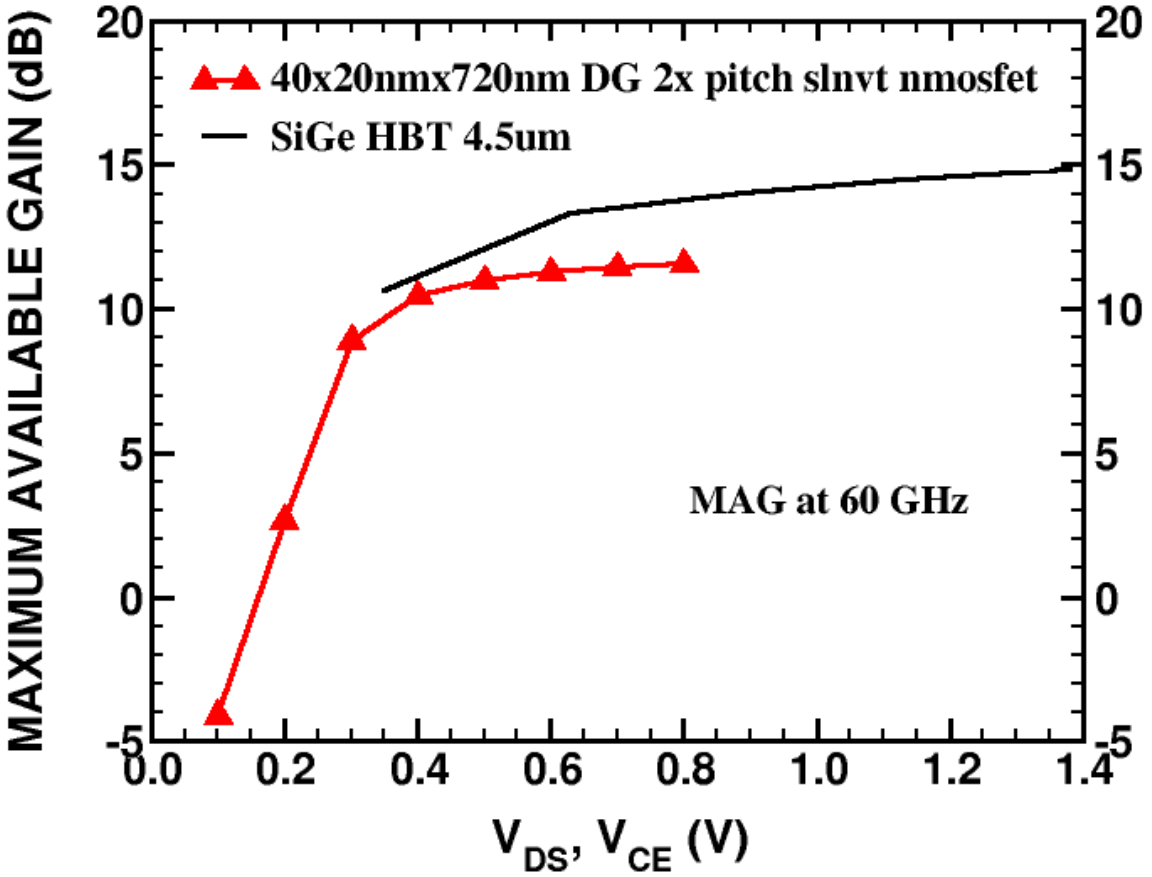
22nm FDSOI



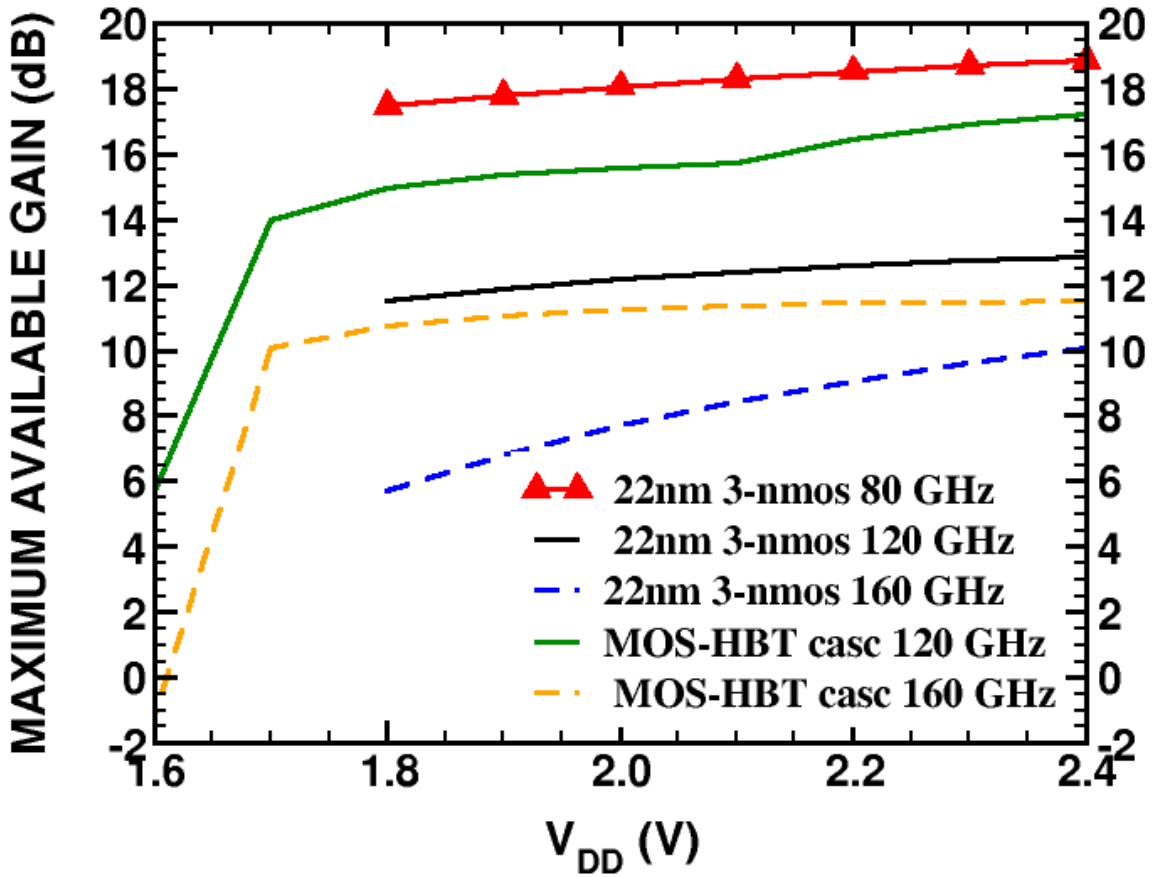
55nm SiGe BiCMOS



22nm FDSOI vs. 55nm MOS-HBT cascodes



22nm n-MOSFET and SiGe HBT at 60 GHz



22nm n-MOSFET cascodes and SiGe BiCMOS cascodes at 80, 120 and 160 GHz

Design methodology summary

- Lay out & extract MOSFETs with different W_f, ½ gate contacts, source/drain contact pitch, and styles
- Simulate or measure C'_{gs}, C'_{gd}, C'_{db}, g'_m, $R_g(W_f)$, R'_s
- Simulate or measure peak-f_T, NF_{MIN}, peak-MAG, J_{opt}, $J_{peak\text{-}MAG}$
- Optimize layout based on NF_{MIN}, peak-MAG at desired frequency
- Now ***design circuits by hand***: Find W, N_f, I_{DS} of all transistors
- Use computer simulation after extraction to design matching network without changing transistor sizes and bias current
- Design/model your inductors, transformers to suit top layout

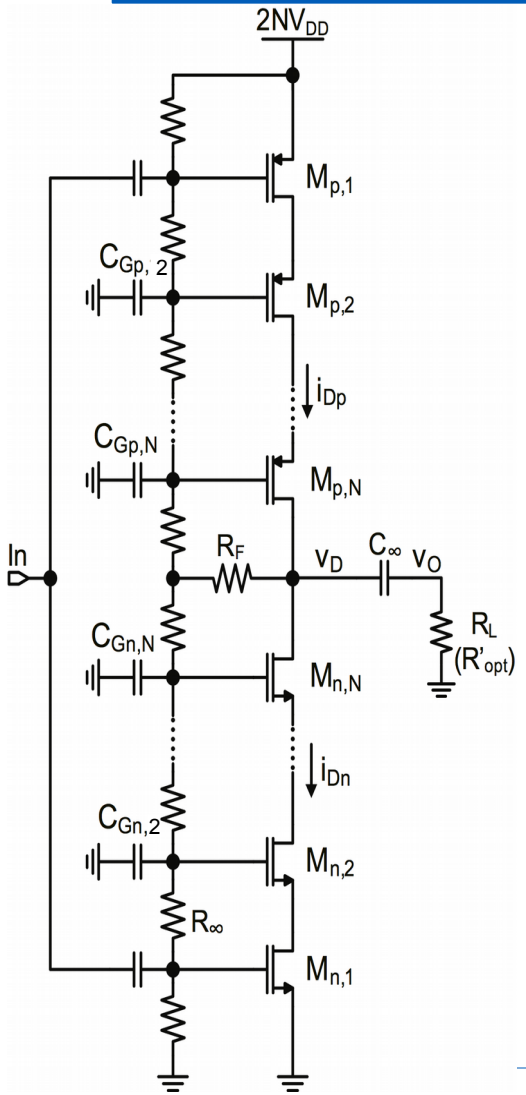
Outline

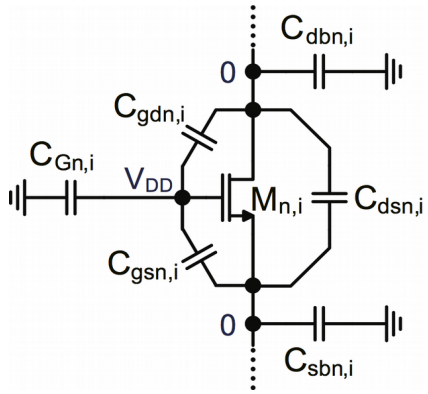
- Unique Transistor Features and Performance
- Design Fundamentals
- **Specific mm-wave and high-speed circuit topologies**
- Design Examples
- Conclusions

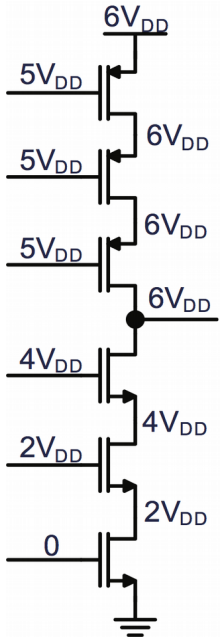
Unique circuit topologies

- Series-stacked, large-swing PA and SiPh modulator driver with individual back-gate control
- 4-terminal mm-wave varactor VCO with small *KVCO*
- Series-stacked doubler - LVT/HVT back-gate control
- Series-stacked switches (as in 180nm/45nm PDSOI CMOS)
- CMOS switches with back-gate control
- 0.8V CMOS Quasi-CML - LVT/HVT back-gate control

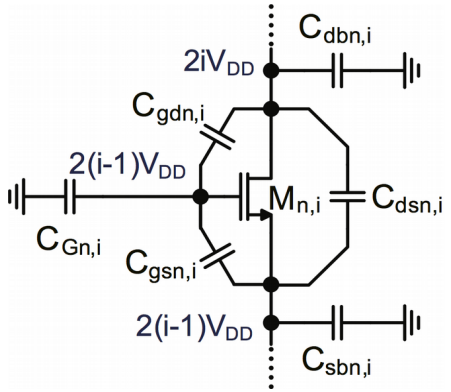
Series-stacked n-MOSFET or CMOS PA/Driver

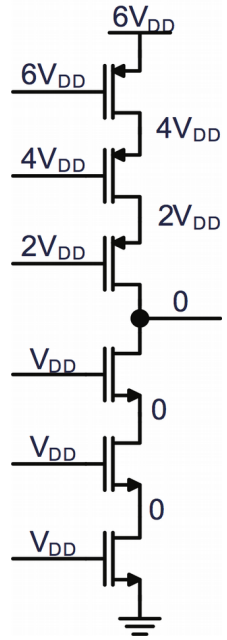






ON





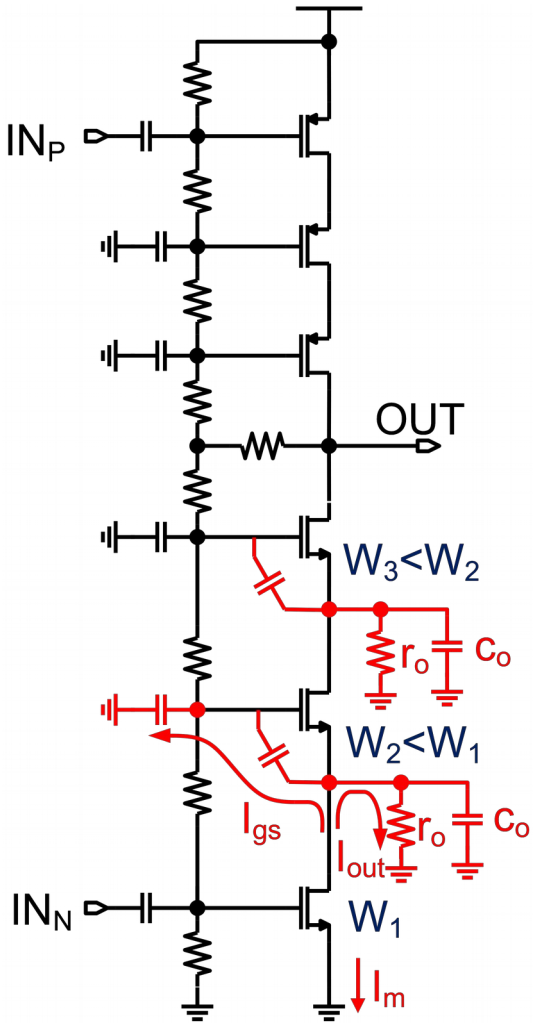
OFF

$$C_{Gn,i} = \frac{C_{gsn,i} + 3C_{gdn,i}}{2i - 3}$$

[I. Sarkas ISSCC, 2012]

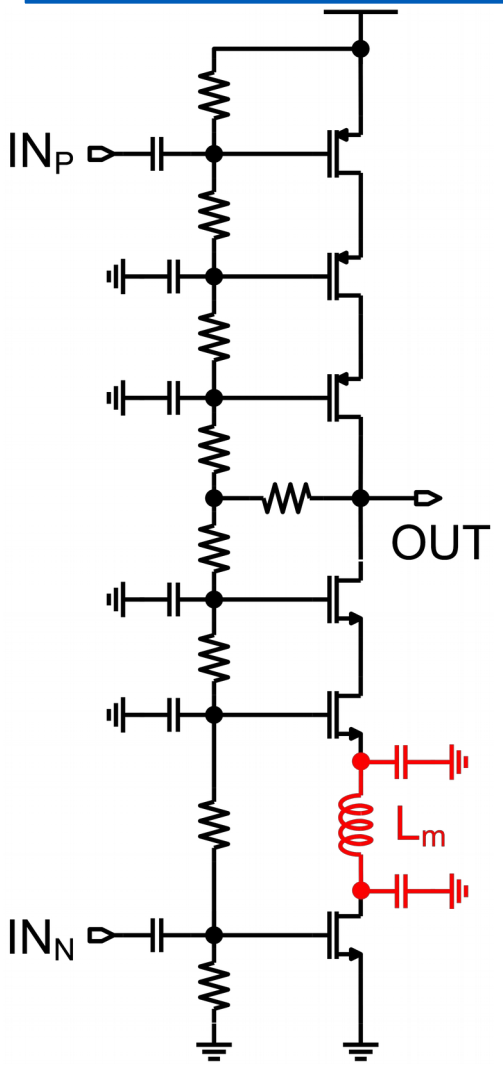
[I. Sarkas IEEE PA Symposium, 2013]

Transistor sizing



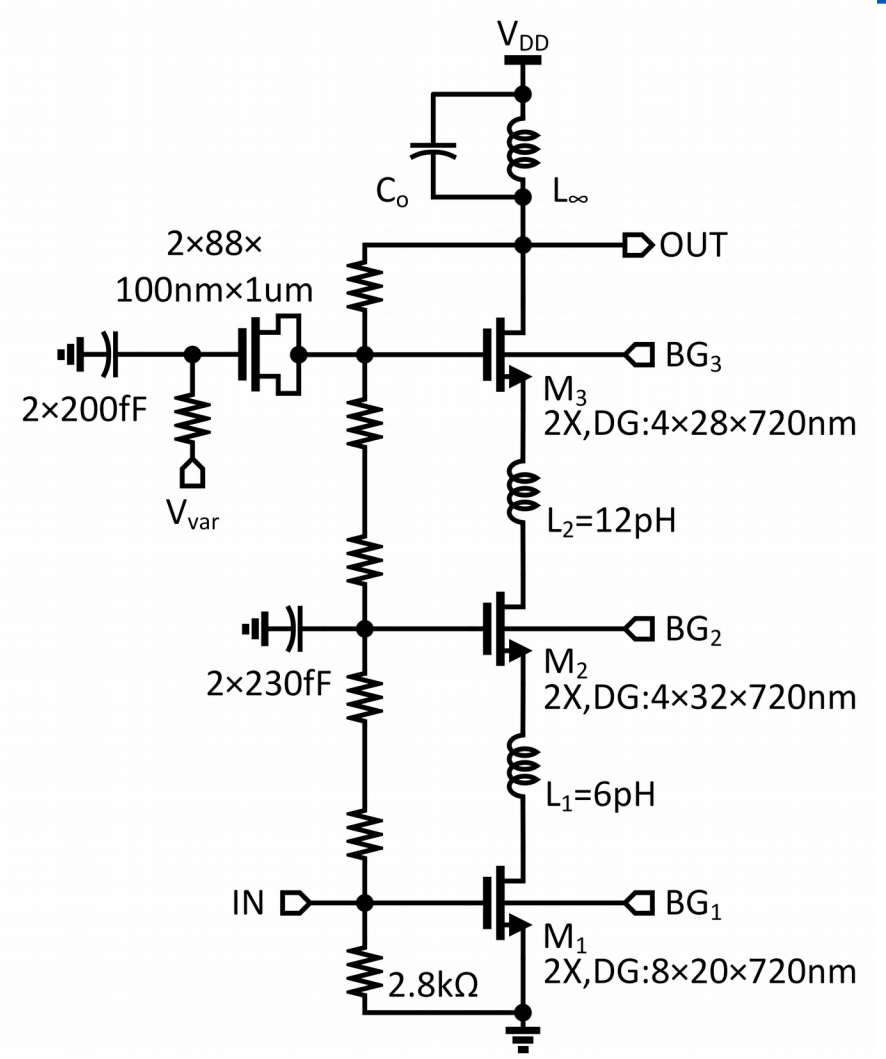
- Dynamic current I_m is reduced higher up in the stack
- Progressively smaller transistor width higher up in the stack can handle the smaller current
- Minimizes C_{out} and increases Z_{in}, Z_{out}, BW_{3dB}

Inductive broadbanding (inductive neutralization)



- Artificial transmission line
- Unlike Miller (negative capacitance) neutralization which improves *MAG* but degrades NF_{MIN} and f_T, it improves
  - *MAG*
  - f_T, and
  - NF_{MIN}
- f_{MAX} remains unchanged (as Miller neutralization)

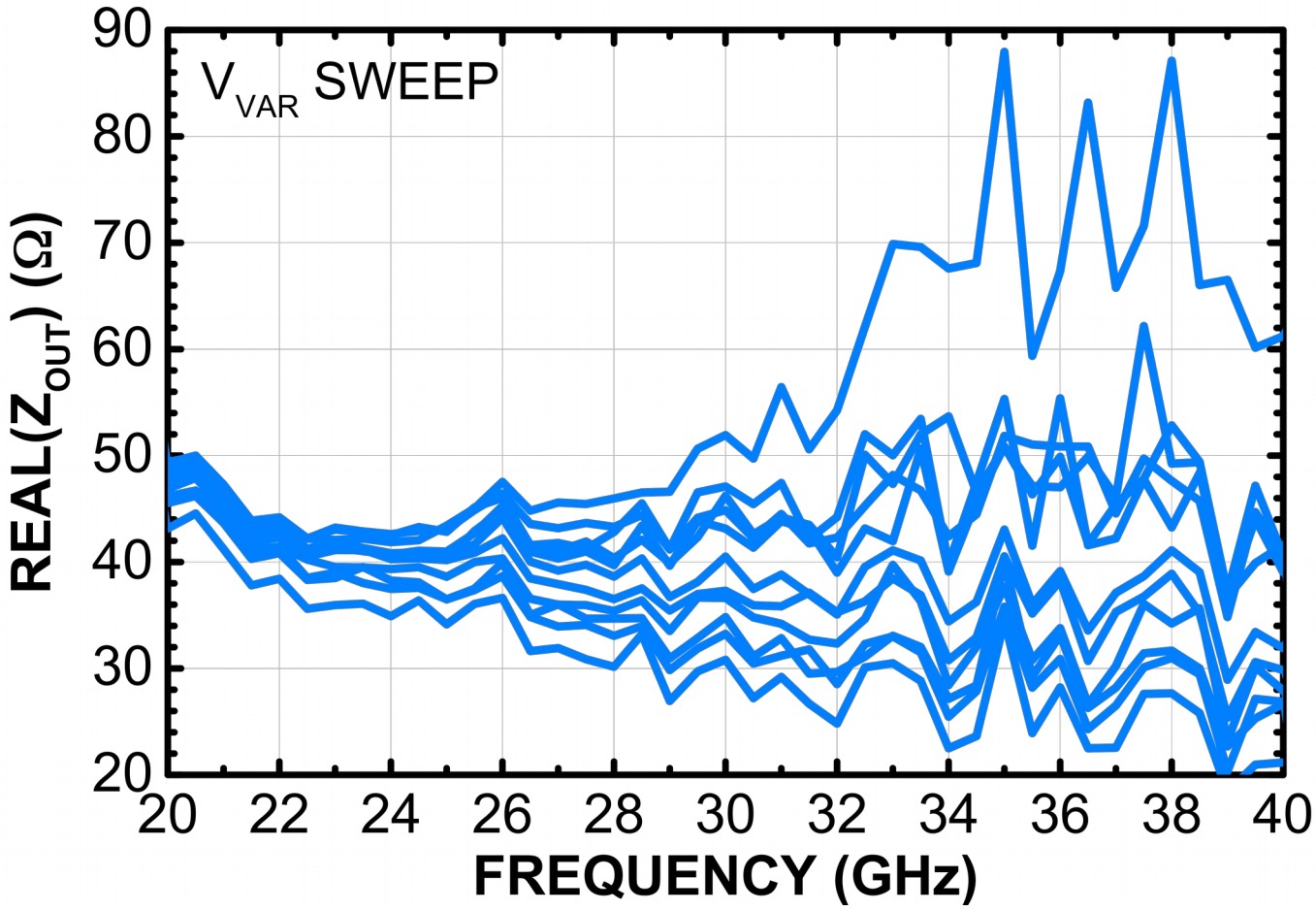
New design freedom in FDSOI



- Increasing backgate voltage in upper stack: LVT n-MOS BG at 1, 2, 3V
- Output matching without matching network from C_i where i=2,3
- Replace C_3 with varactor => adjust output impedance and output swing
- Control reliability of top n-MOSFET

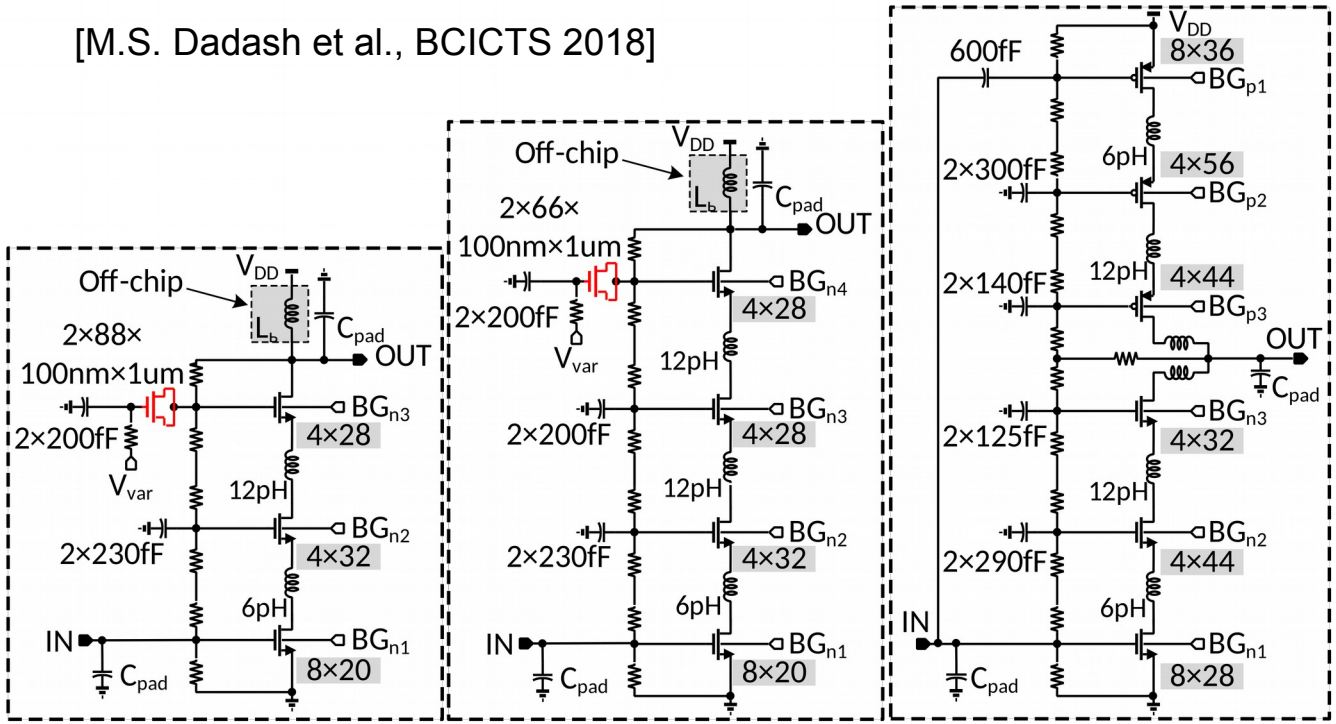
Varactor control of R_{out} in 22nm FDSOI

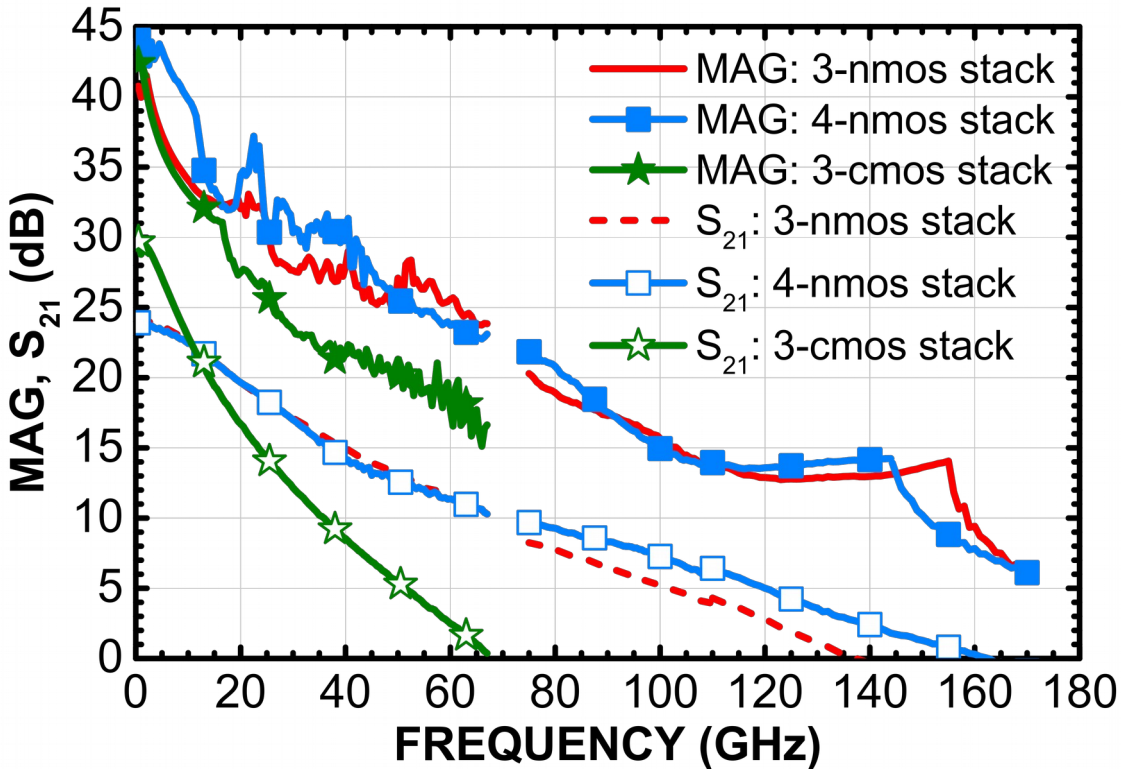
- 4-nmos stack
- Thick oxide varactor
- Control voltage: 1.8-3.8 V



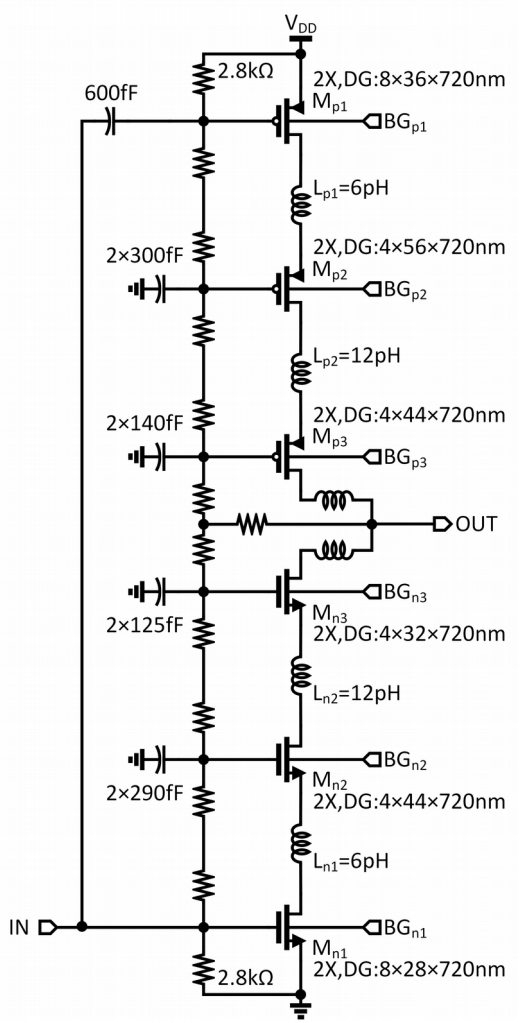
Large-swing/power cascodes in 22nm FDSOI

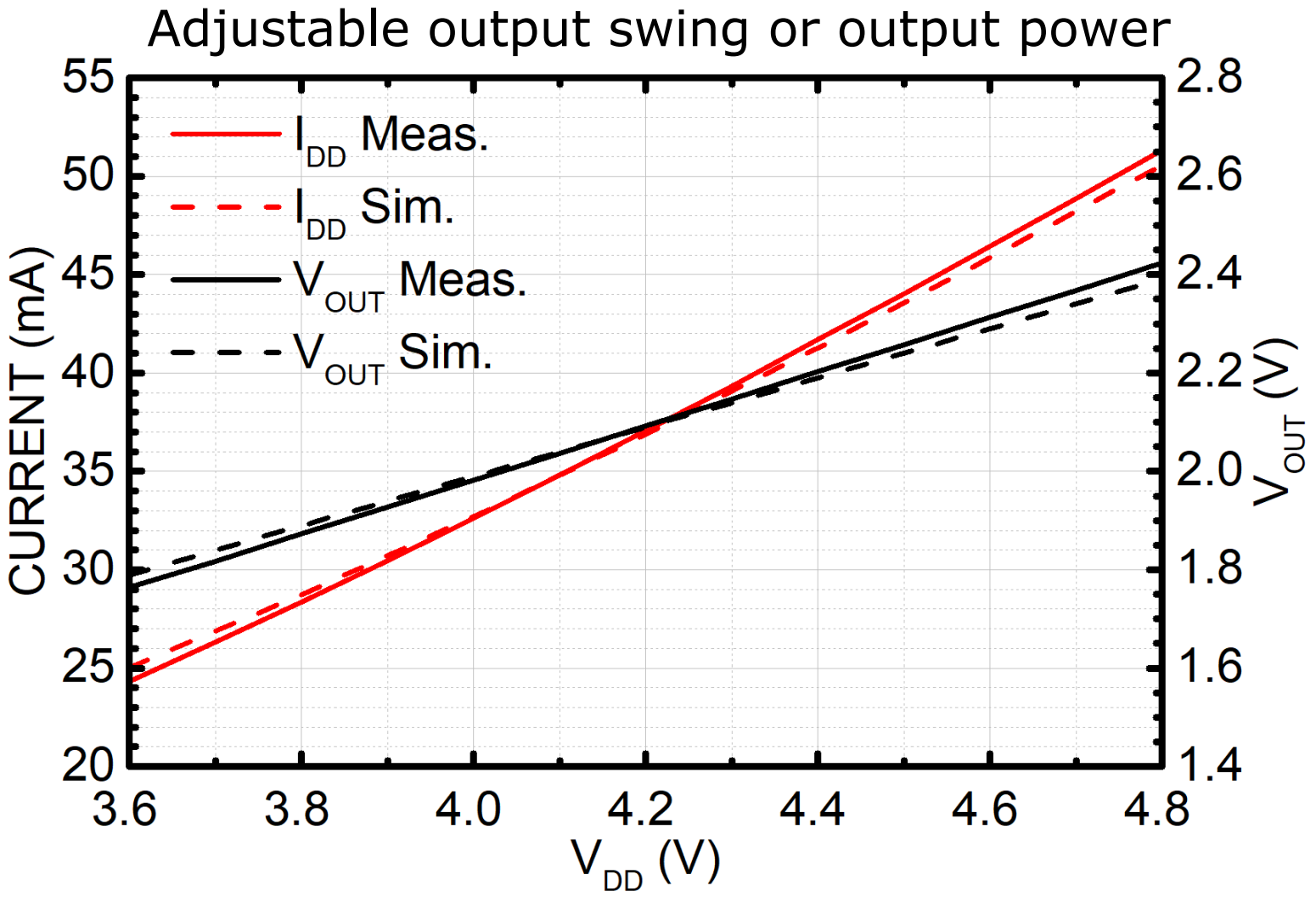
[M.S. Dadash et al., BCICTS 2018]





$V_{DD}/V_{OUT}/I_{DD}$ control in 3-stack CMOS inv 22nm FDSOI





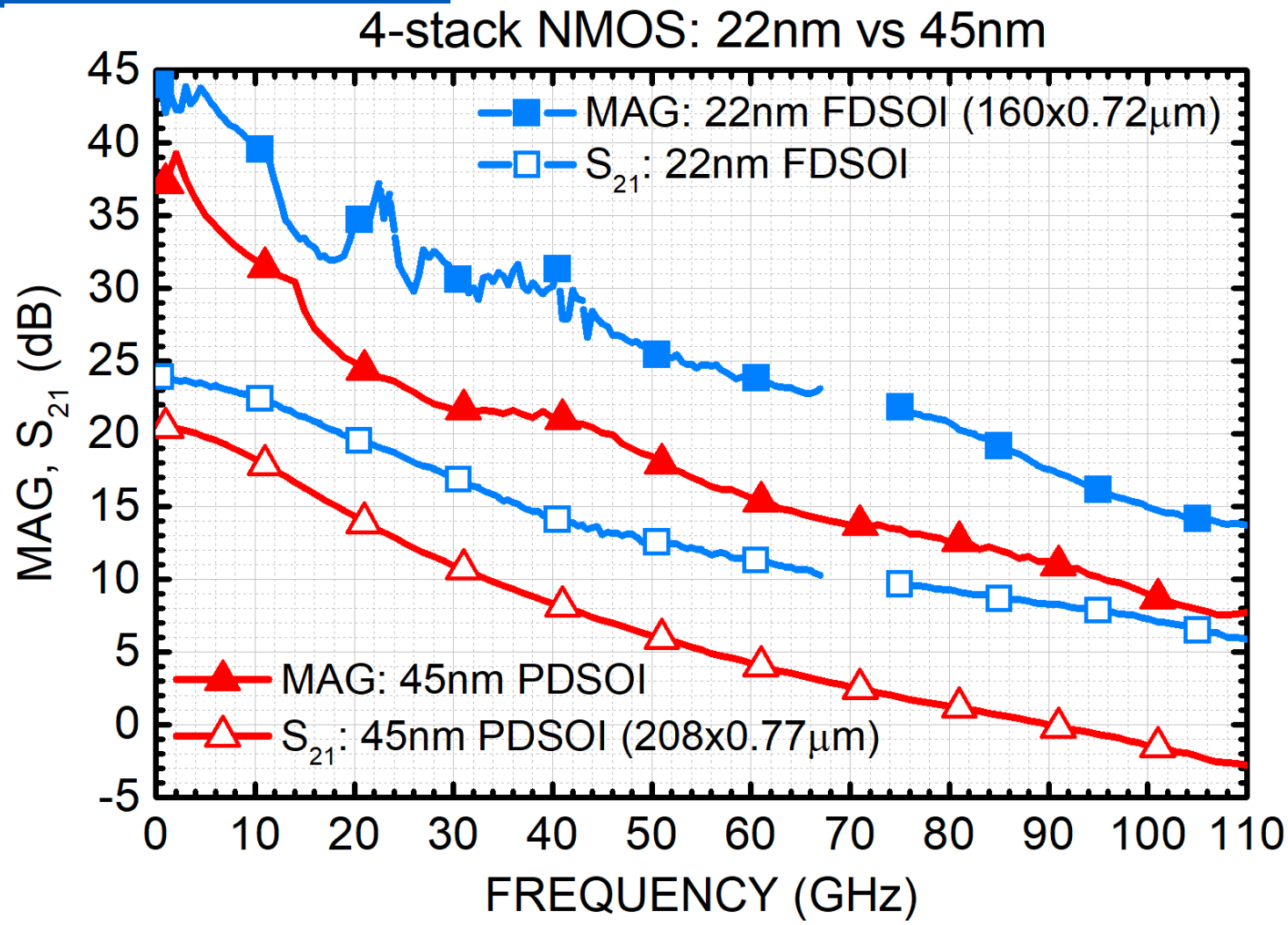
Comparison with 45nm PDSOI

- 3/4-nmos stack

160x720nm=115μm

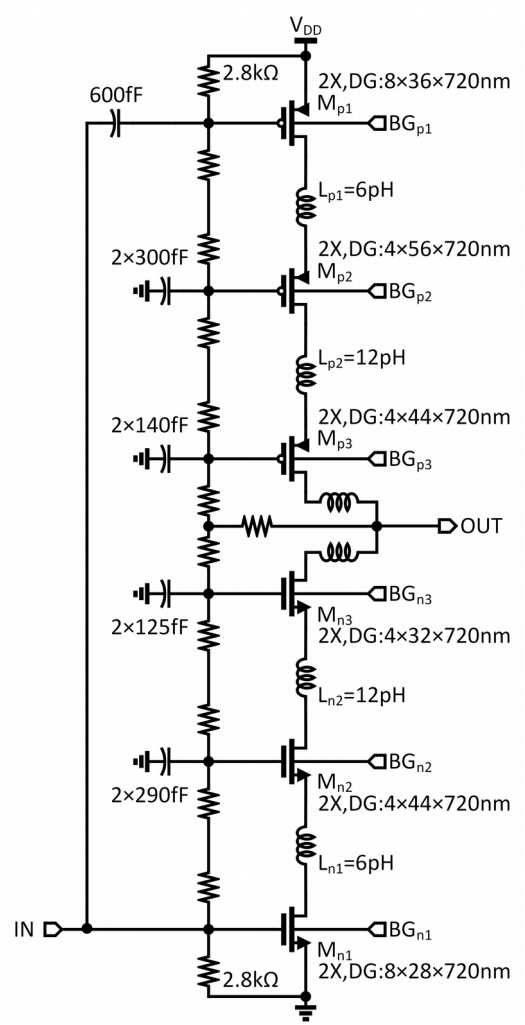
- 3-CMOS inverter stack

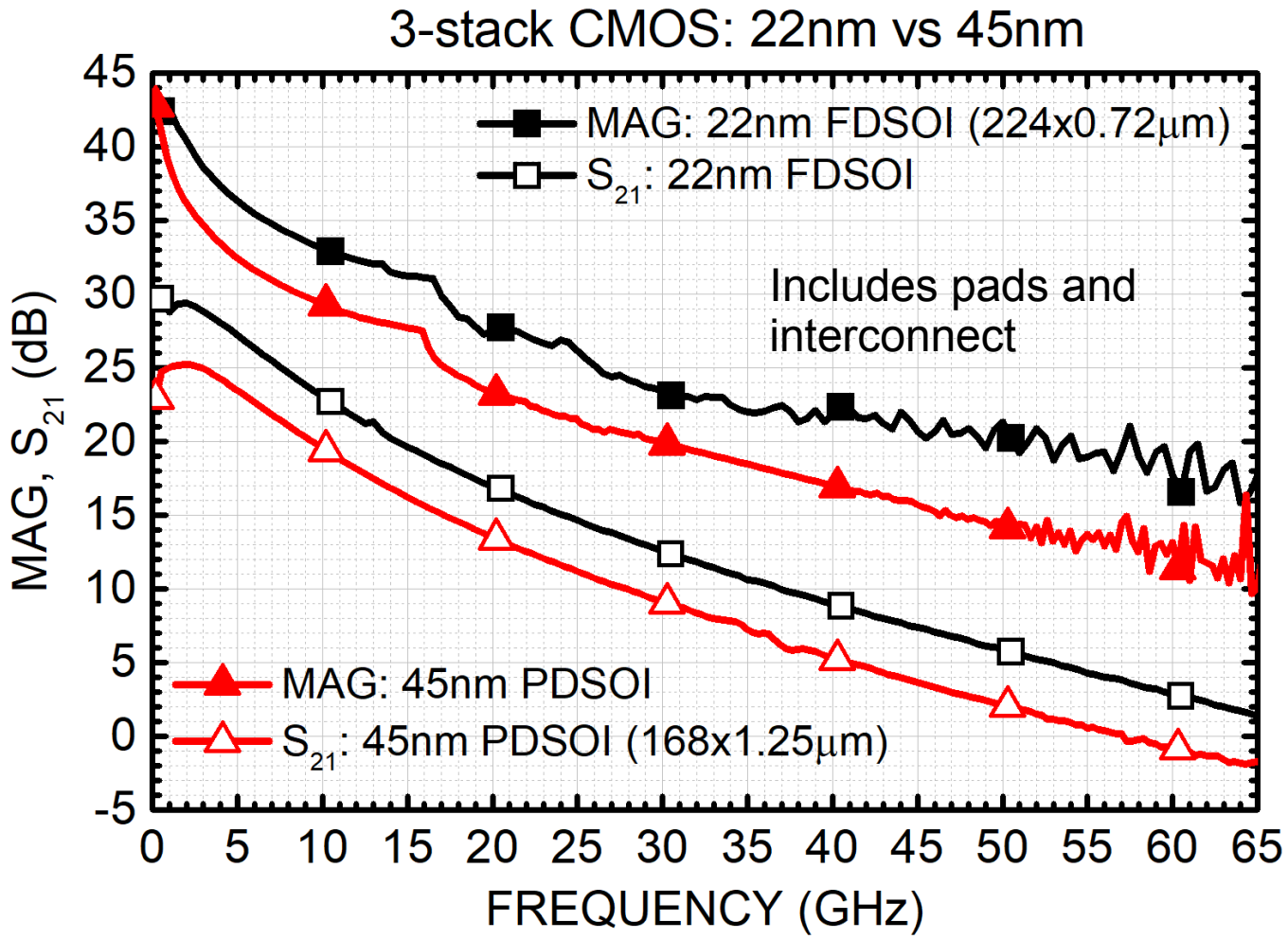
224x720nm=161μm



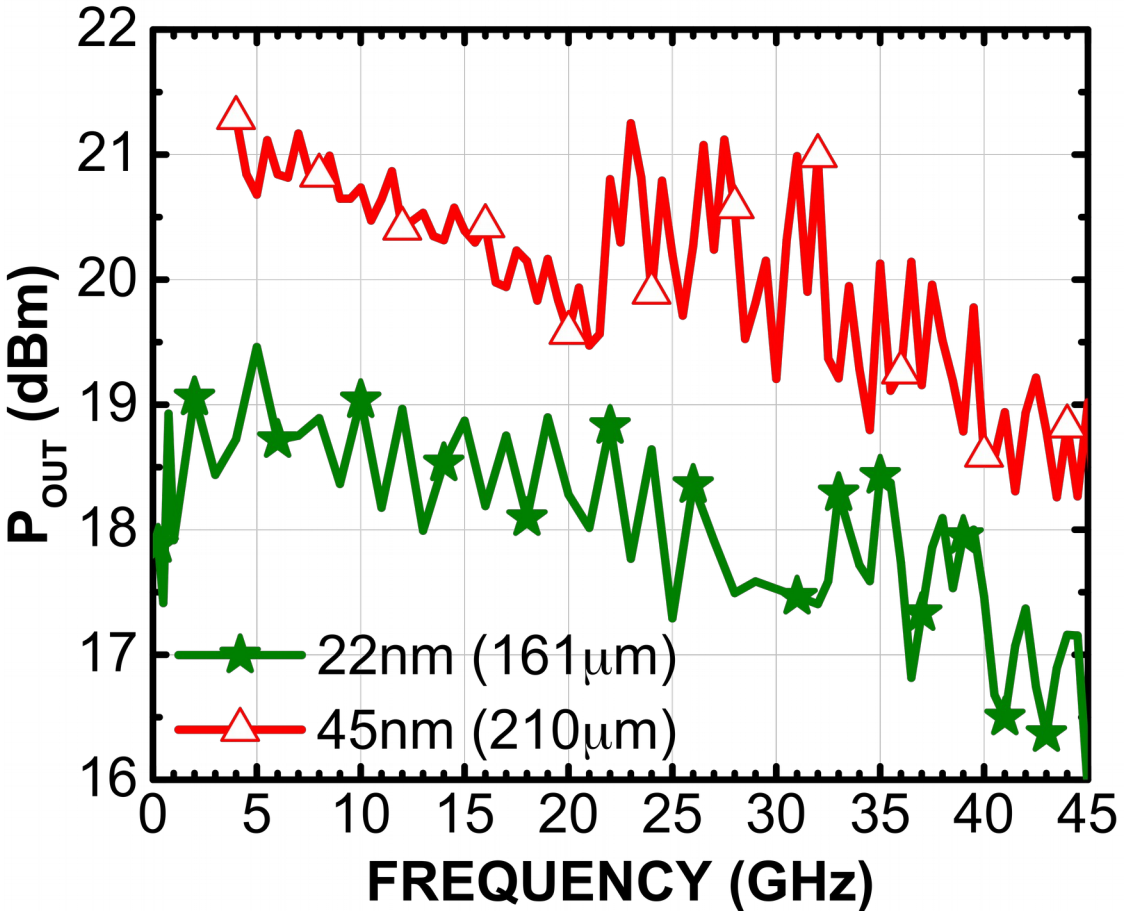
[M.S. Dadash et al., BCICTS 2018]

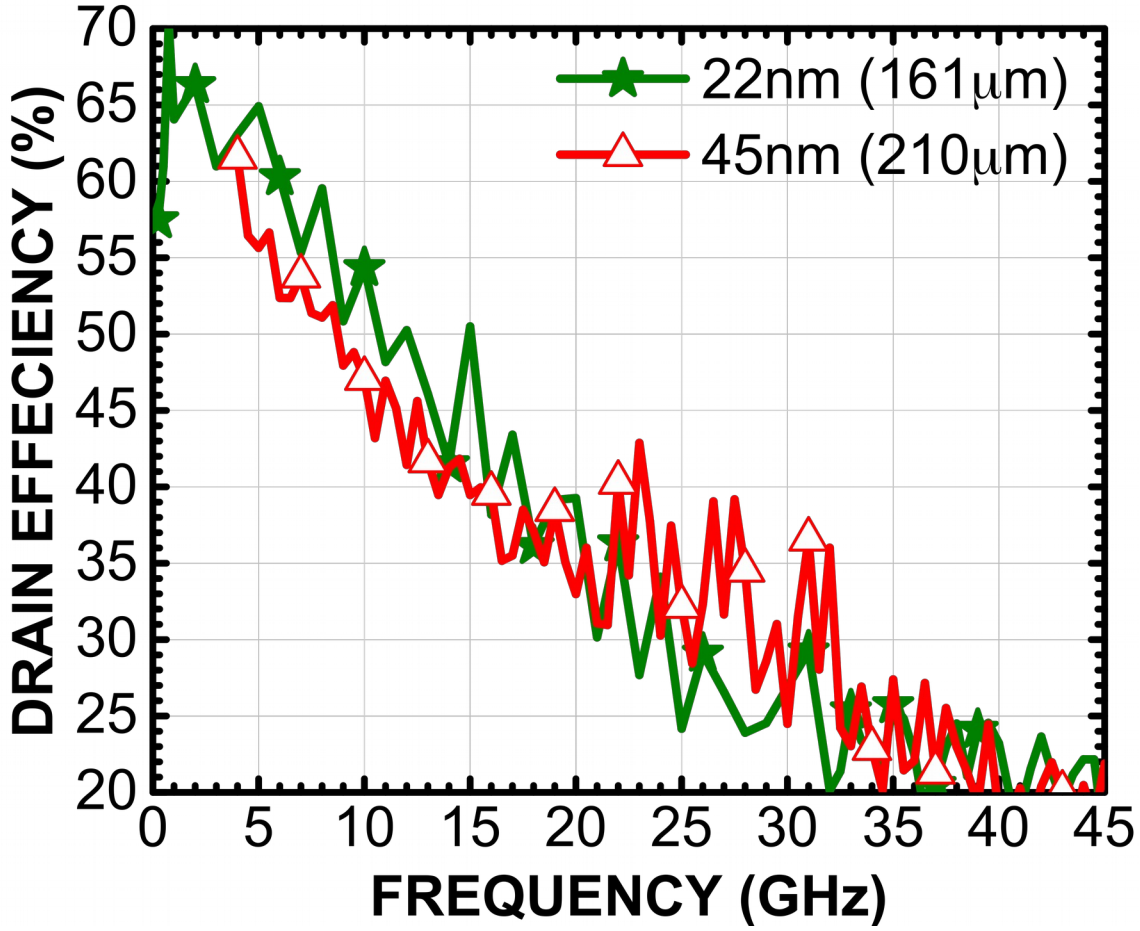
3-stack CMOS inv.: 22nm FDSOI vs. 45nm PDSOI



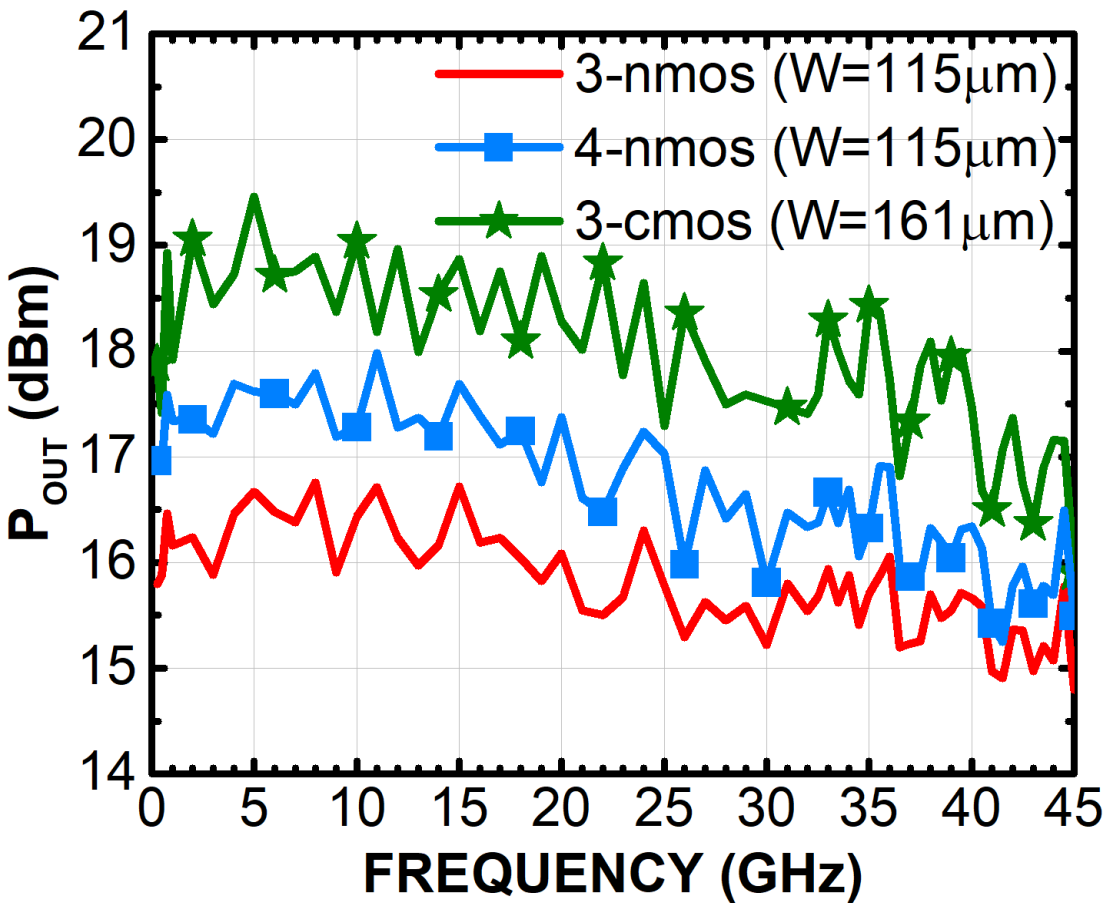


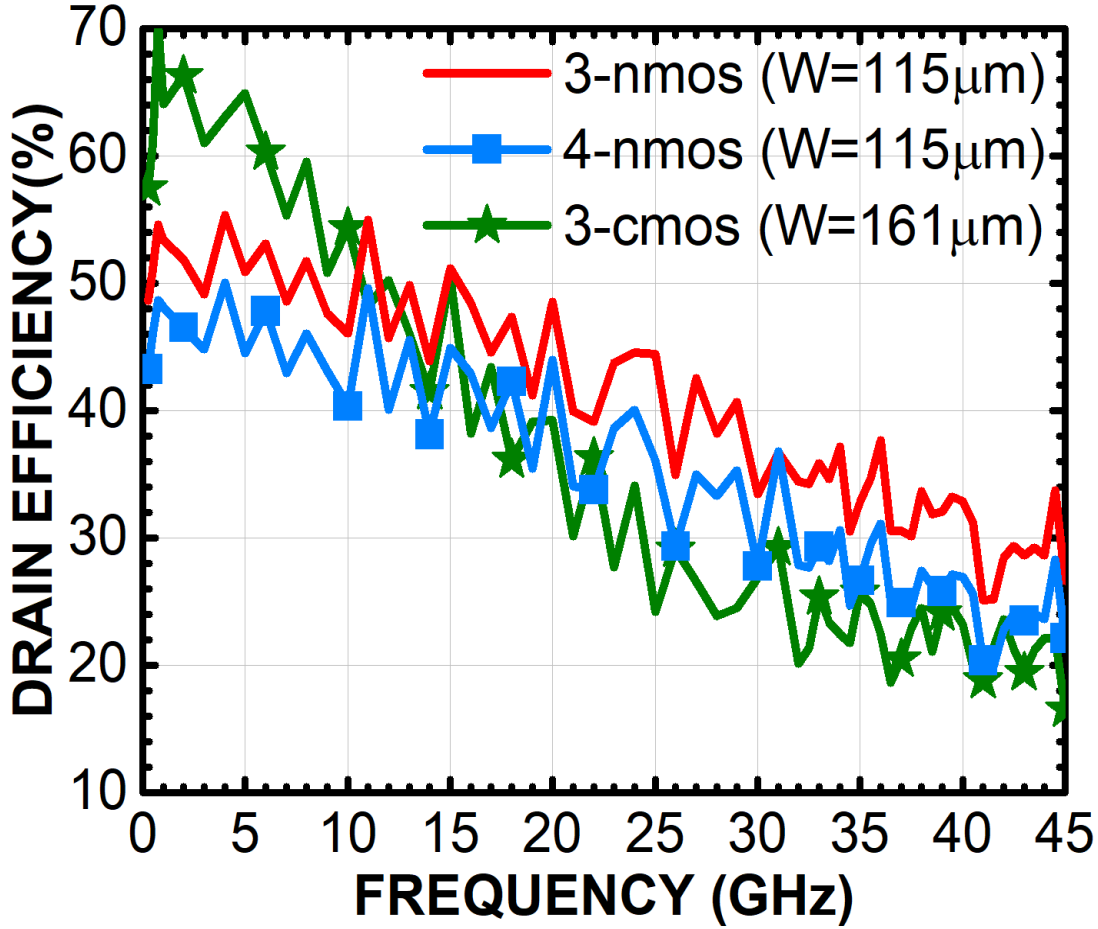
3-stack CMOS PA: 22nm FDSOI vs. 45nm PDSOI





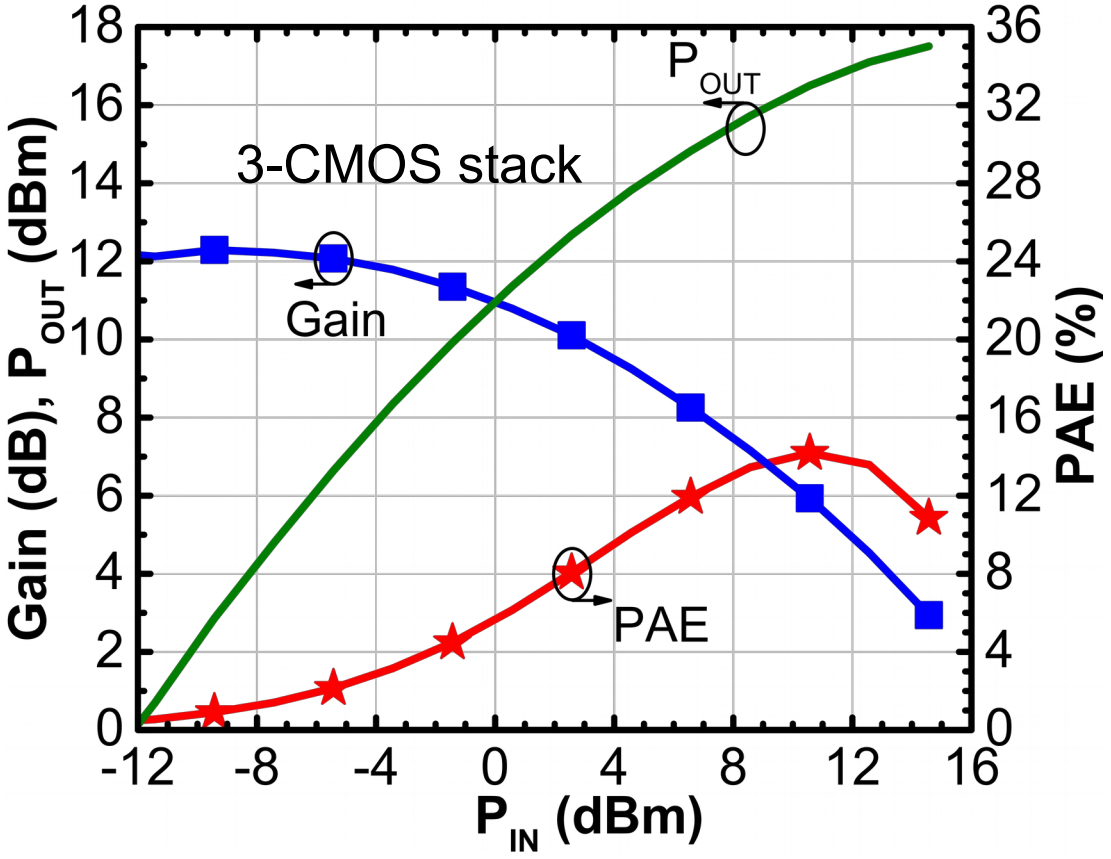
P_{SAT} and drain efficiency vs. frequency

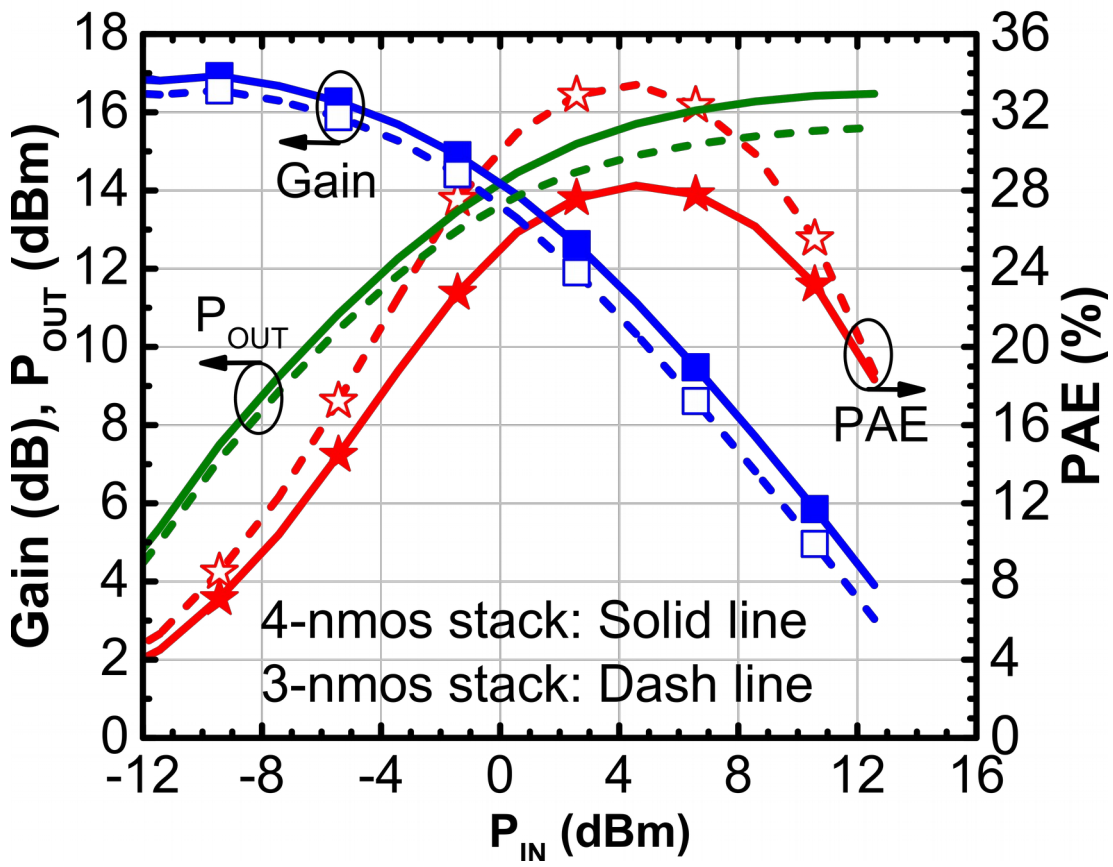




[M.S. Dadash et al., BCICTS 2018]

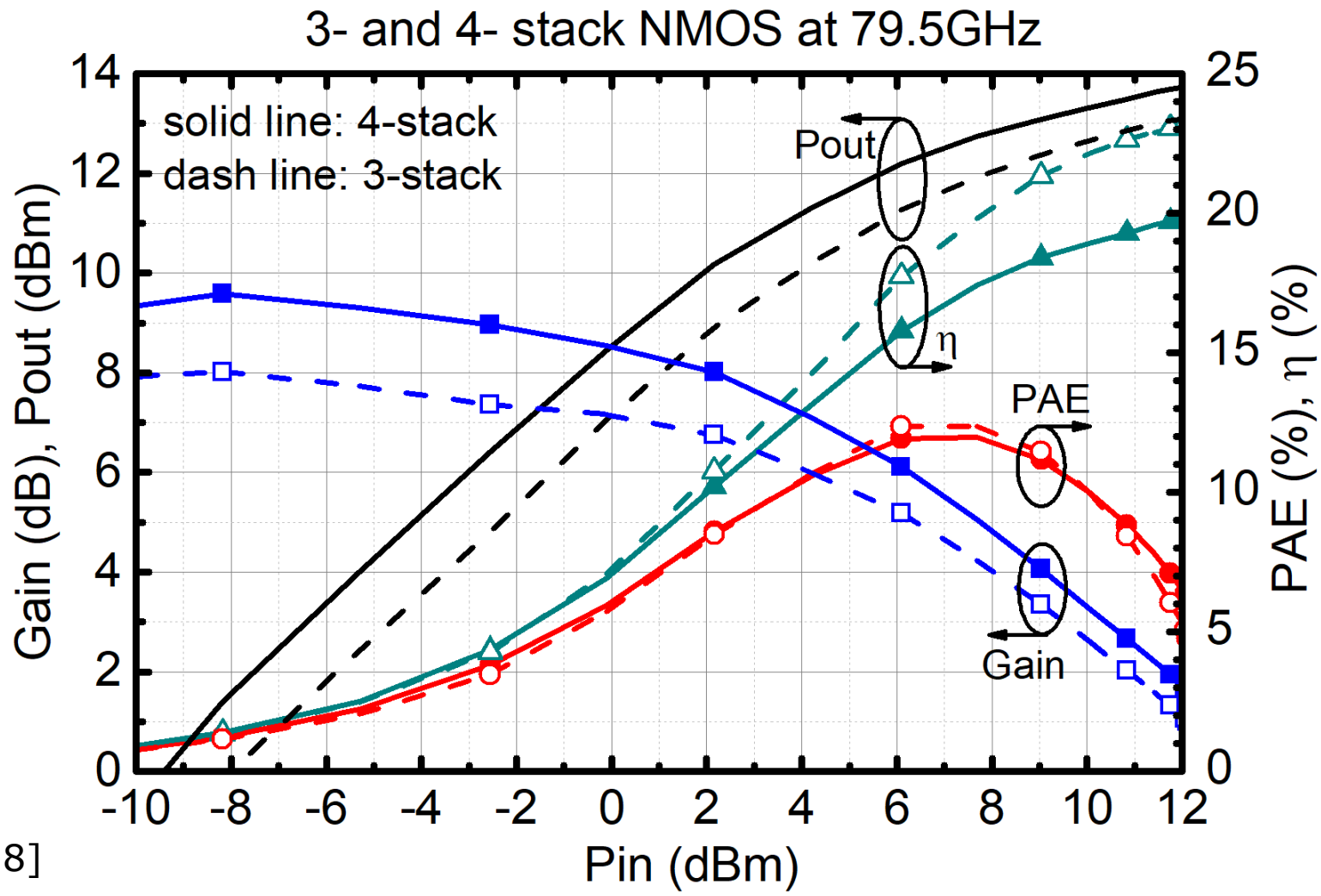
22nm cascodes: 28-GHz P_{OUT}, *PAE*, *G*





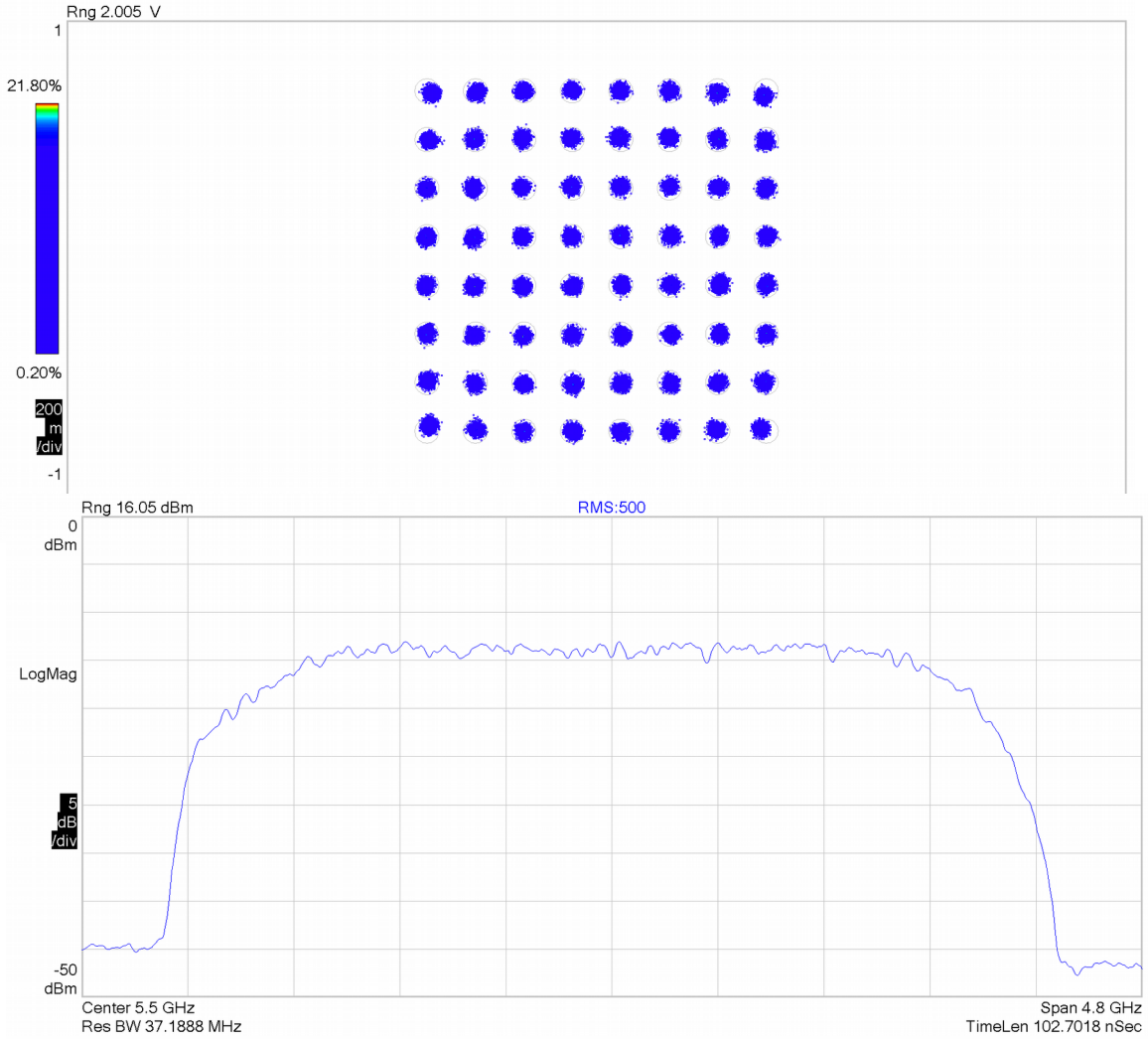
- CMOS cascode => best linearity, output power
- 3-stack n-MOSFET cascode=> best efficiency

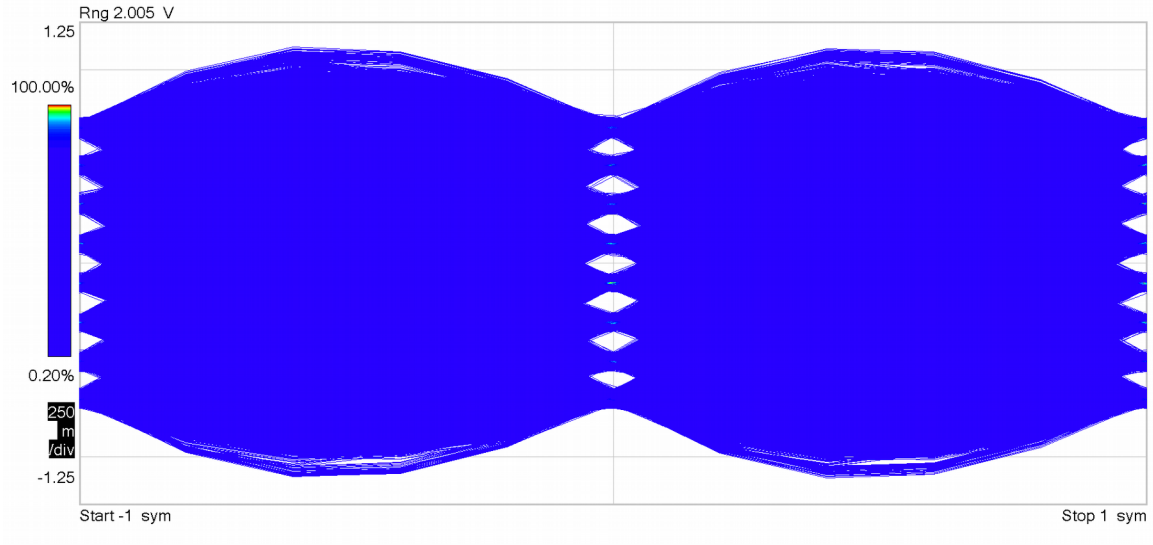
22nm cascodes: 79-GHz P_{OUT}, *PAE*, *G*



[M.S. Dadash, et al., EuMW 2018]

3-CMOS stack 64QAM, 18 Gb/s at 5.5 GHz



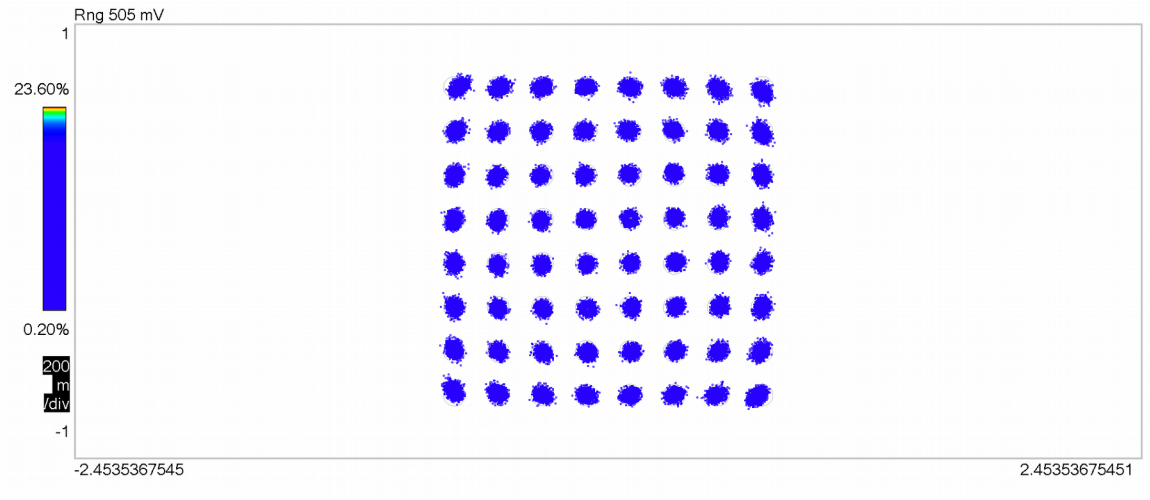


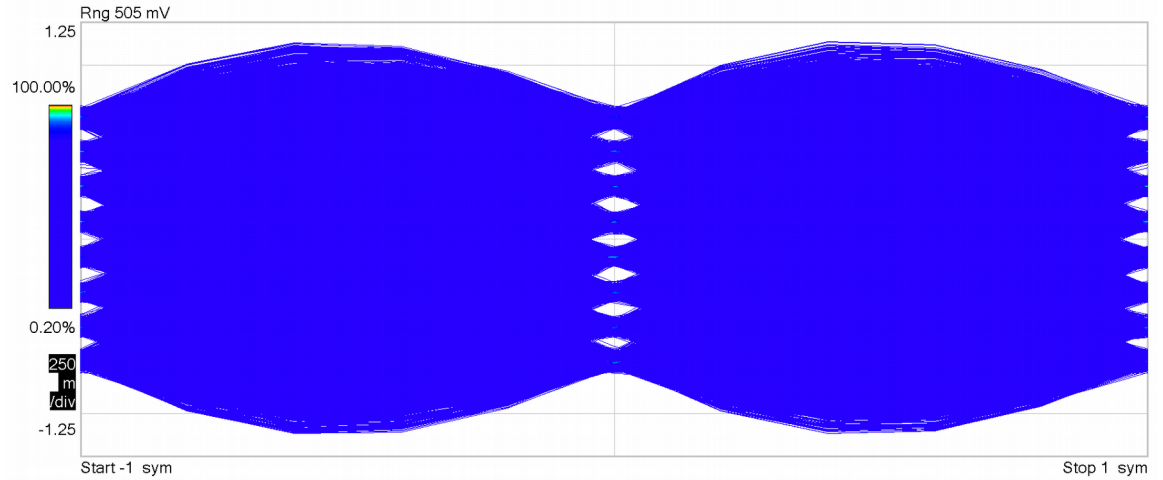
RMS:500

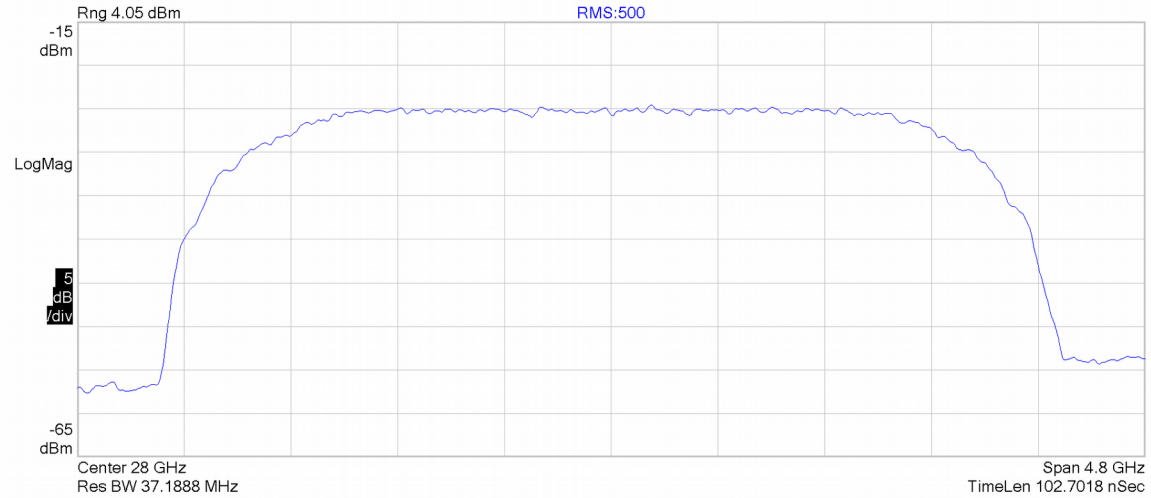
EVM	= 2.1189	%rms	5.6272	% pk at sym	181	
Mag Err	= 1.5701	%rms	-5.0168	% pk at sym	181	
Phase Err	= 2.0056	deg	-9.9991	deg pk at sym	232	
Freq Err	= -698.59	Hz				
IQ Offset	= -56.284	dB	SNR(MER)	= 29.772	dB	
Quad Err	= 132.62	mdeg	Gain Imb	= 0.019	dB	

P_{OUT} = 14 dBm, EVM = -33.6 dB

3-CMOS stack 64QAM, 18 Gb/s at 28 GHz





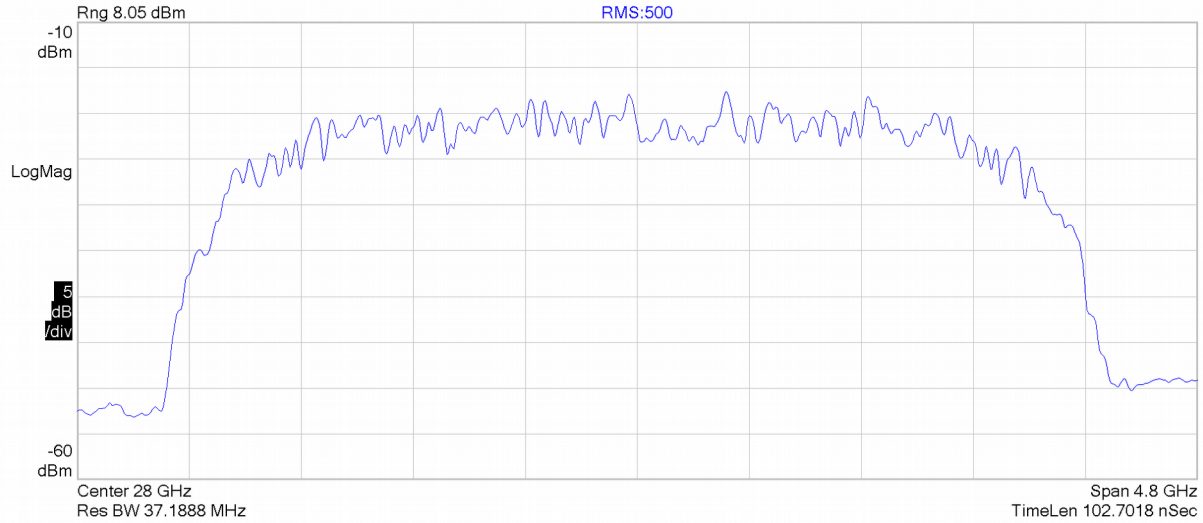


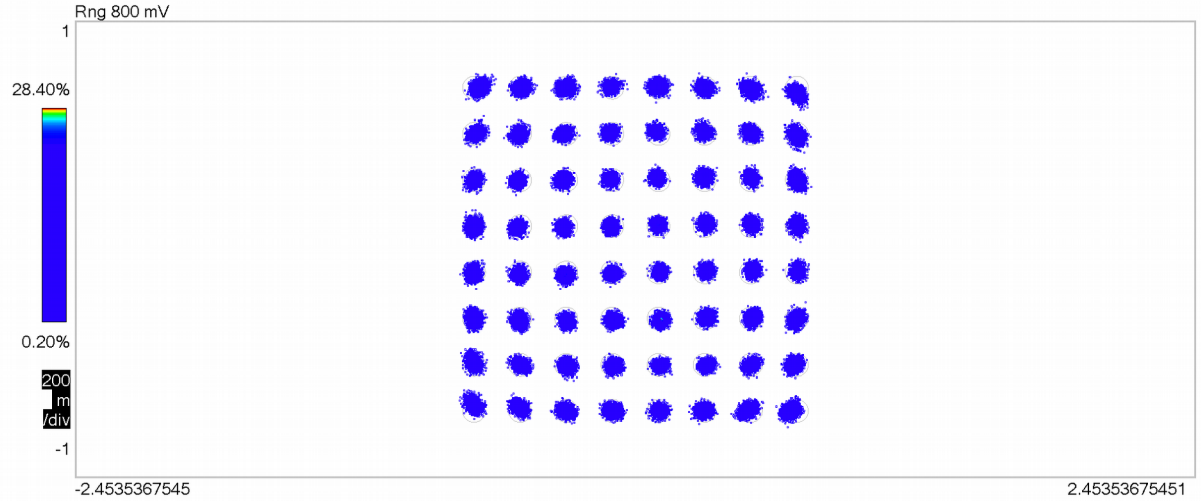
RMS:500

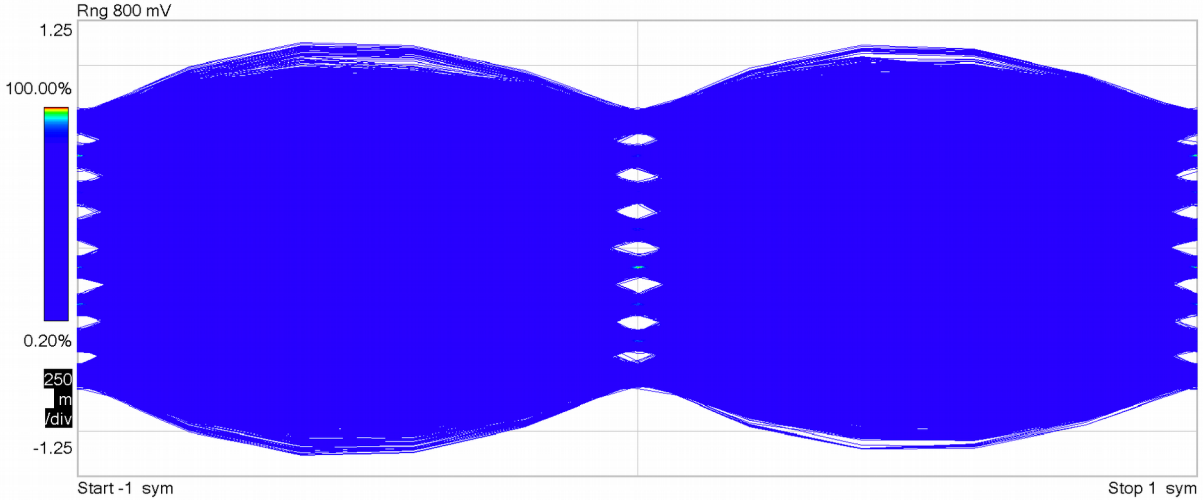
EVM	=	2.4051	%rms	8.2064	% pk	at	sym	111
Mag Err	=	1.5306	%rms	4.5496	% pk	at	sym	163
Phase Err	=	2.3267	deg	11.798	deg pk	at	sym	149
Freq Err	=	-6.7232	kHz					
IQ Offset	=	-55.776	dB	SNR (MER)	=	28.69	dB	
Quad Err	=	139.08	mdeg	Gain Imb	=	0.028	dB	

P_{OUT} = 6 dBm, EVM = -32.4 dB

3-nMOS stack 64QAM, 18 Gb/s at 28 GHz



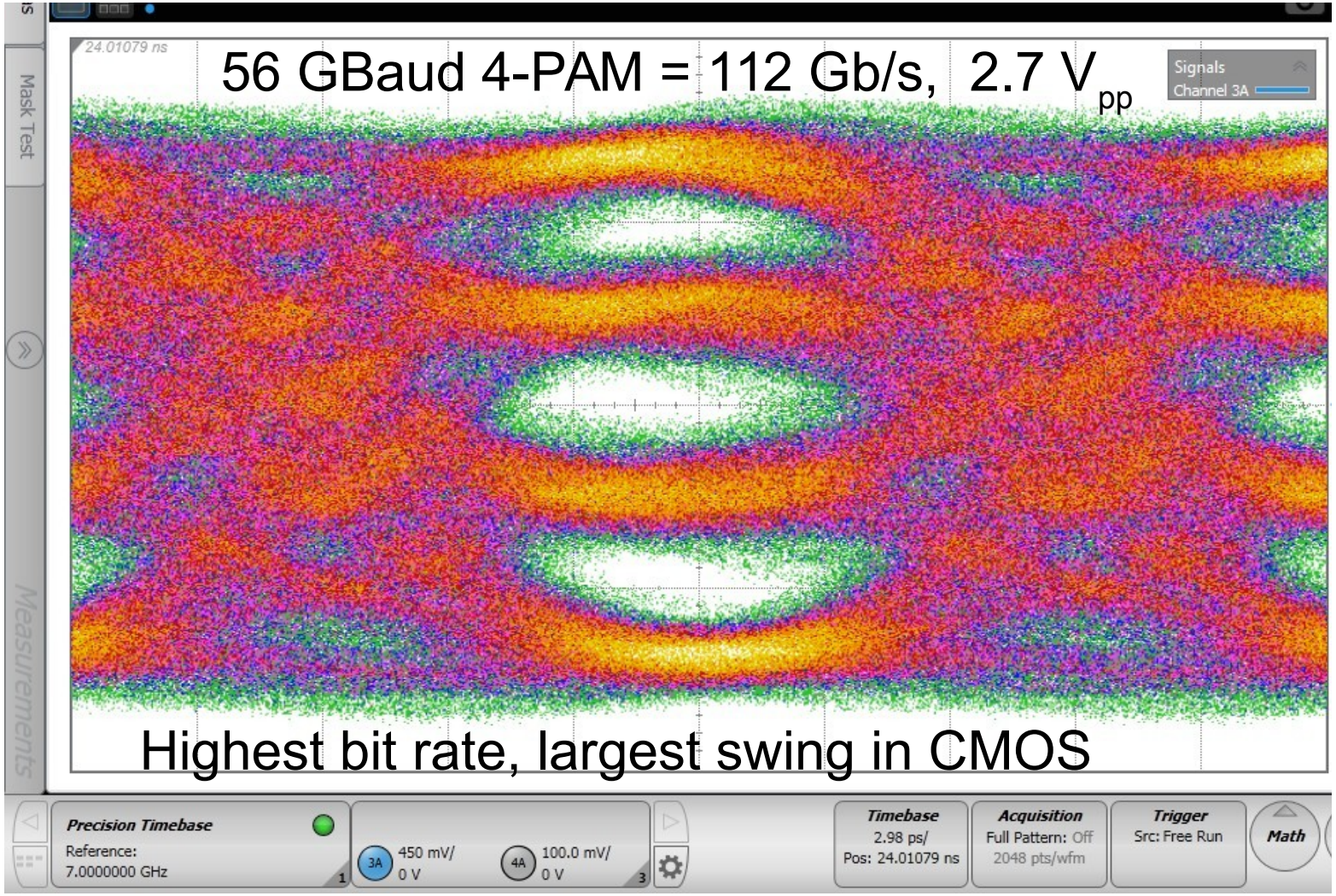




EVM	=	2.5177	%rms	6.2718	% pk	at sym	181
Mag Err	=	1.6438	%rms	4.8331	% pk	at sym	16
Phase Err	=	2.4298	deg	-10.184	deg pk	at sym	37
Freq Err	=	-5.4404	kHz				
IQ Offset	=	-55.794	dB	SNR (MER)	=	28.232	dB
Quad Err	=	142.78	mdeg	Gain Imb	=	0.026	dB

P_{OUT} = 10 dBm, EVM = -32 dB

4-nmos stack optical modulator driver performance

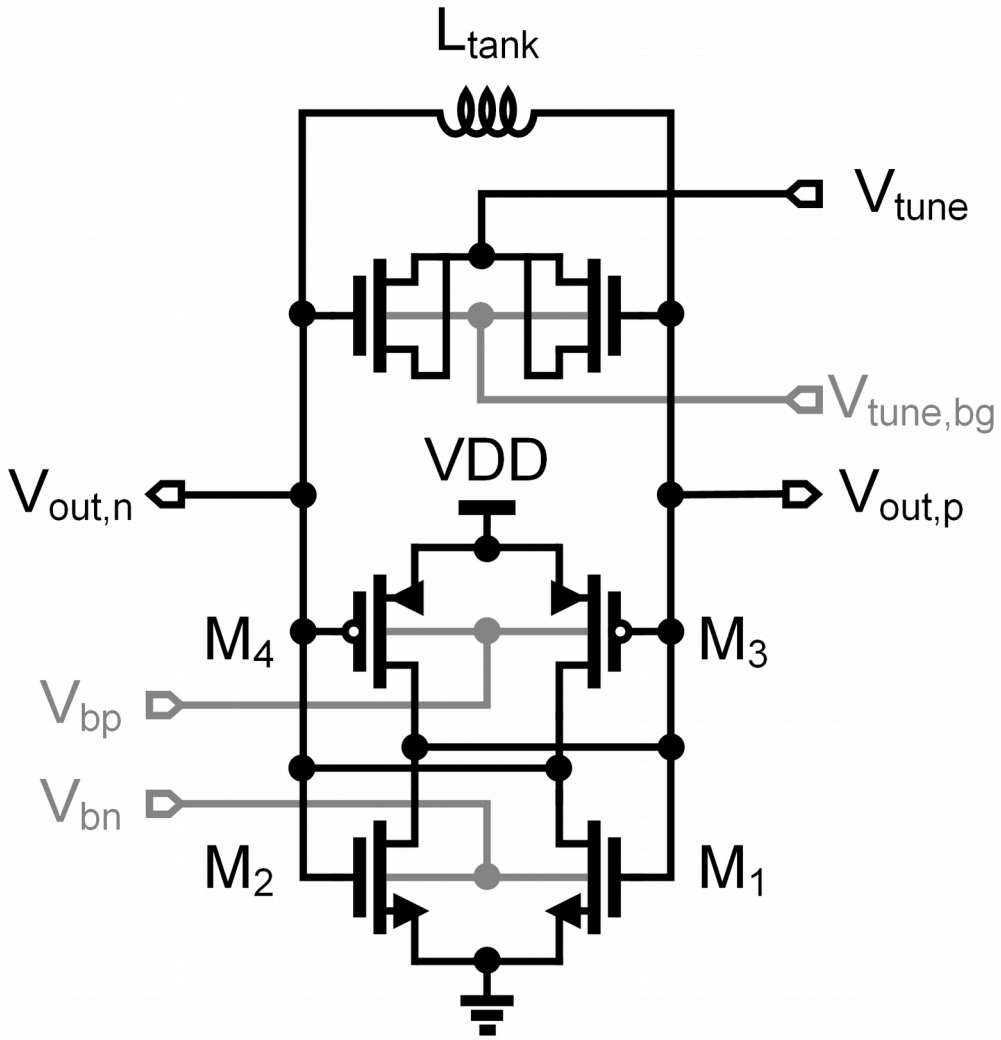


[M.S. Dadash et al., BCICTS 2018]

3-nmos stack optical modulator driver performance

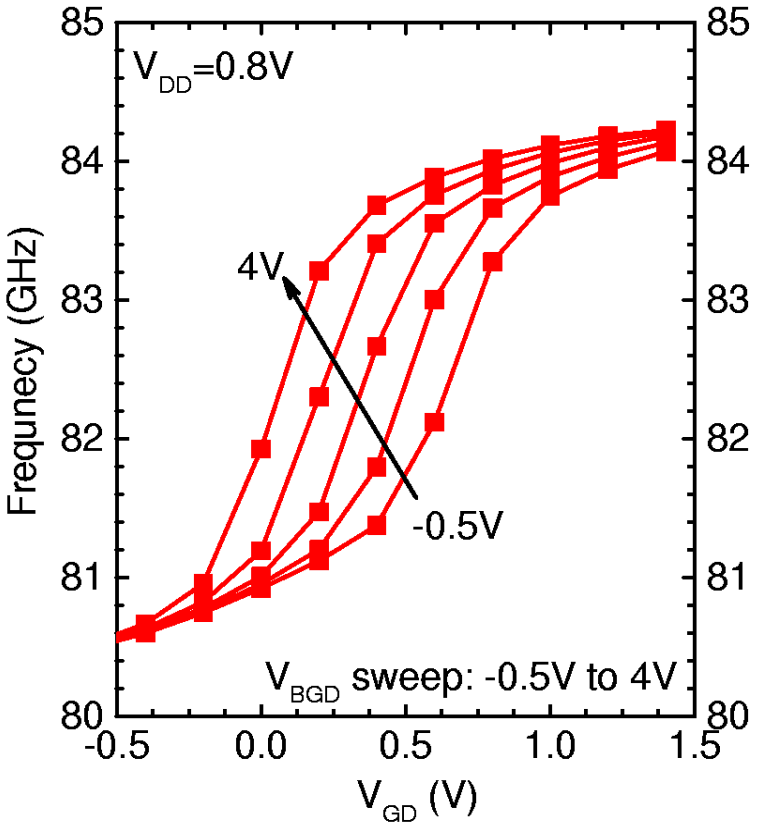
	Tech.	Topology	Data Rate (Gb/s)	Output Swing (V_{pp})	P_{dc} (mW)	Efficiency (pJ/bit)
This work	22nm CMOS	3-CMOS stack single-ended	100 (50GBaud 4-PAM)	NRZ: 4 @ 16Gb/s, 1.8 @ 56Gb/s 4-PAM: 2.1 @ 100Gb/s	230	2.3
This work	22nm CMOS	3-nMOS stack single-ended	112 (56GBaud 4-PAM)	NRZ: 2.7 @ 56Gb/s, 2.2 @ 64Gb/s 4-PAM: 2.4 @ 112Gb/s	140	1.25
ISSC 2018	10nm FinFET	CML differential	112 (56GBaud 4-PAM)	4-PAM: 0.7 @ 112Gb/s	193	1.72
ISSC 2018	14nm FinFET	stacked-CMOS differential	112 (56GBaud 4-PAM)	4-PAM: 0.5 @ 112Gb/s	230	2.06
MTT 2017	55nm SiGe BiCMOS	push-pull differential	168 (56GBaud 8-PAM)	8-PAM: 3.8 @ 168Gb/s 4-PAM: 4.8 @ 128Gb/s	820/600**	4.88/3.57**

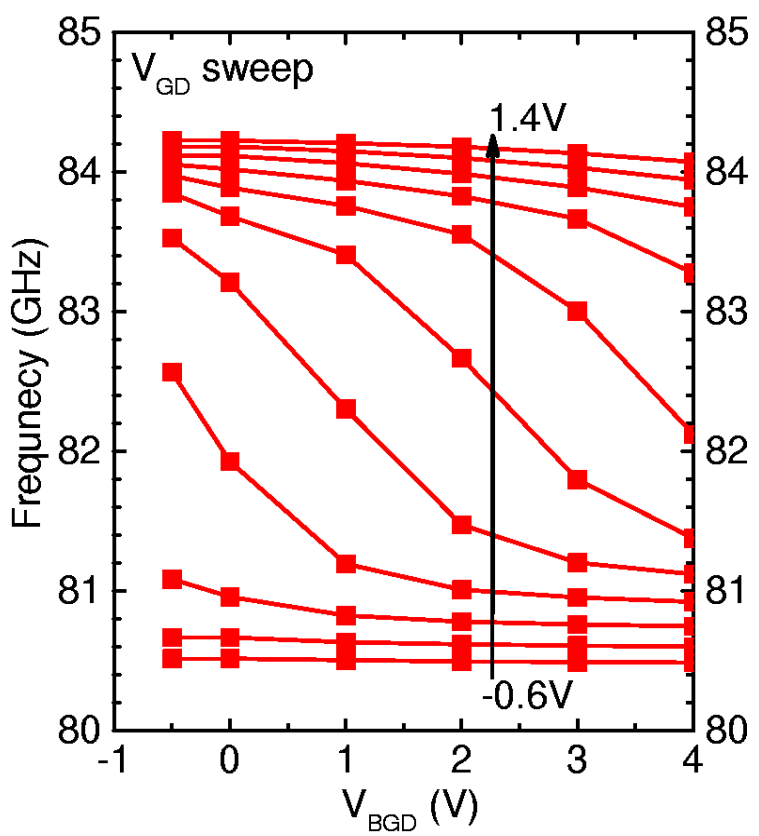
0.8V VCO with 4-terminal Varactor

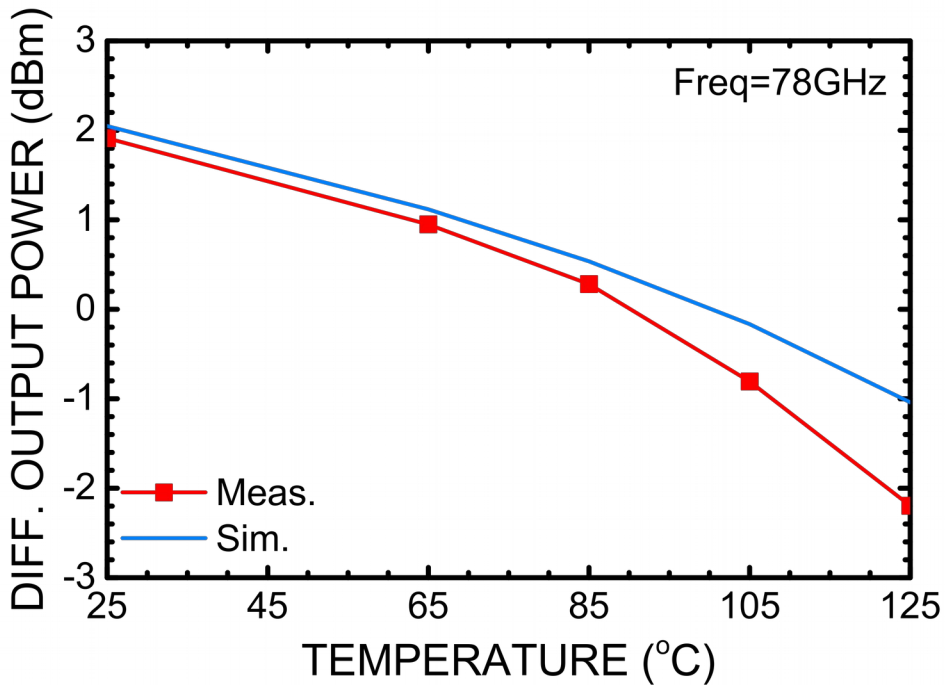


- p-MOS BG at -3 V
- n-MOS BG at 3 V
- Varactor with backgate and D/S control node
- Digital and fine control
- Allows low voltage and high voltage control of KVCO
- 1/f corner => longer gate
- Higher PN due to lower swing

Measured tuning curves vs. top and back gates



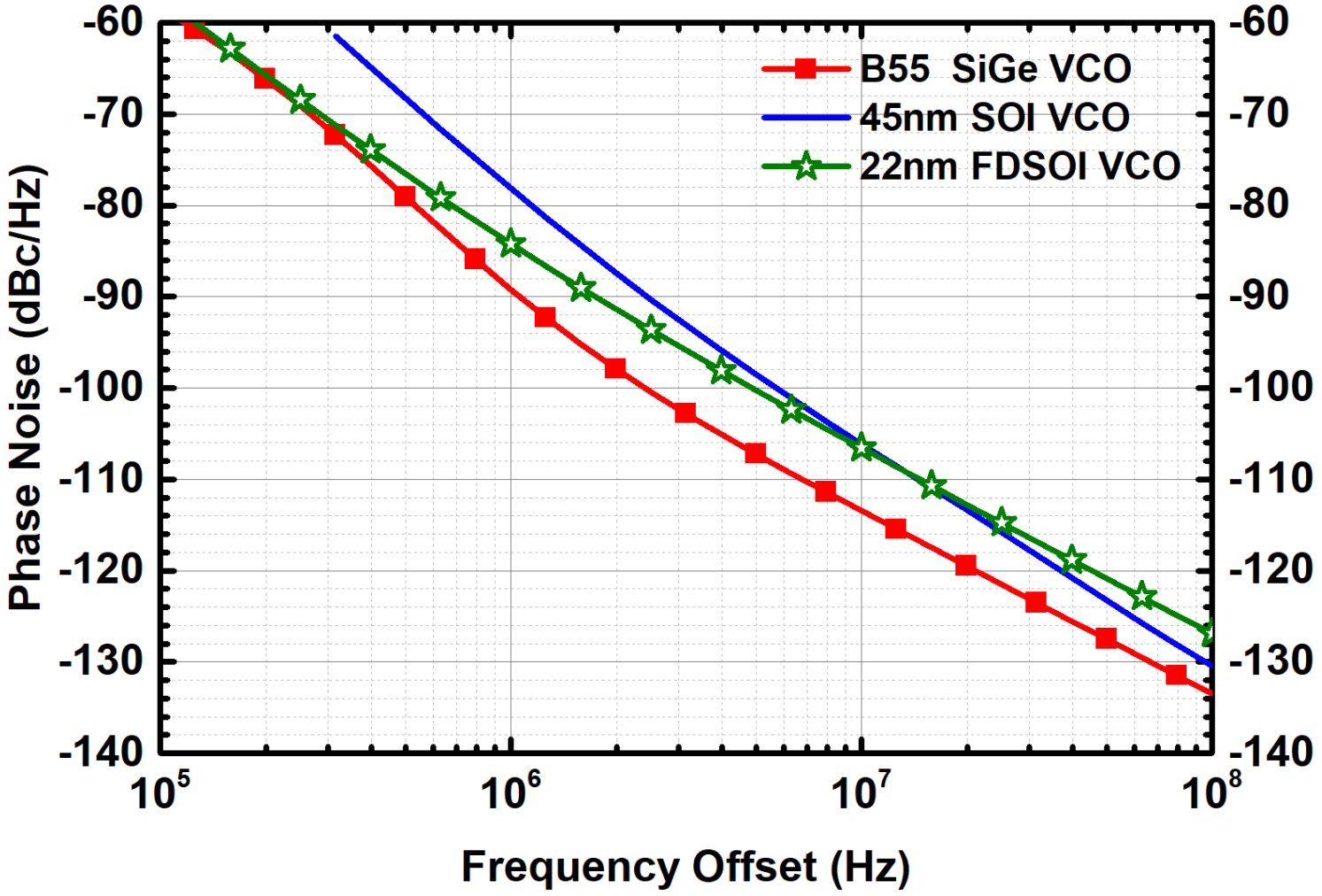




First CMOS cross-coupeld VCO above 70 GHz, P_{out} = 2 dBm (CMOS inv. buffers driving 50Ω

First 80-GHz VCO with static divider chain in CMOS at 125 °C

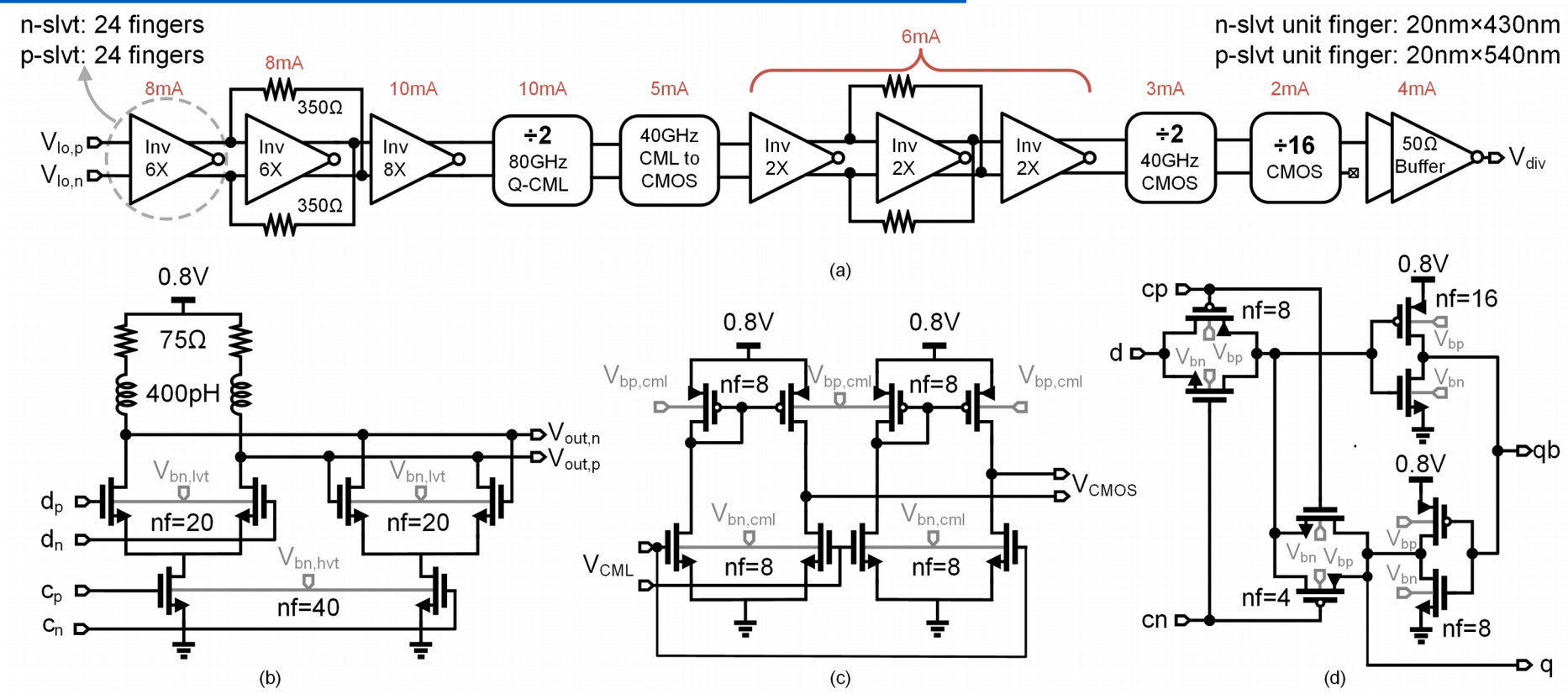
Comparison with 45nm PDSOI, SiGe HBT 60GHz VCOs



Low-power, 3-4mW P_{DC} cross-coupled VCOs for ambient sensors

[S.P. Voinigescu, et al., 2018]

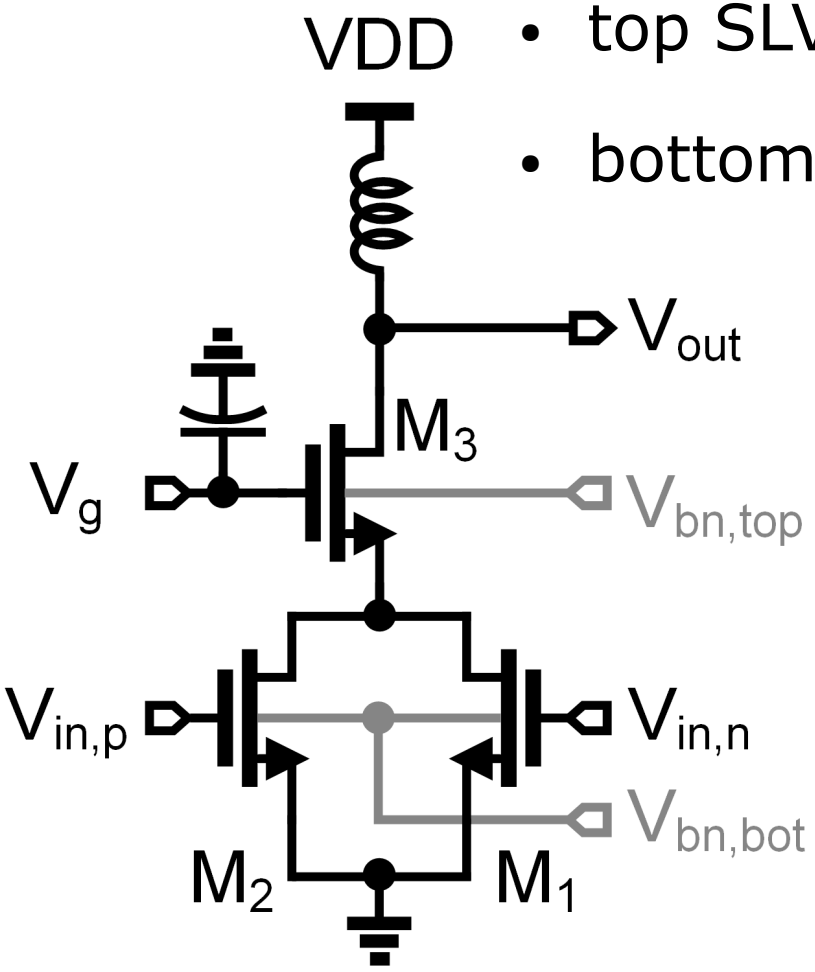
Divider/PLL/LO tree: 0.8V Quasi-CML > 80 GHz

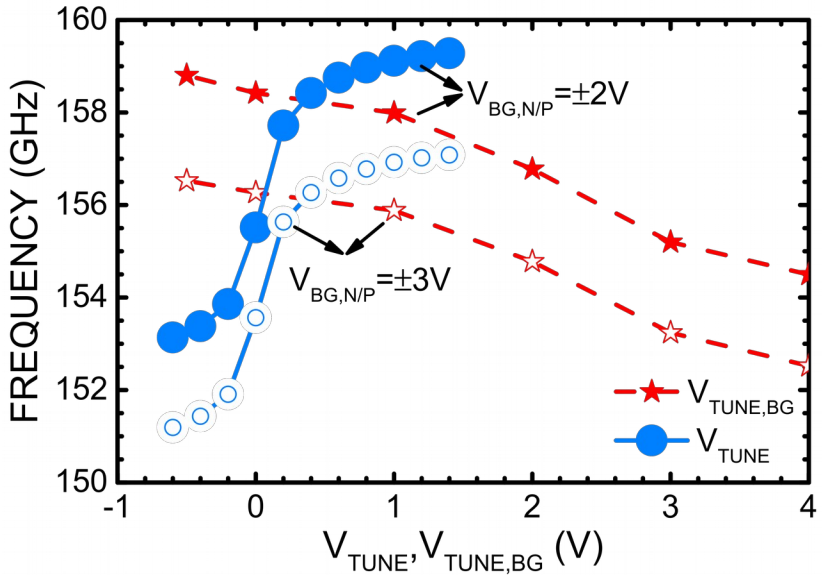


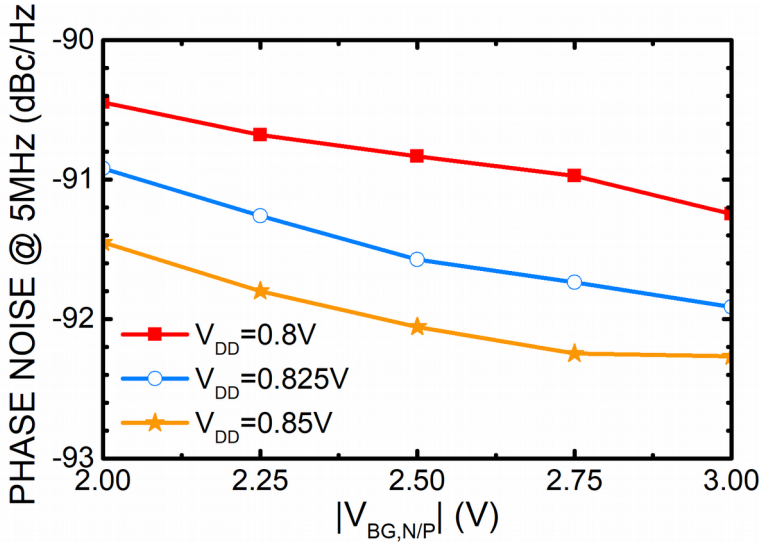
- HVT n-MOS BG at -3 V
- LVT n-MOS BG at 3 V
- $0.4V_{pp}$ quasi-CML swing
- 40-GHz CML-to-CMOS logic

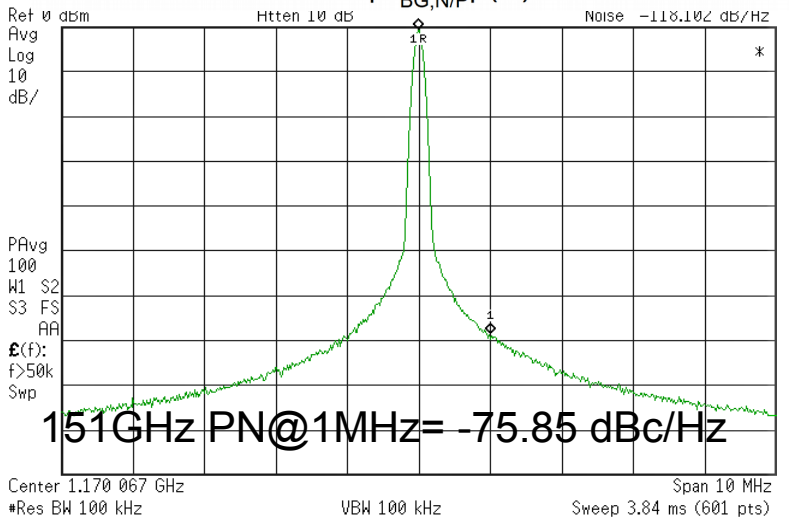
160-GHz doubler source

- top SLVT MOSFET, V_{BG}=2...3 V
- bottom HVT MOSFET V_{BG}=-0.5 V



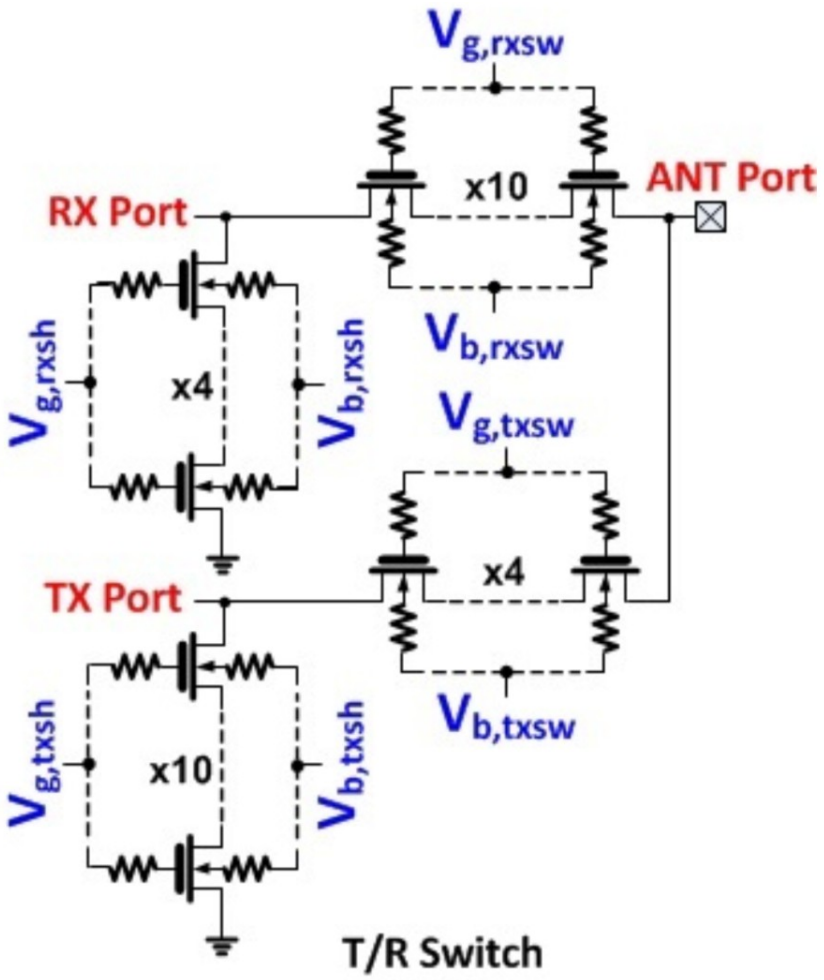






151GHz PN@1MHz= -75.85 dBc/Hz

Series-stacked antenna switches: DC-30 GHz



[Y. H. Chee et al., ISSCC 2017]

- FoM = $R_{on}C_{off}$ = 0.08-0.11 ps
- L_{min} to reduce R_{on}
- W_f >1μm to reduce $R_{on}C_{off}$
- R_G, R_{NW} (2-5 kΩ) reduce C_{off}
- 8-12 series n-FETs
- Series stacking increases P_{1dB}
- P_{1dB} > 30 dBm

[F. Zhang , GF in 22nm CMOS at SOI Consortium, April 2018]

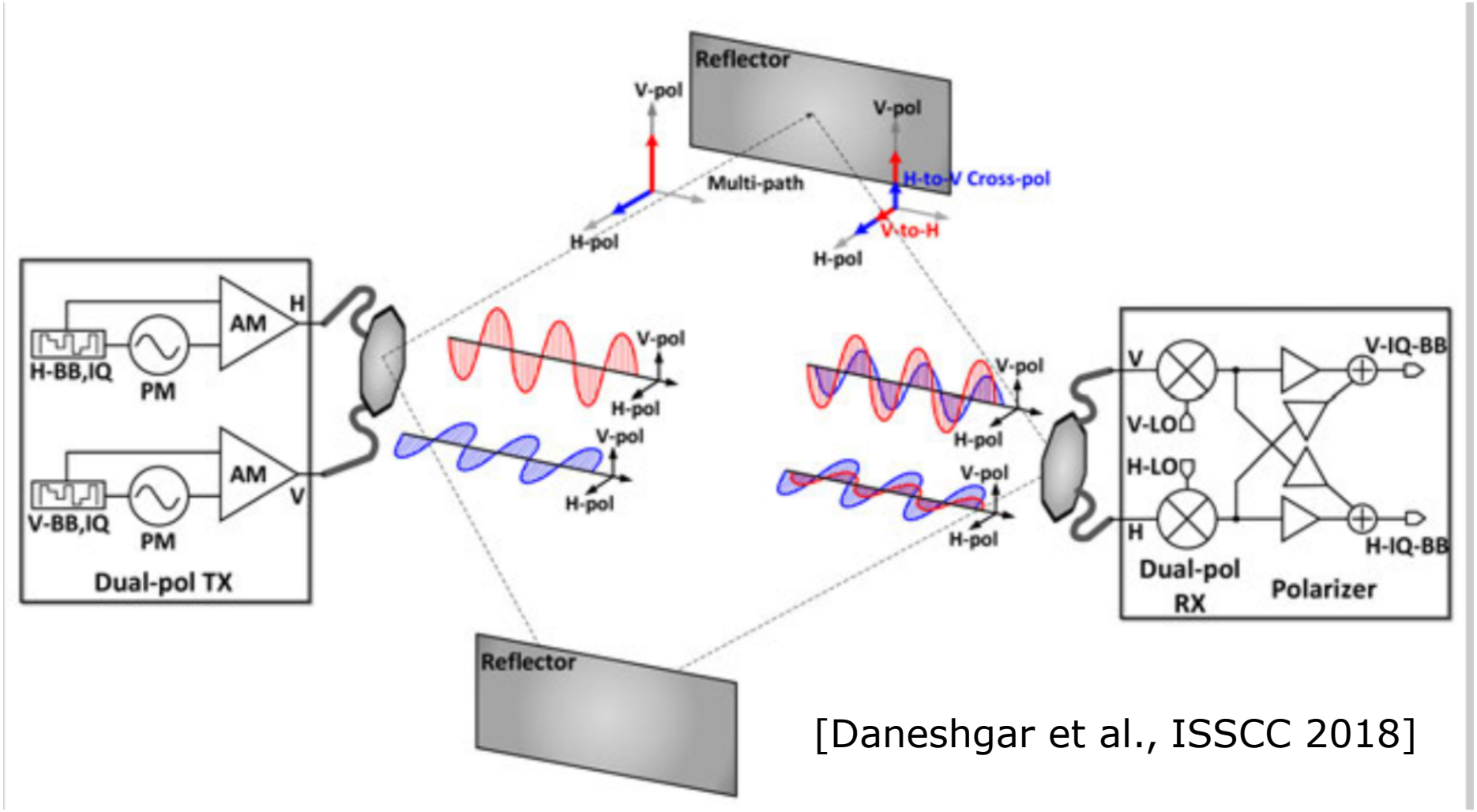
Outline

- Unique Transistor Features and Performance
- Design Fundamentals
- Specific mm-wave and high-speed circuit topologies
- **Design Examples**
- Conclusions

mm-Wave 5G User Terminals?

- We have been there before (2004-2018) at 60 GHz
- Size (antennas, #of dies) and dc power matter
- What if user's hand covers the phased array?
- Circuit topologies have not changed
- 28 GHz should be easier and lower power than 60 GHz

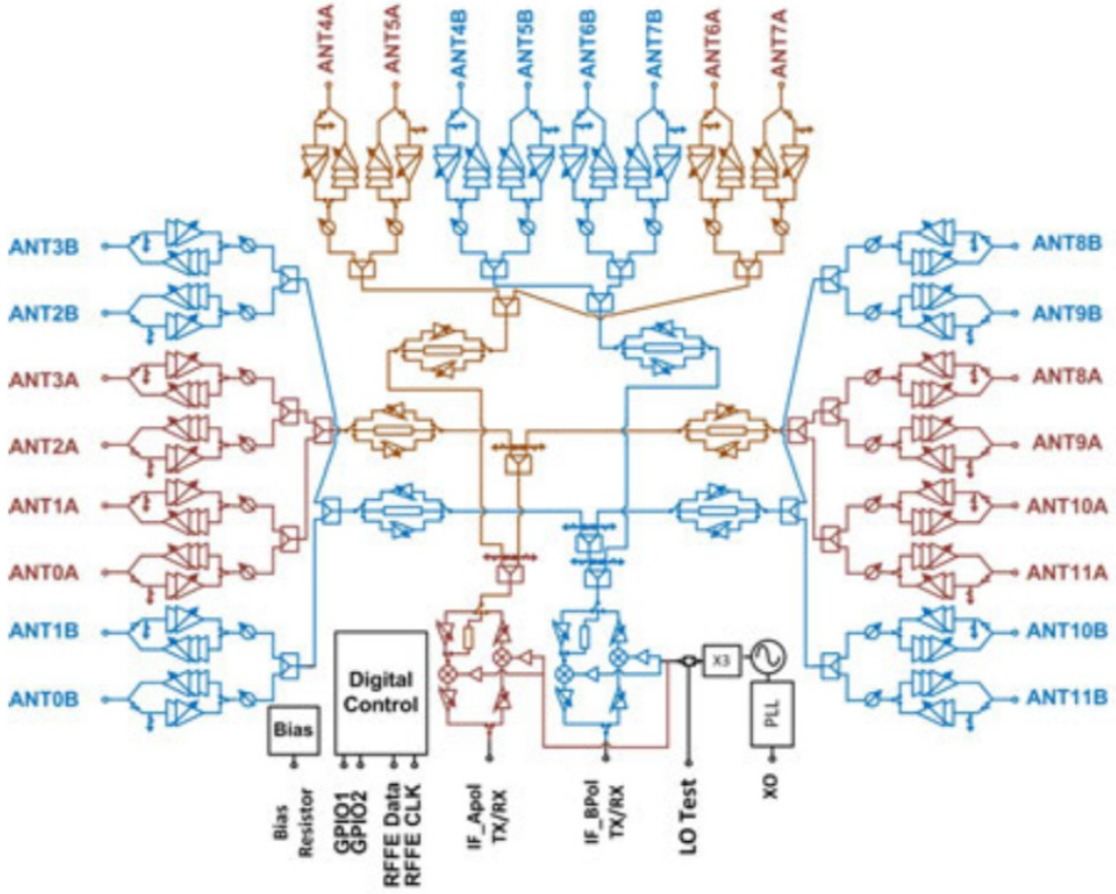
What's new? =>MIMO with dual polarization antenna



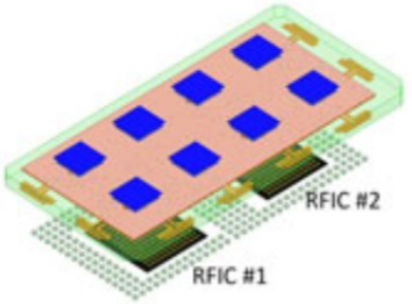
[Daneshgar et al., ISSCC 2018]

28GHz phased-array transceiver in 28nm RFCMOS

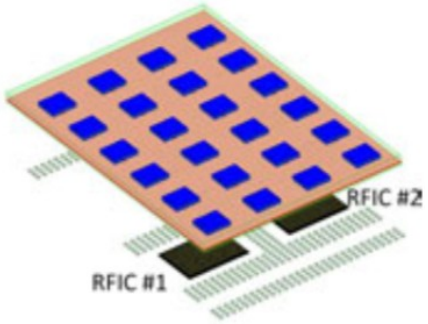
[J.D. Dunworth et al., ISSCC 2018]



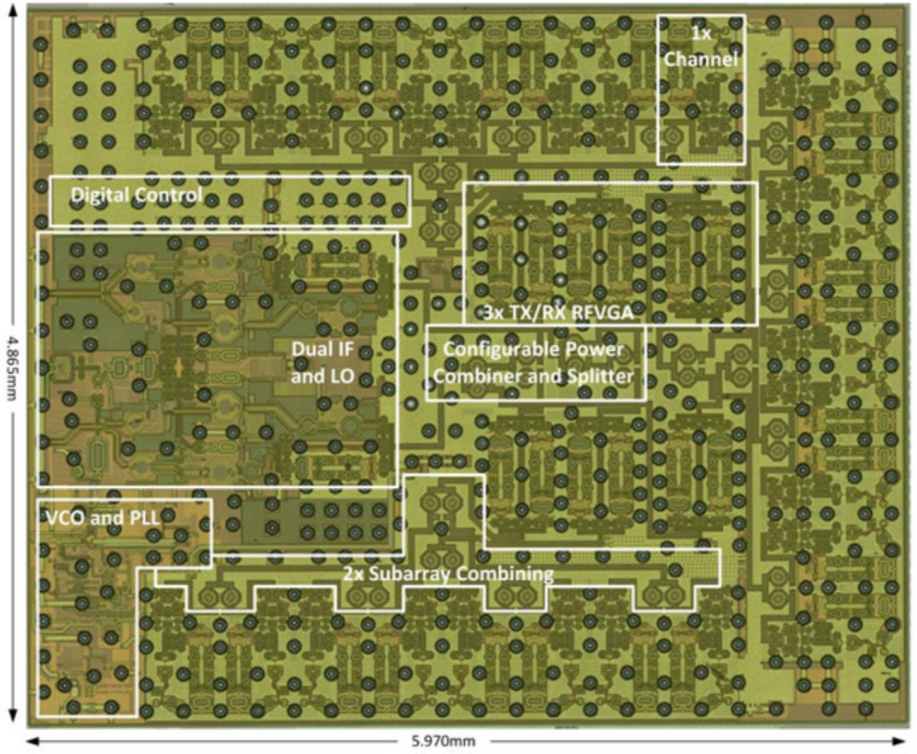
Architecture of 1 RFIC with LEFT, TOP and RIGHT subarrays for A and B polarizations



Flip Chip BGA UE Antenna Module with selectable patch and dipole arrays

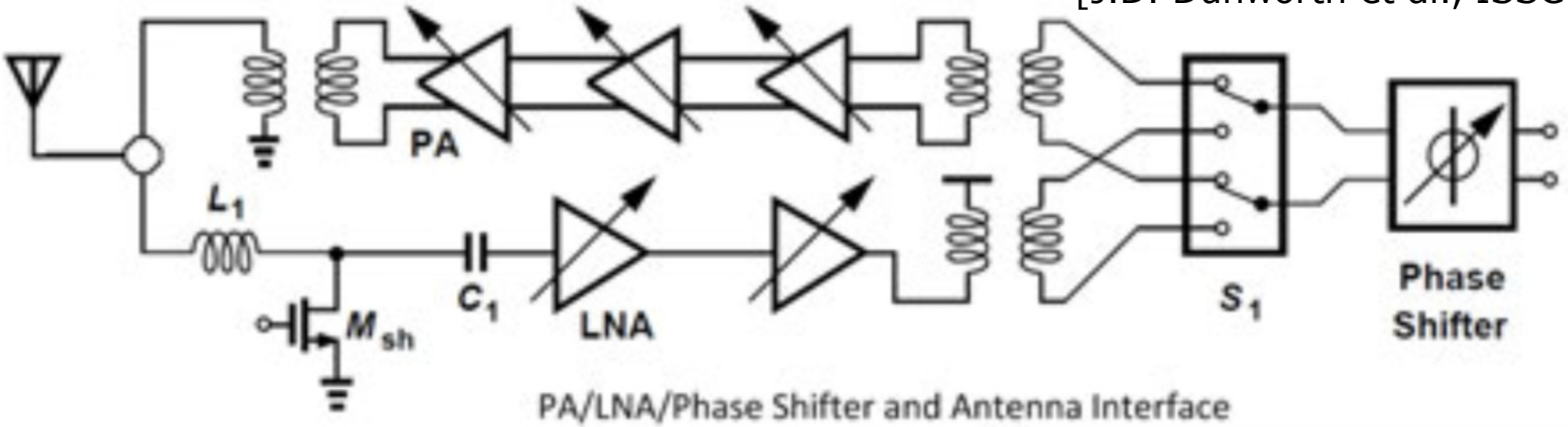


Base Station Antenna Tile with 4x4 Active Patch Array and 2x4 dummies



Bidirectional transceiver lane block diagram

[J.D. Dunworth et al., ISSCC 2018]



- 4-element transceiver phased array for mobile terminals
- MIMO with dual polarization antennas
- 24-element transceiver phased array for base station
- Linear upconverter and transceiver requires backoff => NOT efficient

Comparison of 28GHz phased-array transceivers

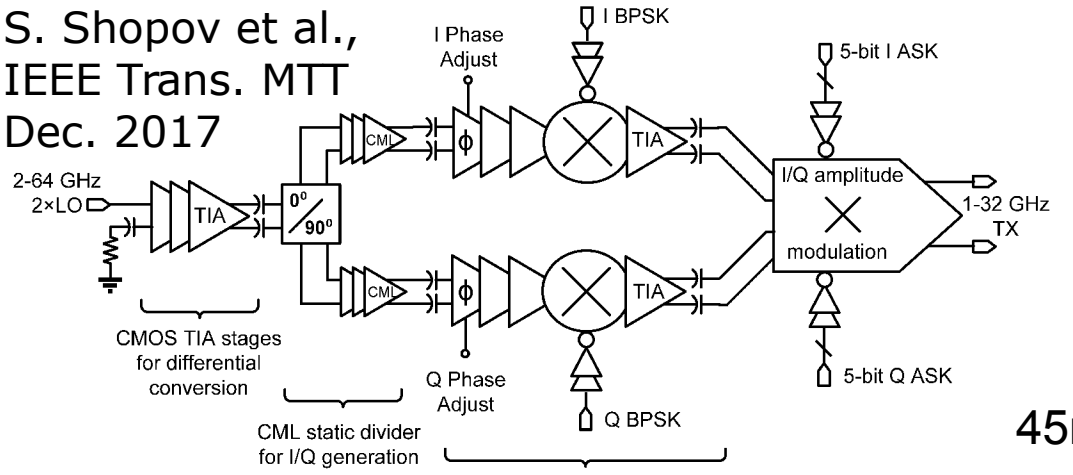
Parameter	This Work	[2]RFIC17	[3]ISSCC17	[4]IMS17	[5]RFIC17
Technology	28nm LP-RF CMOS 1P7M	28nm LP CMOS 1P7M	0.13um SiGe BiCMOS	0.18um SiGe BiCMOS	0.13um SiGe BiCMOS
Simultaneous Polarizations per IC	2	1	2	1	1
Front end channels per IC	24	8	32	4	4
TX Input / RX output interface	6.5GHz IF	Analog IQ BB	3GHz IF	RF	RF
Phase Shifter Resolution	3 bit	3 bit	5 bit	6 bit	5 bit
RF 3dB BW (GHz)	7.5 (TX), 5.5 (RX)	2.2	1.5	7 (TX), 6(RX)	4
TX Gain (dB)	34-44	50-52 (4 patches)	24-32	12	9.4-14.3
TX Psat (dBm)	>14	10.5	16	-	>12.5
TX OP1dB (dBm)	>12	9.5	13.5	10.5	>5.5
TX 64QAM Pout (dBm)	6	3	-	2.5	-
TX 64QAM PAE	7.5%	3%	-	-	-
TX Total Power (W)	0.36 (4xCH)	0.416 (4xCH)	4.6	0.8	1.08
TX Power per Channel (mW)	90	104	287.5	200	270
RX Gain (dB)	32-34dB (4xCH max)	49-50 (4 patches)	28-34	18	8.7 to 11.5
LNA NF w/SW & PS (dB)	3.8-4.4	5.6	6.0-6.9	4.6	4.5-6.9
RX NF (dB)	4.4-4.7	6.7	-	4.6	4.5-6.9
RX Total Power per IC (W)	0.167 (4xCH)	0.291 (4xCH 100MHz BW)	3.3	0.42	0.68
RX Power per channel (mW)	42	73	206	105	170
Die Size (mm x mm)	4.65 x 5.97	2.6 x 2.8	10.5 x 15.8	2.5 x 4.7	2.93 x 2.35
Die Size per channel (mm^2)	1.16	0.91	5.18	2.94	1.72

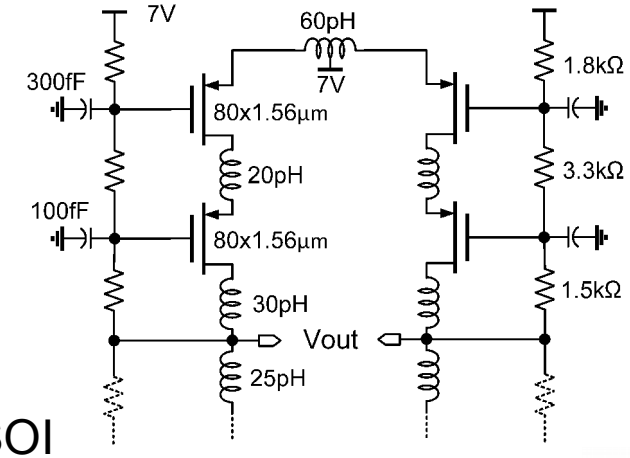
28GHz and 60GHz phased-array elements suffer from poor PAE (<10%) and low P_{sat} = 4..6 dBm

[J.D. Dunworth et al., ISSCC 2018]

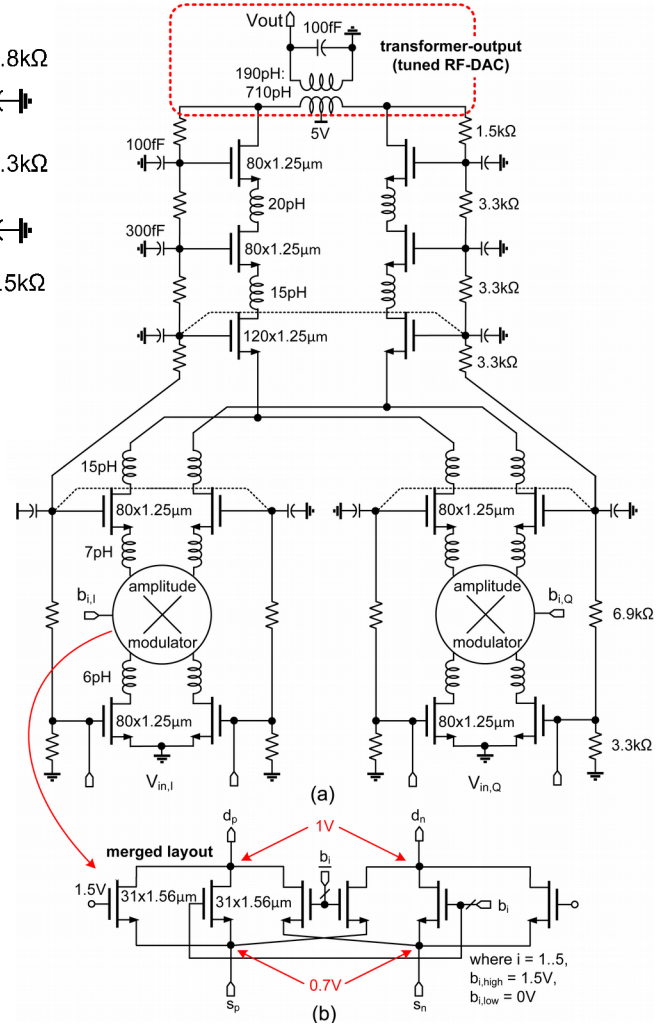
IQ-Power DAC 1-32GHz, 22-32GHz, 18dBm transmitters

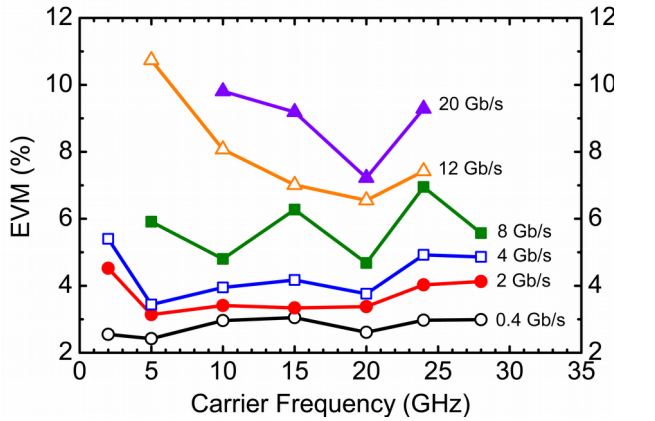
S. Shopov et al.,
IEEE Trans. MTT
Dec. 2017

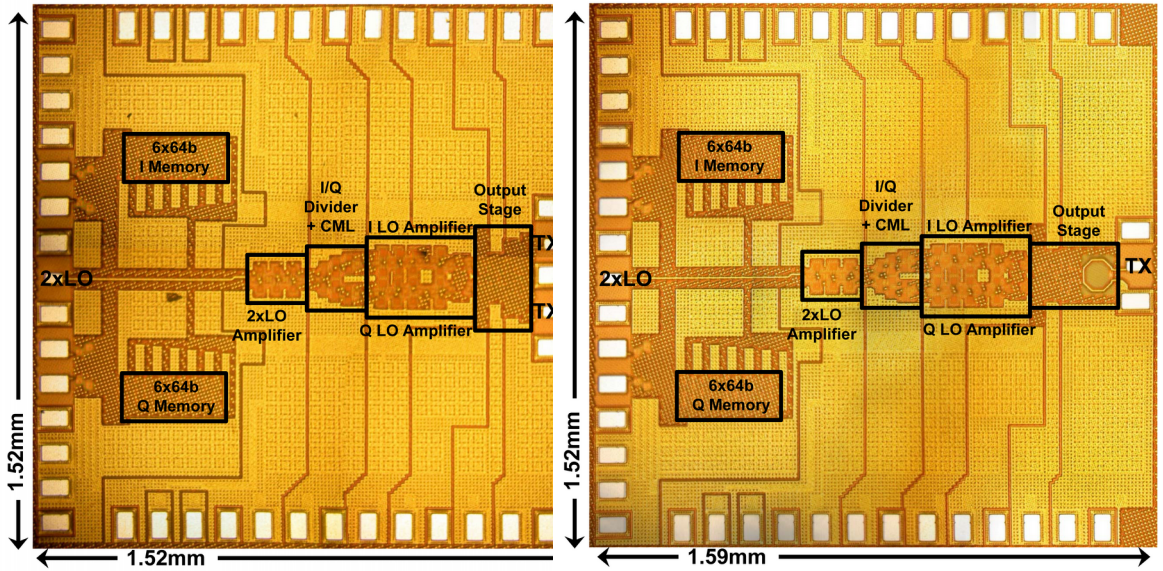




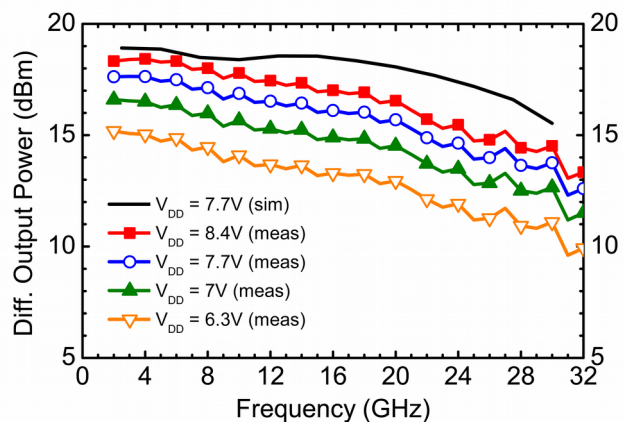
45nm PDSOI

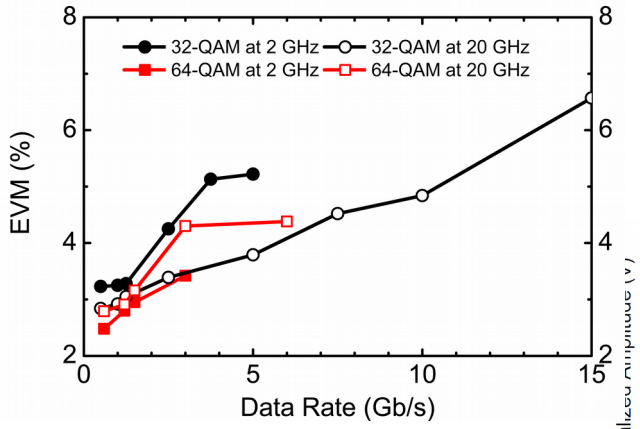


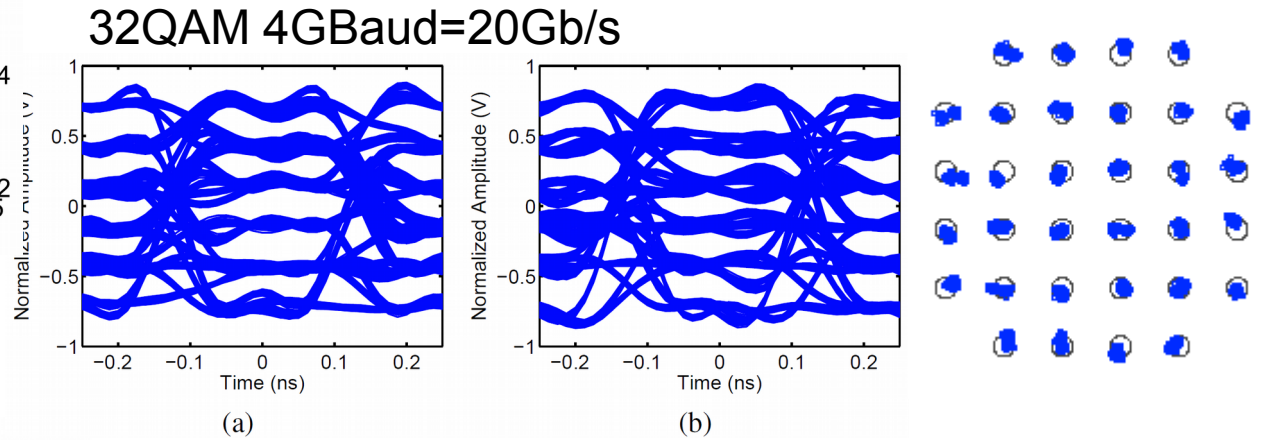


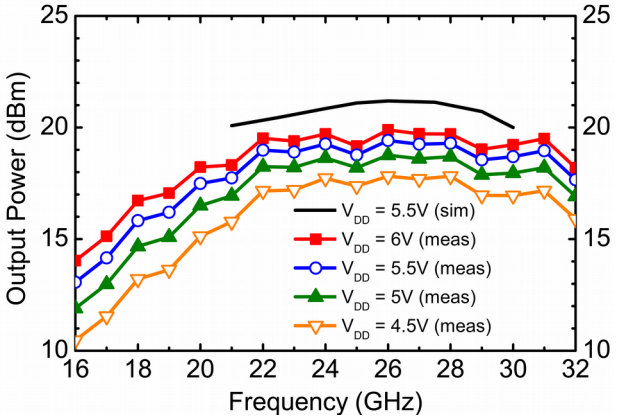


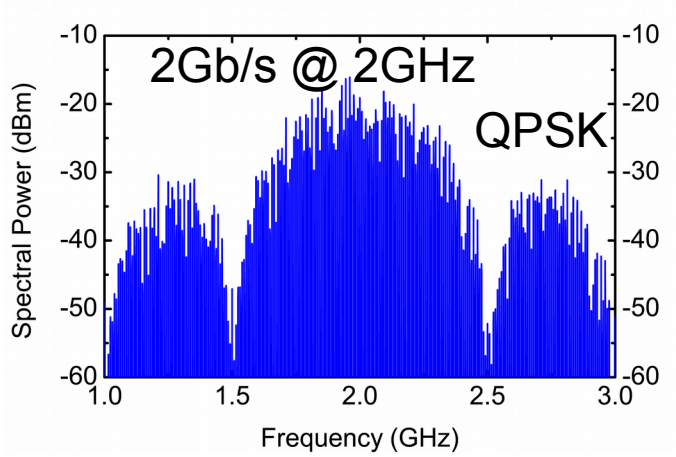
Measured perfomance

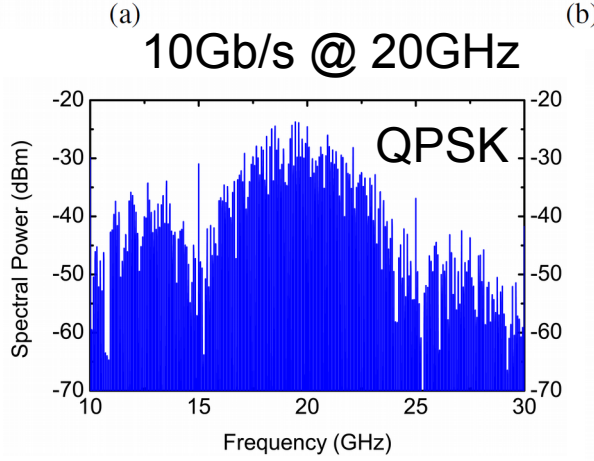


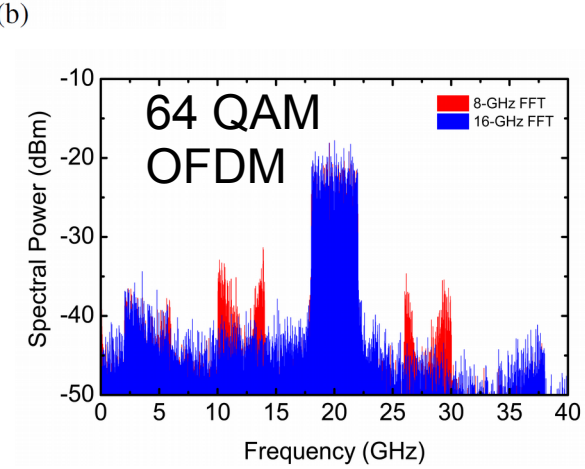










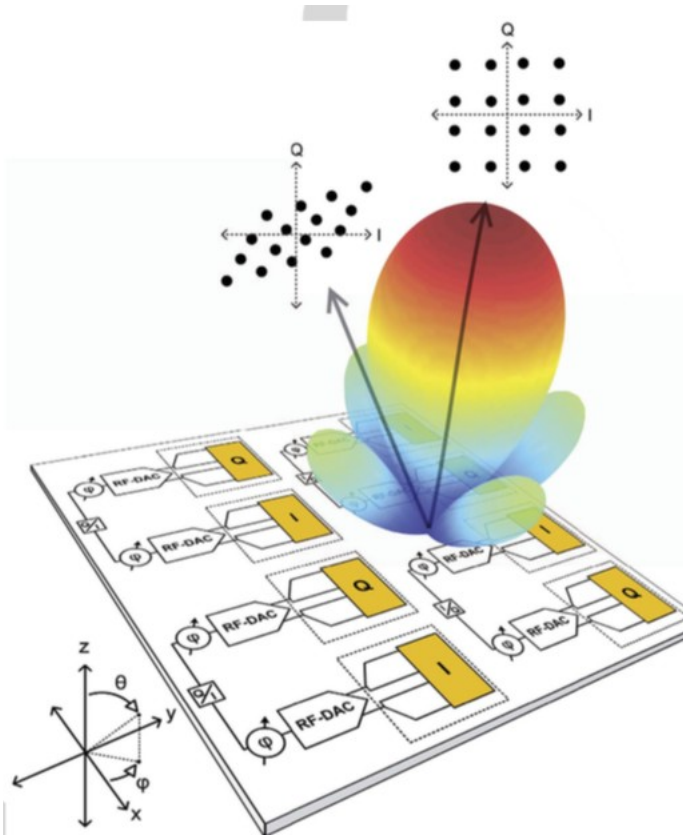


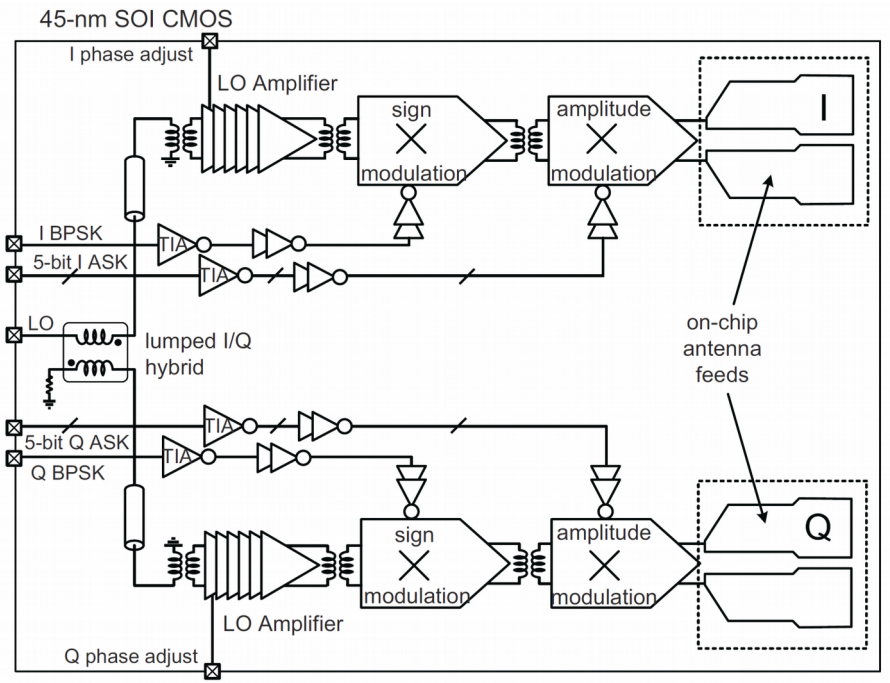
Perfomance comparison with other digital TX

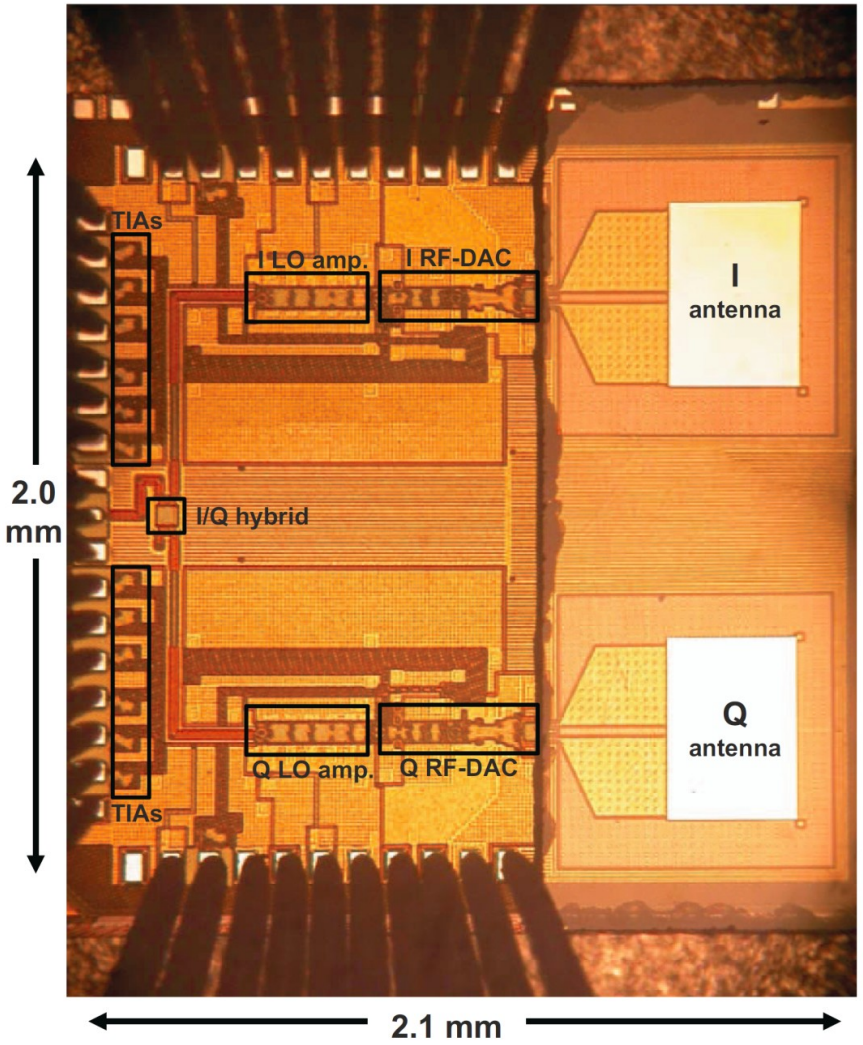
Ref.	Tech.	Freq. (GHz)	3-dB BW (GHz)	Modulation Format	Data Rate (Gb/s)	EVM (%rms)	Energy Eff. (pJ/b)	Gain (dB)	Peak P_{SAT} (dBm)	Peak PAE (%)
This work	45nm SOI CMOS	15–32	18–32	16QAM 32QAM 64QAM	26 30 12	7.9 6.9 4	24.6 29.5 --	> 25	19.9	10.3
This work	45nm SOI CMOS	1–32	1–24	16QAM 32QAM 64QAM	20 15 6	7.2 6.6 4.4	44.6 59.3 150	> 25	18.4	5.8
[9]	45nm SOI CMOS	38–49	42–47	16QAM QPSK	0.04 1.25	8 5.5	675*	7.1	21.3	16
[10]	65nm CMOS	57–64	58–62*	16QAM QPSK	6 3.5	15.5 17.8	43.3 74.3	--	9.6**	17.4
[13]	40nm CMOS	50–67	50–67	16QAM QPSK	6.7 3.3	15 9.3	6.7 14.1	20.3	10.8	--

*Estimated from information available in the paper, **Peak EIRP is 22 dBm

138GHz I/Q 6bit Power-DAC TX in 45nm PDSOI

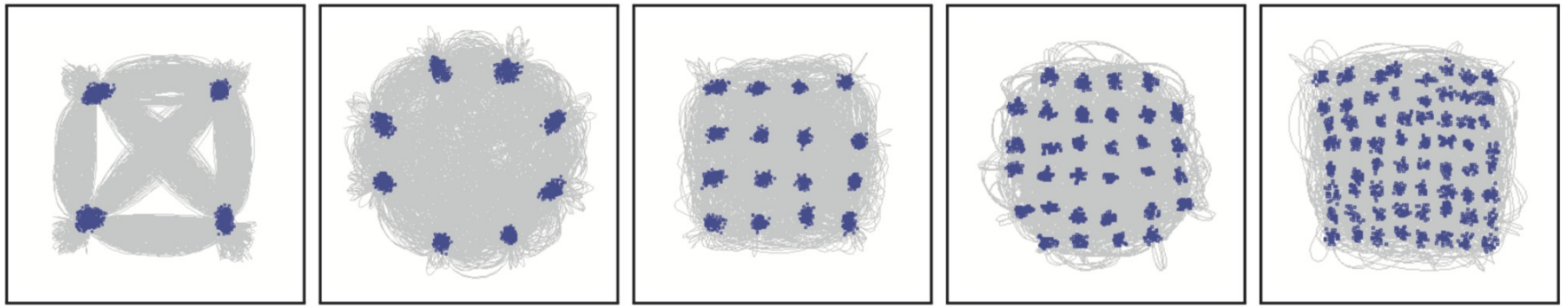




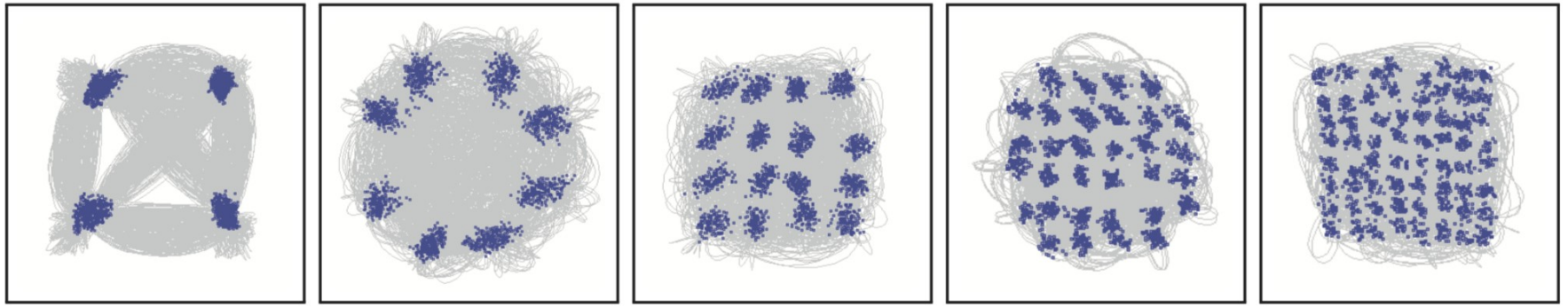


[S. Shopov et al., ESSCIRC 2017]

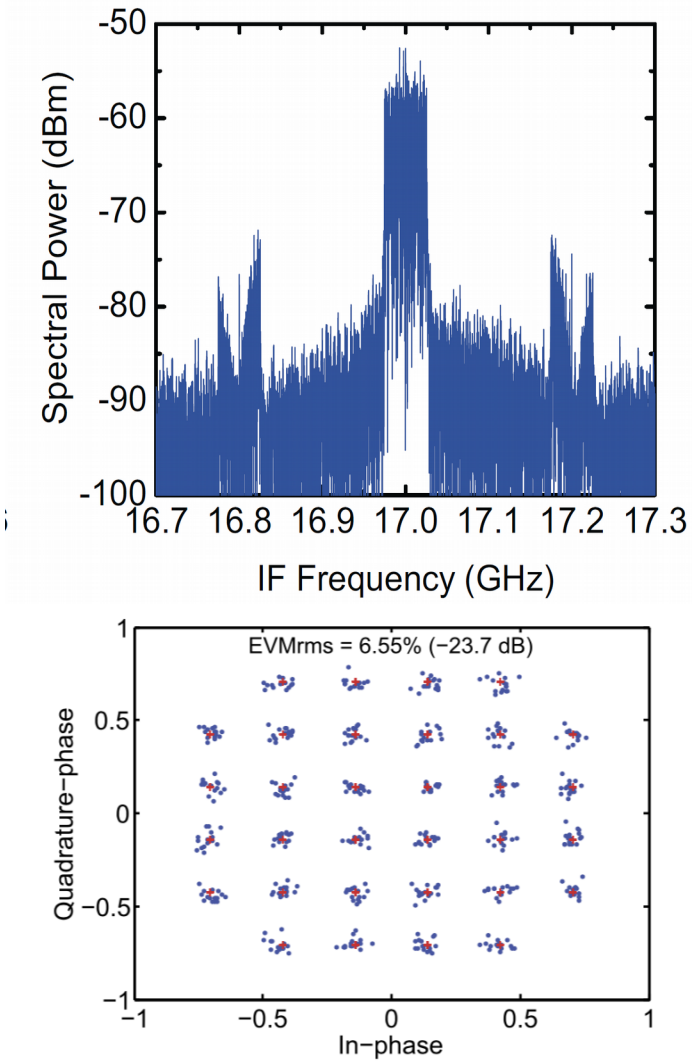
Measured 138GHz constellations and OFDM spectra



1 Gb/s, -21.7dB EVM | 1.2 Gb/s, -21.1dB EVM | 1.6 Gb/s, -20.1dB EVM | 1 Gb/s, -20.7dB EVM | 0.6 Gb/s, -21.2dB EVM

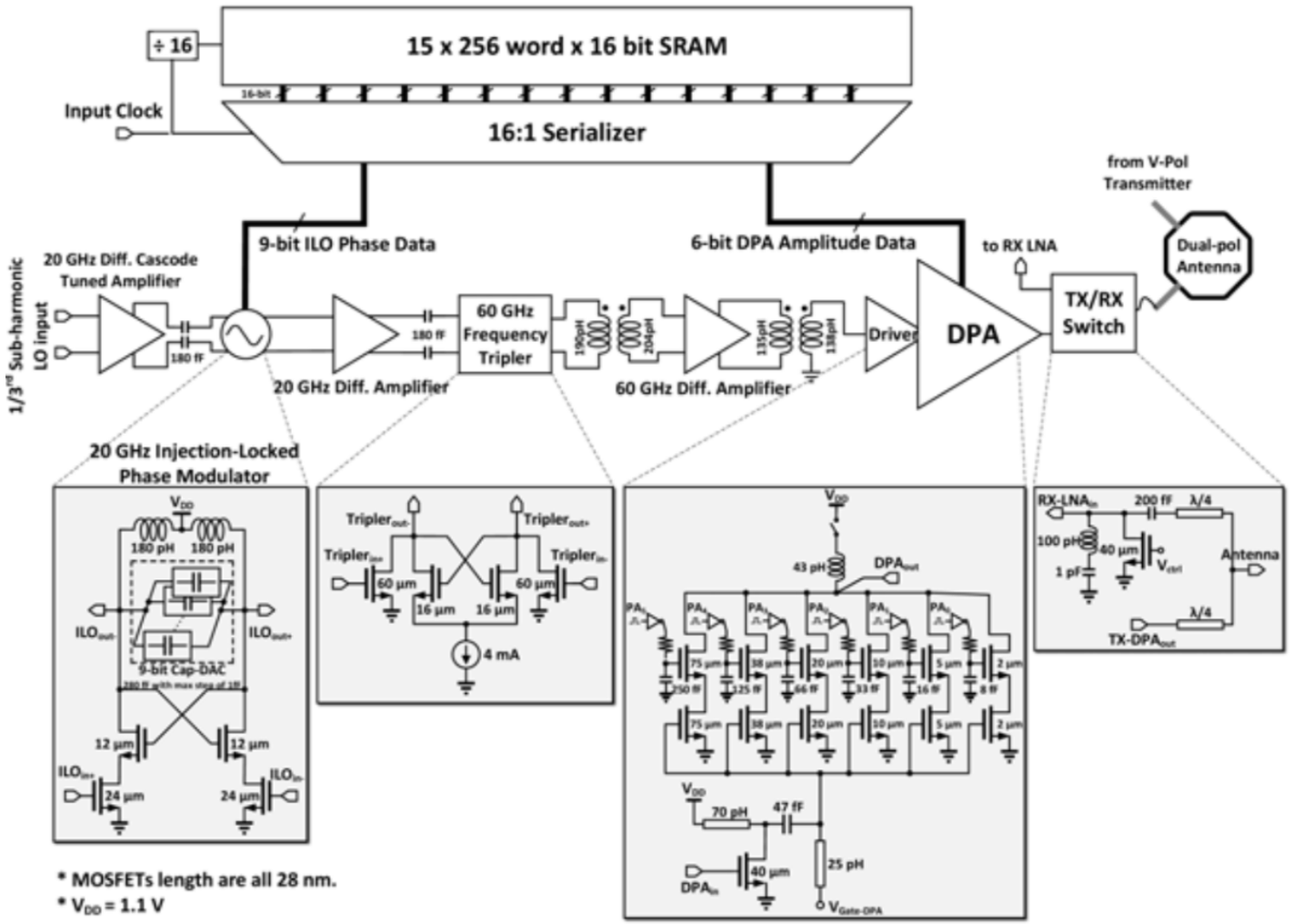


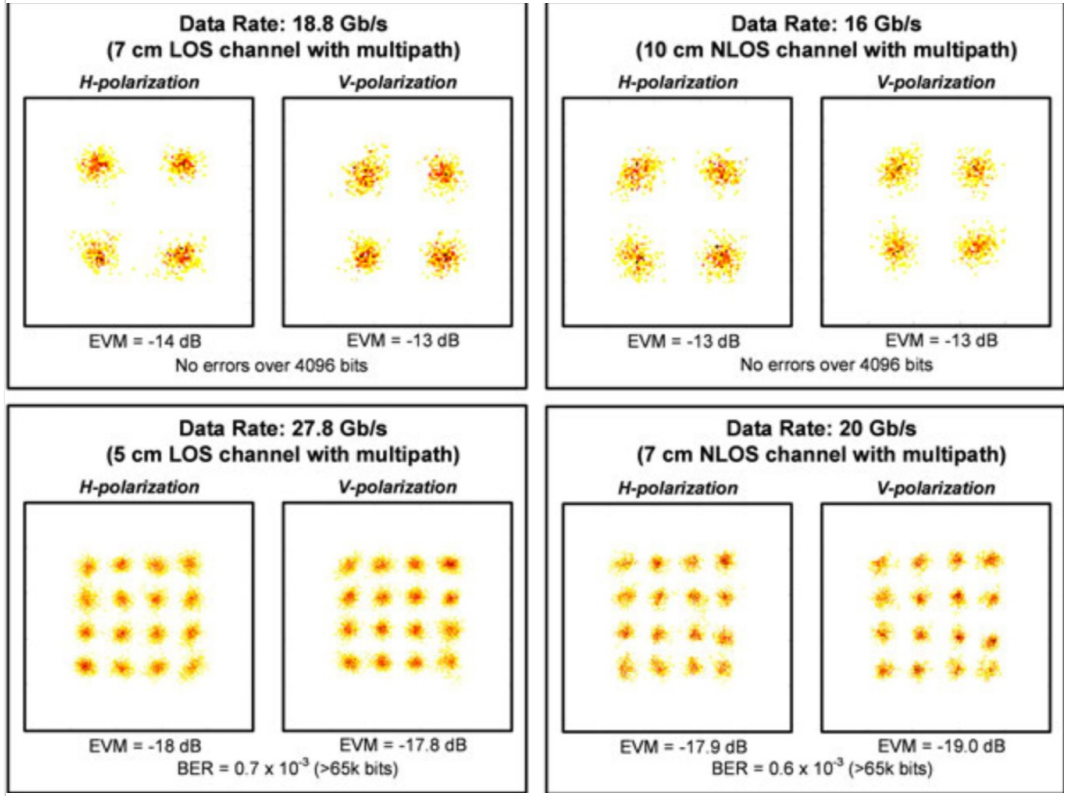
2 Gb/s, -18.0dB EVM | 3.6 Gb/s, -16.0dB EVM | 5 Gb/s, -15.9dB EVM | 4 Gb/s, -17.8dB EVM | 3.6 Gb/s, -19.7dB EVM



Distance > 15 cm limited by microscope height in on-die setup

60GHz polar digital transmitter in 28nm RFCMOS





[S. Daneshgar et al, ISSCC 2018]

60GHz transceiver comparison

Metric	This Work		[4] ISSCC'17	[5] ISSCC'16	[6] ISSCC'14	[7] ISSCC'14
Technology	28 nm CMOS		65 nm CMOS	28 nm CMOS	40 nm CMOS	65 nm CMOS
Integration	TX: Digital polar RX: Direct conv. Ant.: Wire-bond PCB		TX: Direct conv. RX: Direct conv. Ant.: Horn	TX: Direct conv. RX: Direct conv. Ant.: Package	TX: Heterodyne RX: Heterodyne Ant.: Package	TX: Direct conv. RX: Direct conv. Ant.: Horn
TX+RX Ant./Array Gain (dBi)	7 (1TX + 1RX)		28 (1TX + 1RX)	24 (4TX + 4RX)	45 (16TX+16RX)	24 (4TX + 4RX)
DC Power / element	TX + LO: 210 mW[1] RX + LO: 110 mW		TX: 169 mW RX: 139 mW	TX: 167 mW RX: 107 mW	TX: 74 mW RX: 60 mW	TX: 251 mW RX: 220 mW
Constellation	QPSK	16QAM	64QAM	16QAM	16QAM	16QAM
Data Rate (Gb/s)[2]	16	27.8	42.24	7	4.6	28.16
EVM $_{\text{wrt avg.}}$ (dB)	-12.5	-18	-21.1	-20	-19.5	-17.2
pJ / bit / element	20	11.5	7.3	39.3	29.2	16.7
Bits / symbol	4	8	6	4	4	4
Normalized Distance[3] (ND, cm)	13	5	0.35	14.1	14	0.7
pJ / bit / element / ND	1.5	2.3	20.5	2.8	2.4	26.8
Multipath Channel Measurements	Yes		No	No	Yes	No
Die Area (mm²) / element	3.9		7.2	3.9	1	2
MIMO Streams	2		1	1	1	1

[1] Including digital TX driver power at highest rate
[2] Data rate for BER < 1E-3
[3] Link distance (BER < 1E-3) normalized to antenna gain in this work (3.5 dBi averaged over beam-width)

P_{sat} < 5 dBm per element

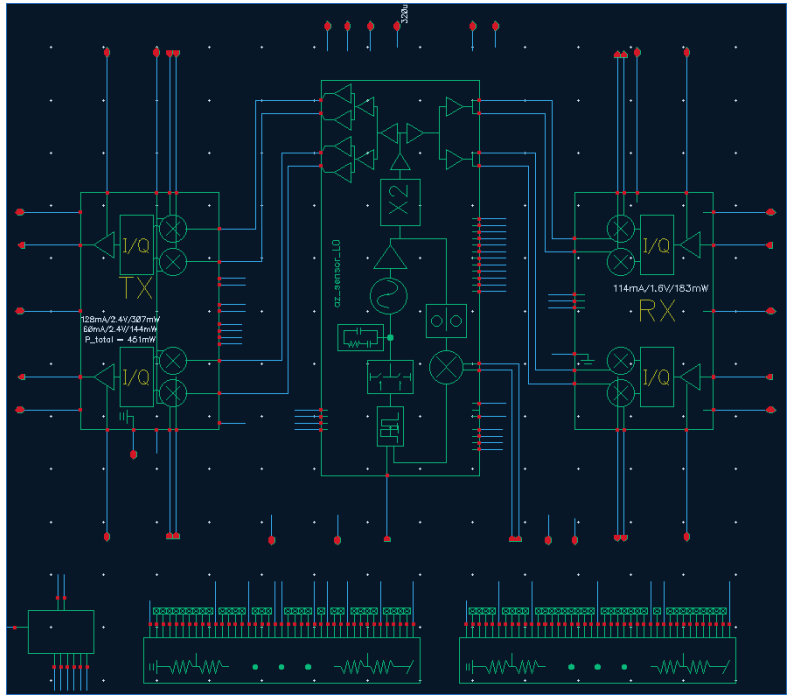
No amount of DPD

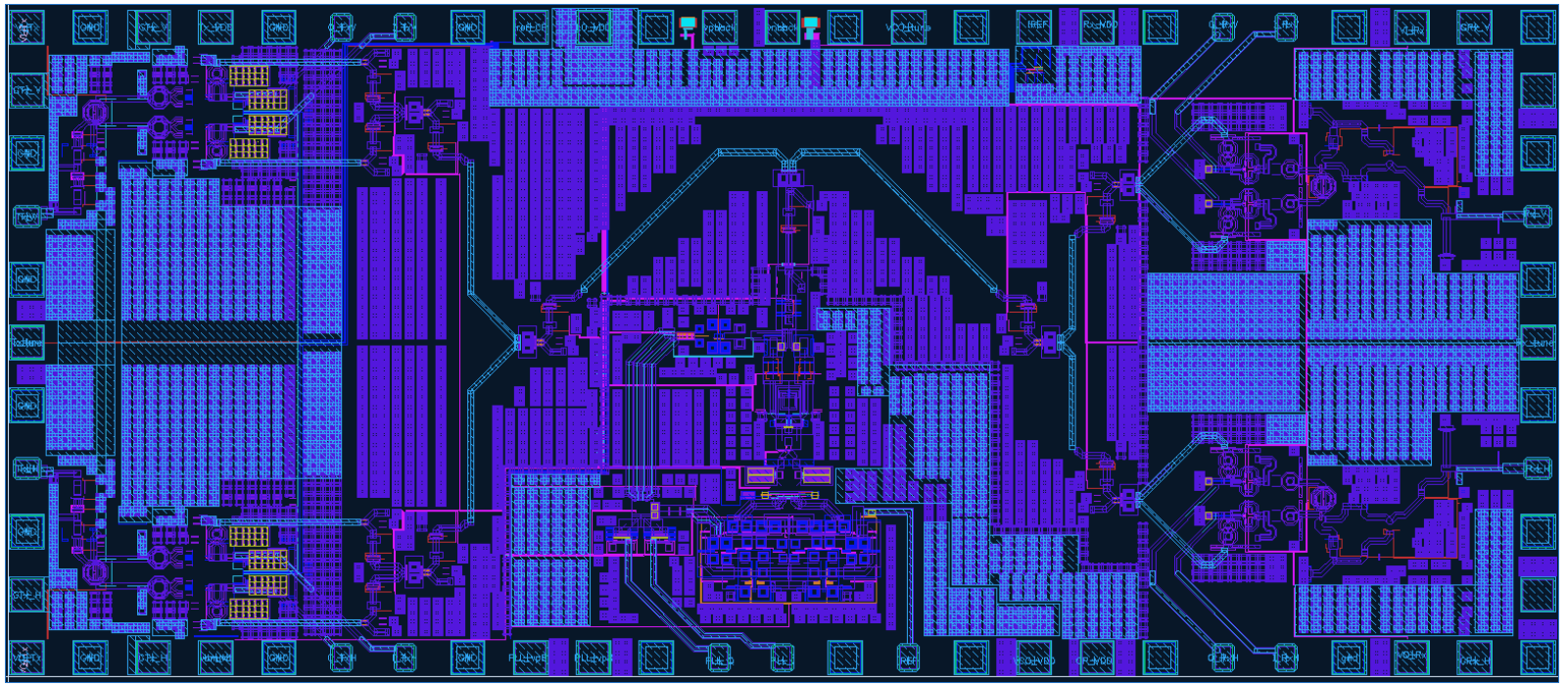
can improve P_{sat}, *PAE*

Phase Noise and *NF*.

[S. Daneshgar et al, ISSCC 2018]

153-162GHz radar sensor/radio MIMO transceiver





P_{sat}=9 dBm per element, I/Q linear up/down conversion

Receiver Gain > 20 dB, NF < 12 dB

10ns PLL settling, PN@1MHz < -110 dBc/Hz at 160 GHz

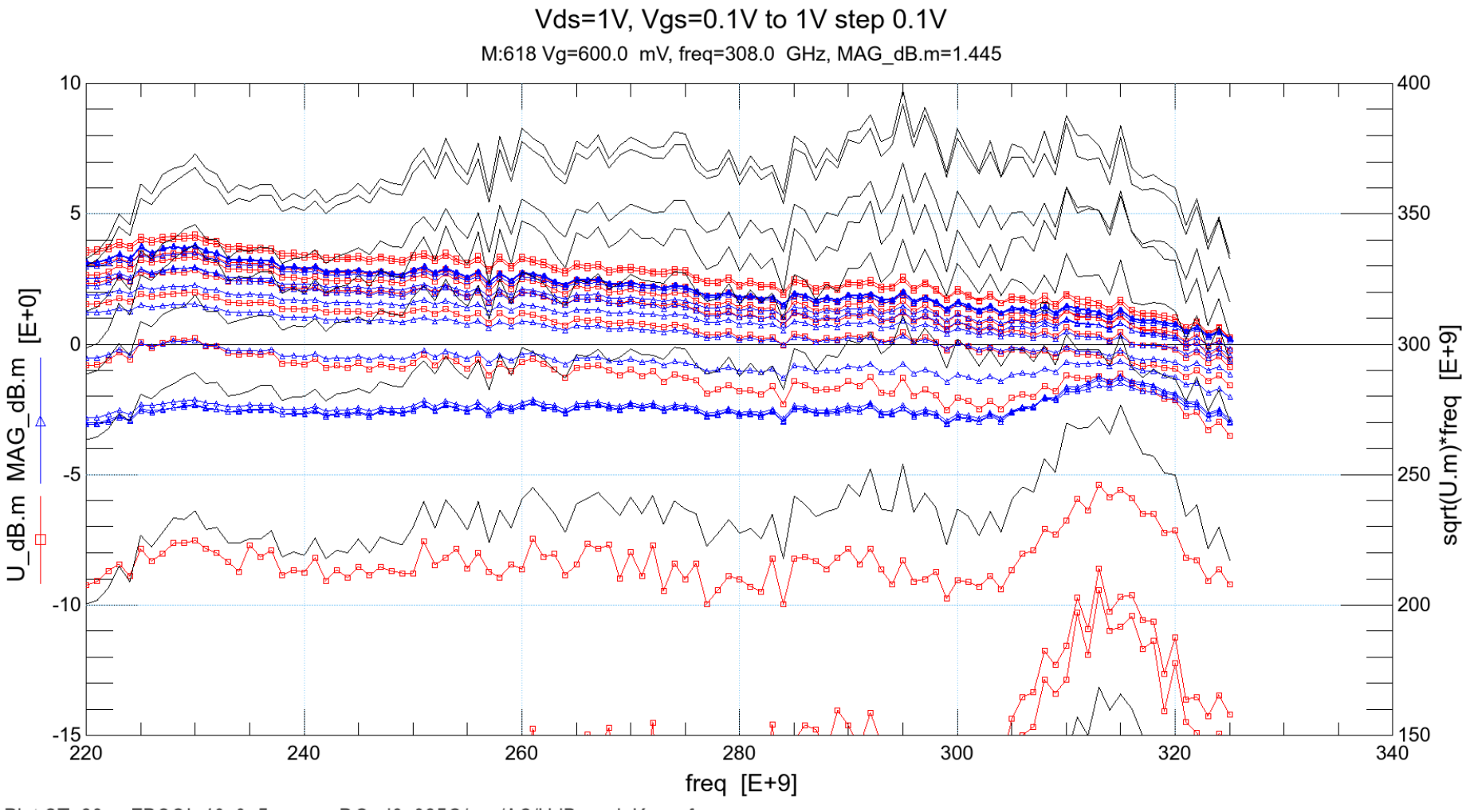
Conclusions

- g_m, f_T, *MAG* < 170 GHz continue to improve with scaling
- Back-gate control of current density, output swing, linearity
- Simpler or series-stacked topologies for PA, large-swing driver
- Similar or better mm-wave and high-speed digital performance than in older nodes with lower power consumption and supply
- Unlike FinFET or planar CMOS, large-swing and large-power as well as low-noise low-power circuits possible

Acknowledgments

- Graduate students: Sadegh Dadash, Stefan Shopov, Shai Bonen, Utku Alakusu, Alireza Zandieh, Ioannis Sarkas, Andreea Balteanu
- GLOBALFOUNDRIES, CMC, and STMicroelectronics for technology access
- NSERC, DARPA, Ciena, Robert Bosch, Finisar for funding
- Jaro Pristupa and CMC for CAD Tools
- Integrand for EMX Software

U and *MAG* vs. frequency at *J*-Band



28nm FDSOI

40x24nmx500nm

N-MOSFET

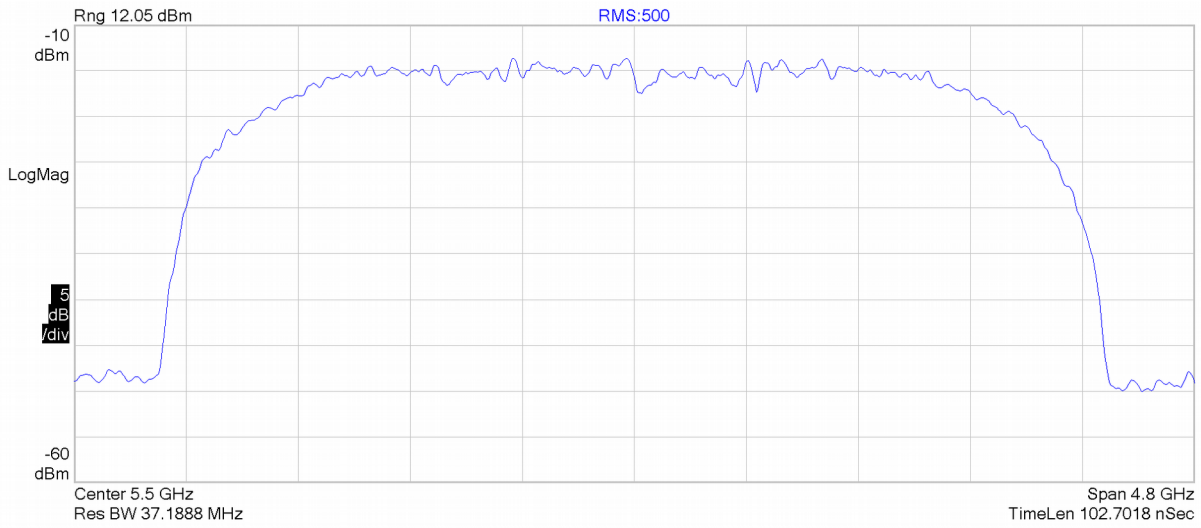
single-gate contact

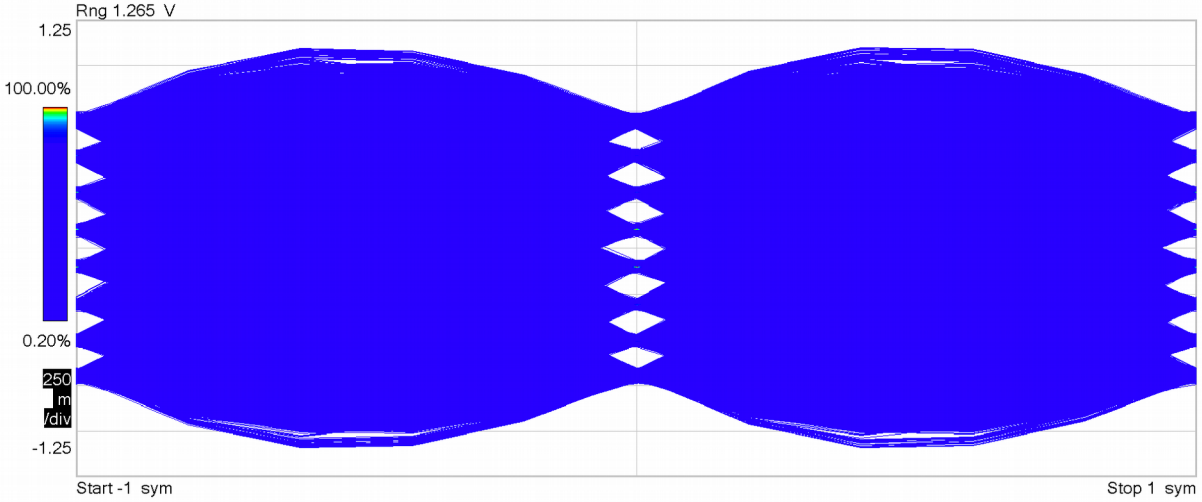
f_{MAX}>350 GHz

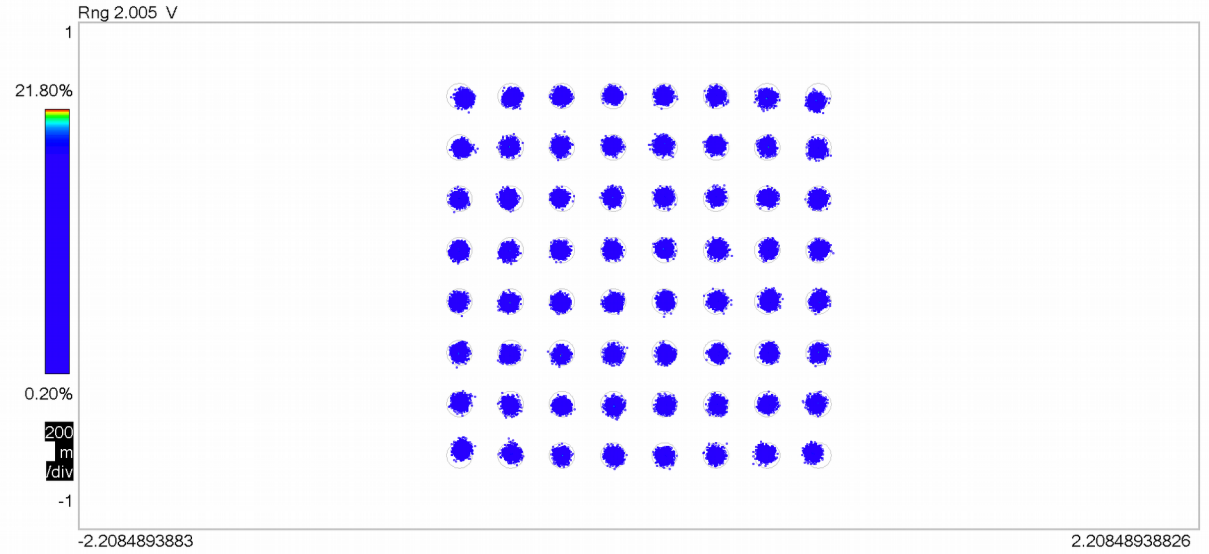
U, *MAG*>0@320GHz

Metal wiring not de-embedded

n-MOS 3-stack 64QAM, 18 Gb/s at 5.5 GHz





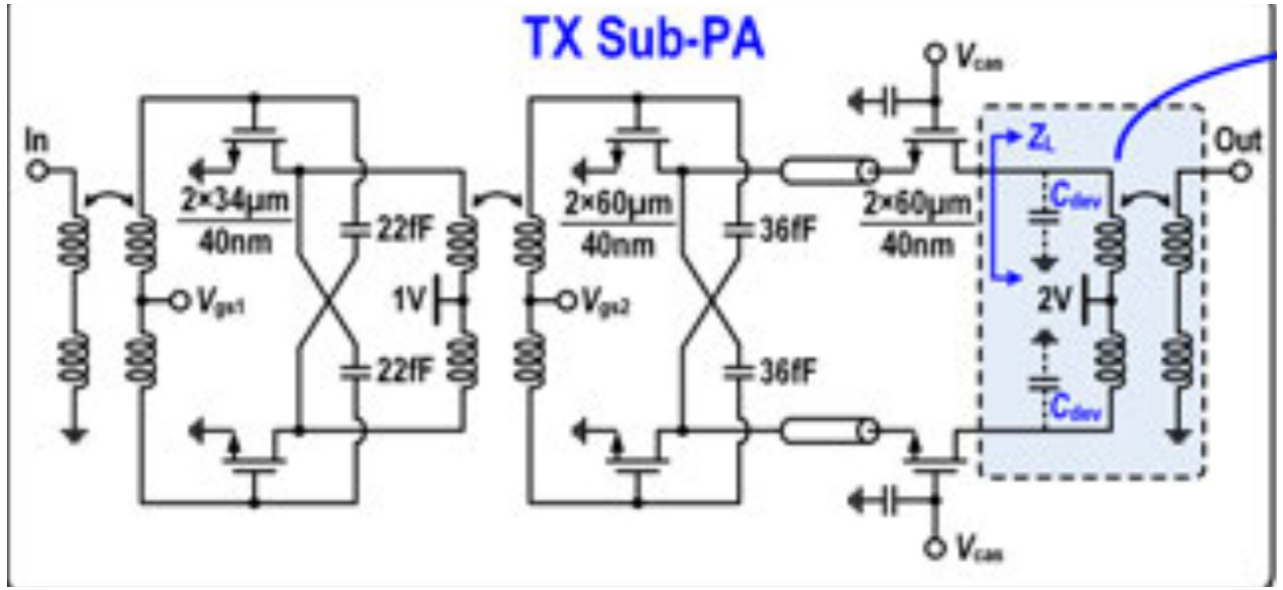


RMS:500

EVM	= 1.5163	%rms	5.1112	% pk at sym	43		
Mag Err	= 1.1992	%rms	-4.8995	% pk at sym	43		
Phase Err	= 1.2811	deg	-6.8757	deg pk at sym	36		
Freq Err	= 458.47	kHz					
IQ Offset	= -59.814	dB	SNR(MER)	= 32.669	dB		
Quad Err	= 129.80	mdeg	Gain Imb	= 0.015	dB		

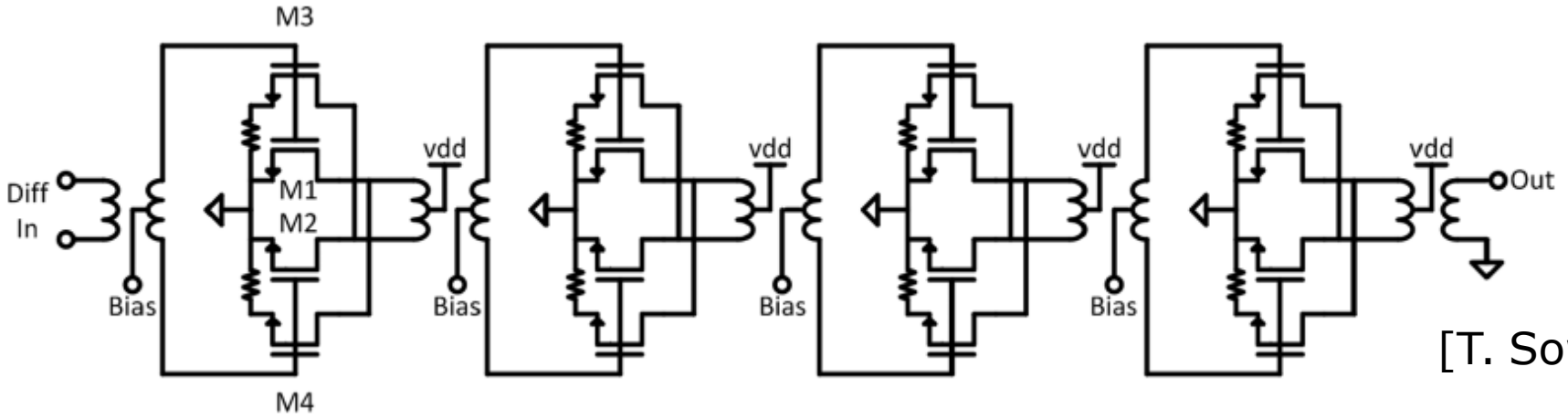
0	242B2F34	1124382D	0506162D	26023F0E	1A28040C	3B3D3E0D	32101716	0D22121F	020F0802	1C0A330B	3826003F
44	1F180811	1E3B2439	2D2D0706	072F0617	2D0E032F	24132C2C	2F2F1615	251A0105	34102410	2C152C1F	290E212B
88	2531002C	1D291F23	0B302300	351A0900	341A2101	24302805	0C133C2E	273B143F	35190939	372A1E1A	20010C31
132	382F0517	140D3310	3F171D08	1B1B2A2C	1C293722	1B1A2A04	1D391D2B	1F320910	36123503	0E202B0D	30100614
176	2D37001F	1B08281D	0B1B2229	1C233233	133F2E1E	3824002E	1D381D03	1E222319	323A1617	250B0325	21022409
220	2B353308	381F030F	20030C20	3A0F1005	14143430	20000C19	393F2F1E	10251004	143C3520		

CMOS 60GHz PAs Use Miller Neutralization



[T. Chi, et al., ISSCC 2018]

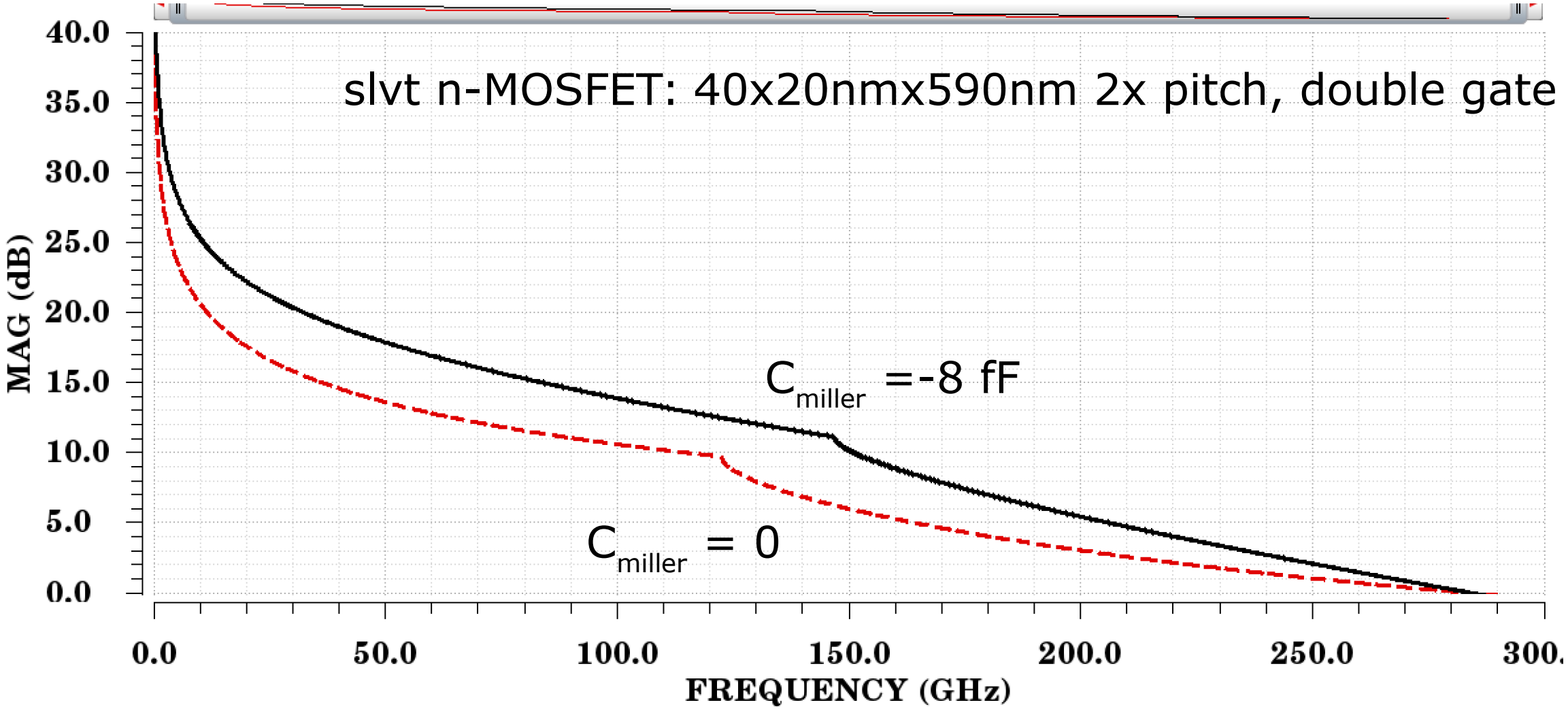
45nm PDSOI CMOS



40nm LP CMOS
28nm RF CMOS

[T. Sowlati, et al., ISSCC 2014/2018]

Why Miller Neutralization?



Dangers of Miller Neutralization: f_T, NF_{MIN} Degradation