Baseband and mm-wave circuit techniques for energy-efficient communication systems at up to 1Tb/s per carrier

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University of Toronto

Qualcomm, October 19, 2012

Credits

Graduate students

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- NSERC, OCE
- Robert Bosch GmbH, DARPA, Ciena, Gennum for funding
- STMicroelectronics, Darpa, Ciena for chip donations

Outline

- Why?
- How?
  - System
  - Baseband
  - Radio transceiver
- Summary

Energy Efficiency of Communication Links

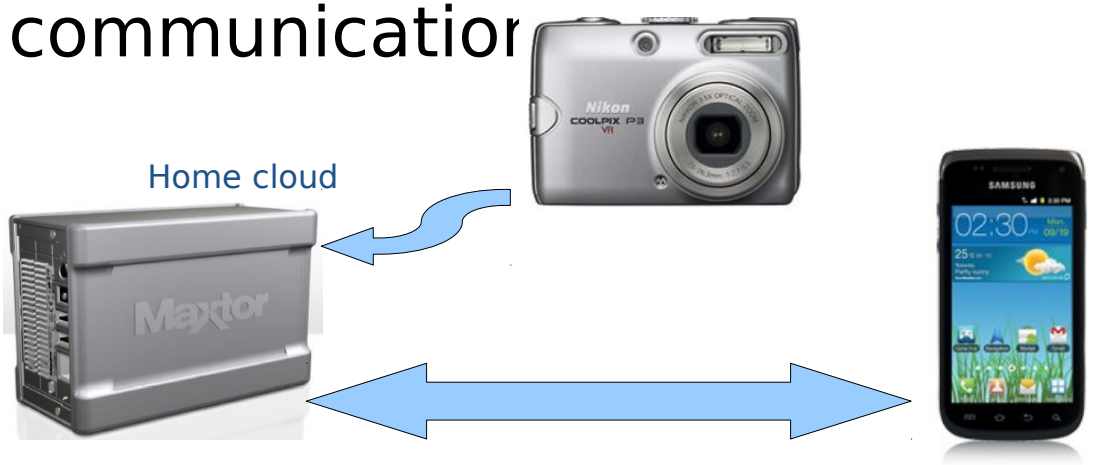
	4G WiMAX	60 GHz LOS Radio	Wireline IEE 802.3.an	Fiber SerDes VCSEL	Fiber DP-QPSK/BPSK
Data Rate	≤1 Gbps	5.3 Gbps	10 Gbps	10 Gbps	50 Gbps
Power	1.76 W	350 mW	2 W	2.5 W	25 W
Distance		2 m	100 m	20 km	3500 km
Energy/bit	1.6 nJ/b	66 pJ/b	200pJ/b	250 pJ/b	500pJ/b
Energy/bit/m		33 pJ/b/m	2 pJ/b/m	12.5 fJ/b/m	0.14 fJ/b/m
Reference	[Krishnamurthy, •RFIC 2010]	[Laskin, •RFIC 2011]	[Gupta, ISSCC 2012]	[Voinigescu, CICC 2001]	[Crivelli, ISSCC 2012]

Need solutions in…

- Wireless, wireline, fiberoptic system architectures that
  - Increase data rate >1 Tb/s carrier (imperative in fiber links)
  - Increase efficiency per bit
- Faster, more efficient circuit topologies
  - CMOS logic at 50-100 Gb/s to save power?
  - Stacked CMOS logic for large swing drivers?
- Can we push the carrier frequency to 300 GHz?

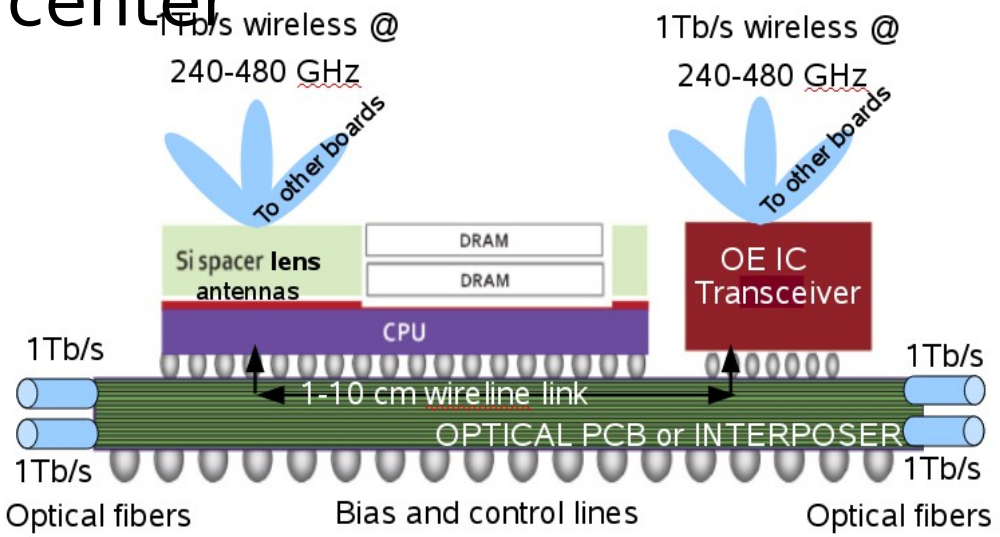
Why Tb/s wireless?

- Near field communication



- Short-range reconfigurable wireless data transmission in the data center

- Board-to-board



Scalable Digital Radio Transmitters

- Can we improve efficiency by increasing the modulation rate per carrier at fixed P_{OUT}?

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- Example: 300 Gb/s with 1 W PA => 3.3 pJ/b
  - But 300 Gb/s with 64 QAM modulation requires 50 Gb/s serial baseband lanes,
  - difficult to realize efficiently with up-conversion transmitter architecture

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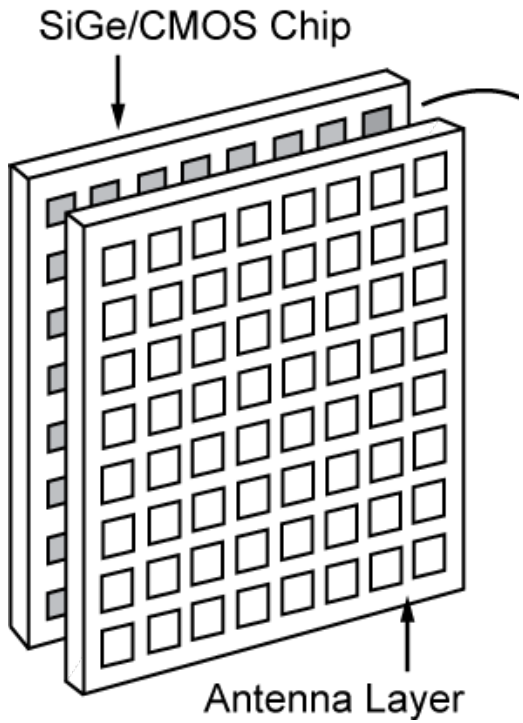
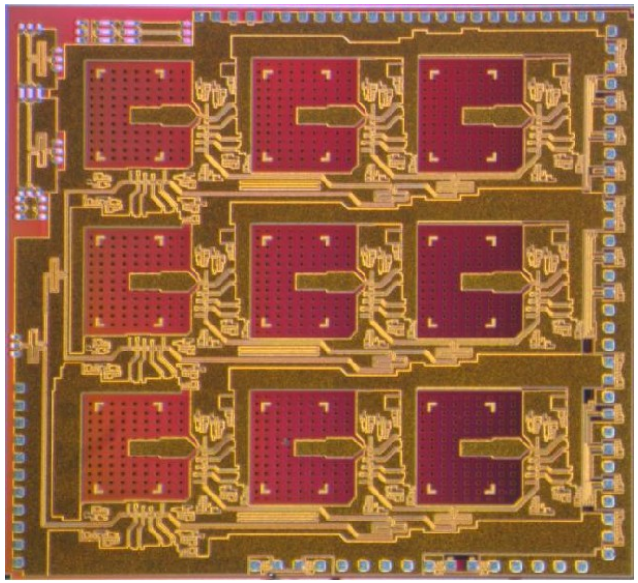
Why 100-300 GHz?

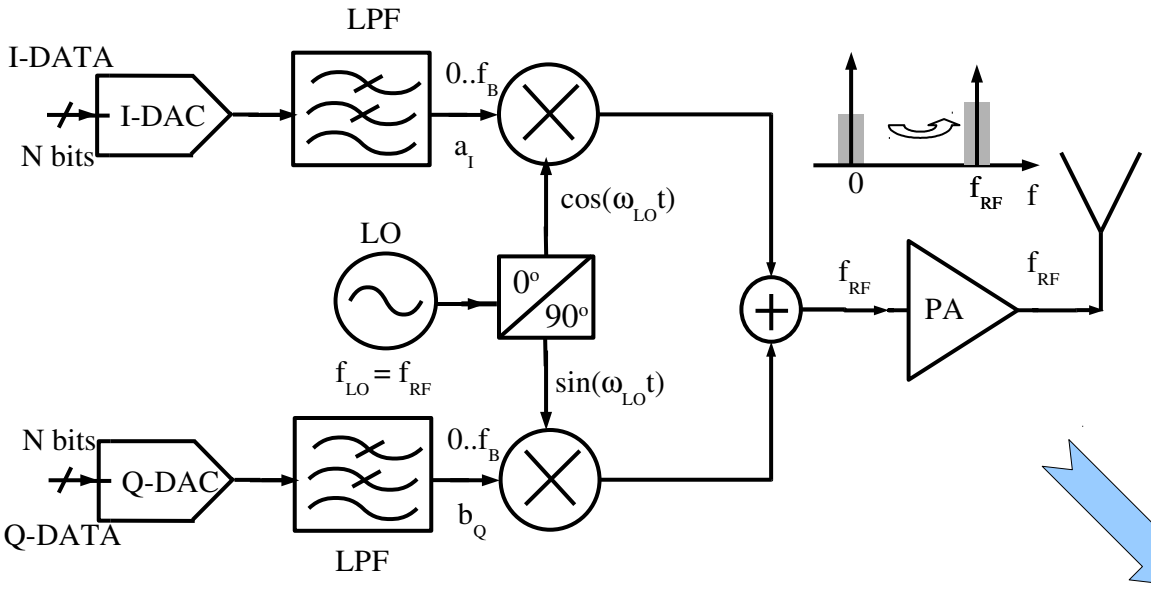


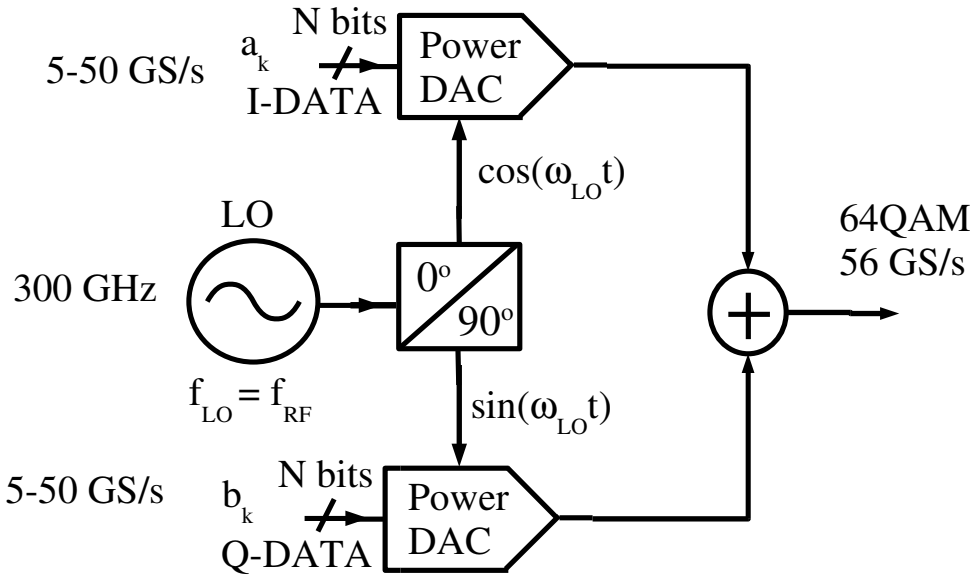
- Silicon transistors with f_{MAX}>400 GHz
- Smaller wavelengths: high res, high BW
- Small antenna size with good gain
- Lower power LNA, mixer, receiver
- But...
  - higher power PLL,
  - reduced P_{out},
  - shorter range ~$1/f^2$ or ~$1/f^4$



Source: G. Rebeiz UCSD

Potential Solution: Direct Modulation TX Radio

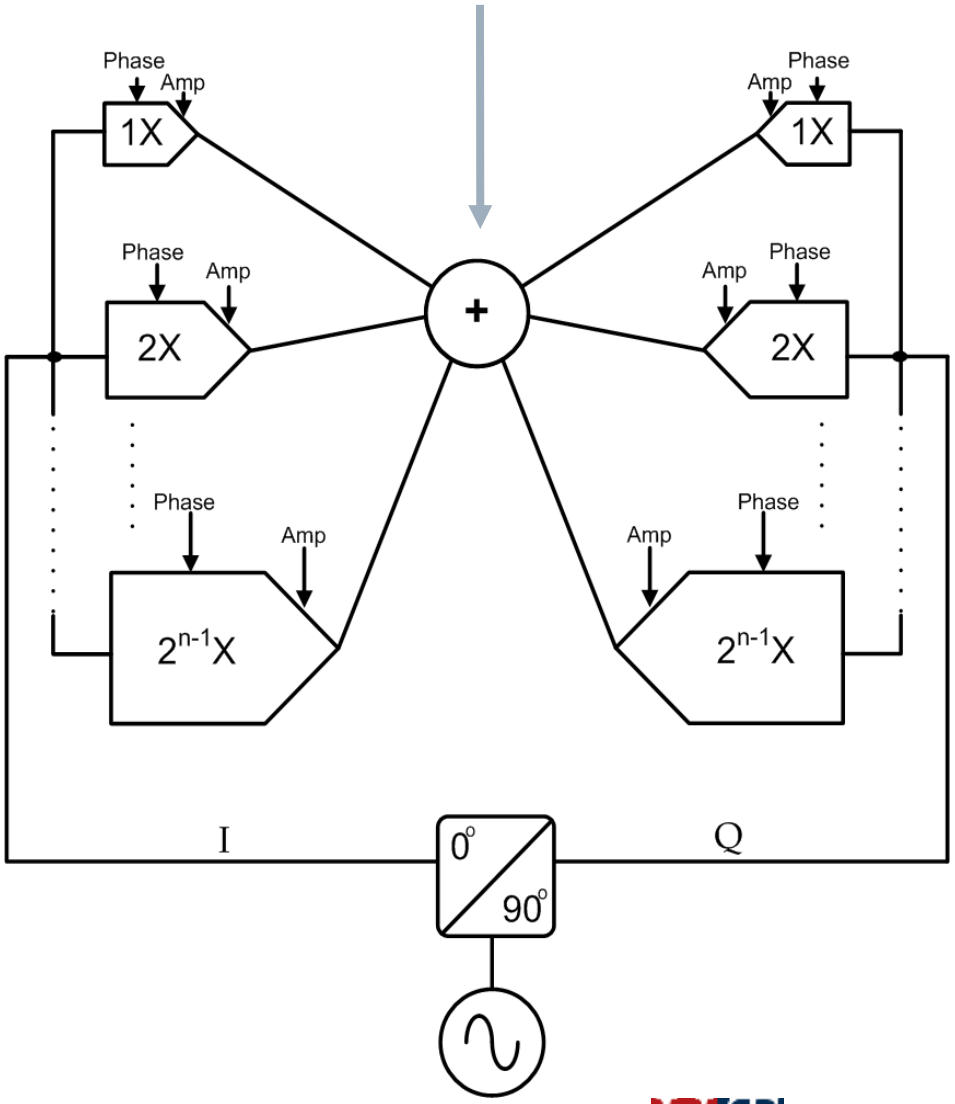




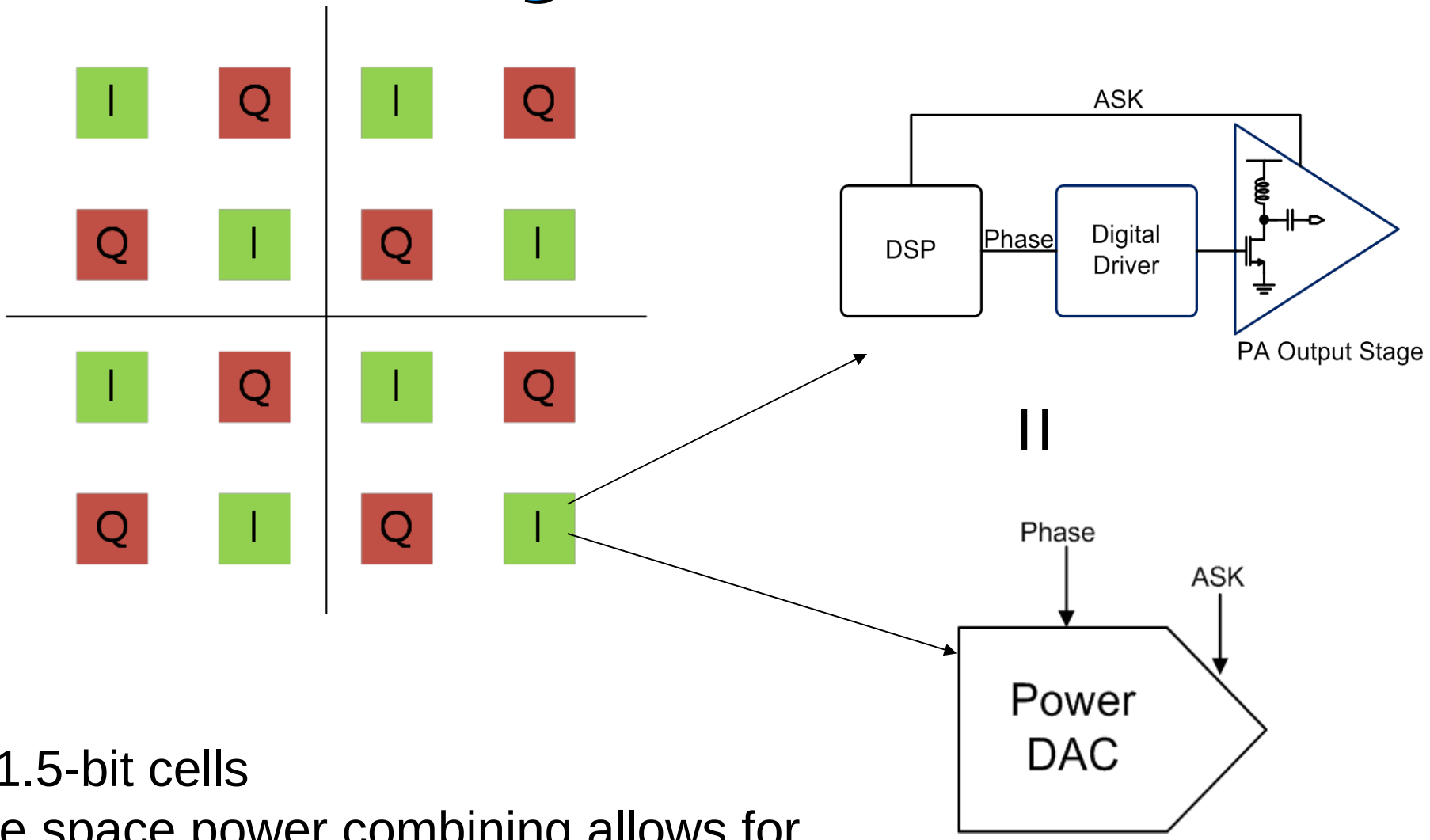
Direct Modulation TX Radio

- Merge DAC with PA
- 1.5-bit polar-modulated, binary weighted PA cells driven in quadrature
- No back-off needed for linearity
- Phase/Amp bits @ 1-50 Gbps

•On chip free-space power combiner

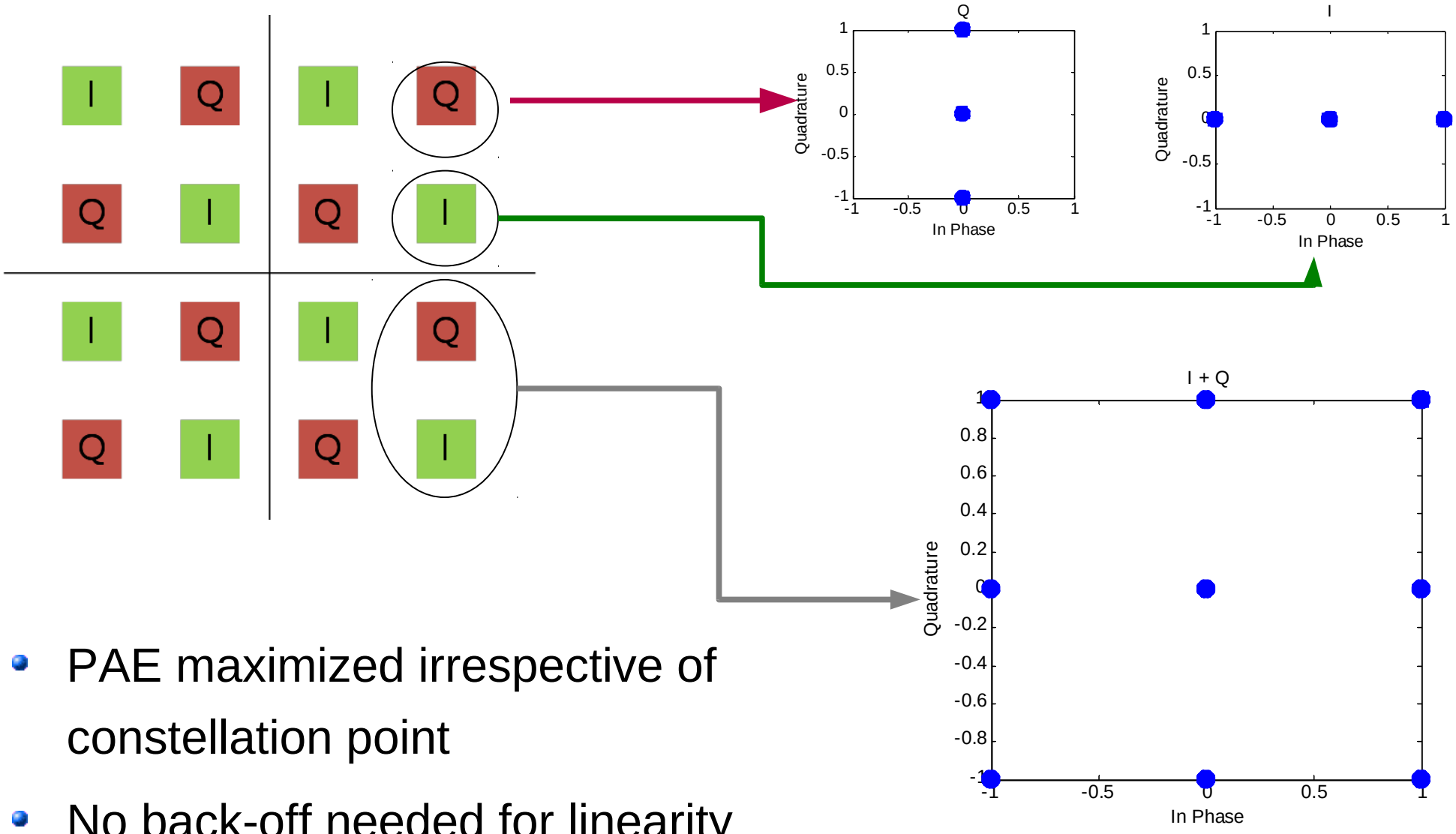


IQ DAC TX with Antenna Level Segmentation



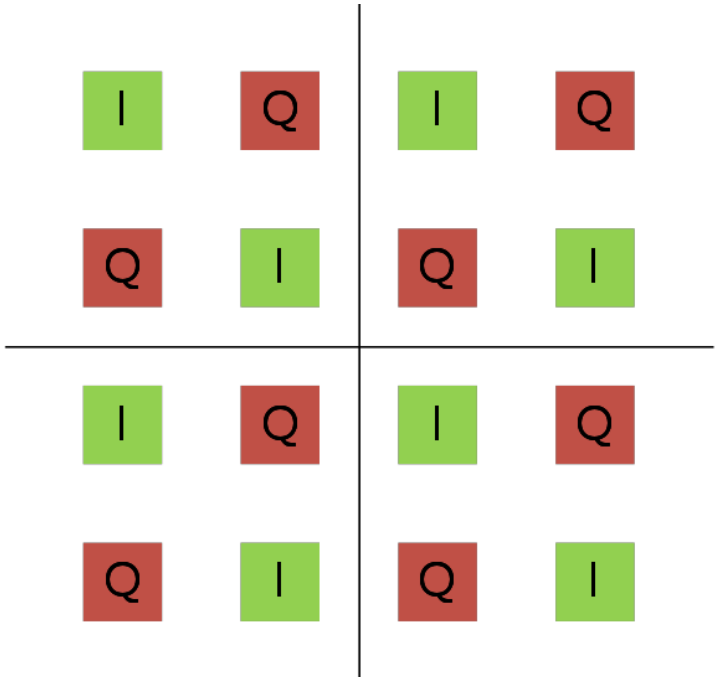
- 16 1.5-bit cells
- Free space power combining allows for antenna segmentation

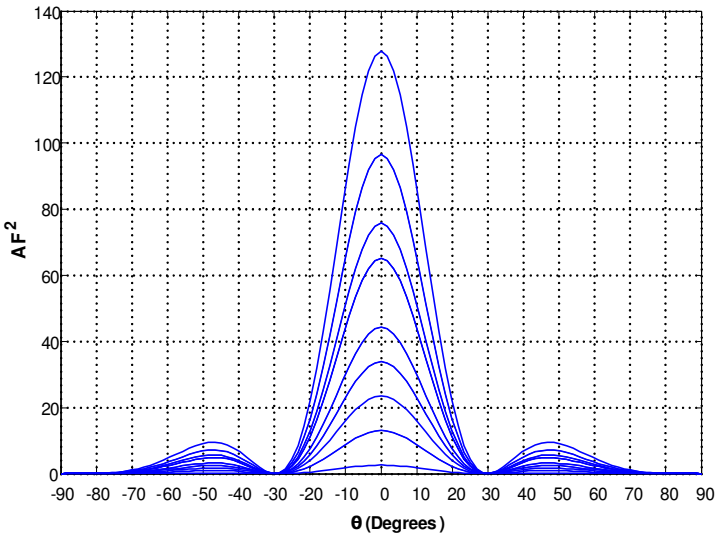
IQ DAC TX Constellation

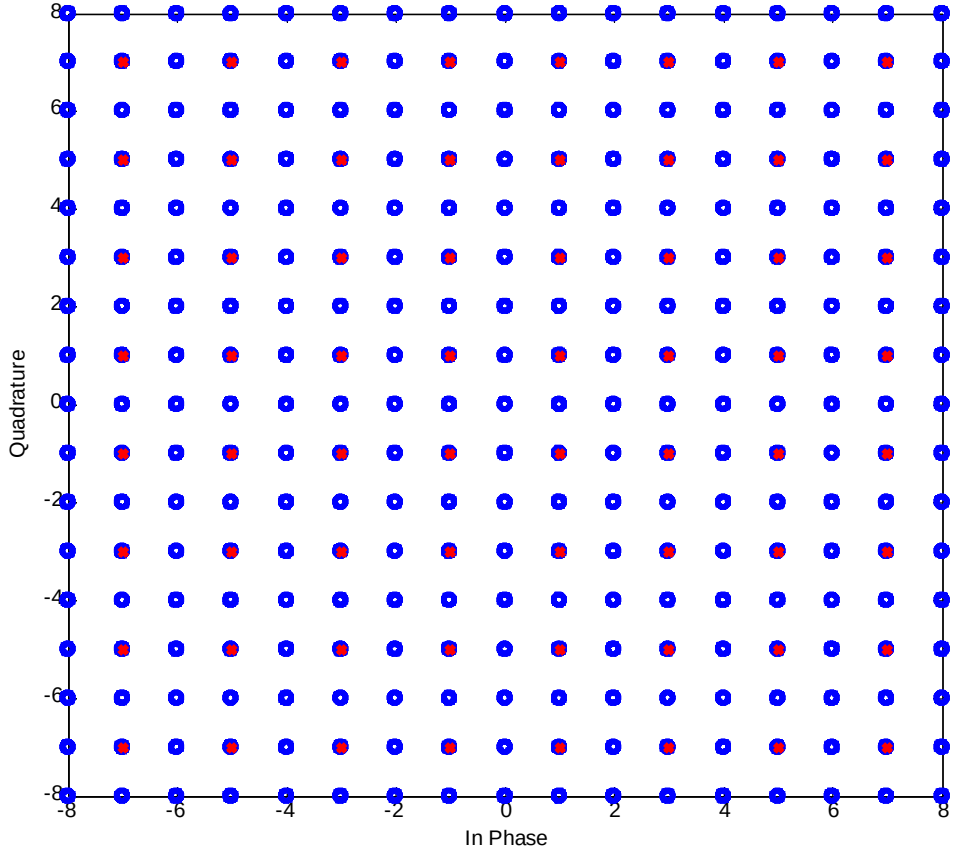


- PAE maximized irrespective of constellation point
- No back-off needed for linearity

Full 8I + 8Q Constellation







64 QAM Constellation Points

8I + 8Q -> 289 Constellation Points >2^8
2 extra bits

Wish list for sub-millimetre wave radio

- 100 Gb/s standard CMOS baseband lanes
  - Efficiency scalable with data rate
- P_{TX} = 10 dBm
- PLL with PN < -90 dBc/Hz in band at 300 GHz
- NF < 12 dB
- P_{DC} < 1W
- BW = 25-30%
- Antenna gain > 20 dB (lens)
- Distance: 10's cm

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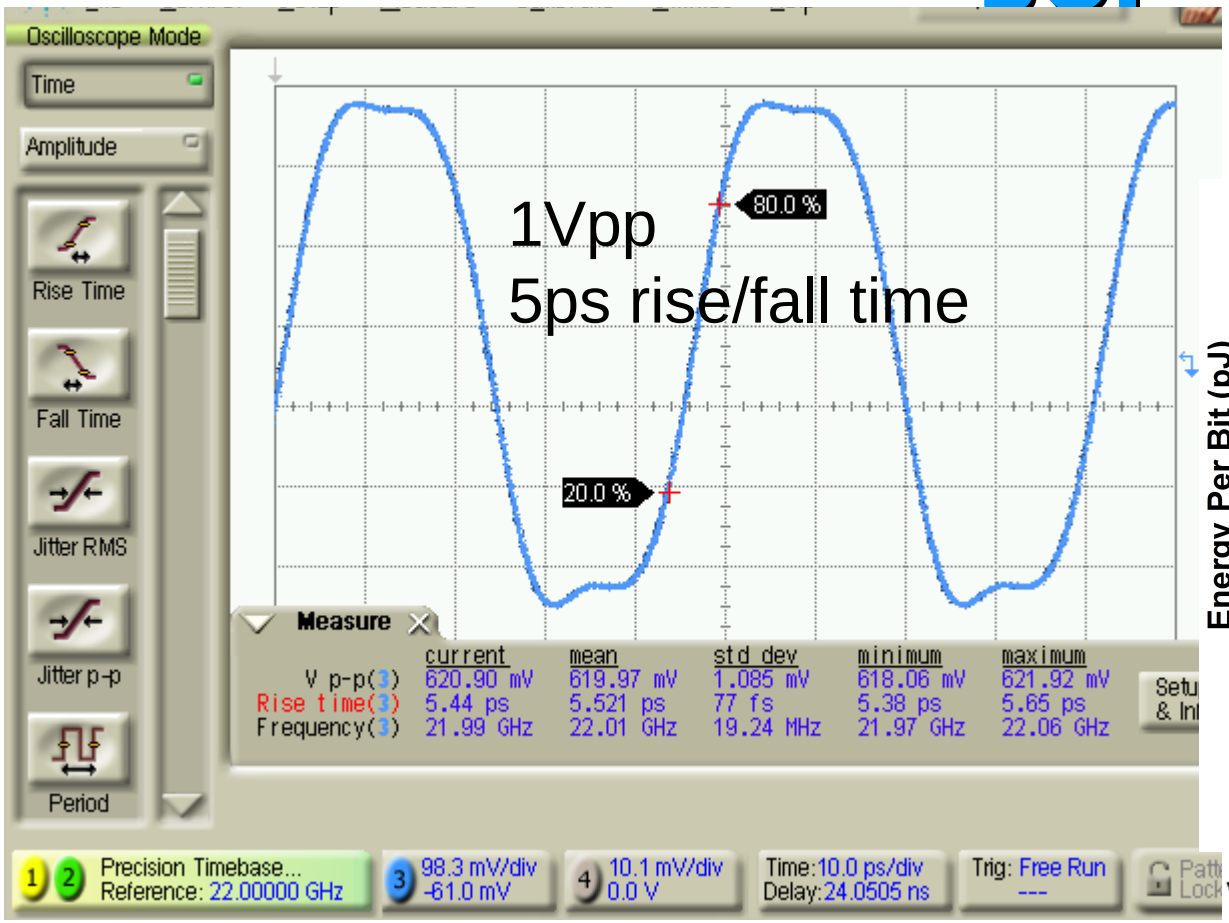
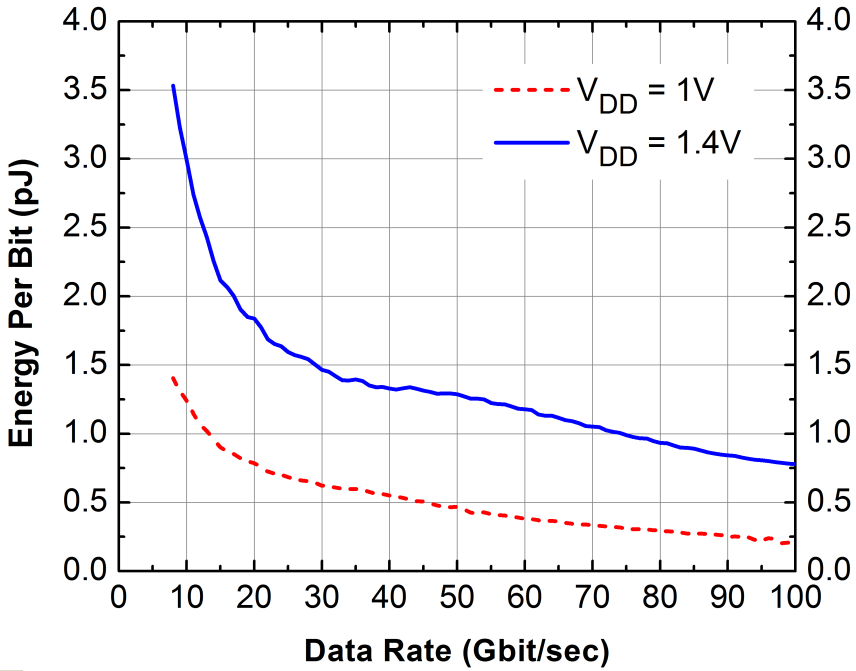
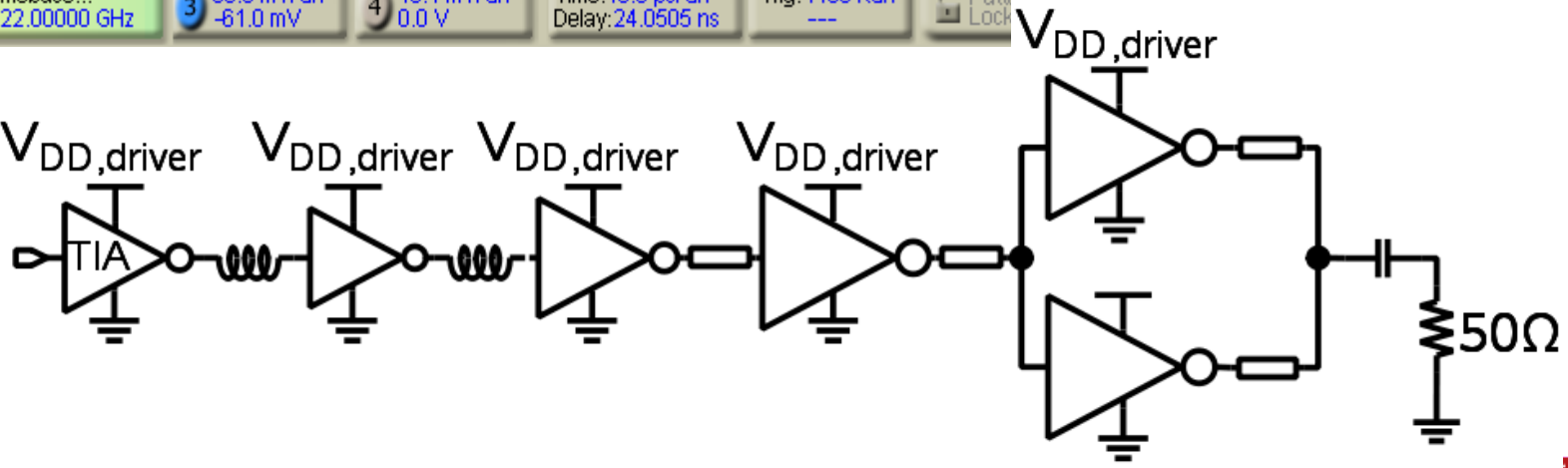
Rise/fall time, efficiency/bit in 45-nm SOI

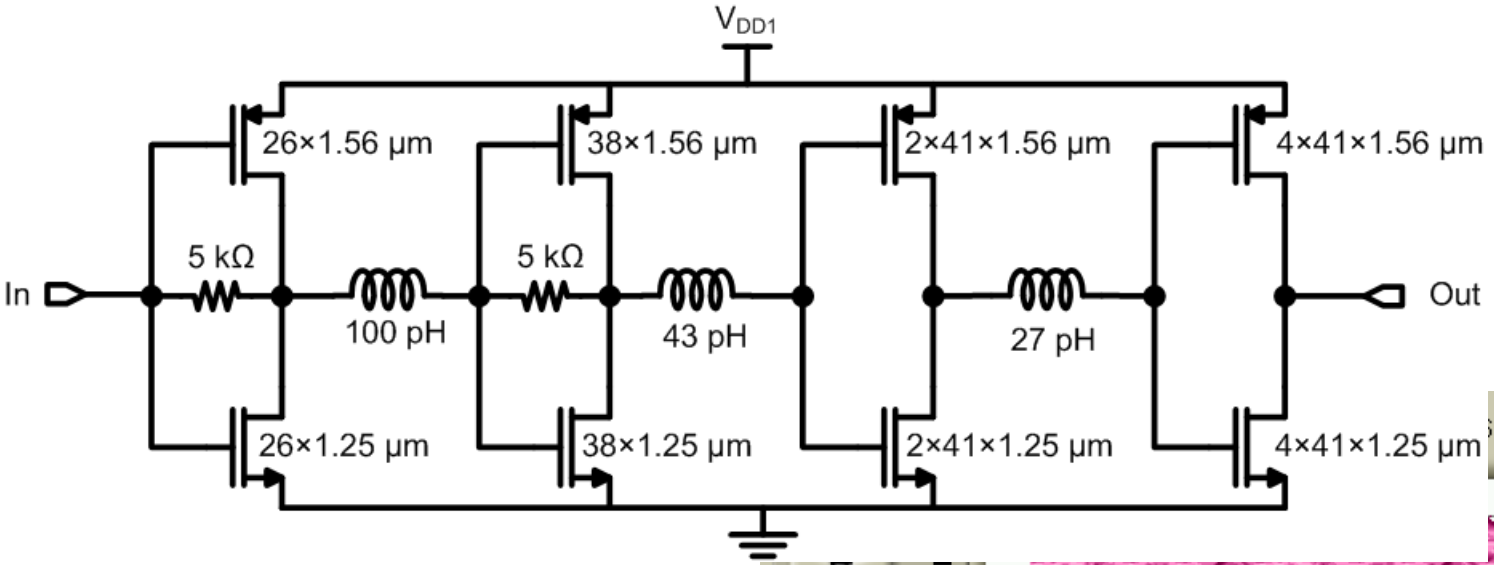


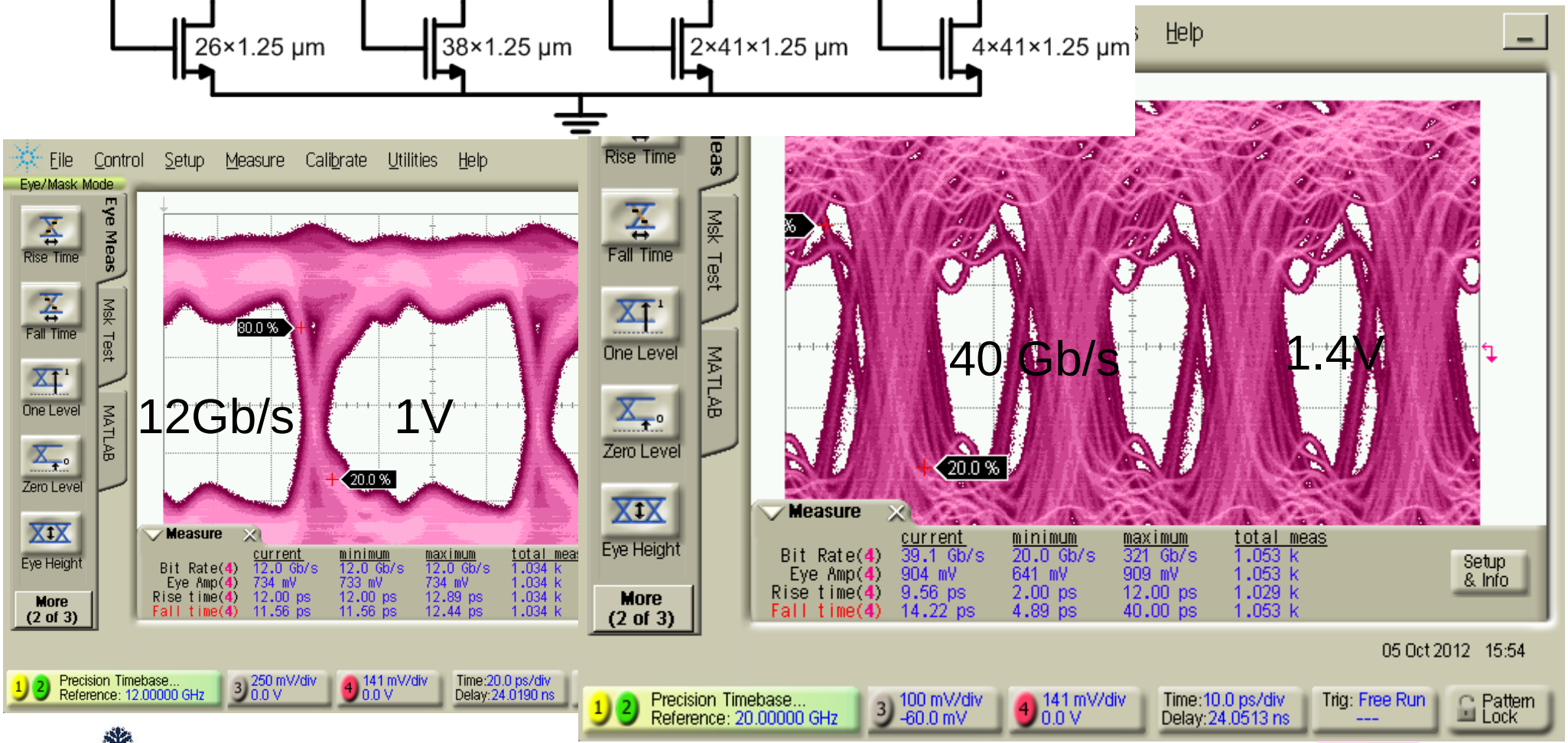
[I. Sarkas, ISSCC 2012]





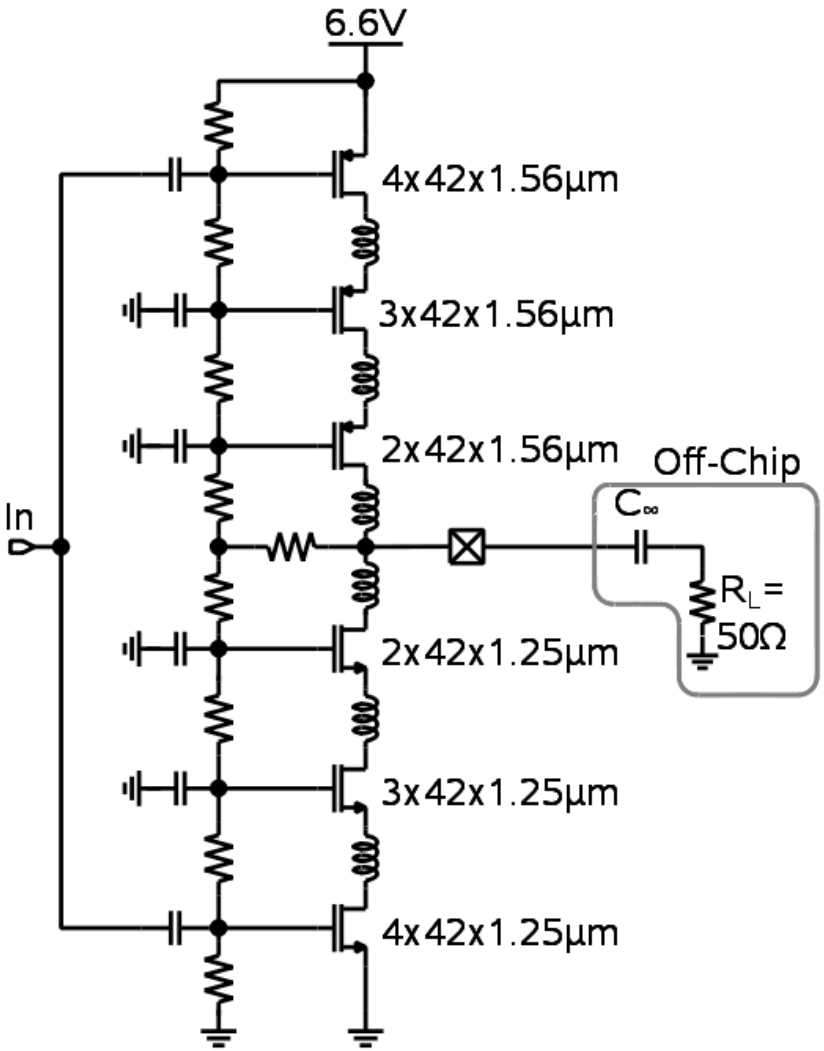
40+ Gb/s inductively-peaked CMOS logic

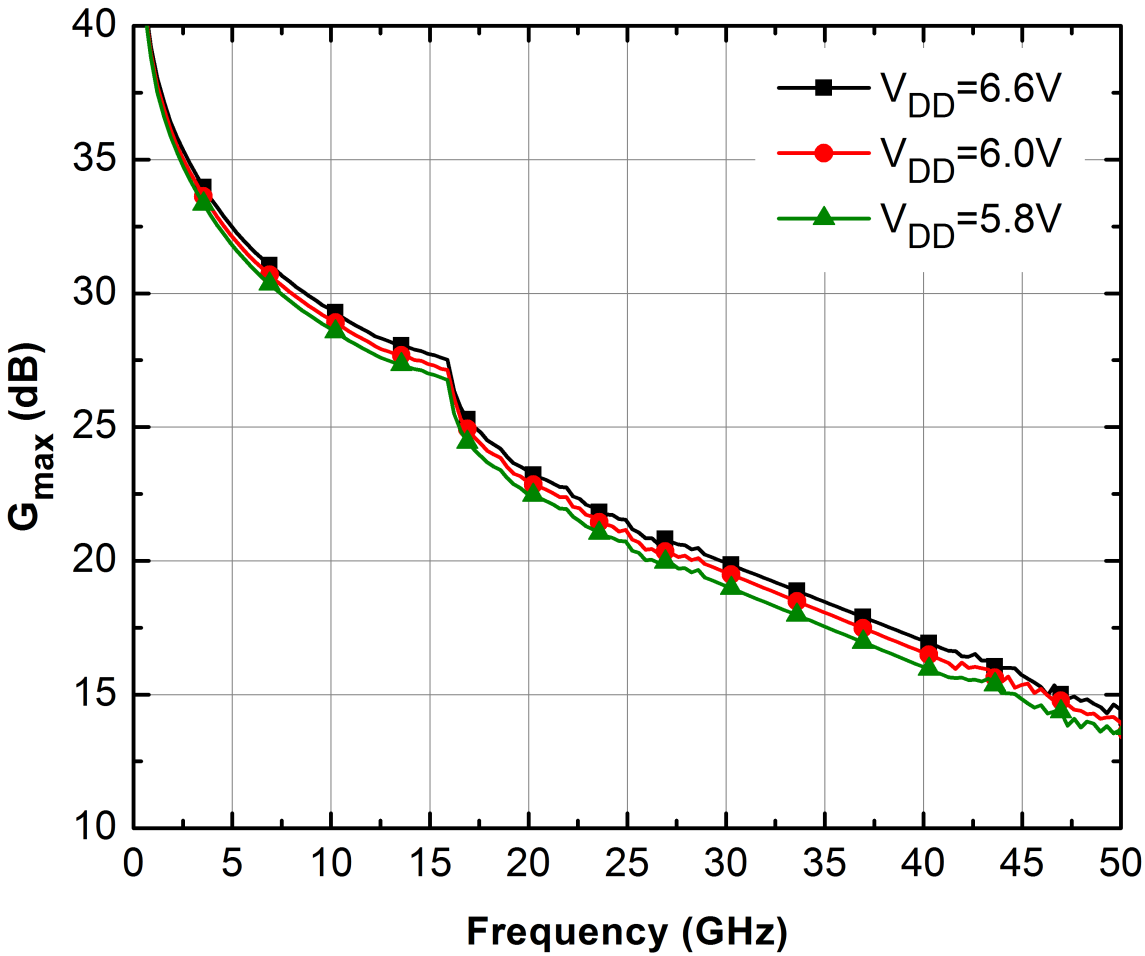




Large swing stacked CMOS inverter LOGIC

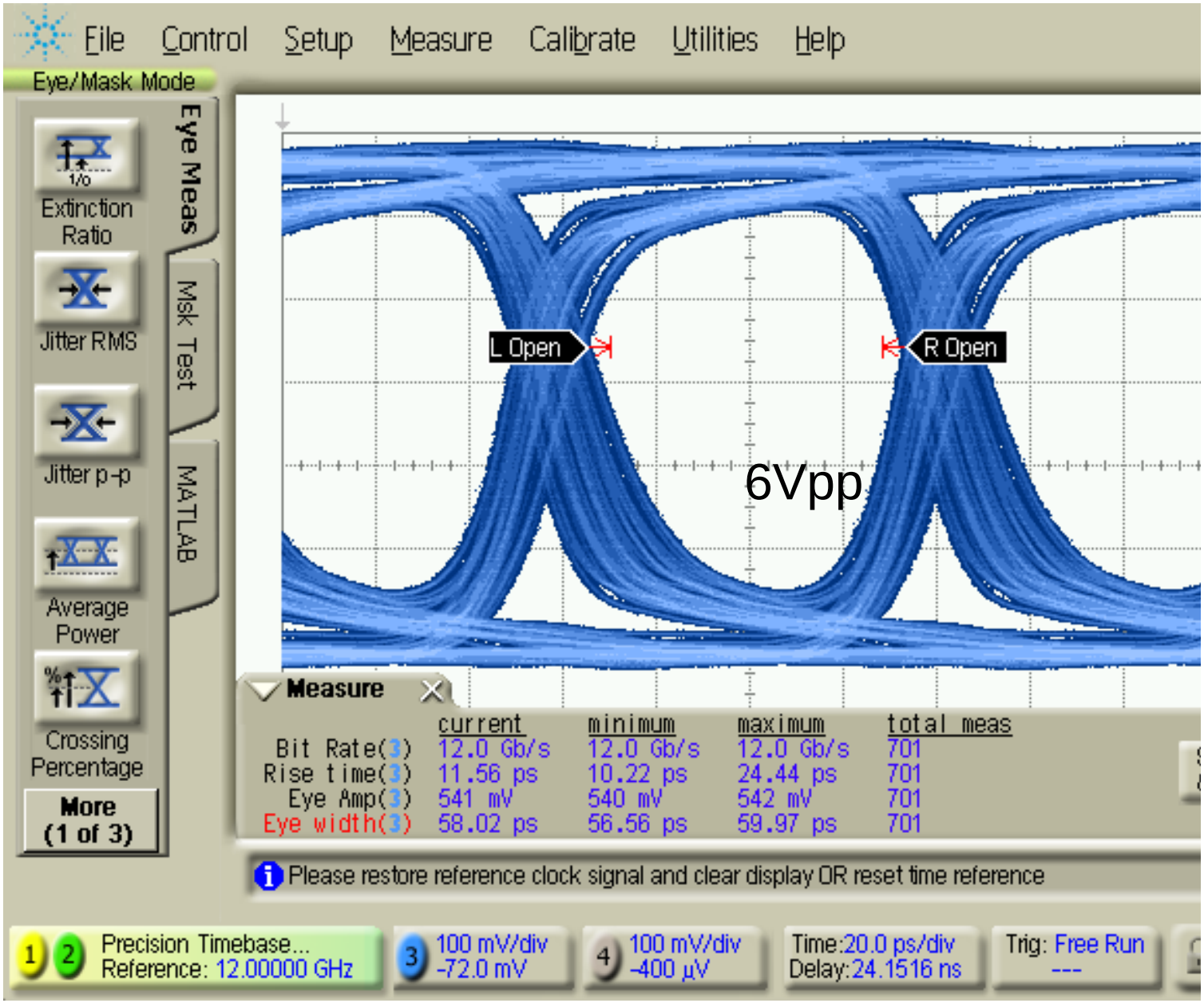
[I. Sarkas, ISSCC 2012]



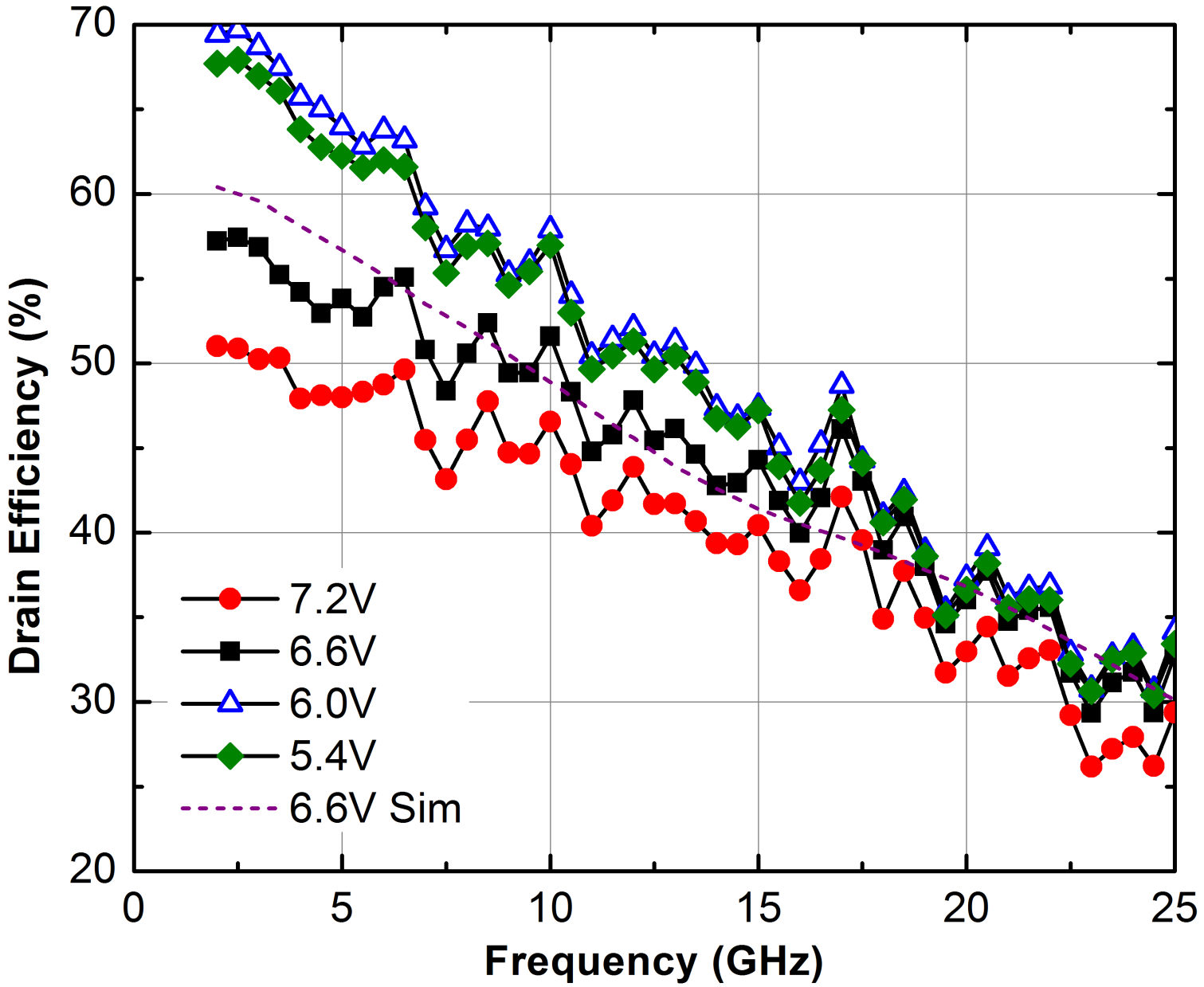


Inspired by
P. Asbeck's group work

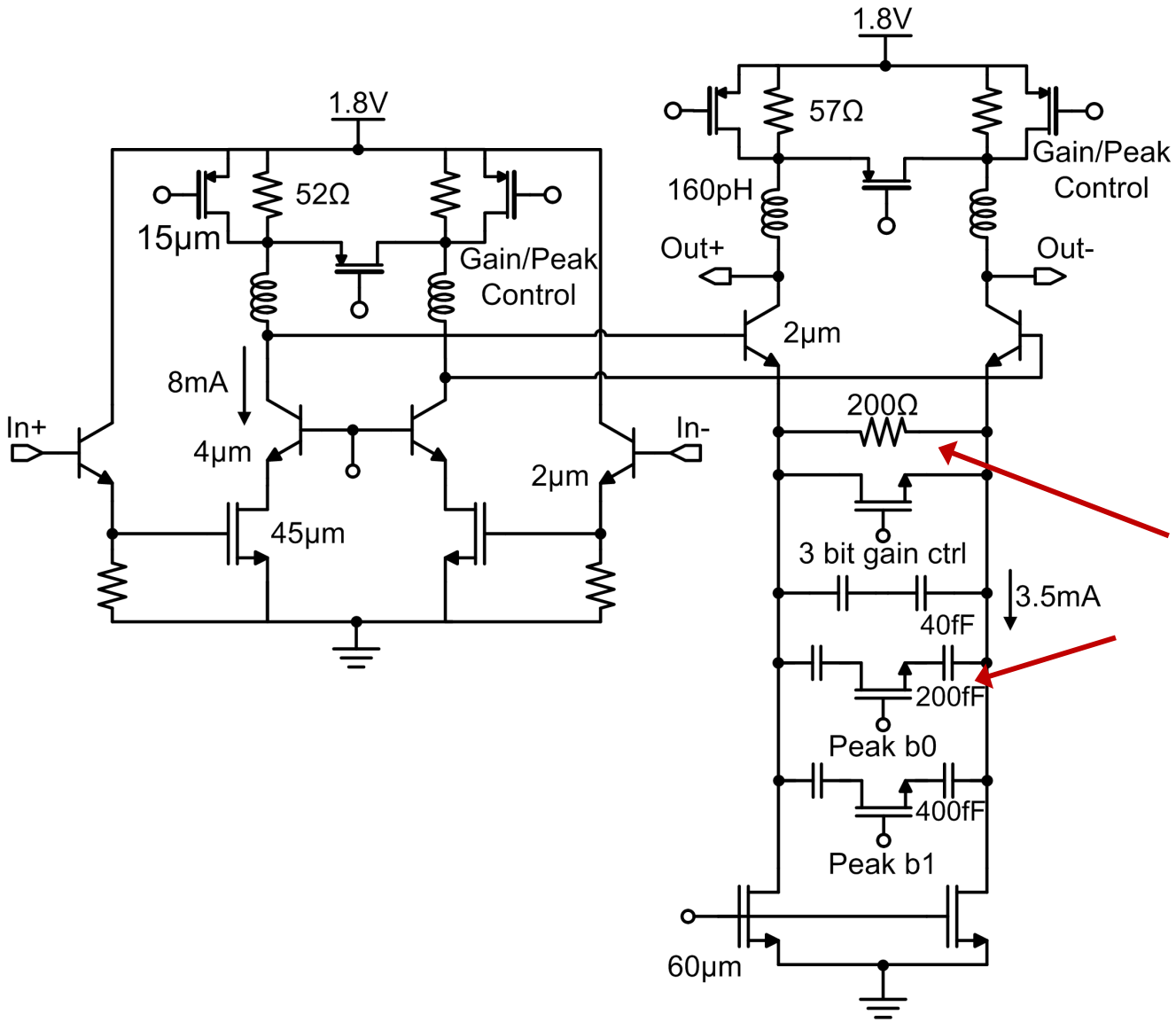
Eye diagrams at 12 Gb/s



Efficiency


70
60
50
40
30
20
0
5
10
15
20
25
Drain Efficiency (%)
Frequency (GHz)
7.2V
6.6V
6.0V
5.4V
6.6V Sim

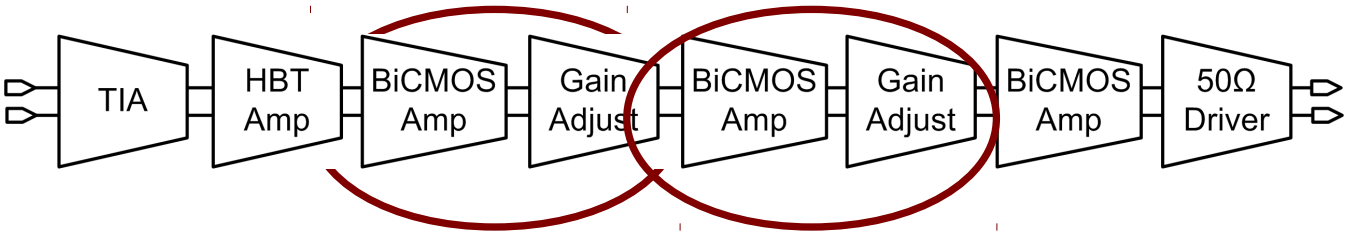
1.8V 80-Gb/s Cable Equalizer



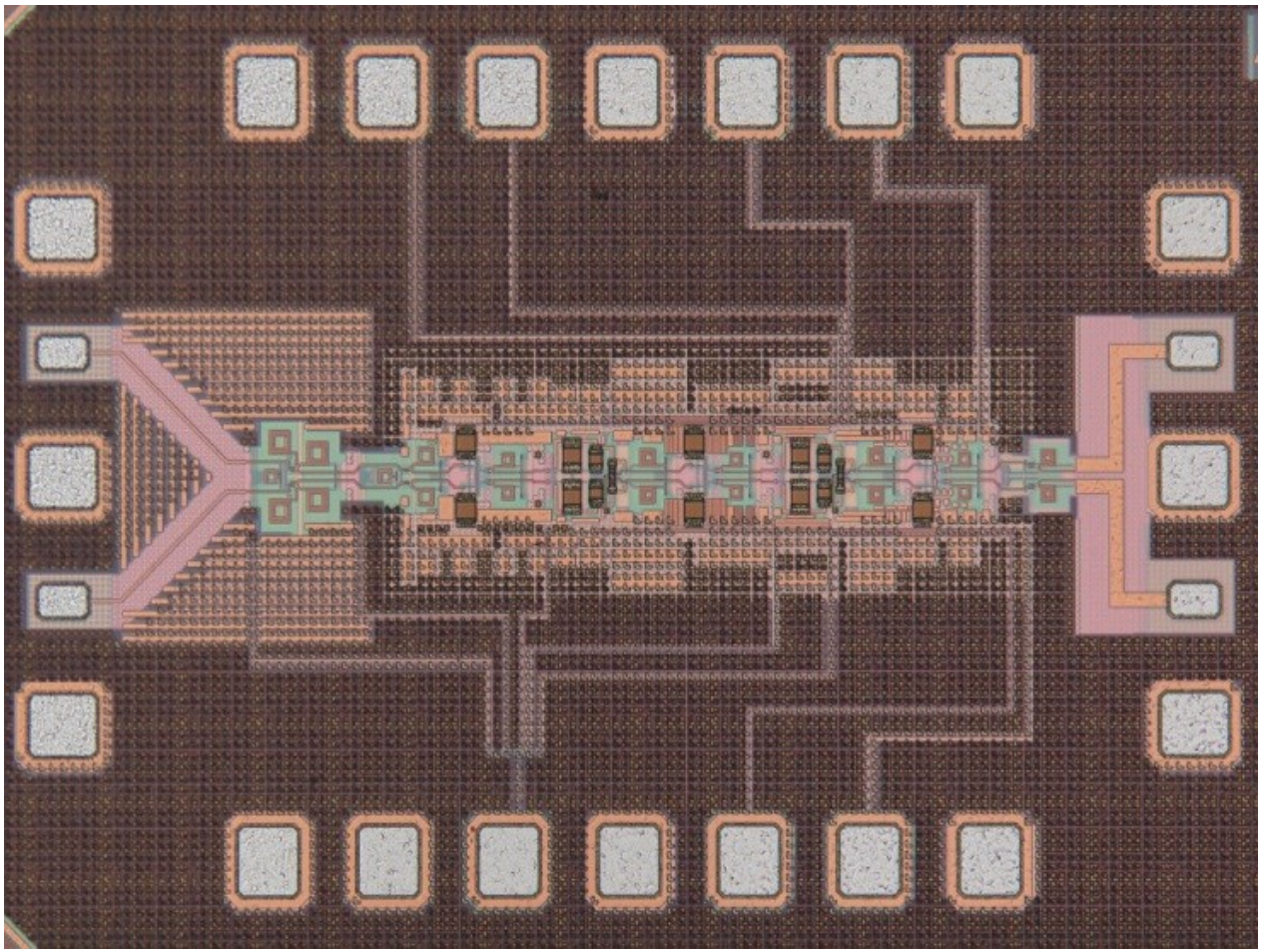
[I. Sarkas CSICS 2012]

Adjustable DC gain also Important for linearity

Adjustable zero frequency

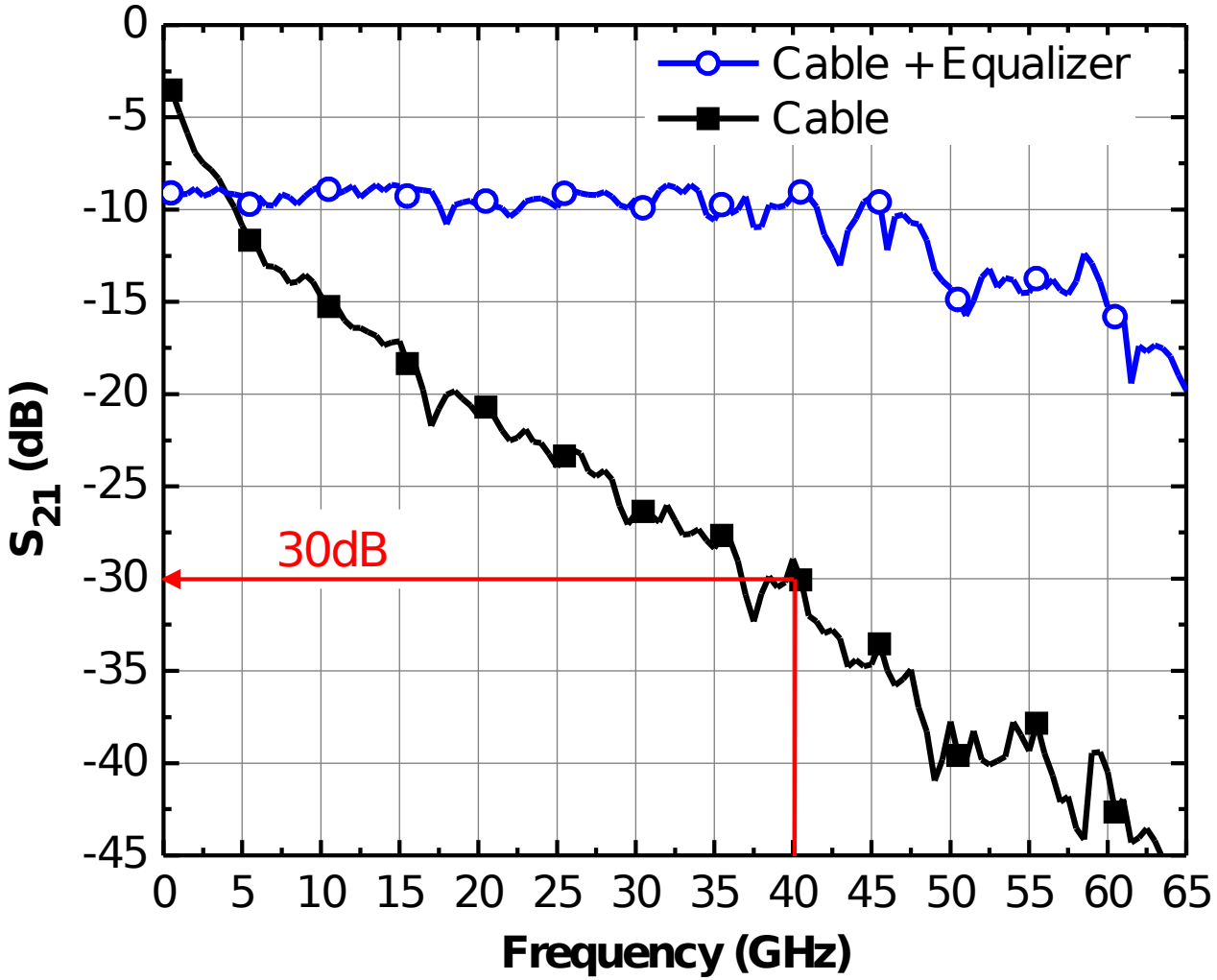


Die Photo



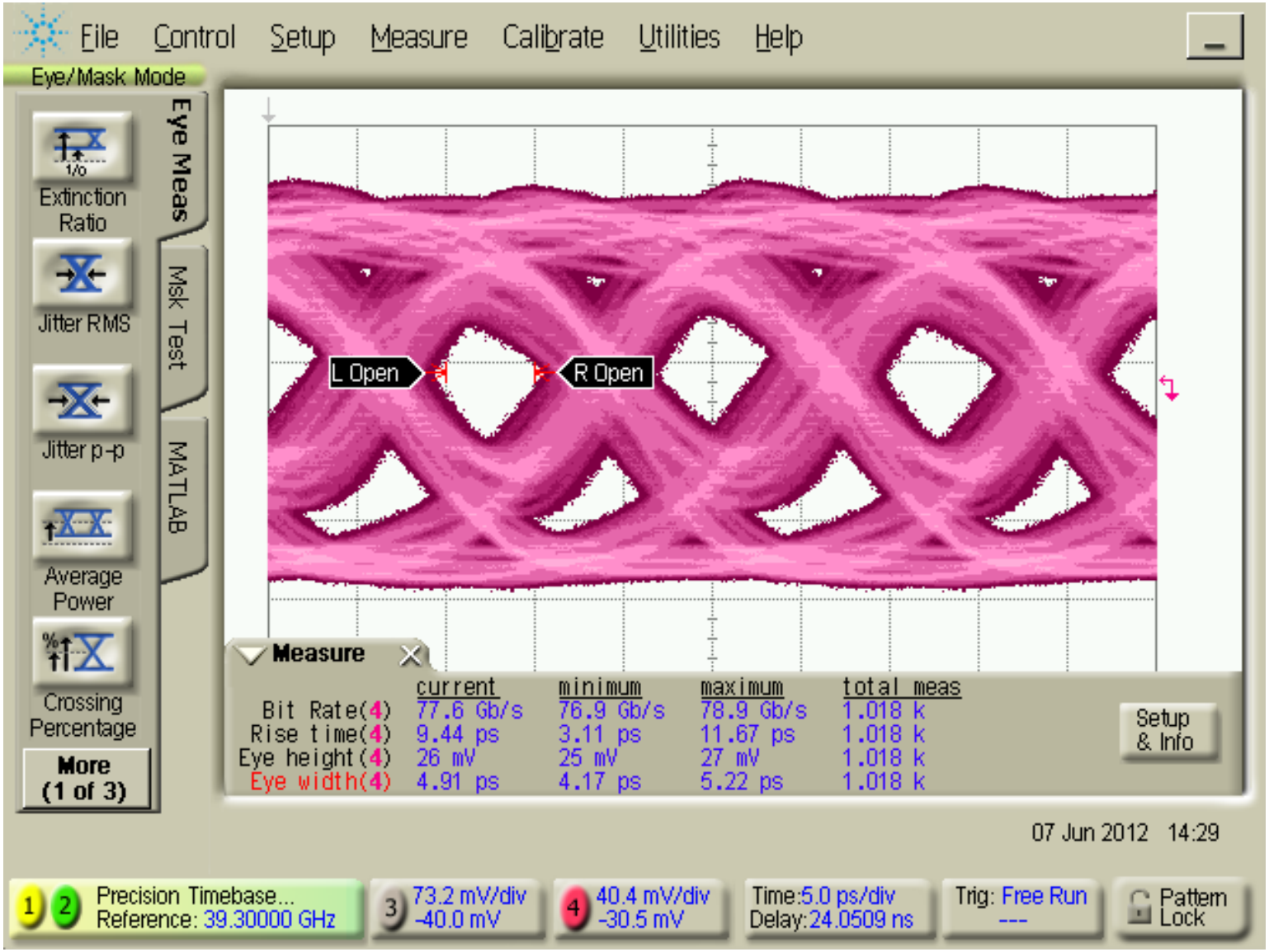
- STMicroelectronics' 130nm SiGe BiCMOS process with f_T/ f_{MAX} =220/280 GHz
- 1×0.7mm P_{DC} = 250mW

3.9m Cable Equalized S-parameters



- 30dB loss @ 40GHz
- BW = 50GHz after equalization

3.9m Cable – Equalized Eye



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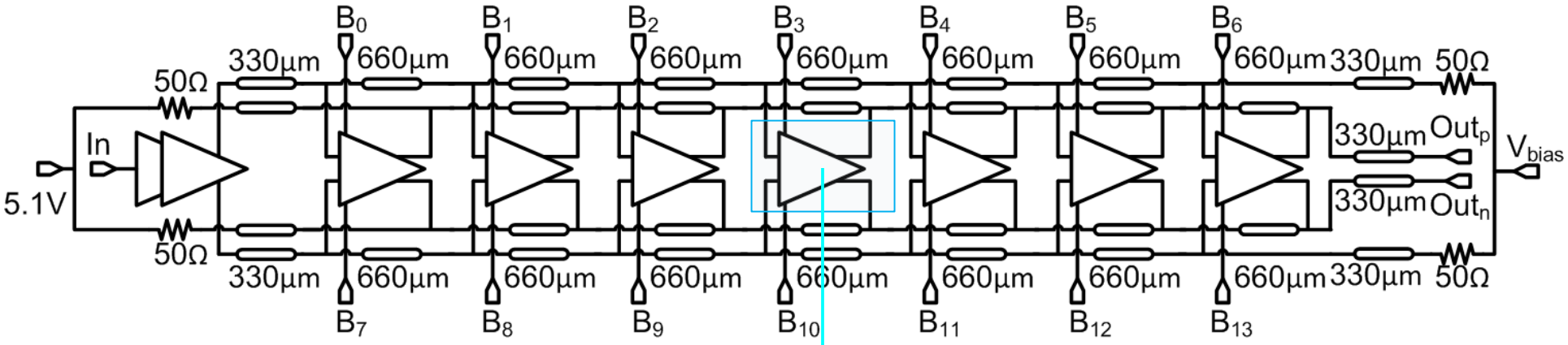
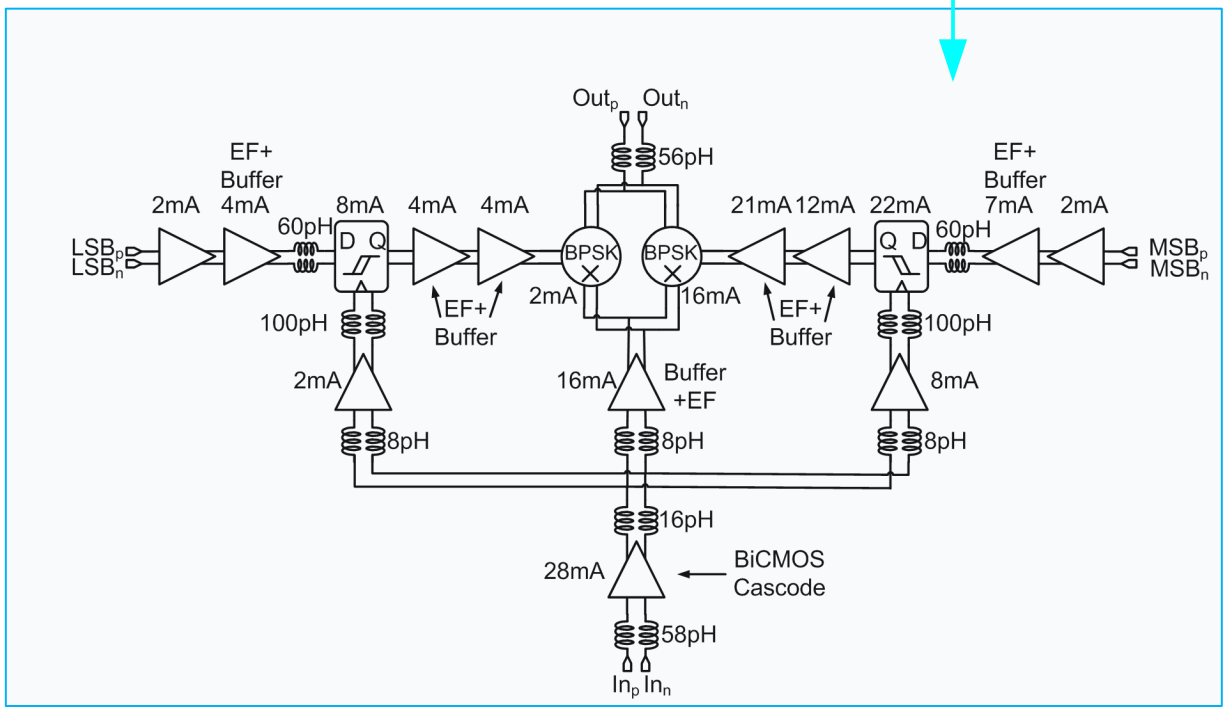
Outline

mm-wave Transceivers

- Broadband and Tuned mm-wave DAC Transmitters
- 150-170 GHz Transceiver with 3 on Die Antennas
- 143-150 GHz SUCCESS Sensor with BIST
- Potential Solutions for H-Band

6Vpp, 50-GS/sec, 6-bit RZ-DAC





P_{DC} = 5W

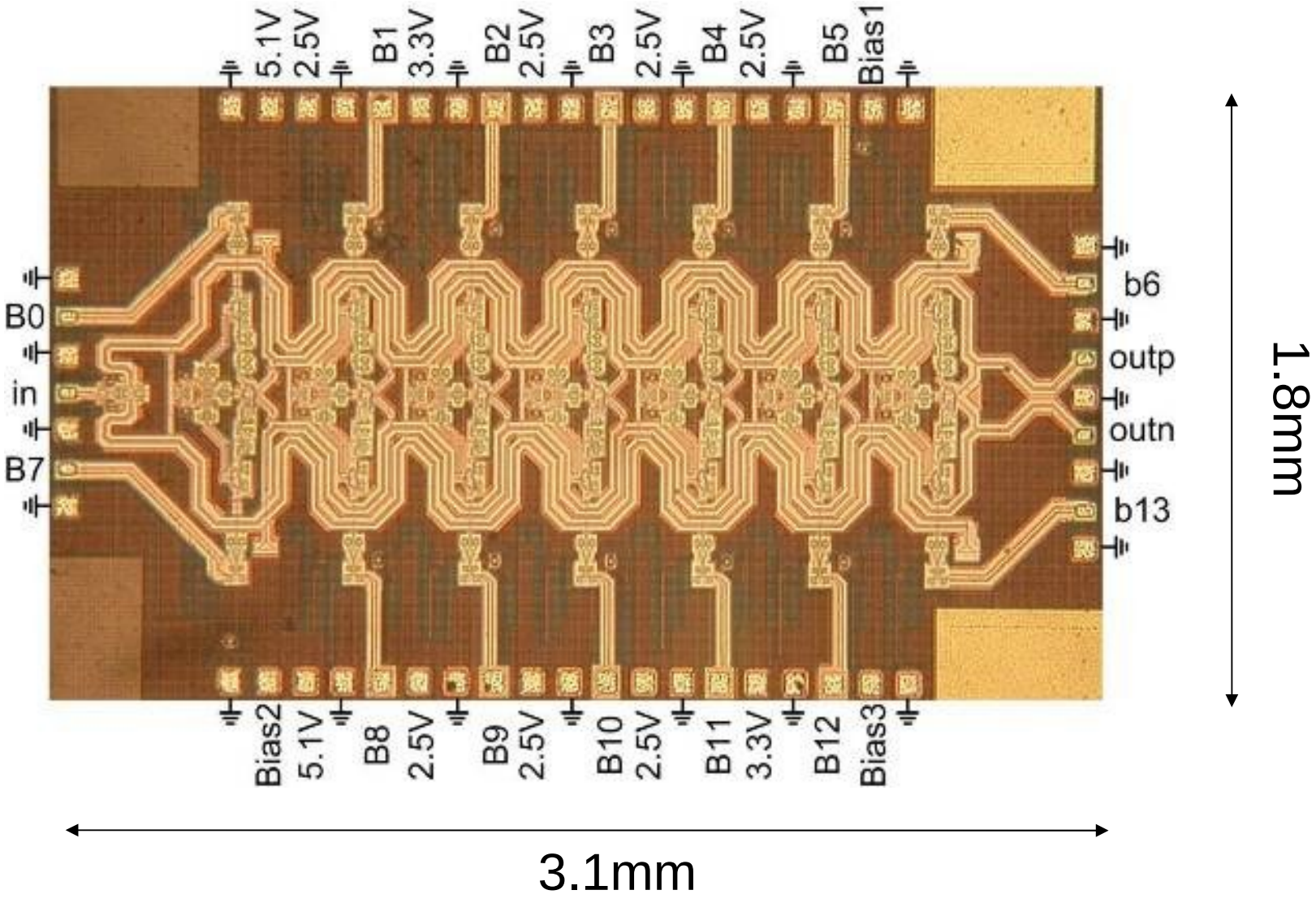
Output stage = 1.2W

14 CML bit streams at 50 Gb/s => 3.8W

[A. Balteanu IMS 2012]

- Distributed Segmentation: 7 MSBs and 7 LSBs in 8:1 size ratio
- Each bit retimed at up to 50 GHz

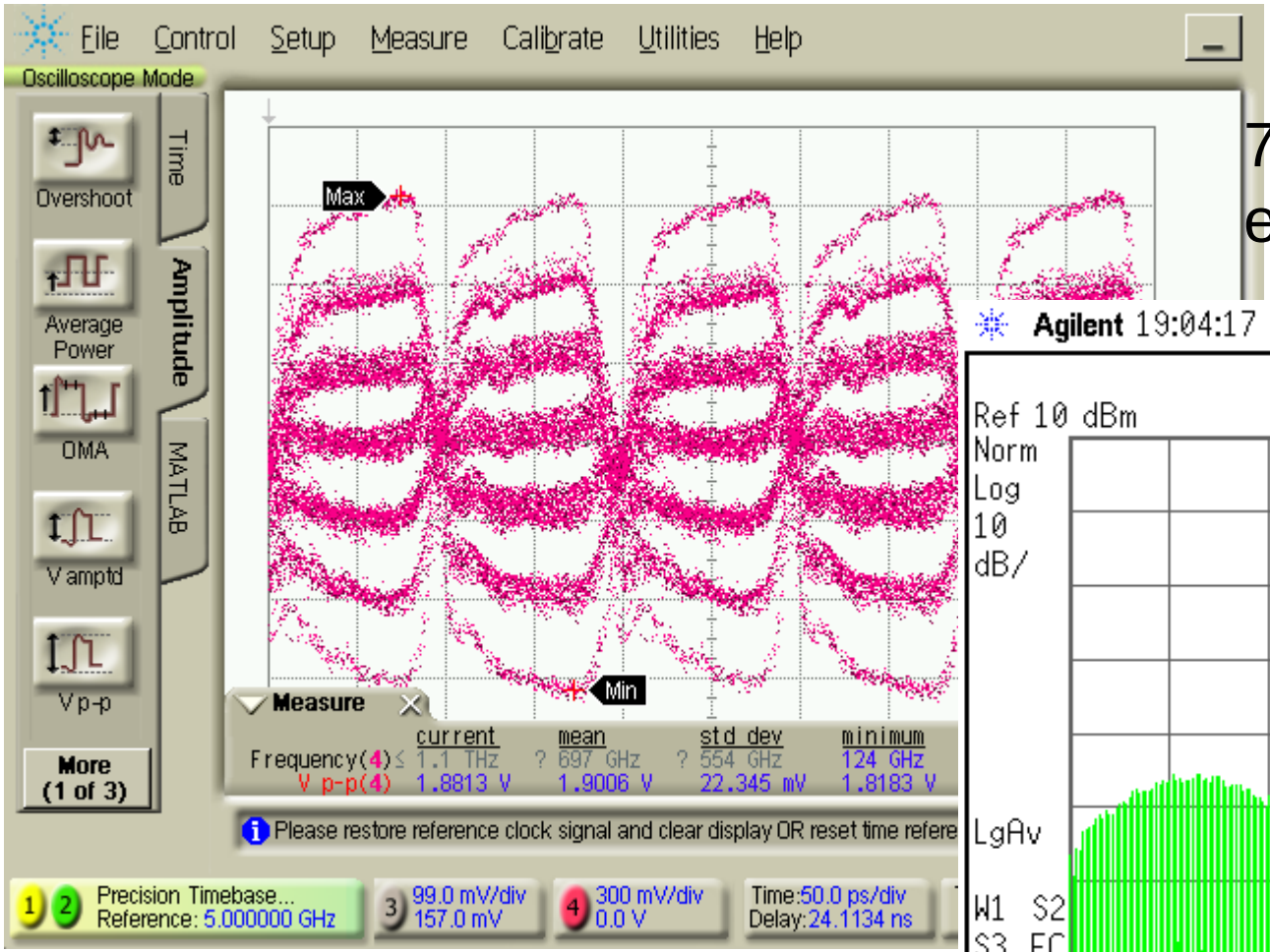
Die Photo (V1)



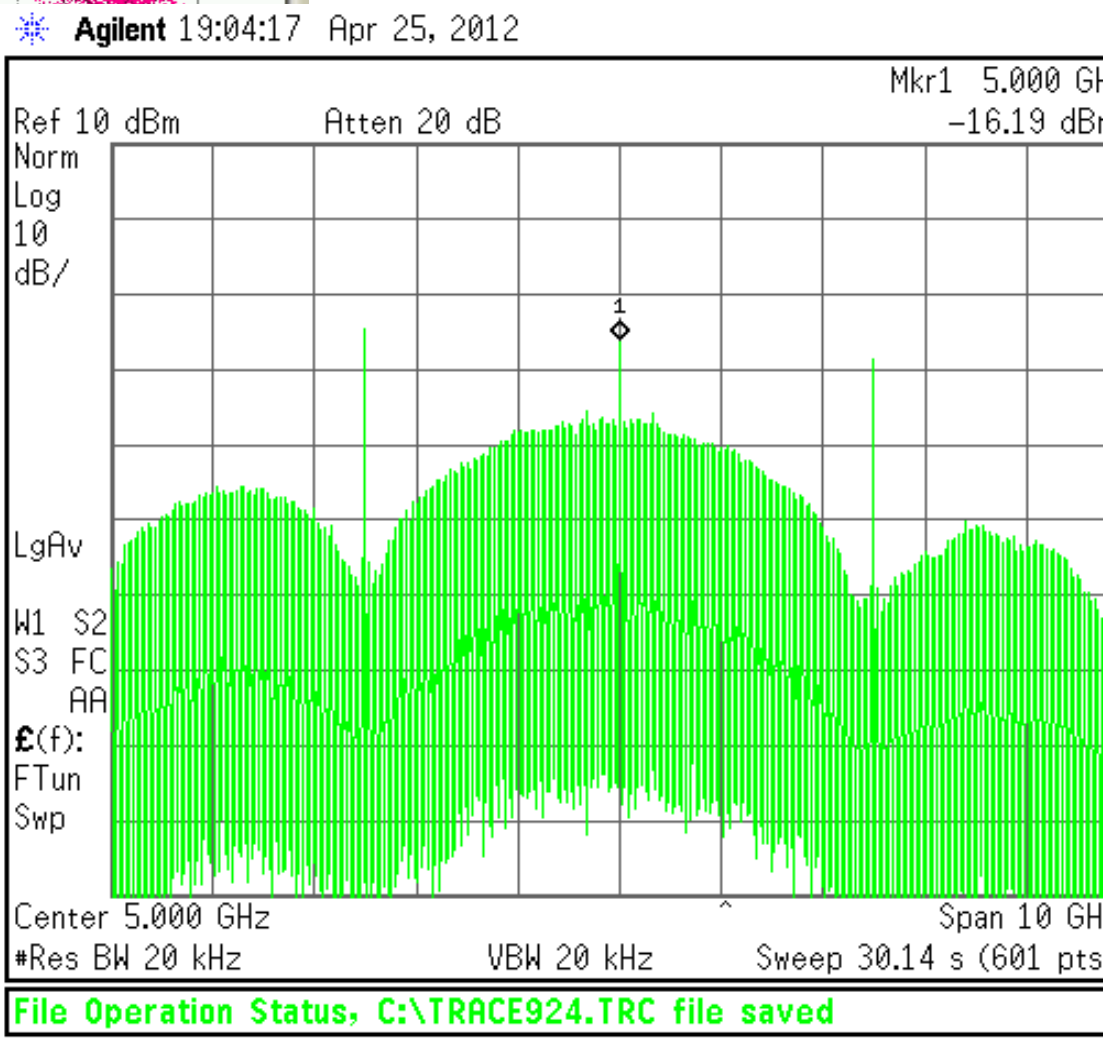
ST's 130-nm SiGe BiCMOS Production Process

f_T/f_{MAX} = 230/280 GHz

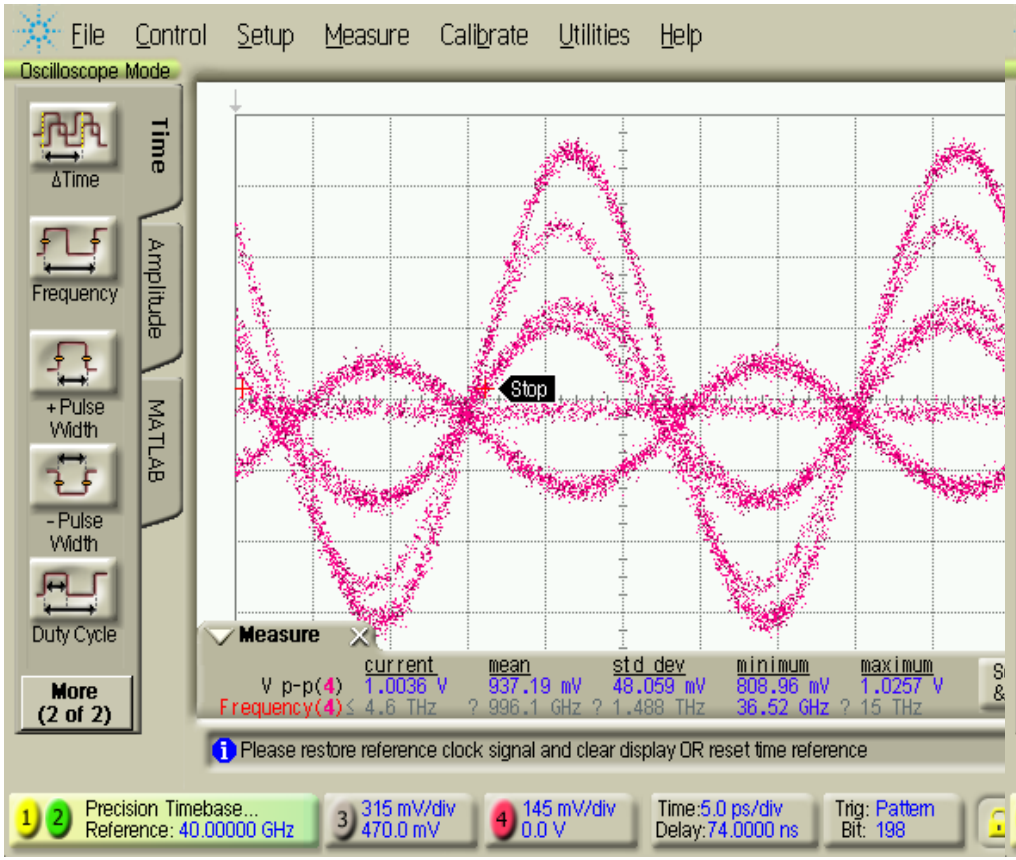
5 GHz large signal swing, spectra

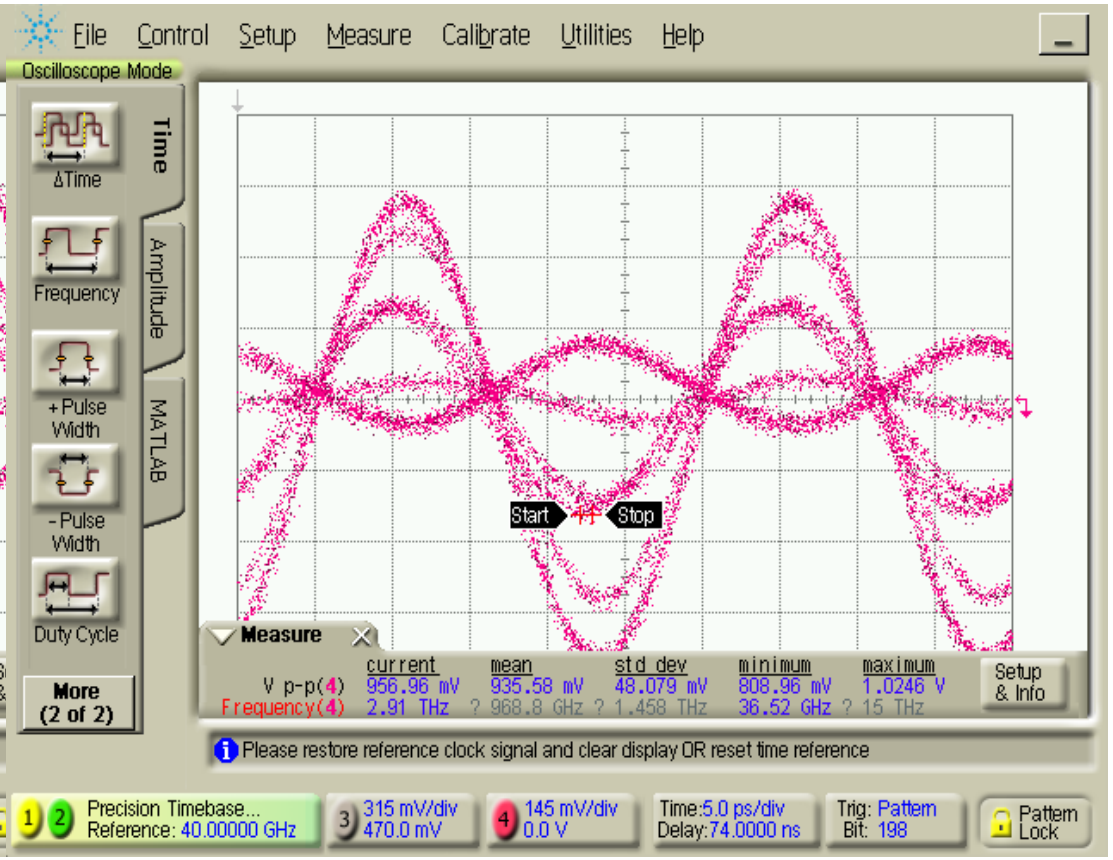


7 MSBs switching at 2.5Gb/s each



40 GHz with Sign Reversal

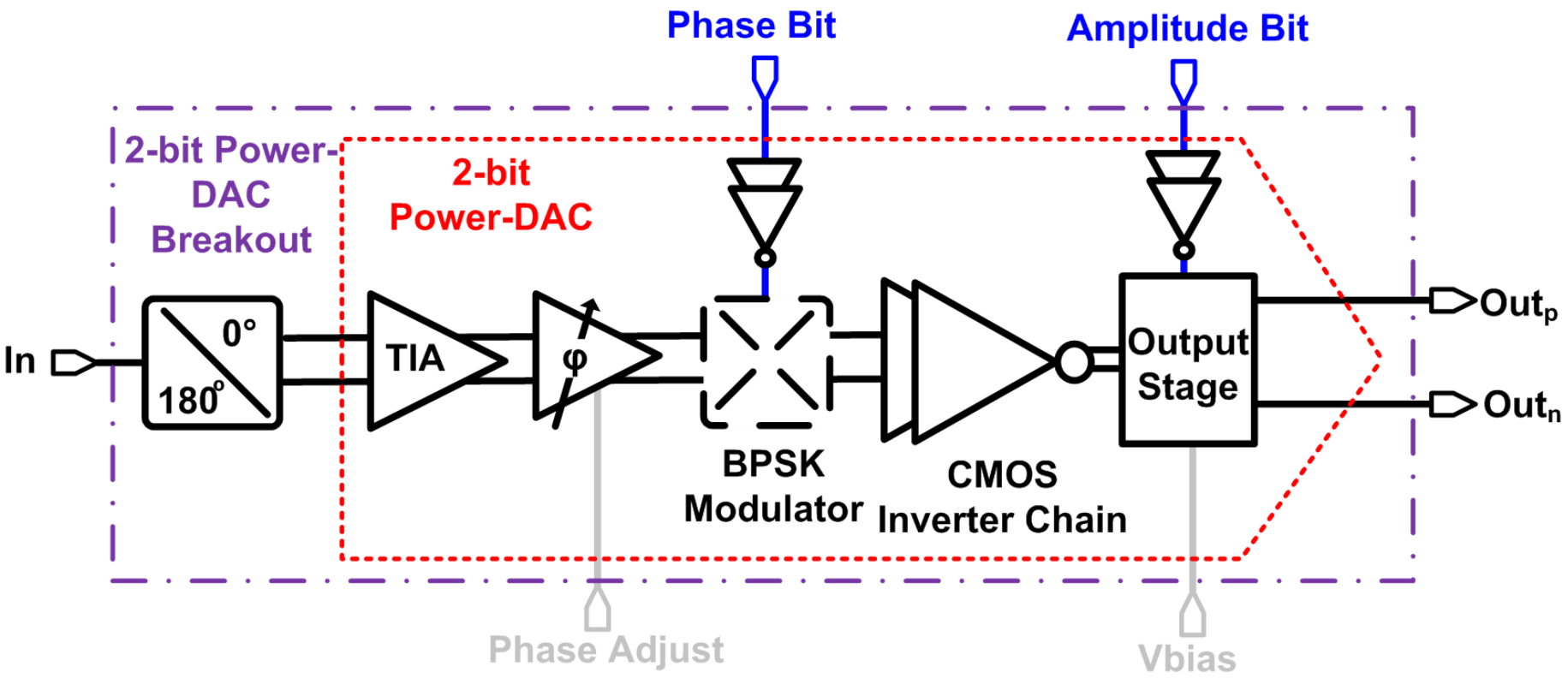




4 MSB's switching at 1.25 Gb/s
Retimed at 40 GHz
all other MSB's = "0"

4 MSB's switching at 1.25 Gb/s
Retimed at 40 GHz
all other MSB's = "1"

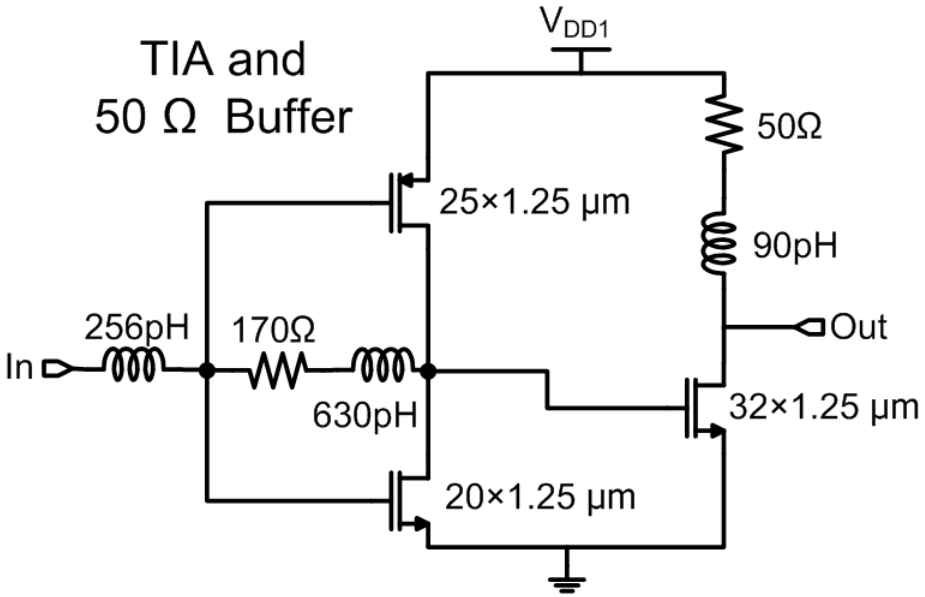
Power-DAC Cell with N-MOS output stage

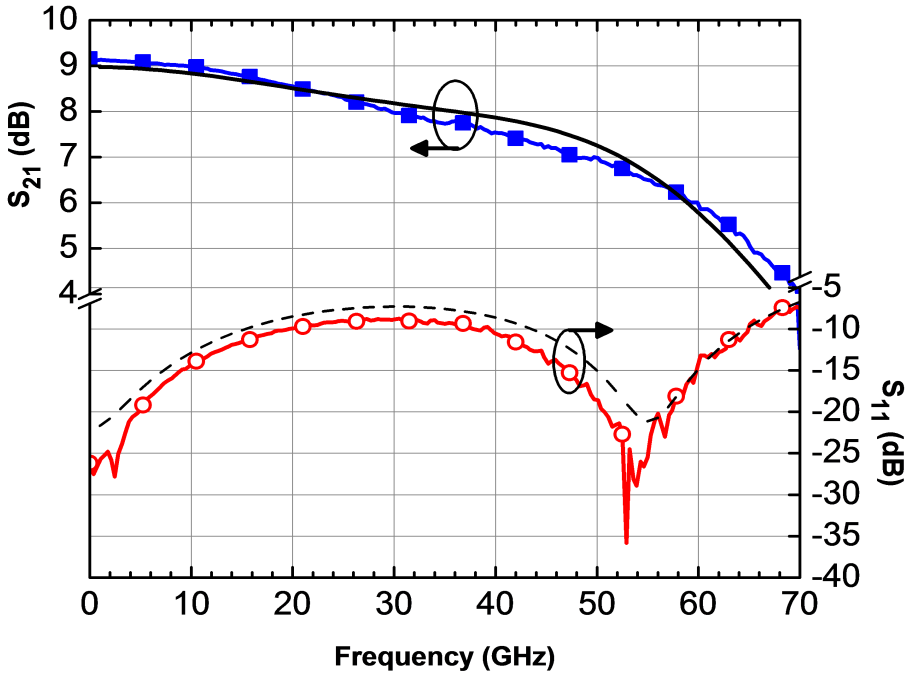


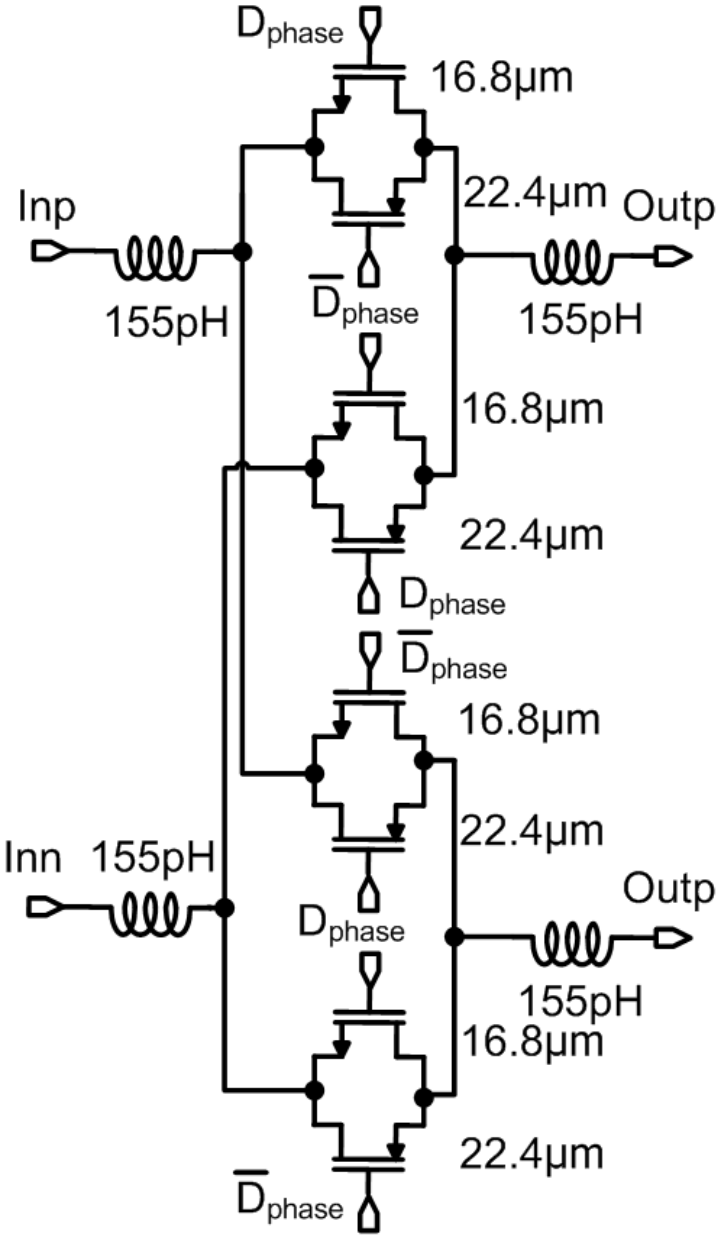
- DC – 50 GHz in 45-nm SOI
- CMOS inverter based. Purely digital
- Scalable to 240 GHz using tuned LO path

[A. Balteanu RFIC-2012]

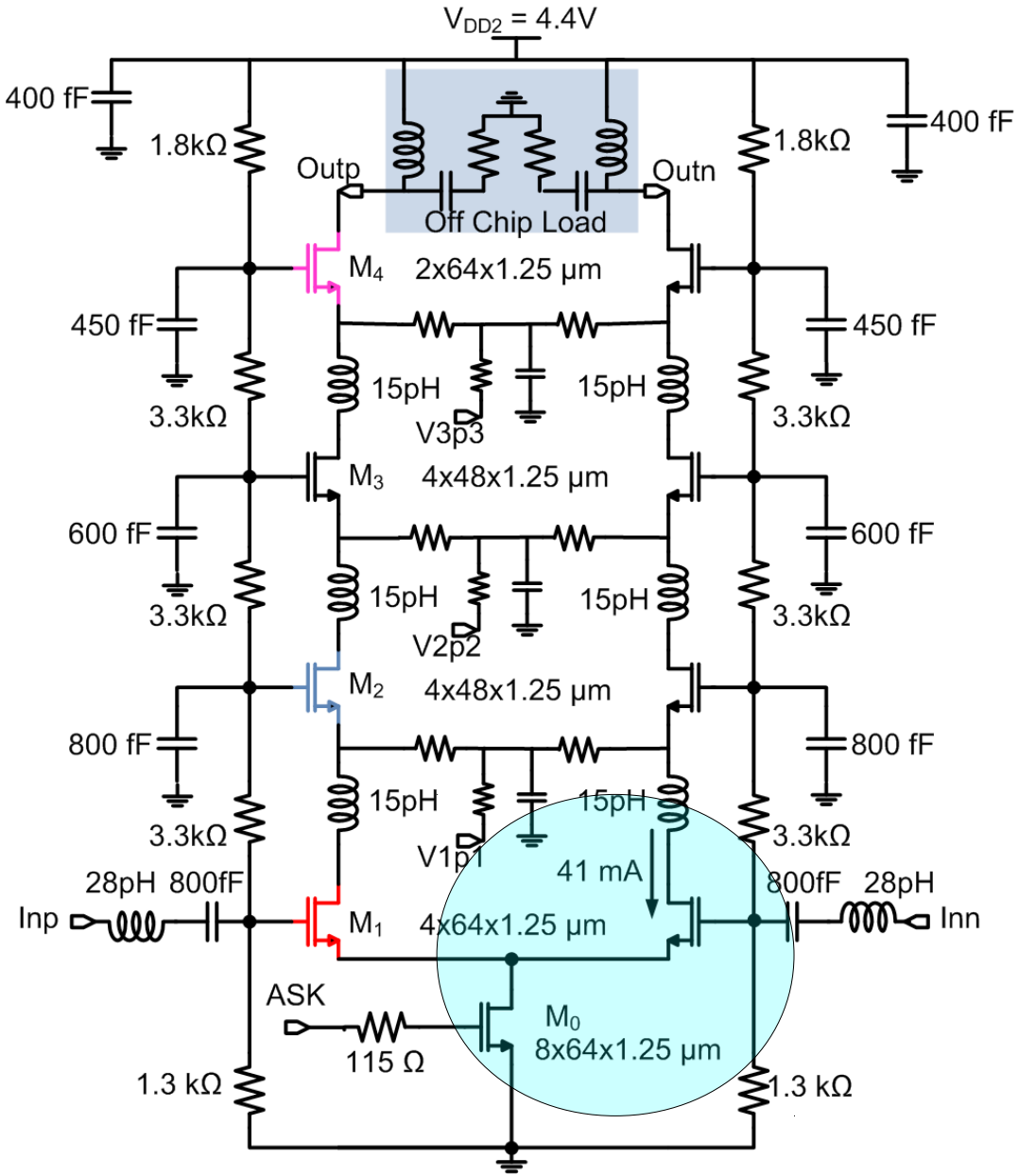
TIA, BPSK Modulator

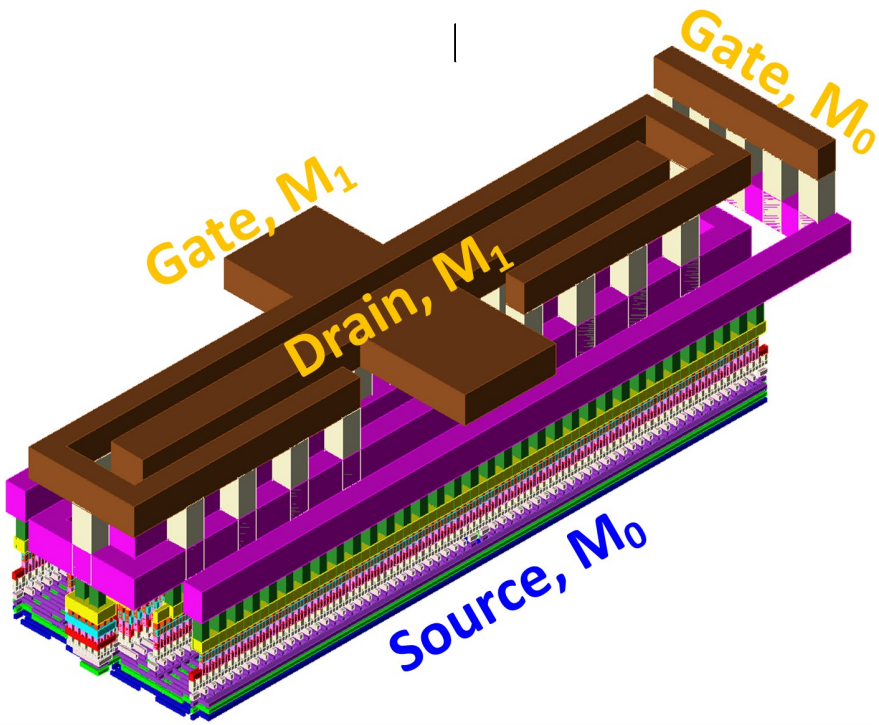




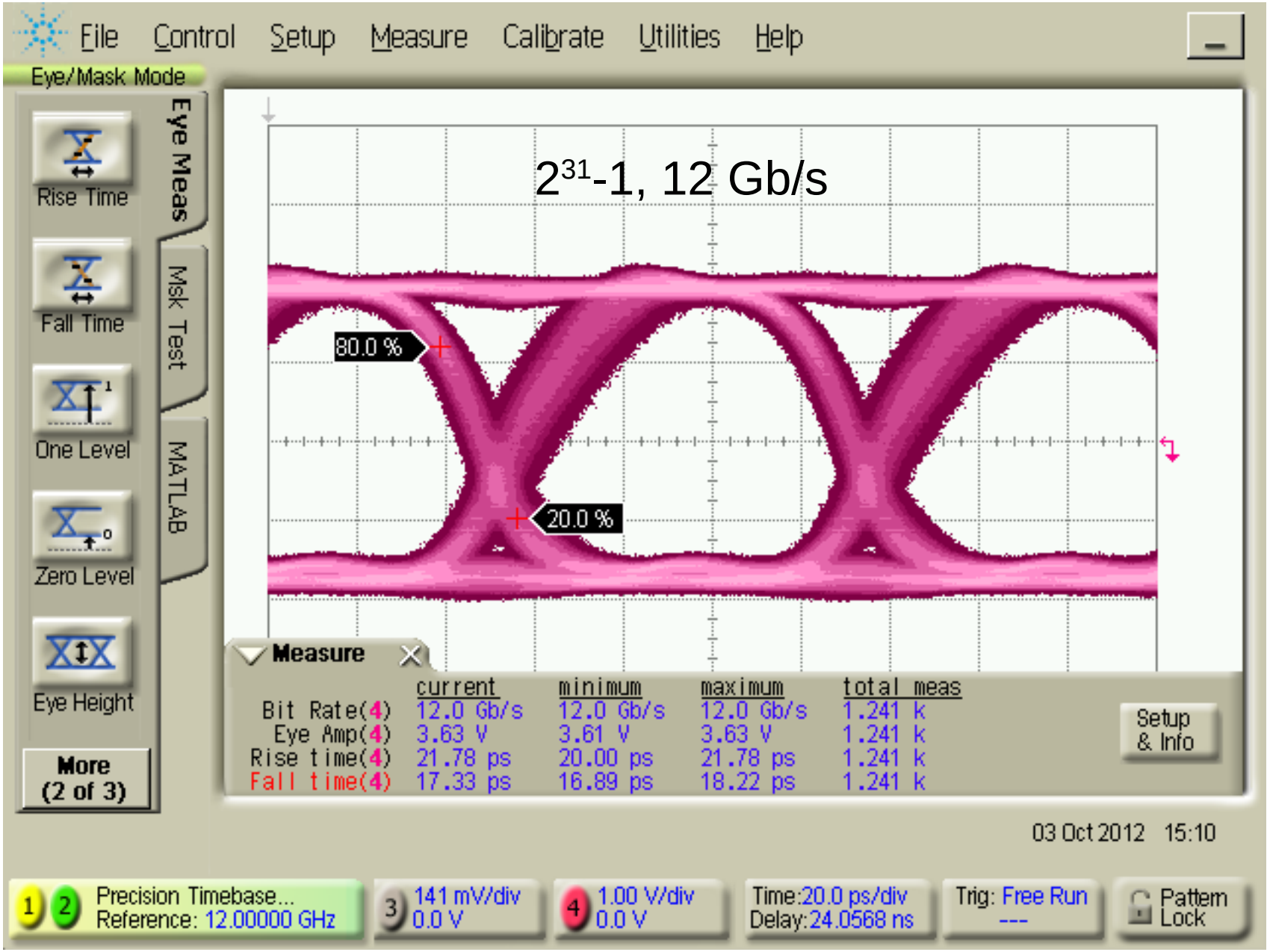


Differential output stage with On-Off switch

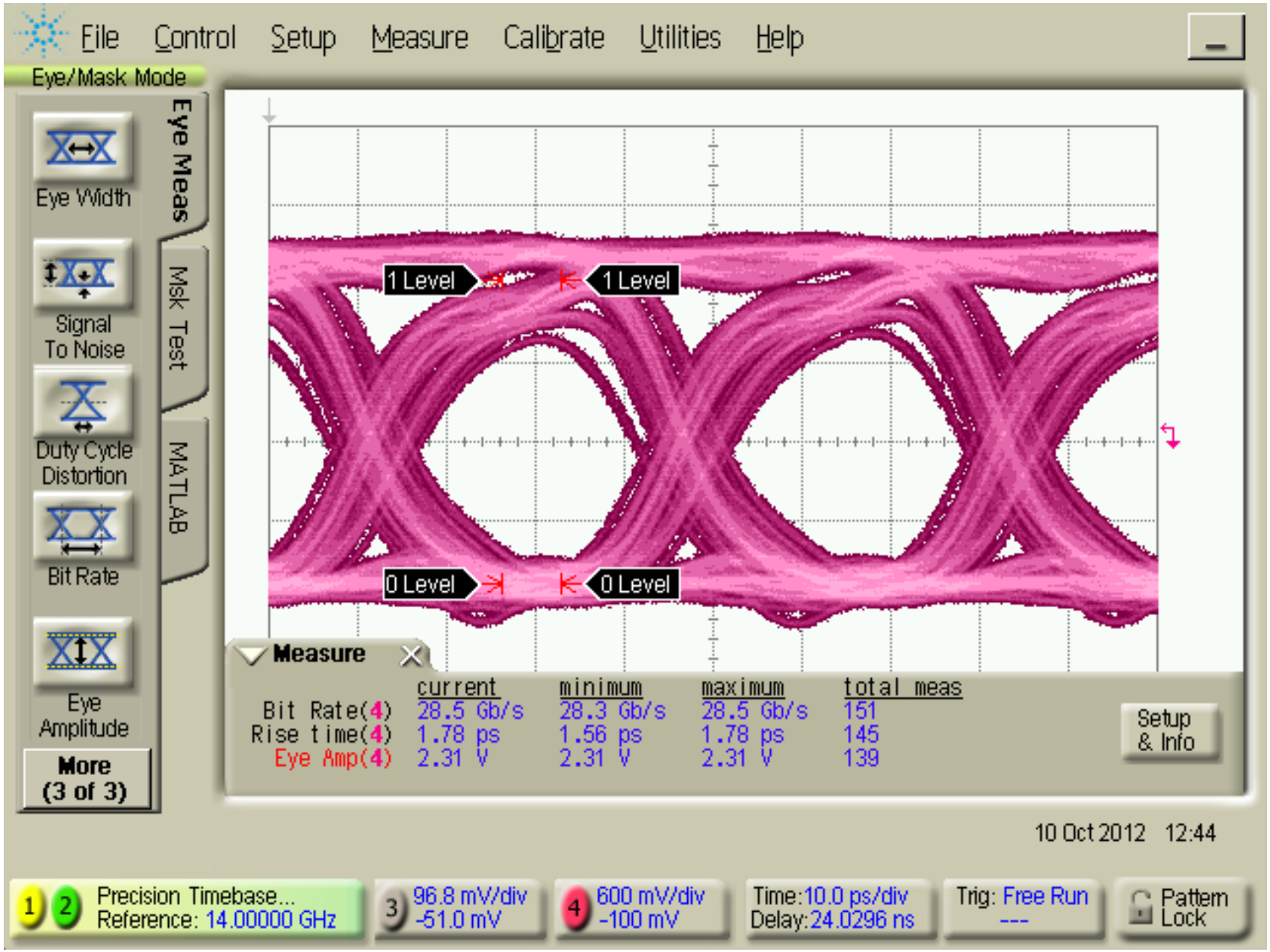




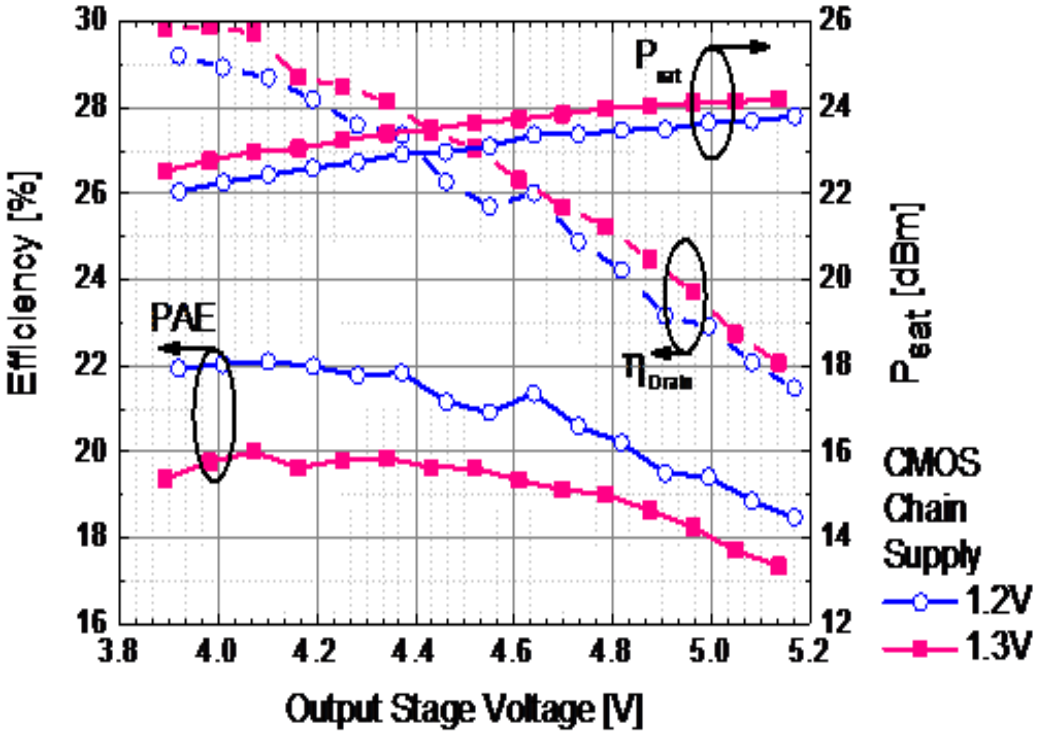
4-Stacked n-MOS Cascode

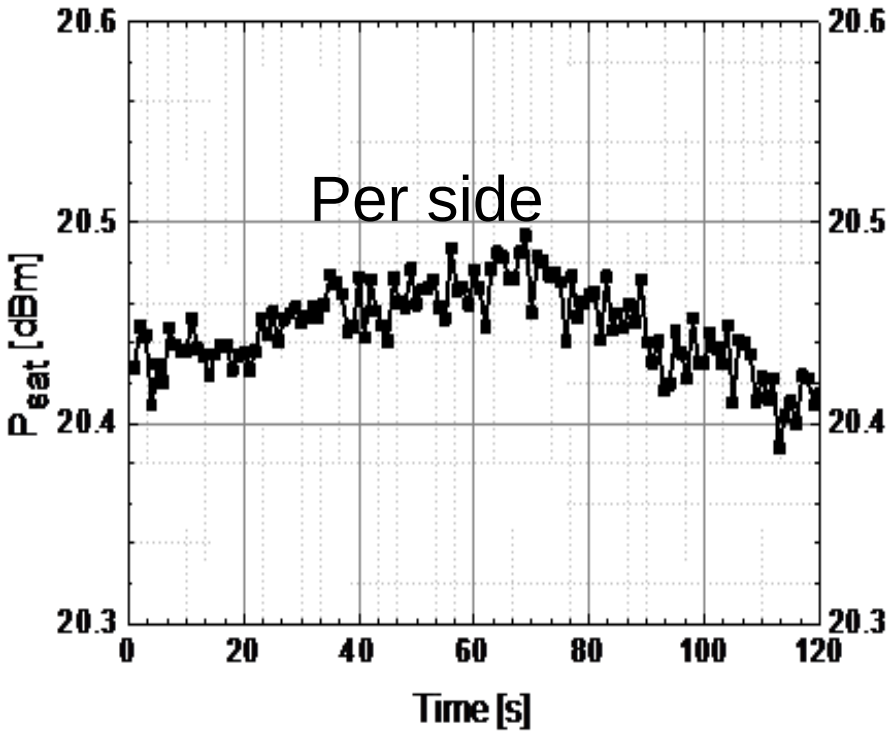


DAC Cell: 28 Gb/s Eyes



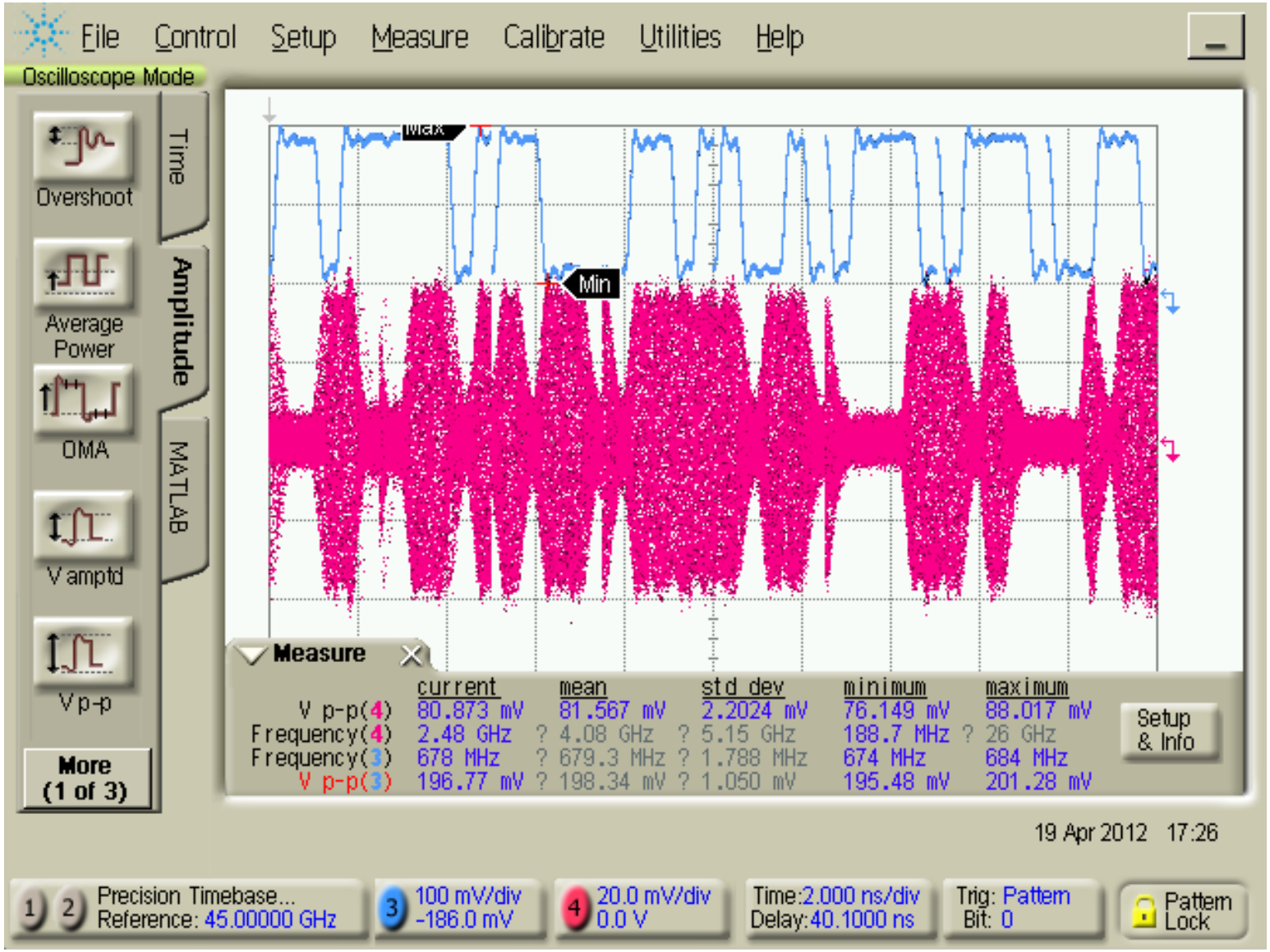
Pout of 45-GHz DAC cell vs. time



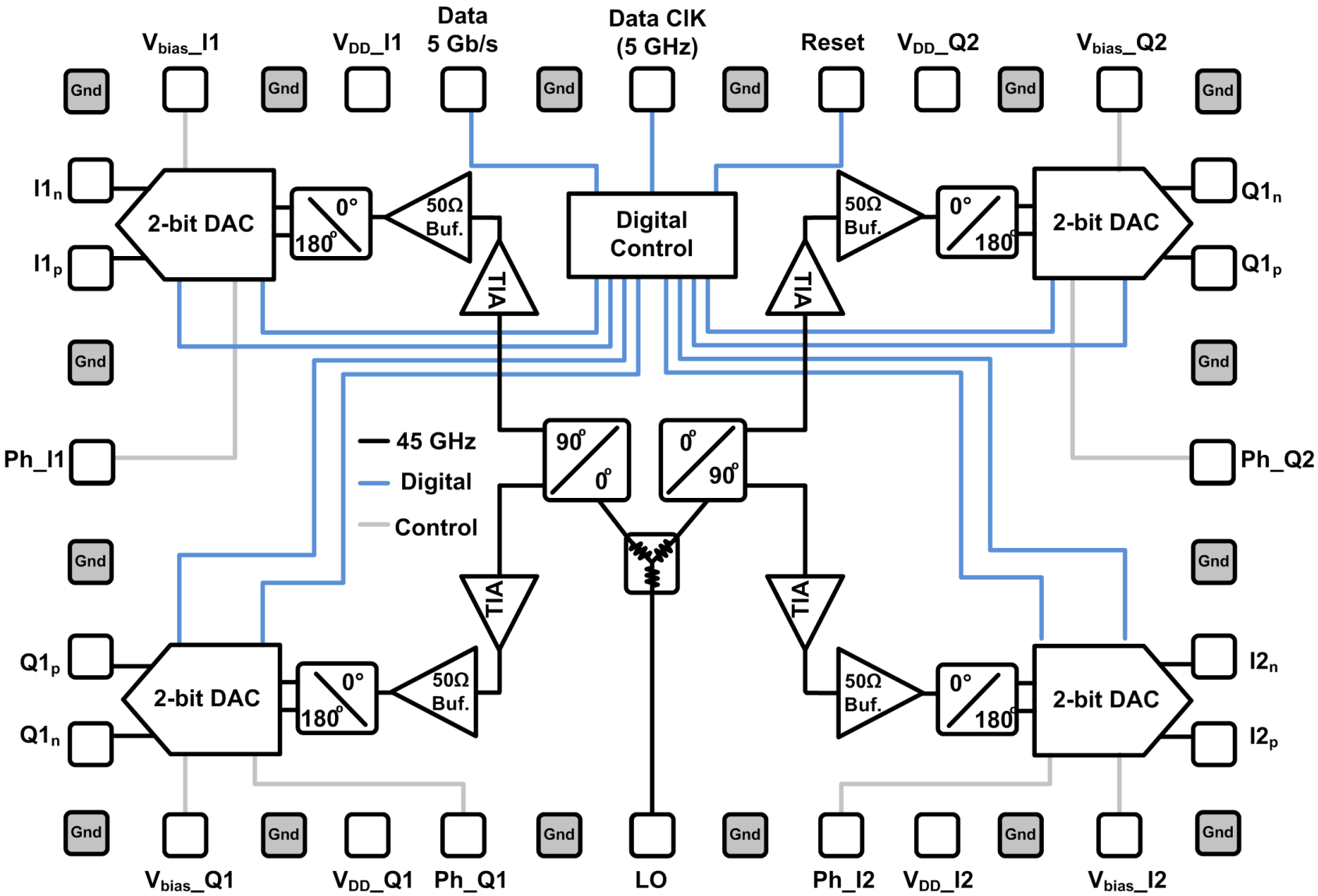


- P_{sat} =23 dBm, η_{Drain}=30%, PAE=20%, 4.1V/1.3V
- P_{sat} =24.3 dBm, η_{Drain} =22%, PAE=16.3%. 5.1V/1.4V

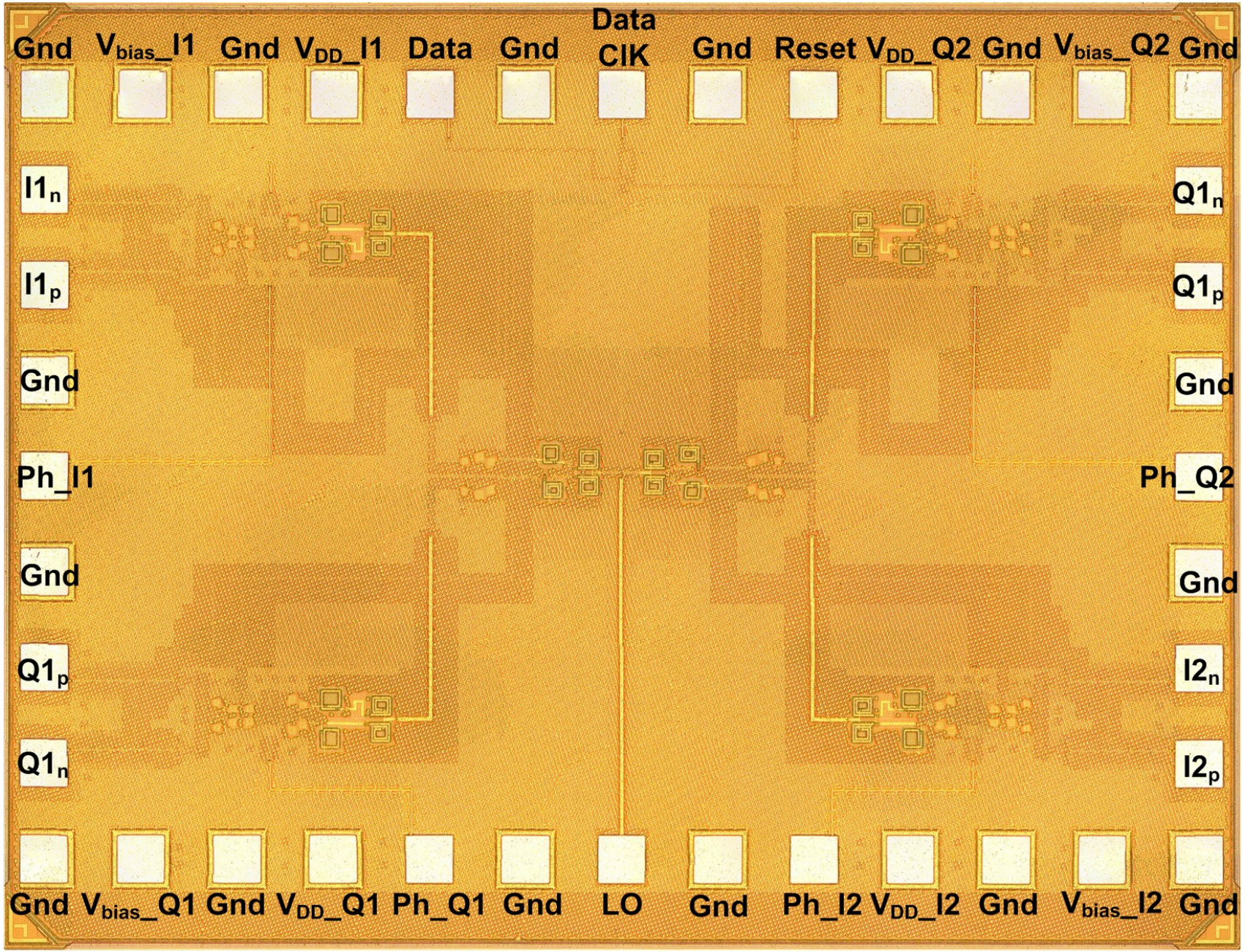
2-Gb/s ASK+ 2-Gbs BPSK Mod of 45-GHz Carrier



45-GHz 8-bit IQ DAC chiplet



Die photo

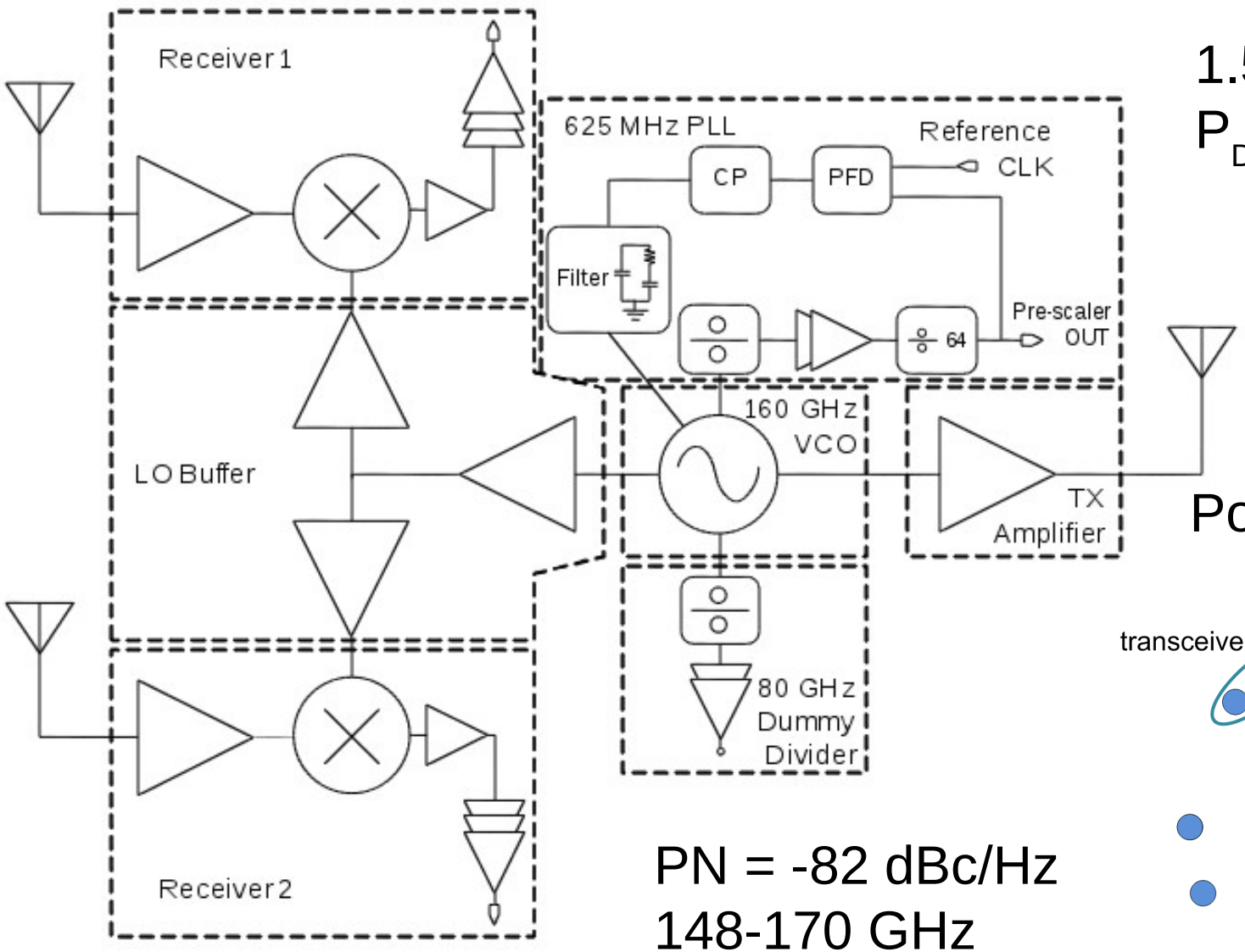

Gnd
V_{bias}_I1
Gnd
V_{DD}_I1
Data
Gnd
Data CIK
Gnd
Reset
V_{DD}_Q2
Gnd
V_{bias}_Q2
Gnd
$I1_n$
$I1_p$
Gnd
Ph_I1
Gnd
$Q1_p$
$Q1_n$
$Q1_n$
$Q1_p$
Gnd
Ph_Q2
Gnd
$I2_n$
$I2_p$
Gnd
V_{bias}_Q1
Gnd
V_{DD}_Q1
Ph_Q1
Gnd
LO
Gnd
Ph_I2
V_{DD}_I2
Gnd
V_{bias}_I2
Gnd

Outline

mm-wave Transceivers

- Broadband and Tuned mm-wave DAC Transmitters
- 150-170 GHz Transceiver with 3 on Die Antennas
- 143-150 GHz Sensor with BIST
- Potential Solutions for H-Band

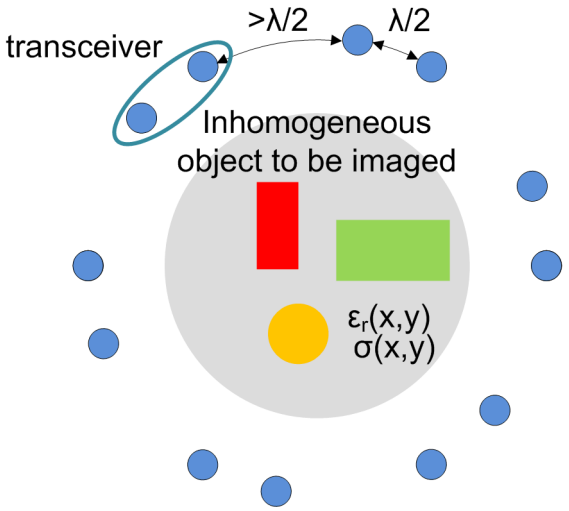
Dual Receive Channel Transceiver



1.5/2.5/3/3.6V

P_D = 1.8 W

Pout = 1 dBm



PN = -82 dBc/Hz

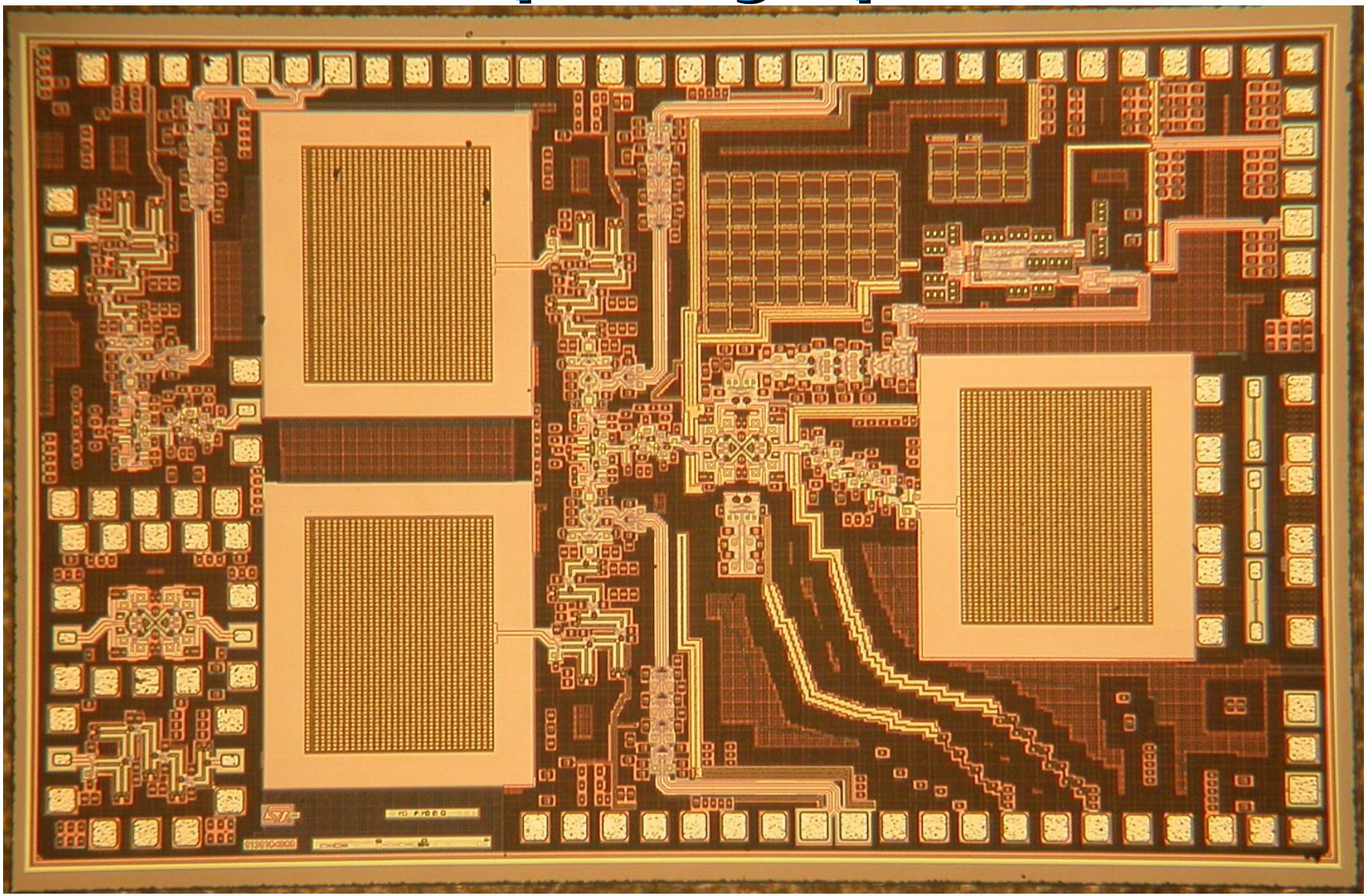
148-170 GHz

RX Gain = 27 dB

NF = 12 dB

[I. Sarkas et al., MIKON-2012]

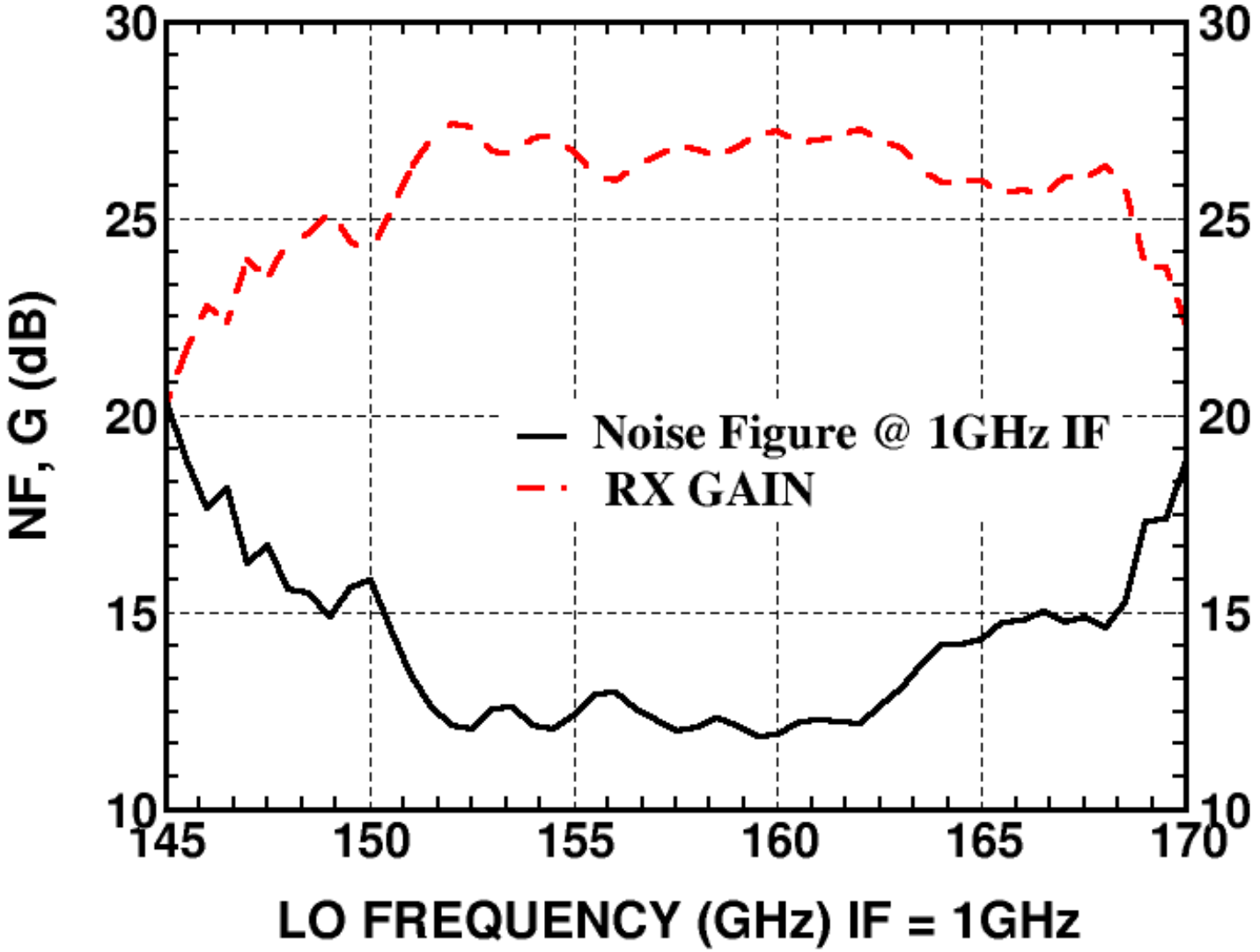
Die photograph



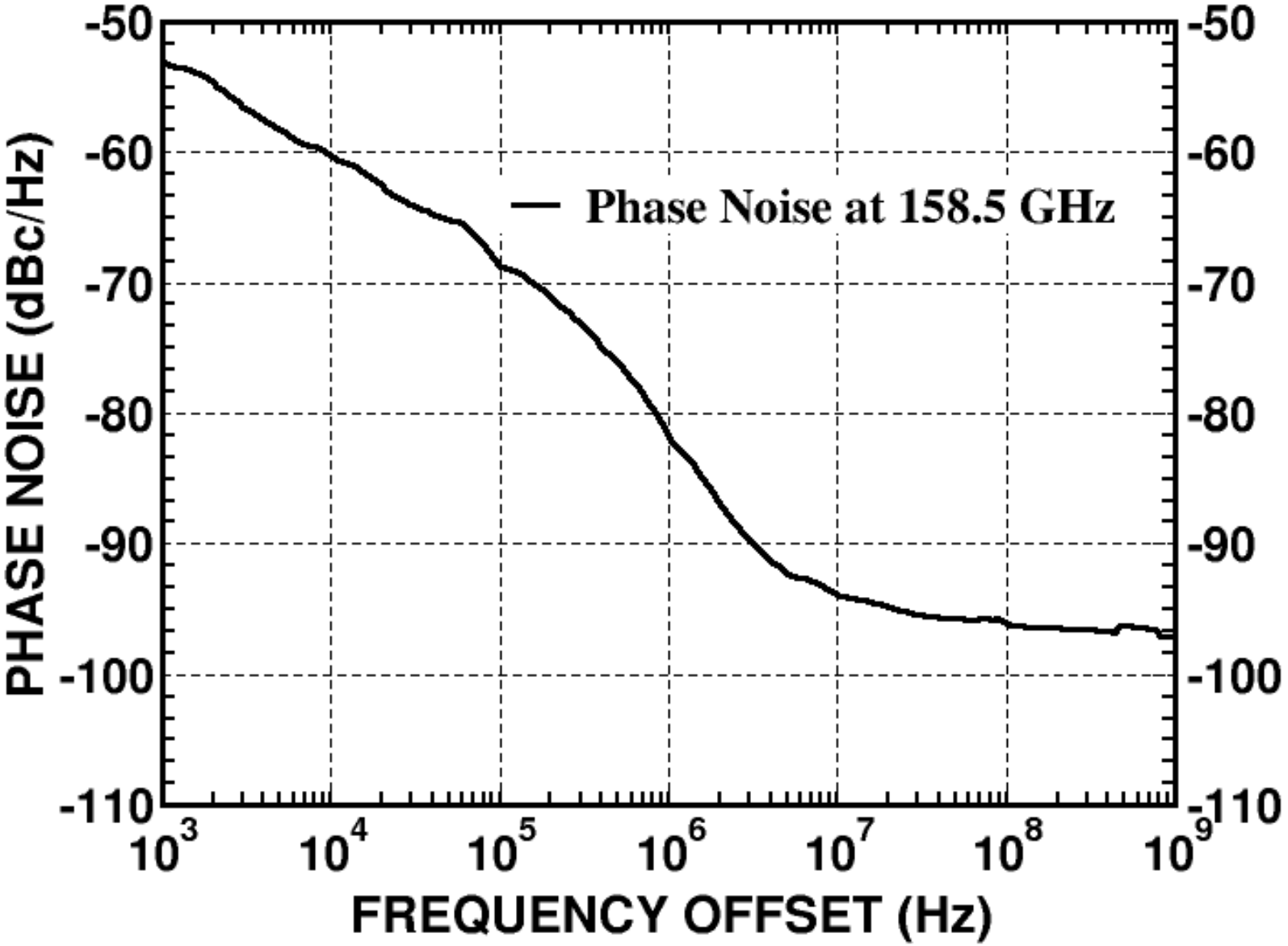
Chip: 2.1mm×2.9mm

130-nm BiCMOS9MW: SiGe HBT f_T= 230 GHz, f_{MAX} = 280 GHz

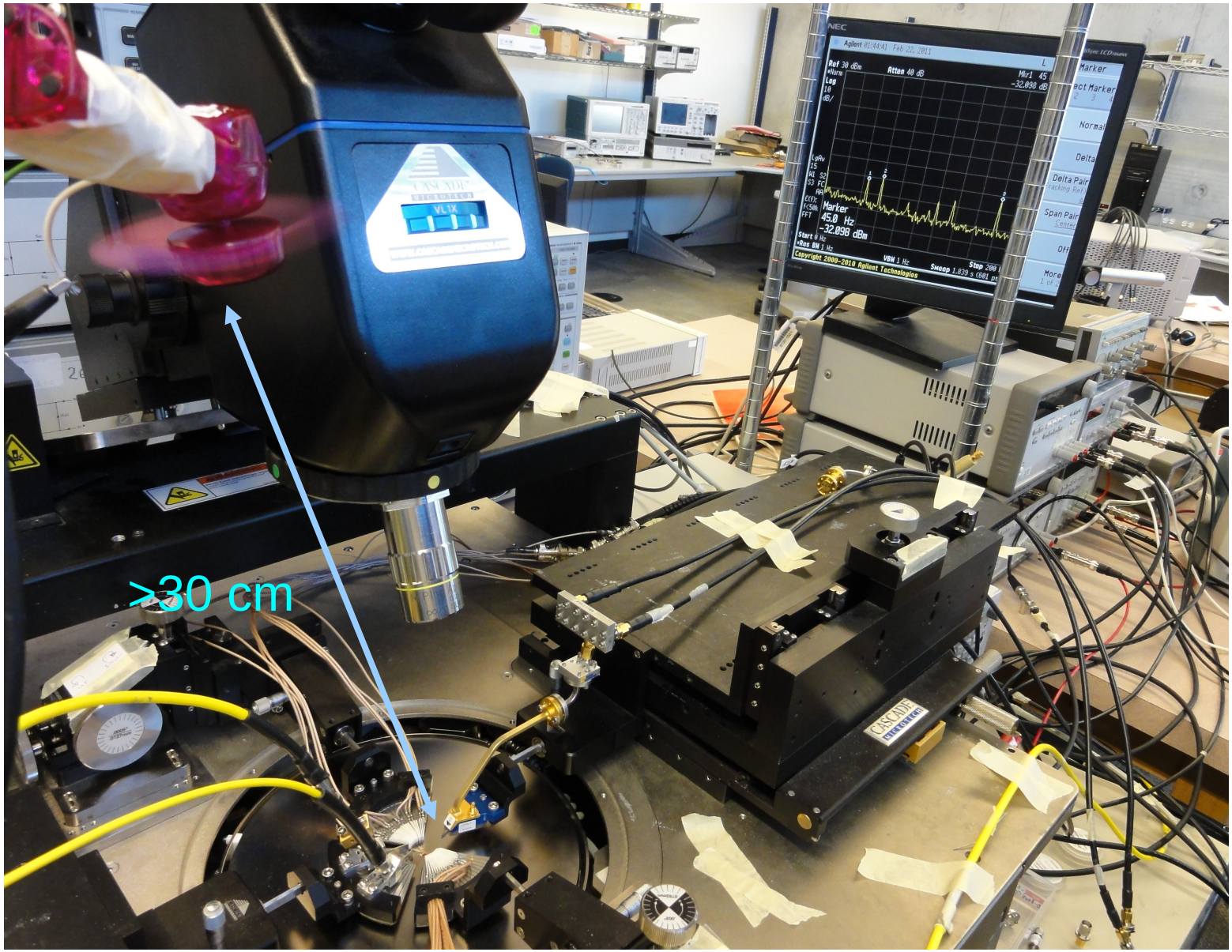
RX Breakout Gain and Noise Figure



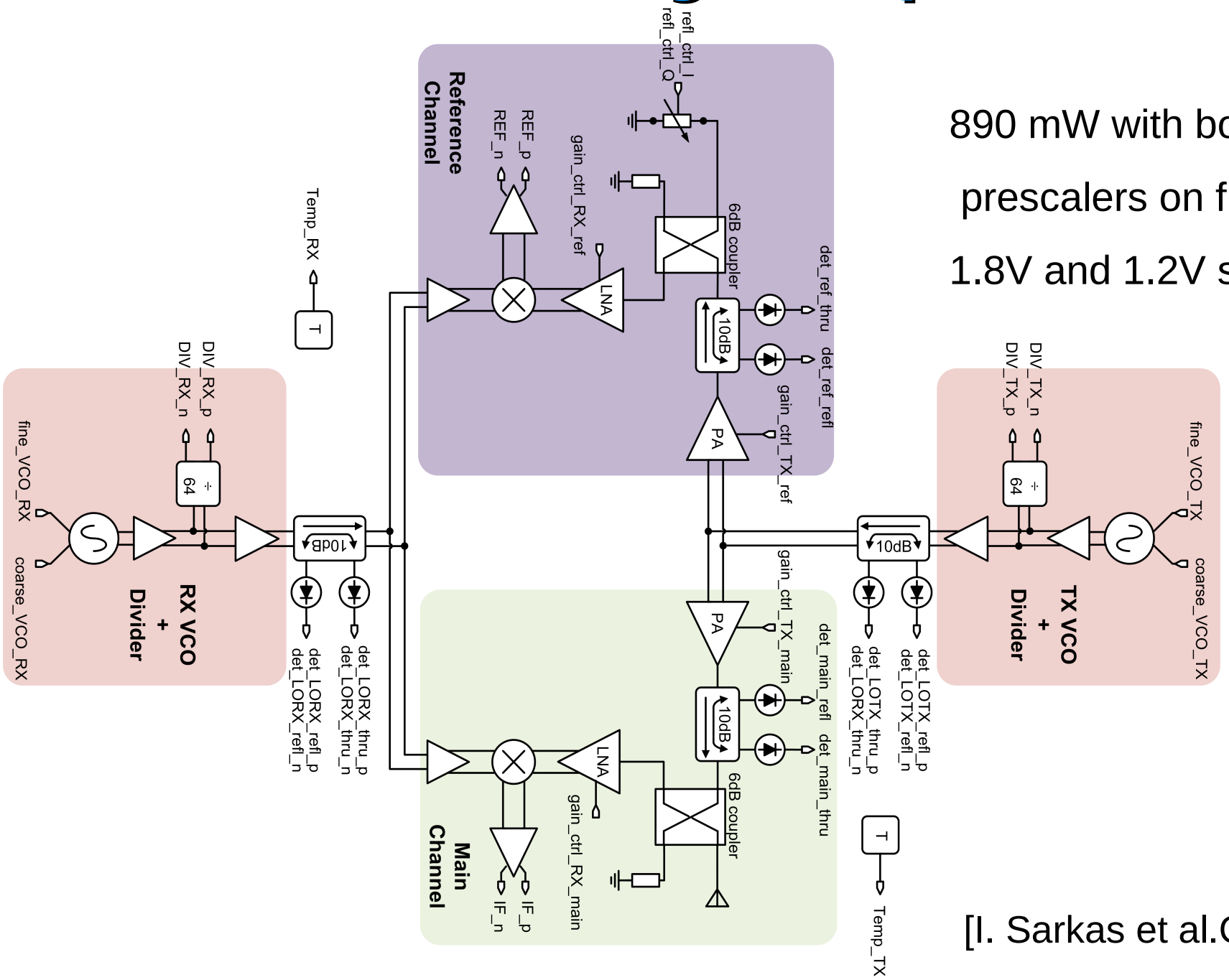
Transceiver PLL Phase Noise



On-die Doppler Test



Monostatic single-chip sensor



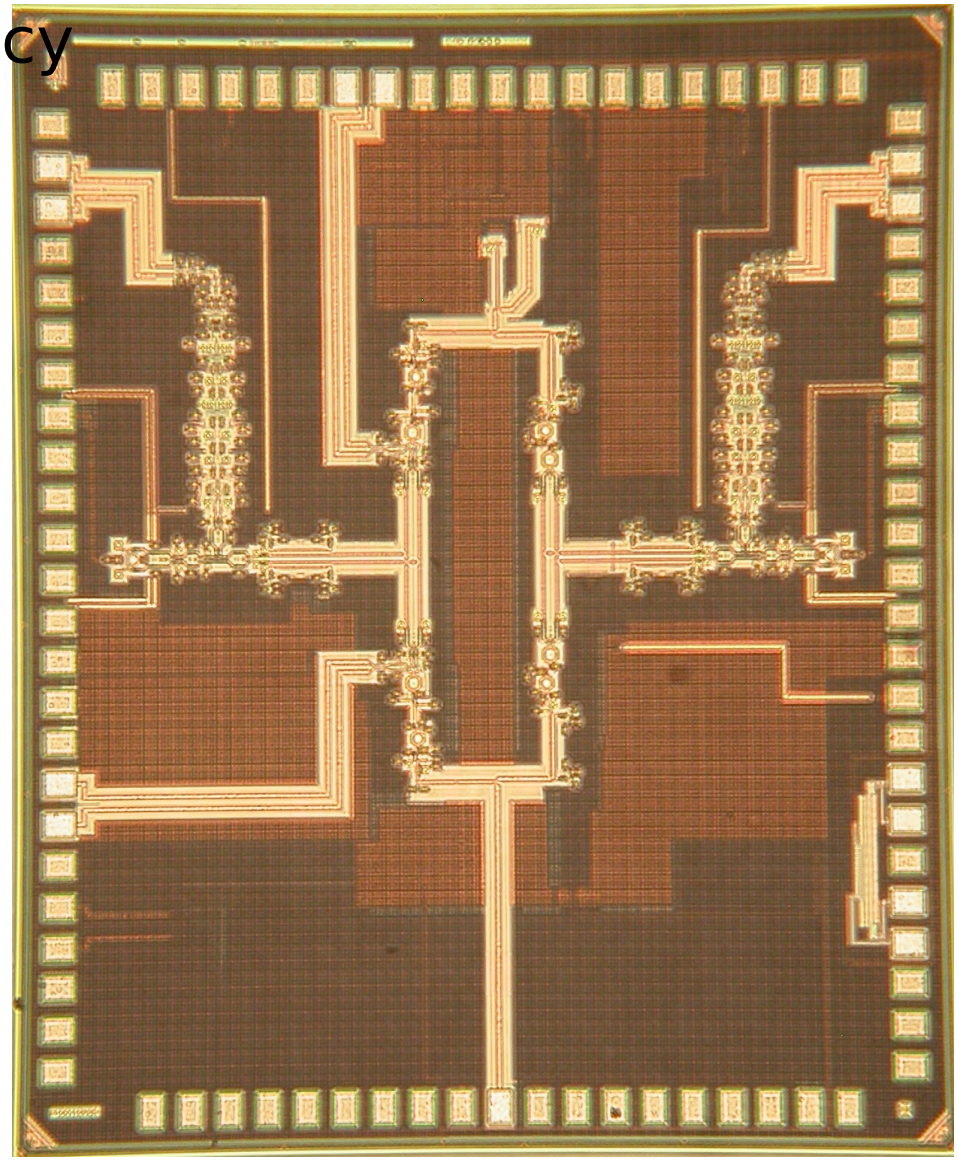
890 mW with both prescalers on from 1.8V and 1.2V supplies

[I. Sarkas et al.CSICS 2012]

Layout and performance summary

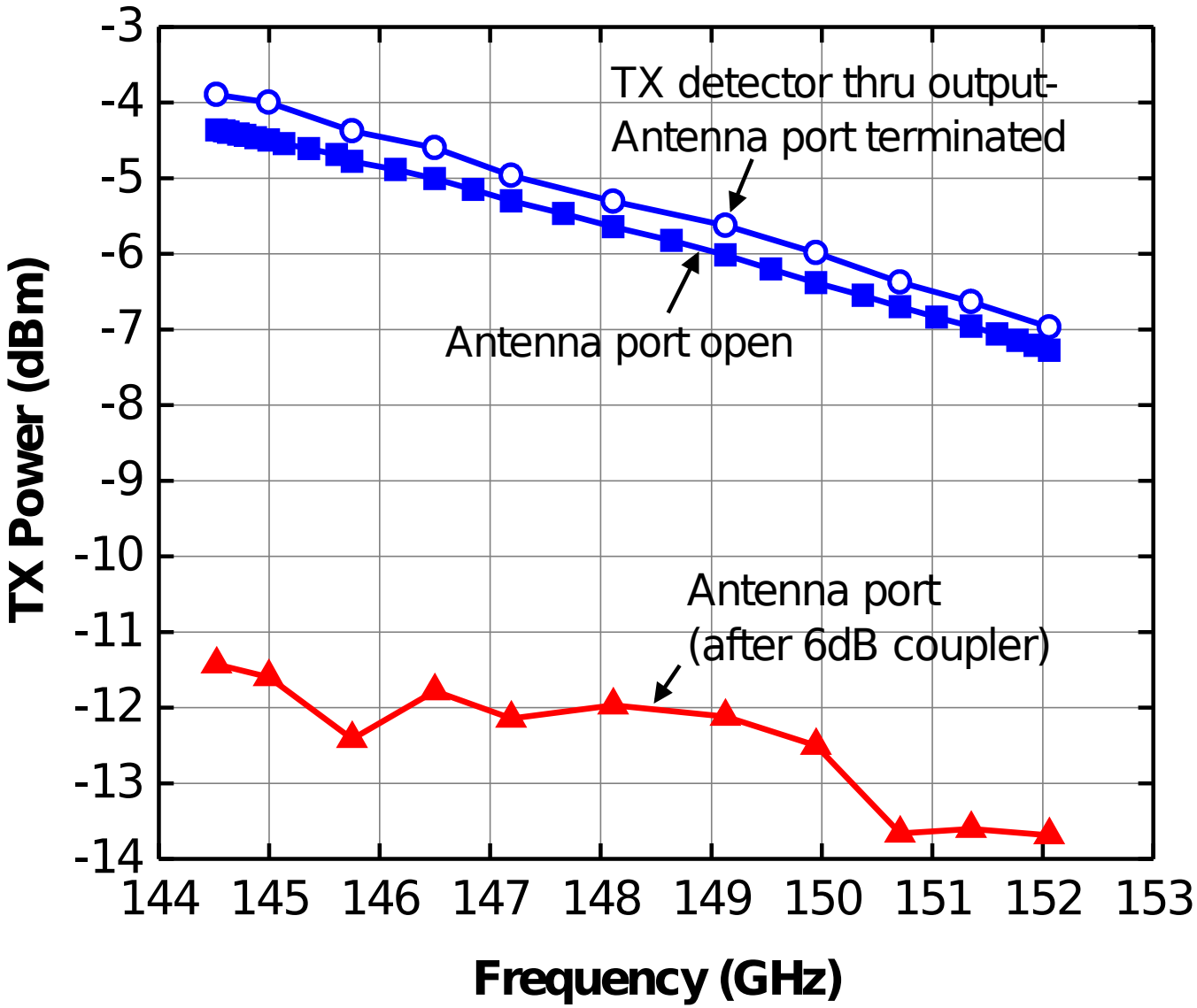
- Tuning range 142-152 GHz
- Highest fundamental frequency transceiver
- NF<10 dB, Pout >-6 dBm.
- PN < -83 dBc/Hz at 1MHz

2.6mmx2.3mm



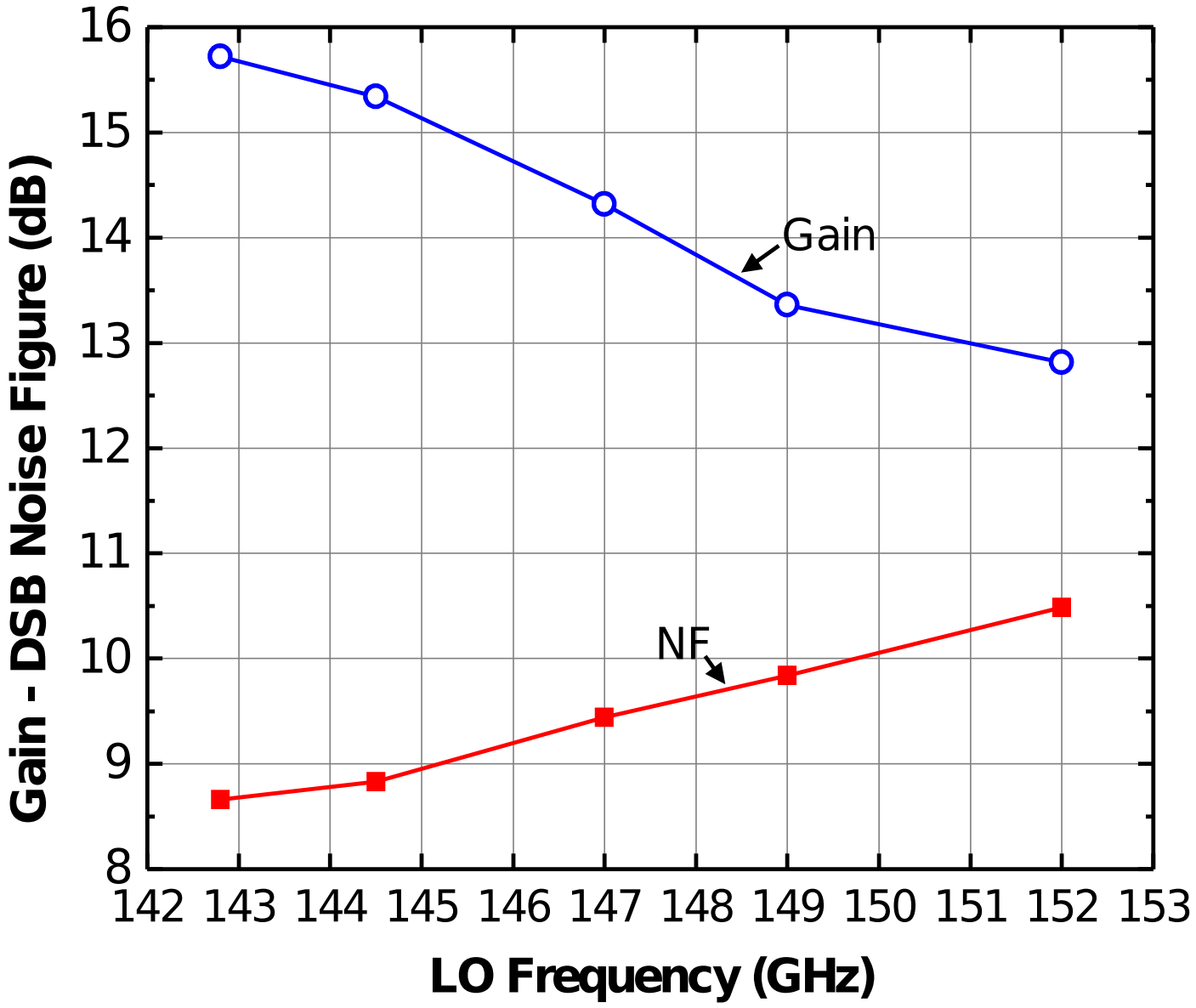
Block	Count	Power (mW)
VCO	2	2×76
Divider chain	1	145
LO dist	1	115
TX	1	230
RX	1	165
Total		**807**

Measured output power



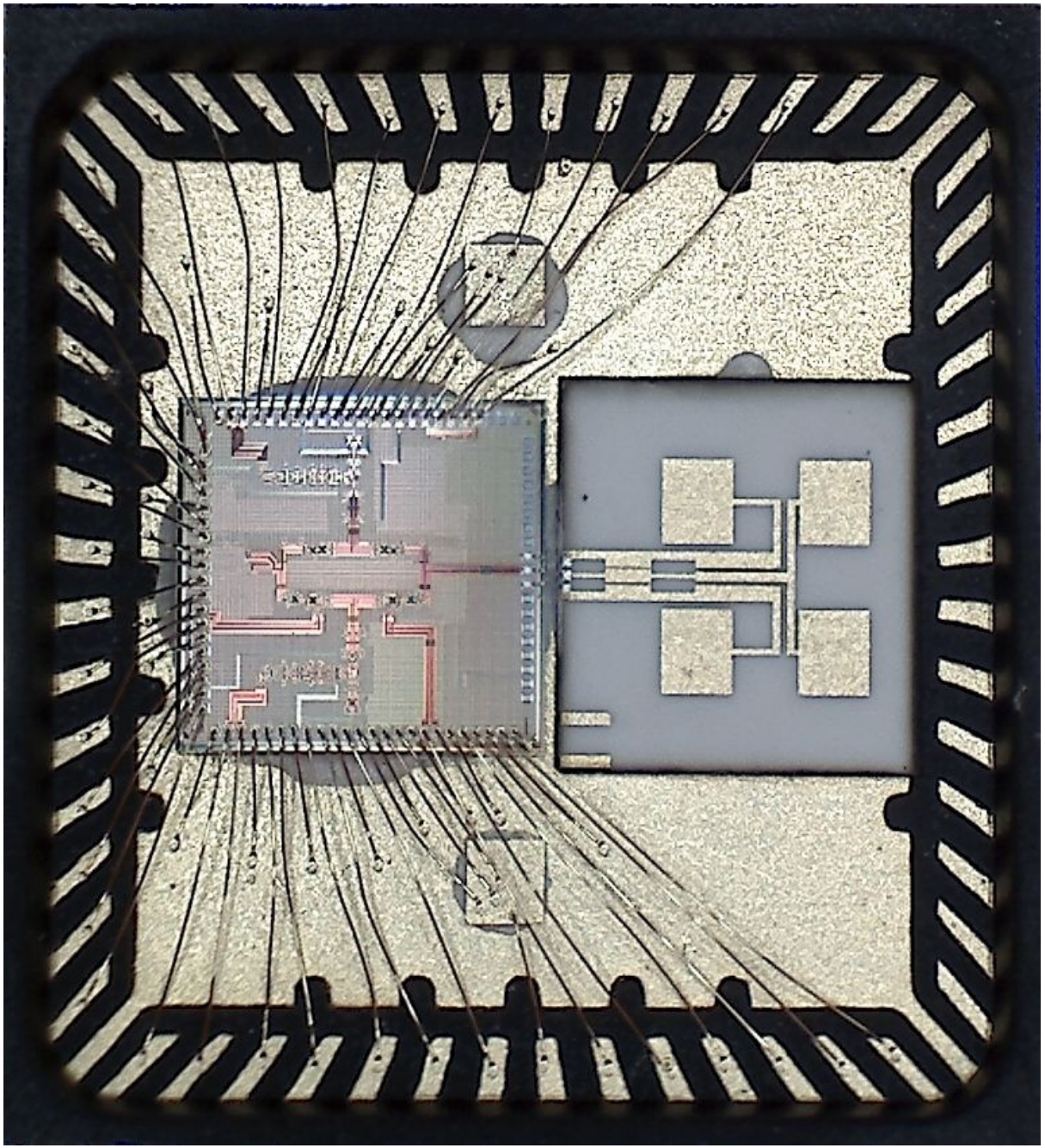
- Power at antenna port measured with ELVA power sensor
- On-chip and external measurements track very well

Receiver Gain and Noise Figure



Low noise figure: 8.5-10.5dB

Antenna and die in package



- QFN package with bondwire transition to antenna on alumina

Courtesy of Robert Bosch GmbH. Krarlsruhe Institure of Technology and
EU SUCCESS project partners

Outline

Mm-wave transceivers

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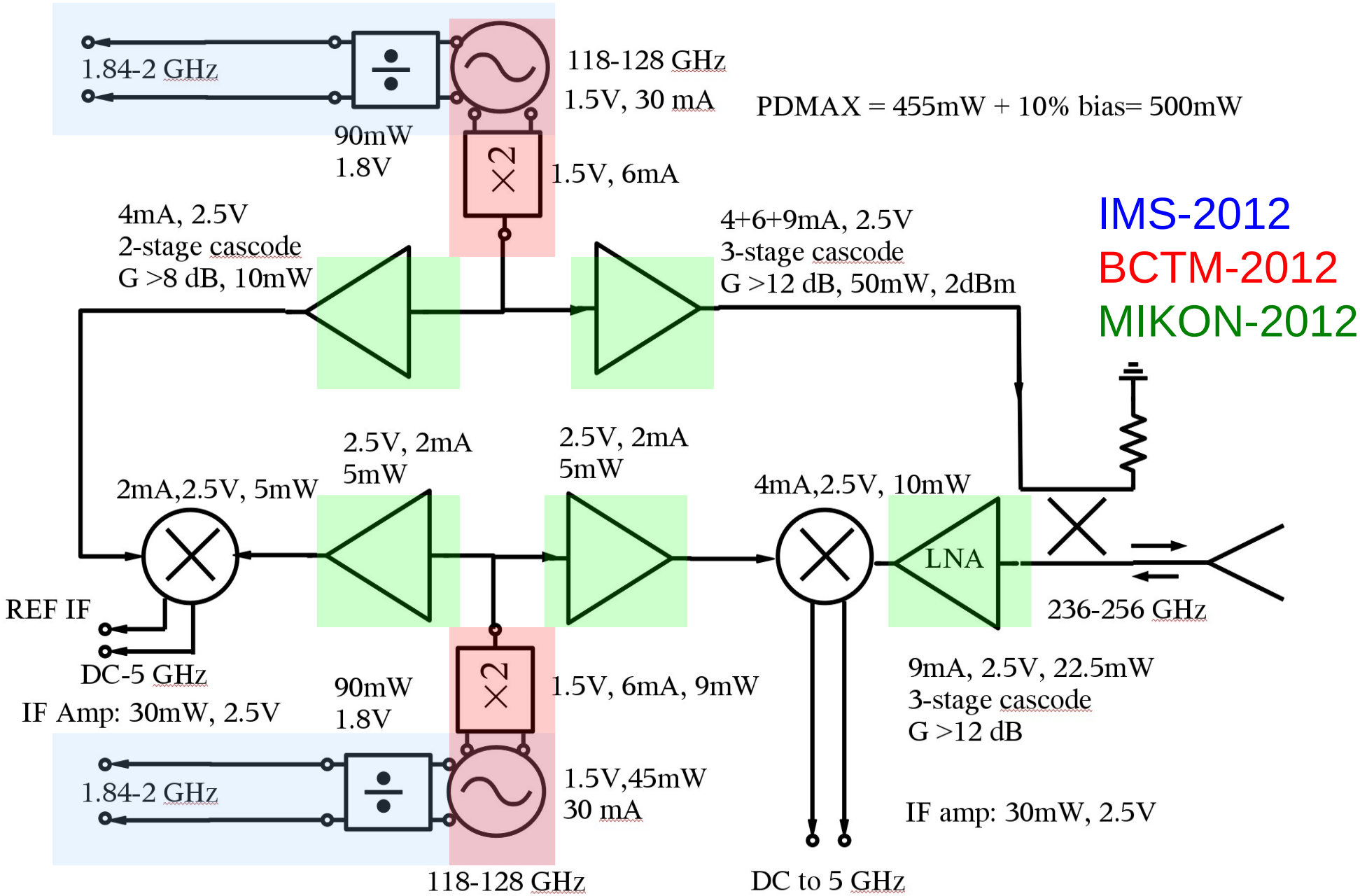
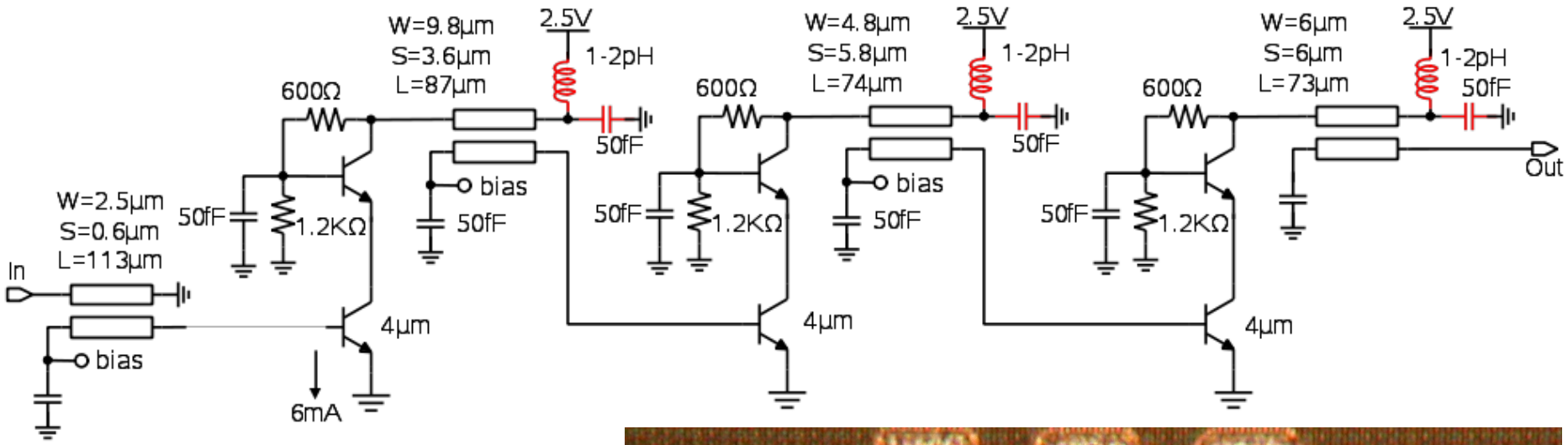
What's Next: 240-GHz Transceiver?

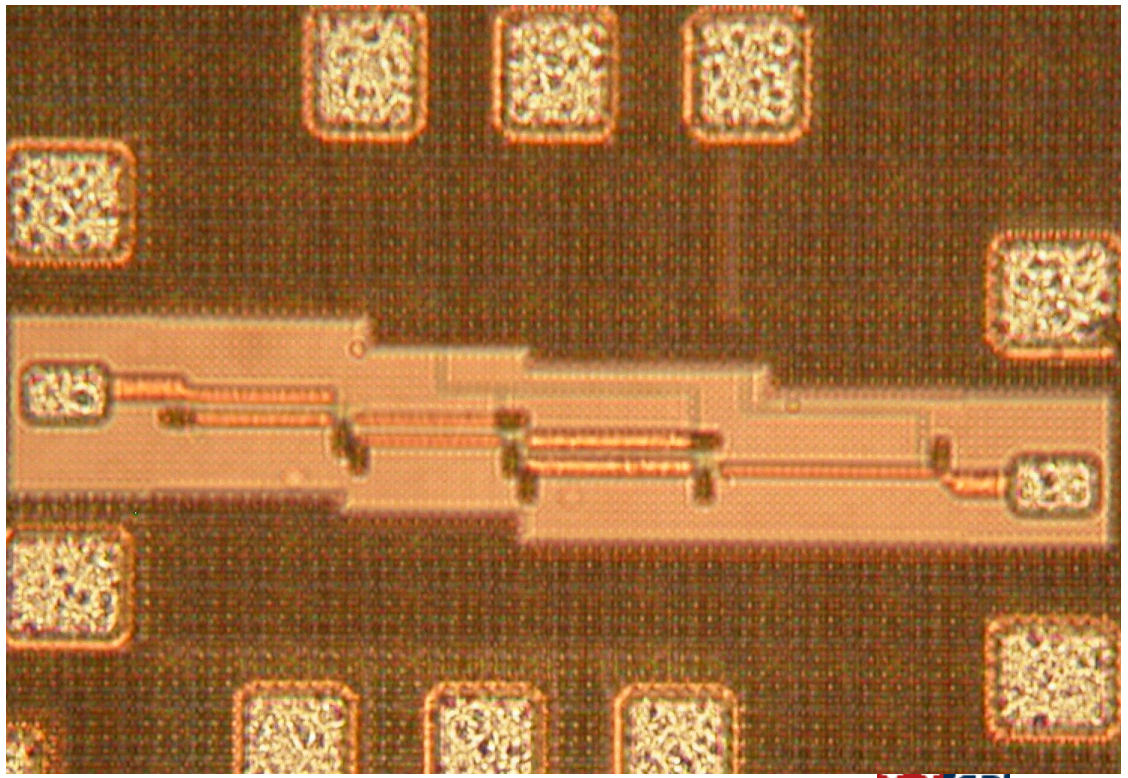


240-GHz Amplifier



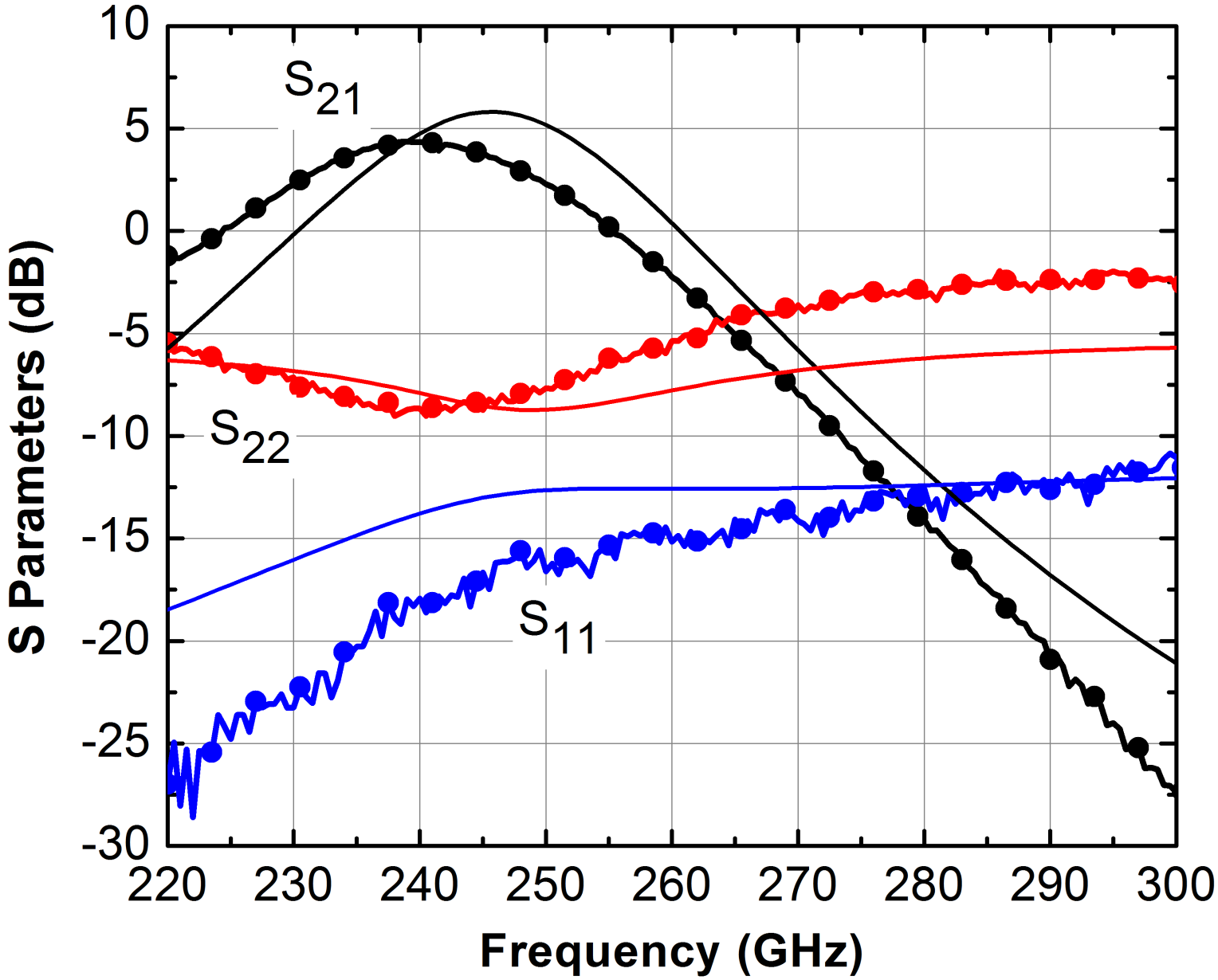
P_D = 37.5 mW

G = 4.5 dB @ 240 GHz

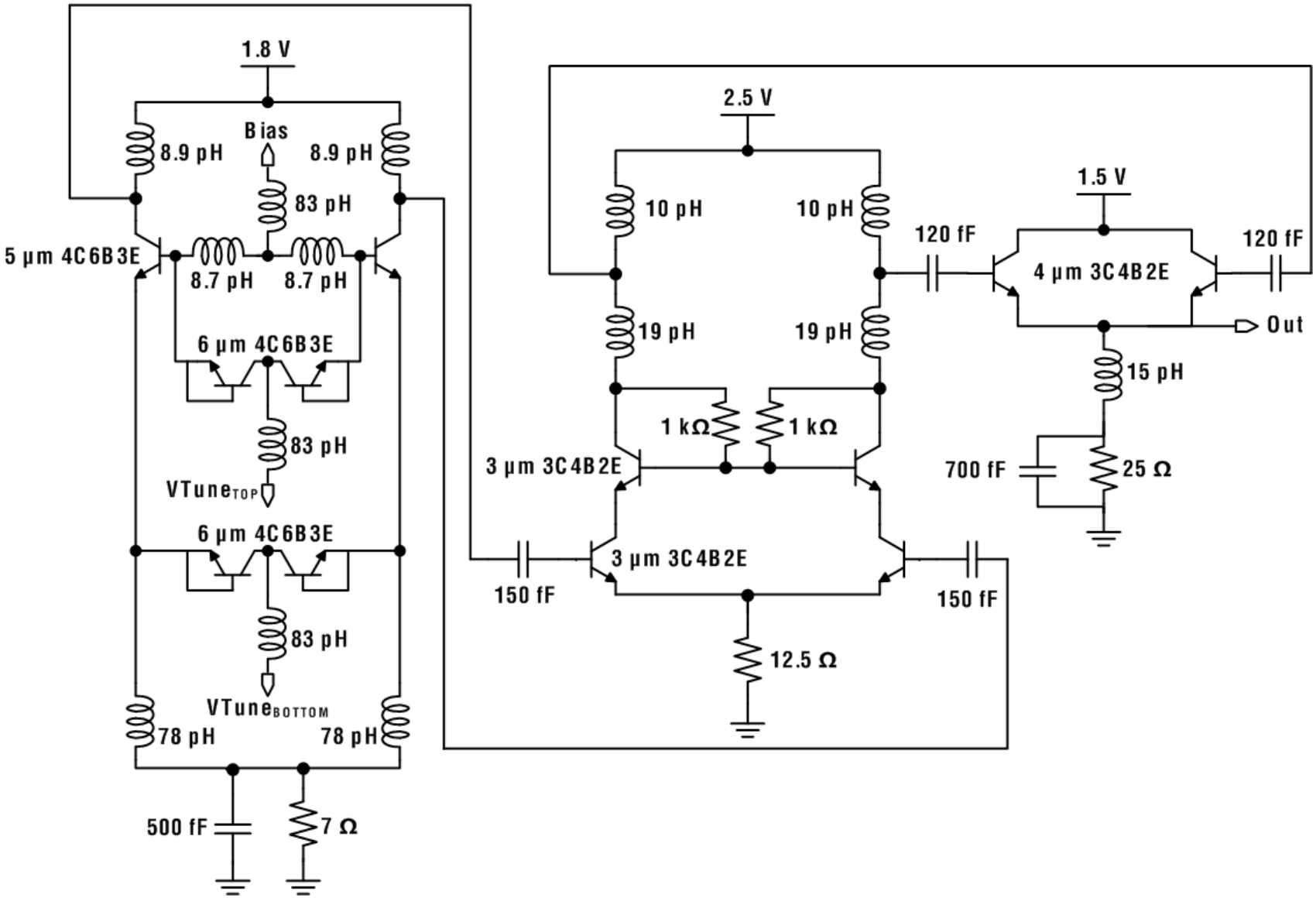


[I. Sarkas et al, MIKON 2012]

240-GHz Amplifier

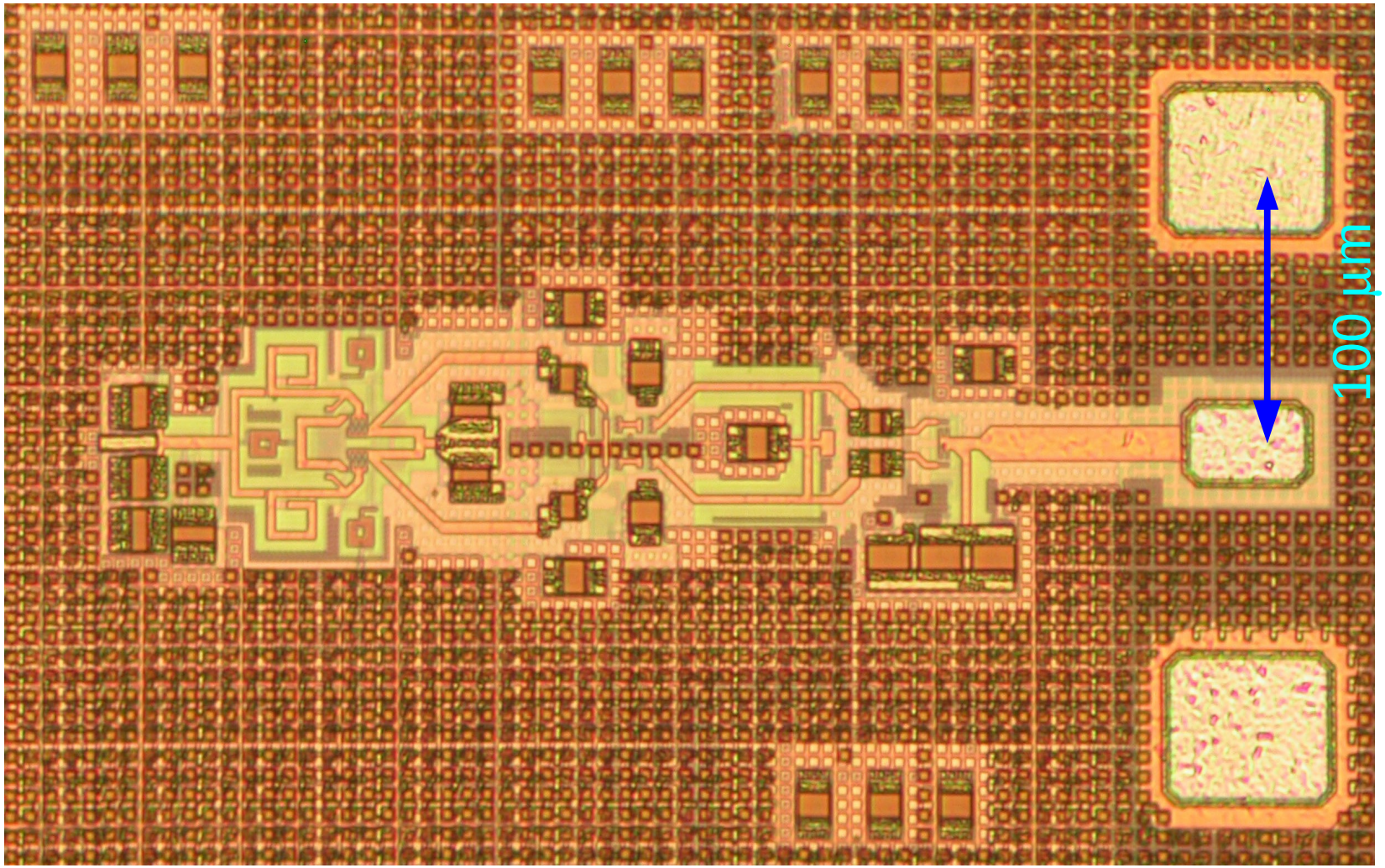


300-GHz VCO-Doubler

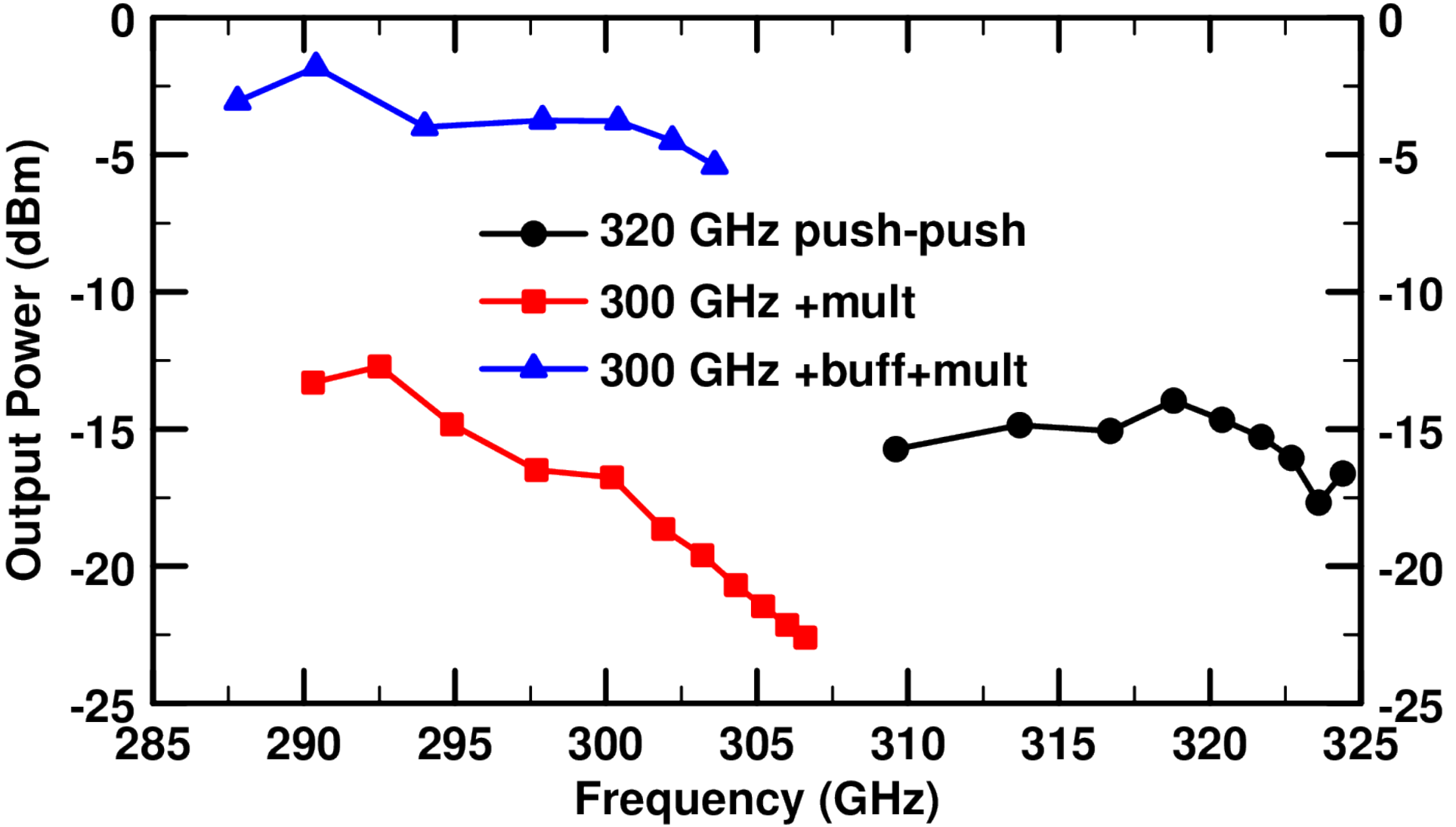


[A. Tomkins et al., BCTM 2012]

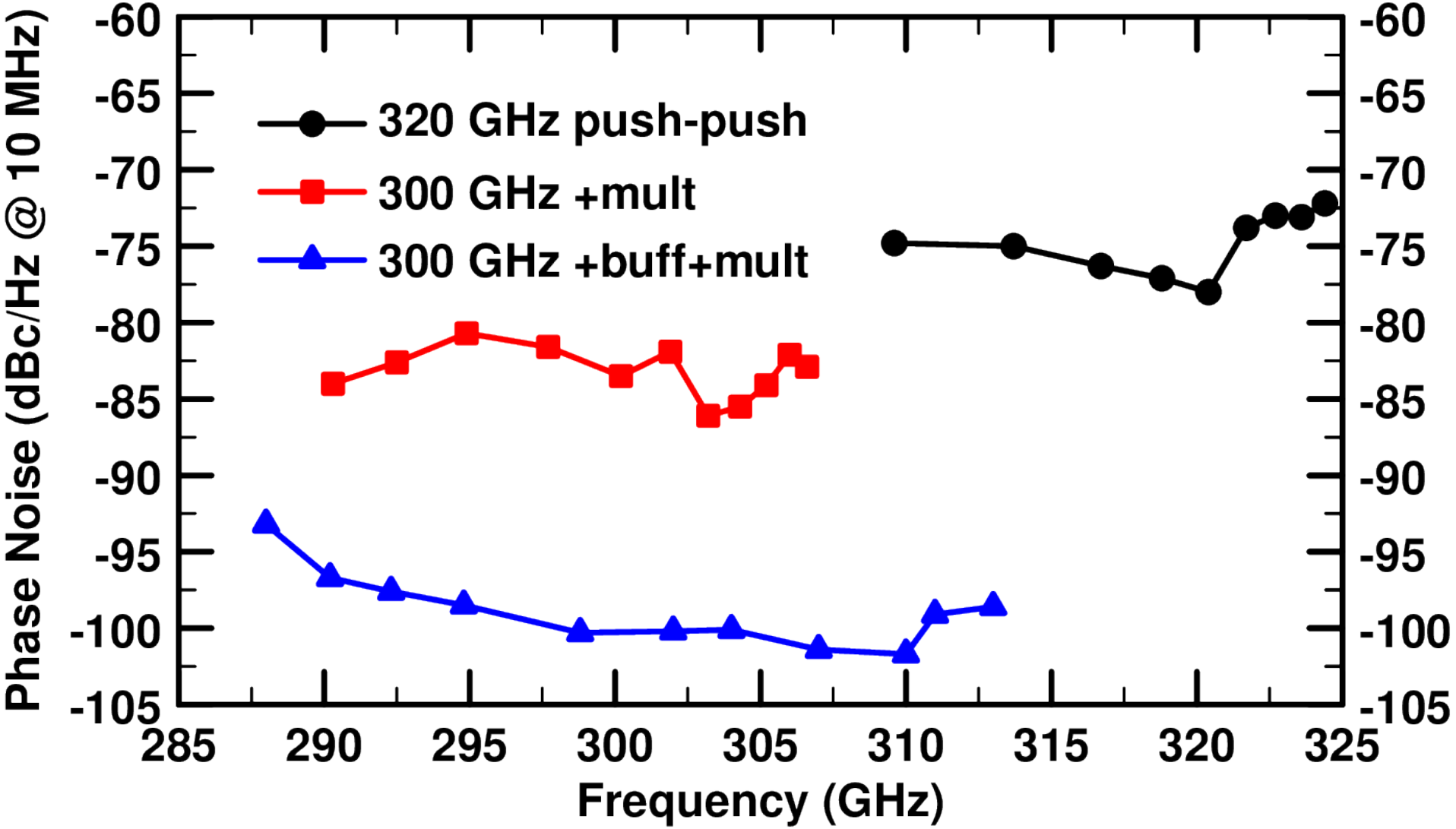
Layout



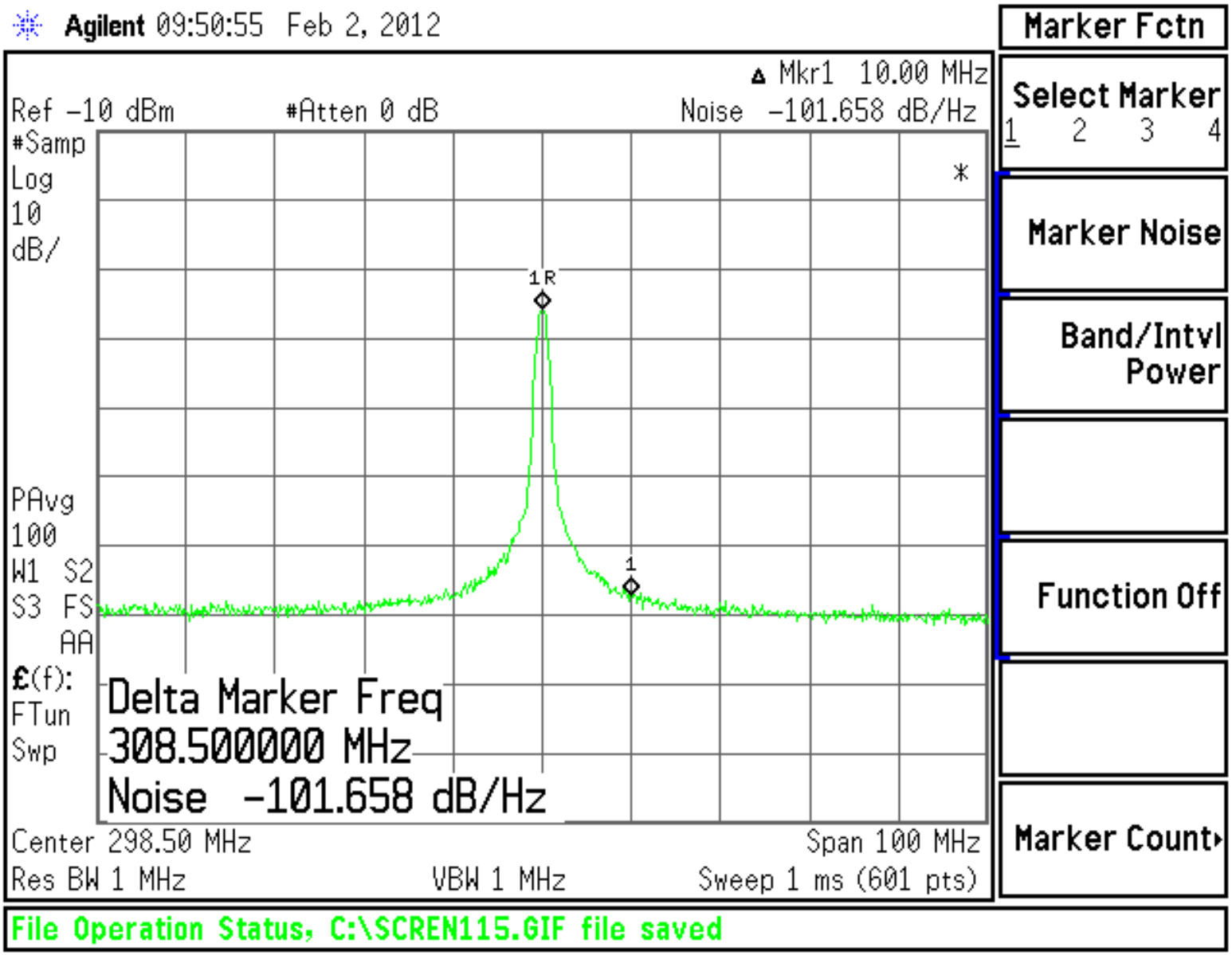
300-GHz Signal Source Comparison



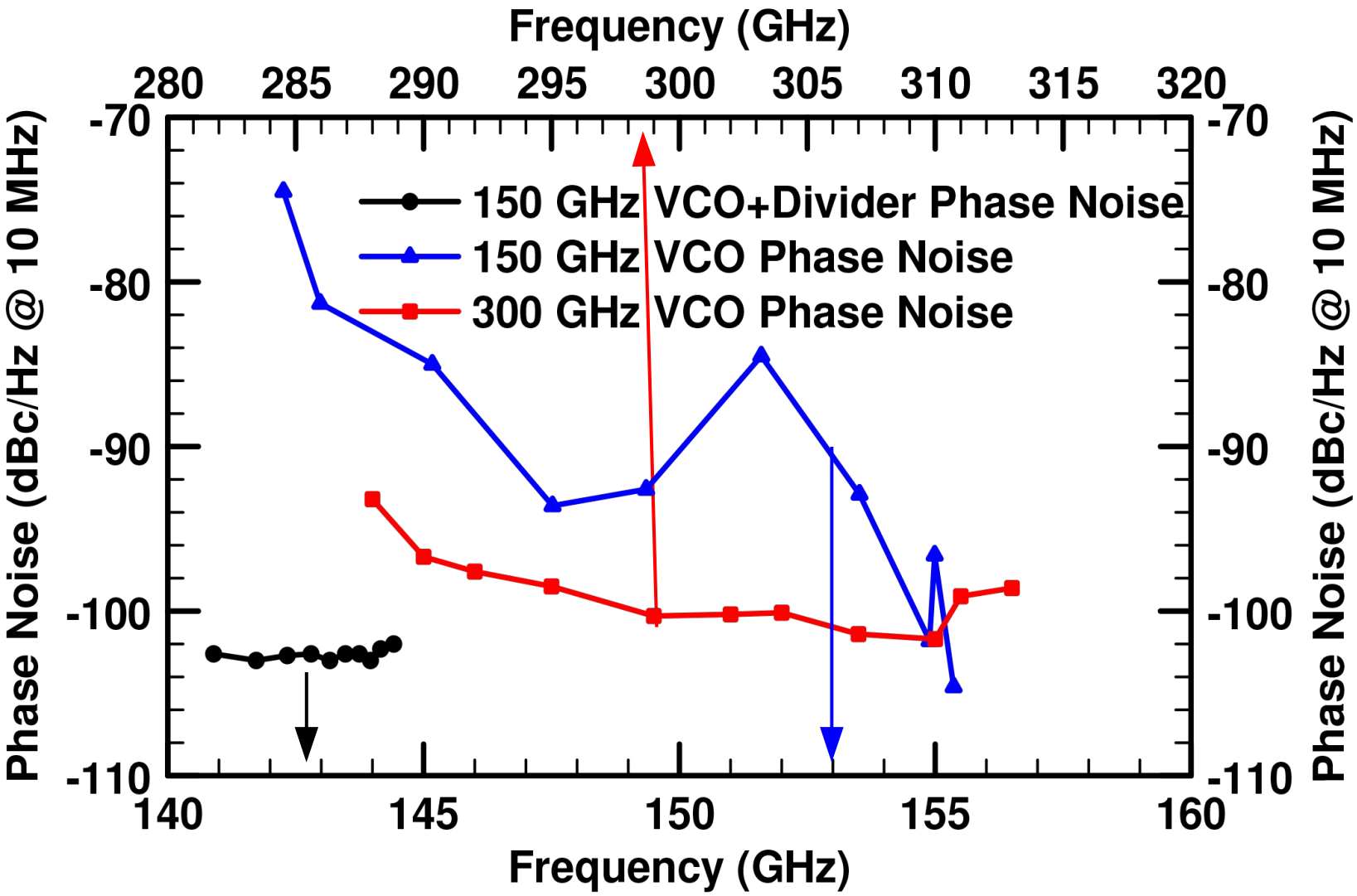
300-GHz Signal Source Comparison (ii)



Phase Noise of VCO-doubler at 309 GHz



300-GHz vs. 150-GHz Phase Noise

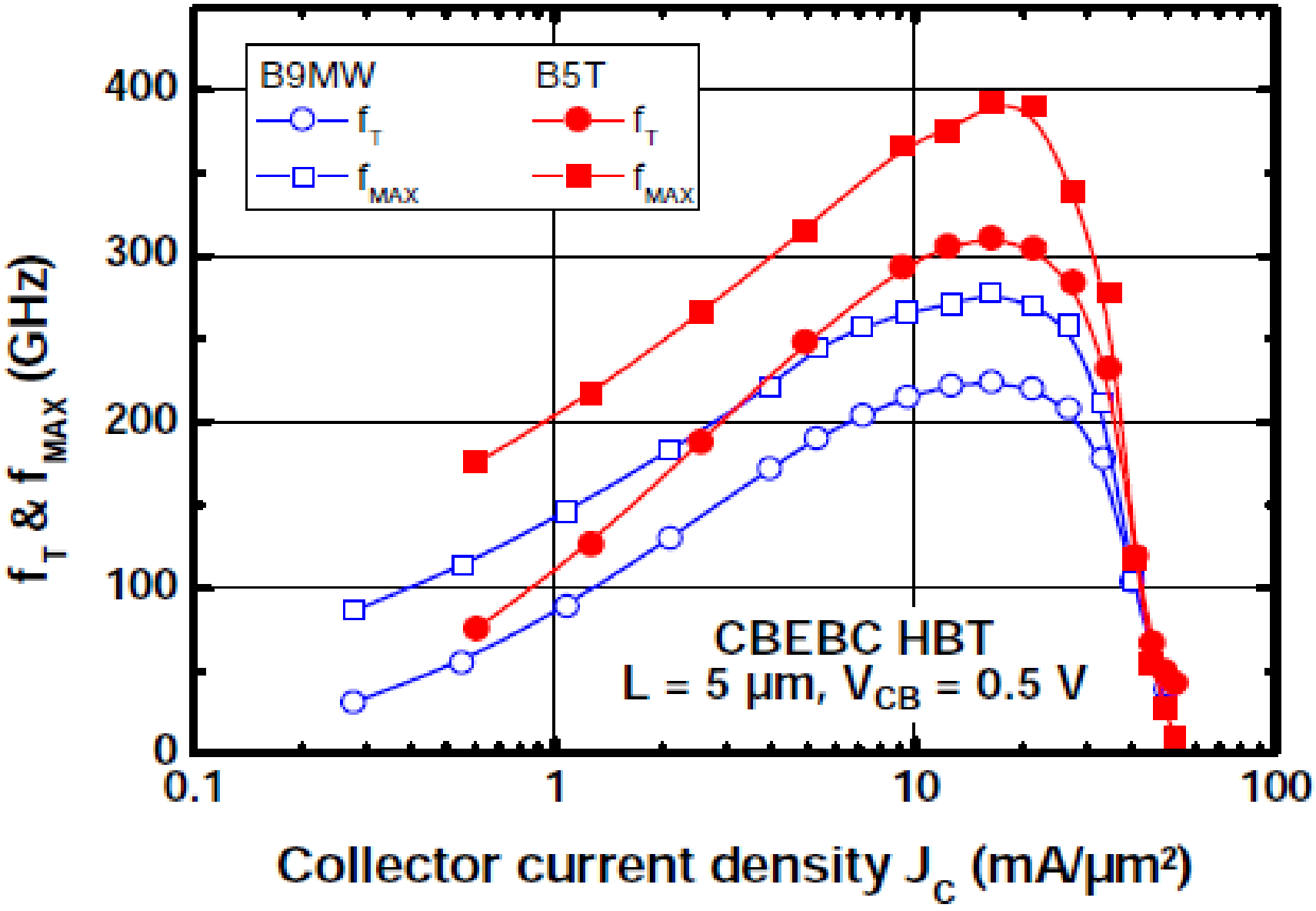


SAME VCO in BOTH!

Conclusions

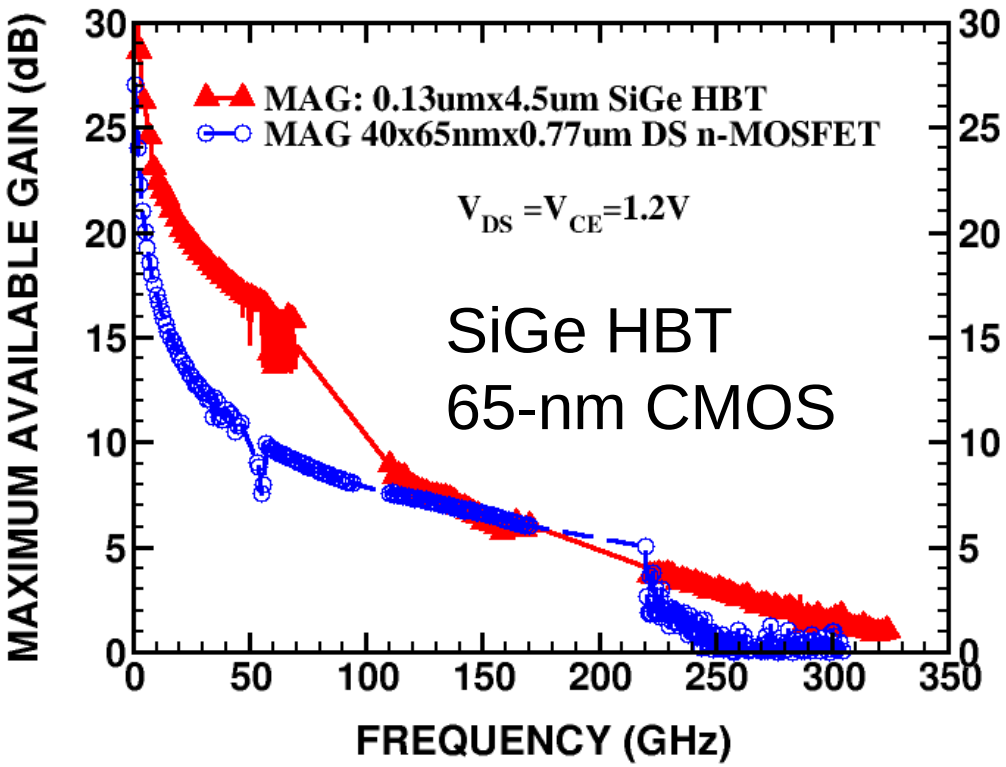
- Why?
  - Because we can!
  - “Cloud” unsustainable without 10x speed and 100x efficiency improvement
  - Need 1Tb/s for near field and intra data center comms
- How?
  - 50-100 Gb/s inductively peaked CMOS logic
  - Mm-wave Power-DAC Transmittter
  - ADC-based receiver equalization
  - H-Band SoCs with on-die antennas
  - Low-cost QFN package

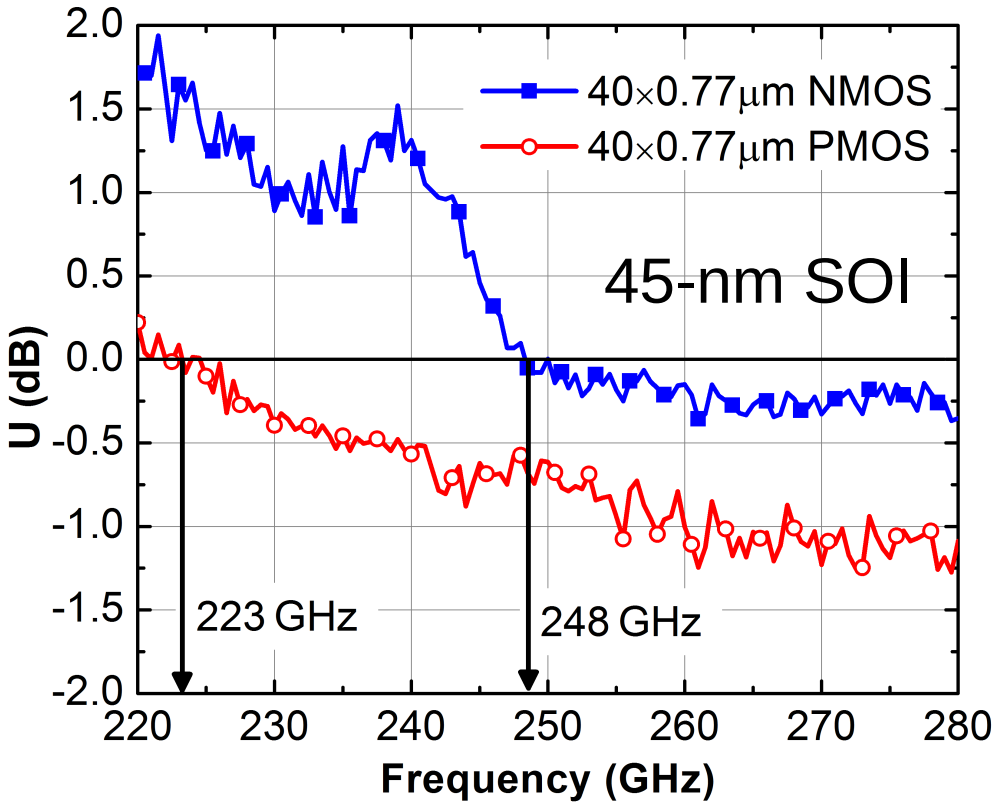
SiGe HBT: BC9MW vs. B5T



[Pascal Chevalier, CSICS-2012]

Si Transistor Performance at G-Band





Comparison Table

Reference	[2]	[6]	[3]	[4]	This Work
Technology	32 nm CMOS	65 nm CMOS	180 nm SiGe	130 nm SiGe	130 nm SiGe
Peak Freq.	14	20		52	57
Gain @ peak (dB)	10 (RX)		12	12.1	26
Min. Gain (dB)	0 (RX)			-19	-14
Equalization	29 dB @ 14 GHz	9 dB @ 20 GHz	17 dB @ 24 GHz	18 dB @ 30 GHz	30 dB @ 40 GHz
P_{DC} **(mW)**	693	80	750	337	250
FOM[pJ/bit]	24.7	2	15	5.6	3.15

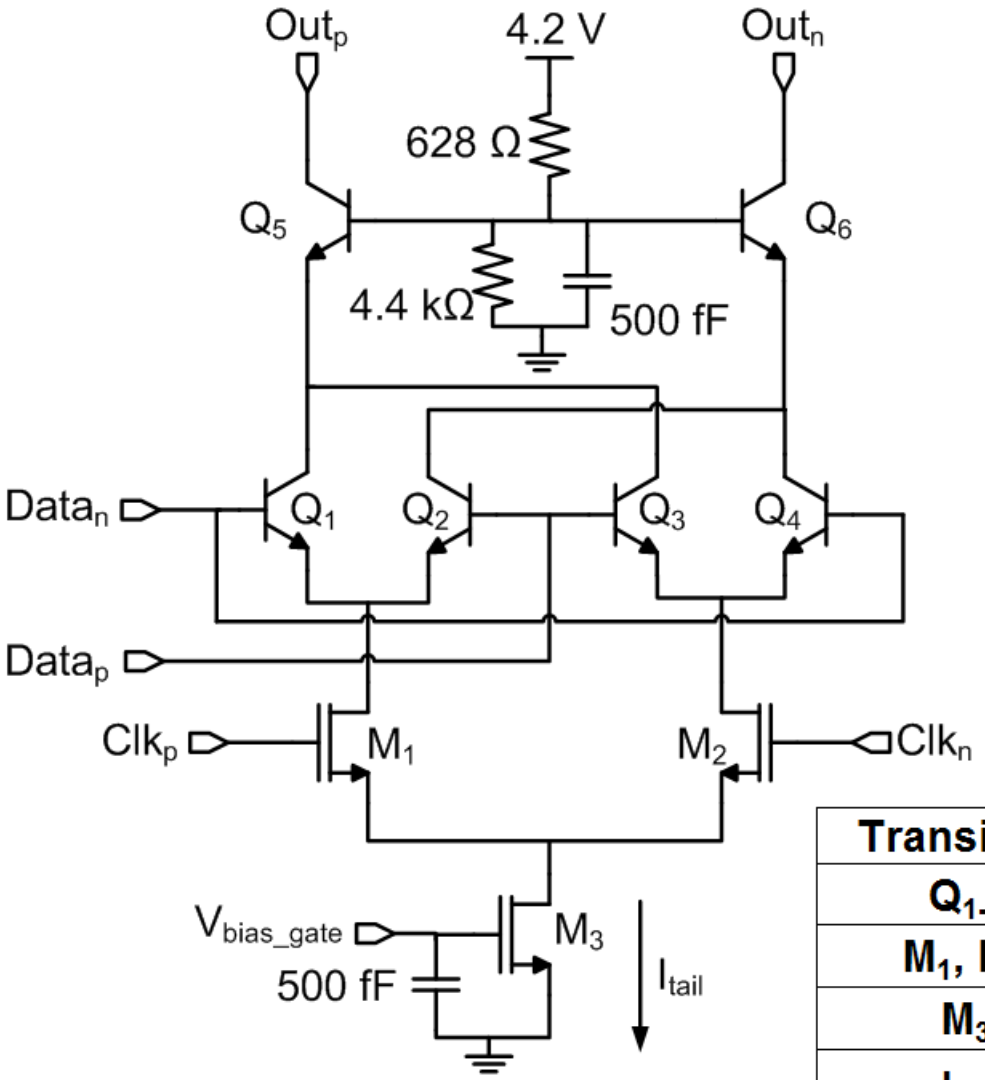
[2] J. Bulzacchelli *et al.*, "A 28 Gb/s 4-Tap FFE/15-Tap DFE Serial Link Transceiver in 32 nm SOI CMOS Technology," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 324–325.

[3] A. Hazneci *et al.*, "49-Gb/s, 7-Tap Transversal Filter in 0.18 μmSiGe BiCMOS for Backplane Equalization," in *IEEE CSICS*, Oct. 2004, pp. 101–104.

[4] A. Balteanu *et al.*, "A Cable Equalizer with 31 dB of Adjustable Peaking at 52 GHz," in *IEEE BCTM*, Oct. 2009, pp. 154–157.

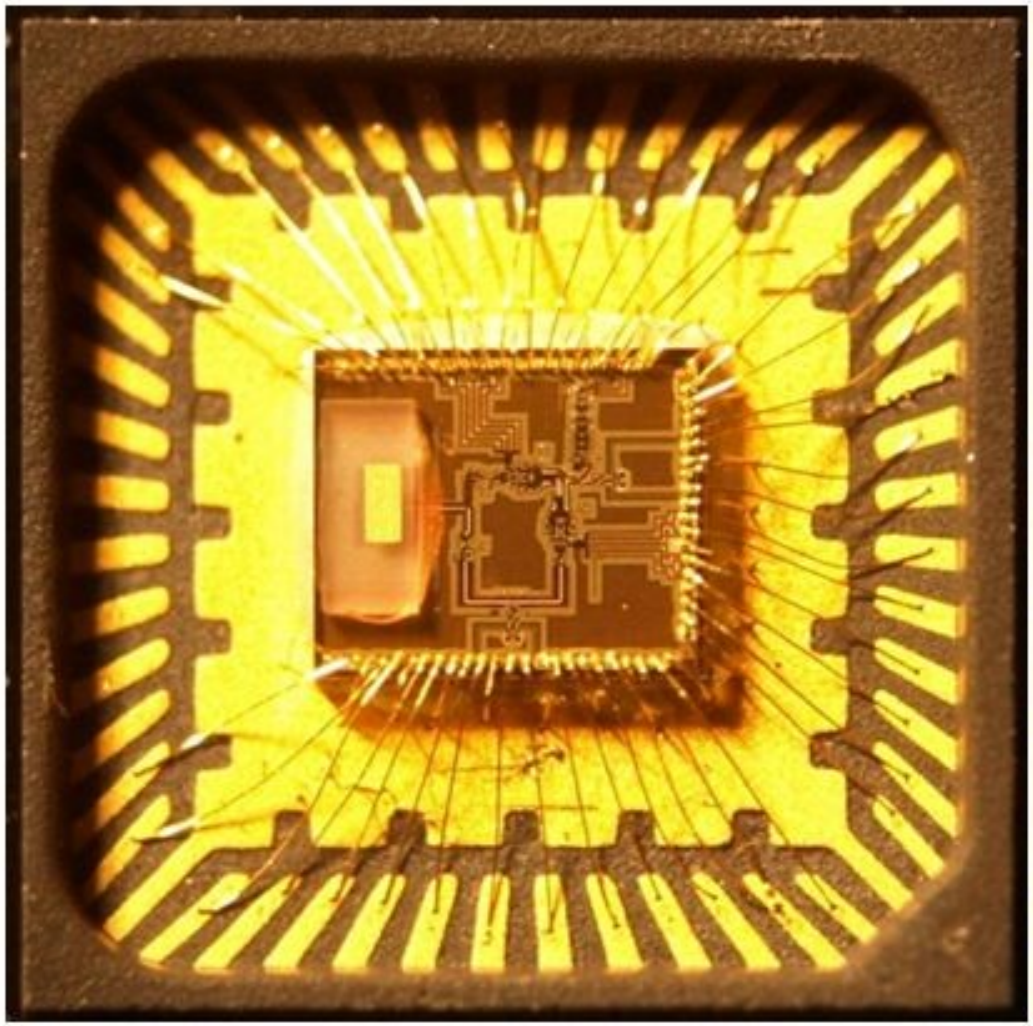
[6] A. Momtaz *et al.*, "An 80 mW 40 Gb/s 7-Tap T/2-Spaced Feed-Forward Equalizer in 65 nm CMOS," *IEEE JSSC*, vol. 45, no. 3, pp. 629–639, Mar. 2010.

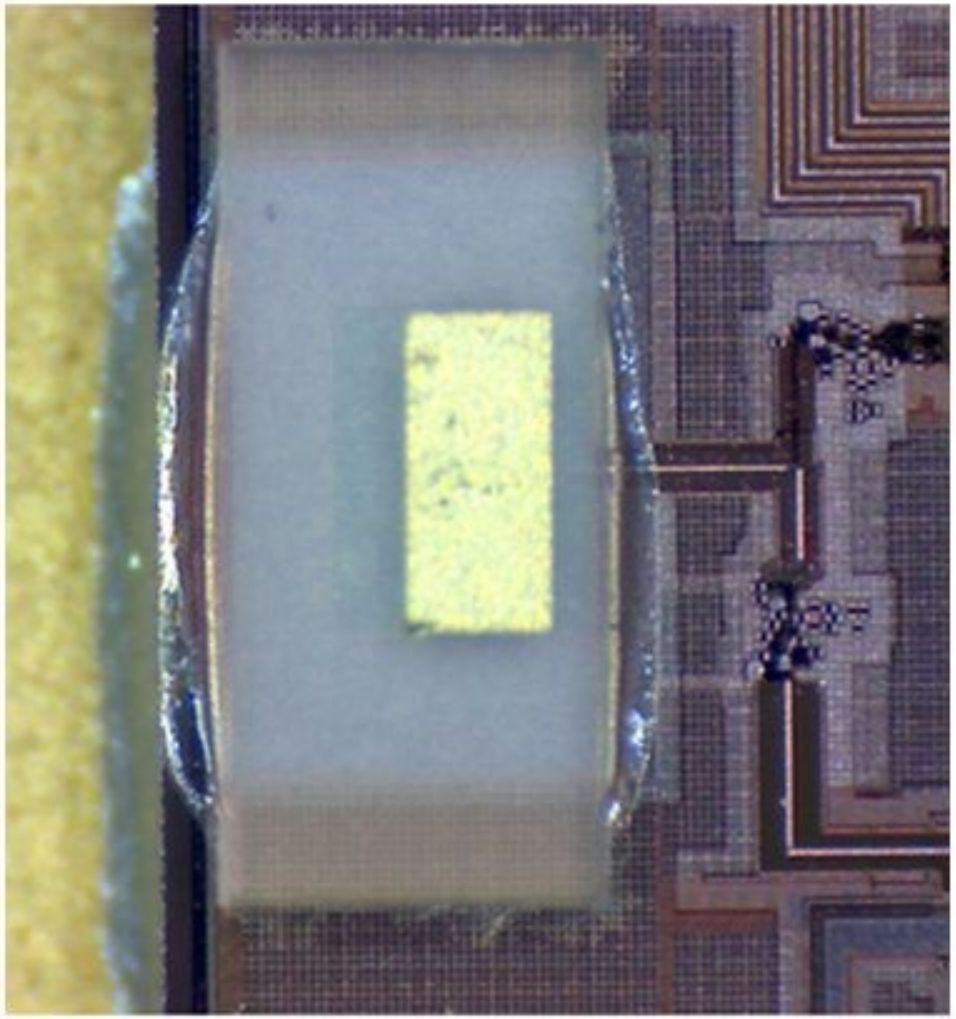
BPSK Cell Schematics



Transistor	LSB	MSB
$Q_{1\text{-}6}$	1 µm	4×2 µm
M_1, M_2	3×2 µm	24×2 µm
M_3	5×4 µm	40×4 µm
I_{tail}	2 mA	16 mA

120 GHz Antenna above IC in QFN





Chip: 2.2mm×2.6mm

Package: 7mm×7mm

[I. Sarkas Trans MTT, March 2012]