SiGe BiCMOS AND CMOS TRANSCEIVER BLOCKS FOR AUTOMOTIVE RADAR AND IMAGING APPLICATIONS IN THE 80-160 GHz RANGE

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Abstract

This paper examines the suitability of advanced SiGe BiCMOS and sub 65nm CMOS technologies for applications beyond 80GHz. System architectures are discussed along with the detailed comparison of VCOs, LNAs, PAs and static frequency dividers fabricated in CMOS and SiGe BiCMOS, as required for automotive cruise-control radar, high data-rate radio, and active and passive imaging in the 80GHz to 160GHz range. It is demonstrated experimentally that prototype SiGe HBT and BiCMOS technologies have adequate performance for all critical 80GHz building blocks, even at temperatures as high as 125 C. Although showing promise, existing 90nm GP CMOS and 65nm LP CMOS circuits at these frequencies remain significantly inferior to their SiGe counterparts.

1. Introduction

Potential applications of silicon ICs in the 80-160 GHz range include automotive cruise control (ACC) radar [1], millimeter-wave passive [2],[3] and active [4] imaging, and 10Gb/s short-range wireless links [5]. Over the last 4 years, several publications have explored the implementation of 77GHz IC building blocks in SiGe HBT technology [7]-[18]. Although mm-wave CMOS oscillators have been reported at frequencies as high as 194 GHz [19], only recently the phase noise and tuning range of 77GHz CMOS VCOs have become competitive with those of SiGe BiCMOS implementations [20]. Several 90nm and 65nm CMOS amplifiers operating in the 80-100 GHz range with less than 10dB gain have recently been announced [21] or are in press [4],[22].

The interest in SiGe BiCMOS and CMOS for mm-wave SOCs has been kindled by the favorable impact that transistor scaling has on practically all transistor high-frequency figures of merit (FoMs), and by the hope that the expected lower wafer cost will unravel a wide range of new applications and consumer

products. Integration beyond the basic building blocks, at the receiver, transmitter and even transceiver level, has already been demonstrated in SiGe HBT technology at 77 GHz [23]-[27] and at 160 GHz [28]. An amplifier with over 15 dB gain at 140 GHz, the highest in silicon, has also been fabricated [28]. This paper compares transistor and basic building block performance in SiGe HBT, SiGe BiCMOS and nanoscale CMOS technologies for mm-wave SOCs and discusses the most suitable system architectures that lead to the lowest power dissipation, smallest die area and die cost.

2. SiGe HBT vs. 65nm n-MOSFET performance comparison

Benefiting from the clear guidelines set forth by the International Roadmap for Semiconductors (ITRS), CMOS technology scaling has continued unabated to nanometre dimensions. Power dissipation, noise figure, and phase noise performance of mm-wave ICs all improve with scaling. At the same time, Fig. 1 illustrates that SiGe BiCMOS technology now retains a three-generation lithography advantage over CMOS in terms of f_T and f_{MAX} [29] and therefore results in significantly lower product development cost.

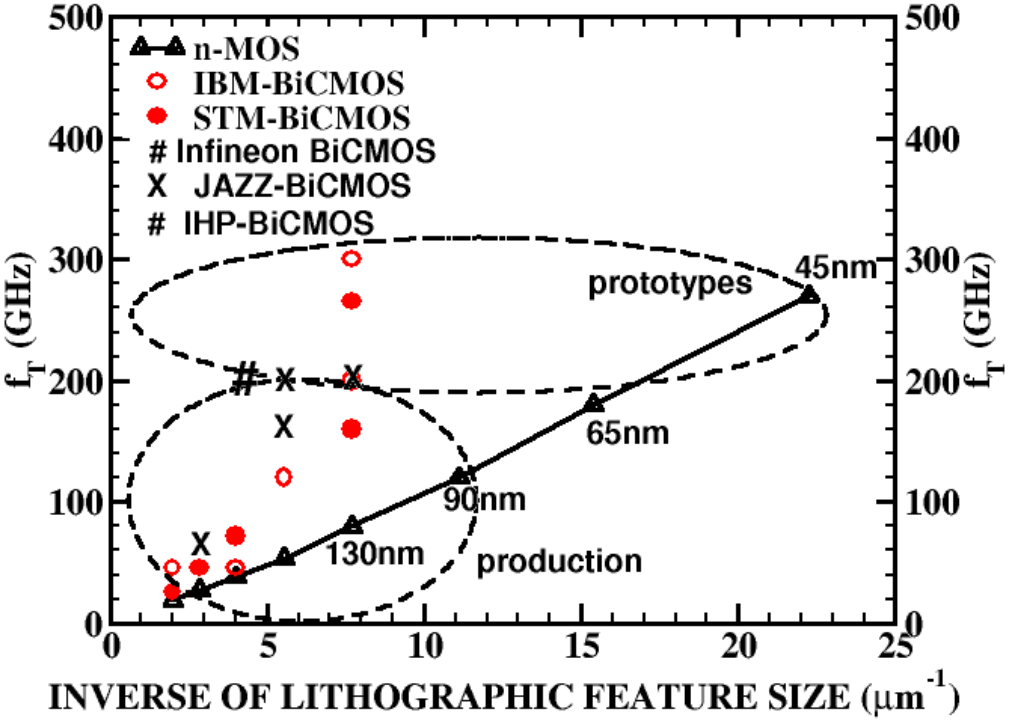

Fig. 1 f_T scaling in CMOS and SiGe BiCMOS technology nodes [29]

Fig.2 compiles the measured f_T, f_{MAX} and NF_{MIN} characteristics of a 65nm×90×1μm low-power (LP) n-MOSFET, and of a 3×0.13μm×2.5μm SiGe HBT, as a function of drain current, and collector current, per unit gate width and emitter length, respectively [30]. In both devices f_{MAX} reaches 300 GHz and

NF_{MIN}, measured at 40 GHz, is about 1 dB, comparable to that of InP HEMTs. The HBT has 40% higher f_T and its optimal bias current densities for minimum noise or maximum gain are 5-6 times larger than in the 65nm MOSFET. Both devices are biased at a drain-source (collector-emitter) voltage of 1.2V, but the HBT can also operate safely with collector-emitter voltages exceeding 1.6V in common emitter CE, and beyond 3V in common base CB configurations [31]. At comparable f_{MAX}, the higher current densities and voltage swing, lower collector-substrate capacitance, along with the higher transconductance, give the HBT a significant advantage over MOSFETs in power amplifiers [32] and high-speed output drivers [33]. Furthermore, as illustrated in Fig. 3, even though the MOSFET has lower noise figure below 15 GHz, because of the higher f_T, the HBT noise figure increases at a slower rate at mm-wave frequencies, making it more suitable for LNAs above 60 GHz. Note that in Fig. 3 the MOSFET optimum noise bias does not change with frequency, whereas the optimum noise current density and, therefore the f_T, increase with frequency for HBTs.

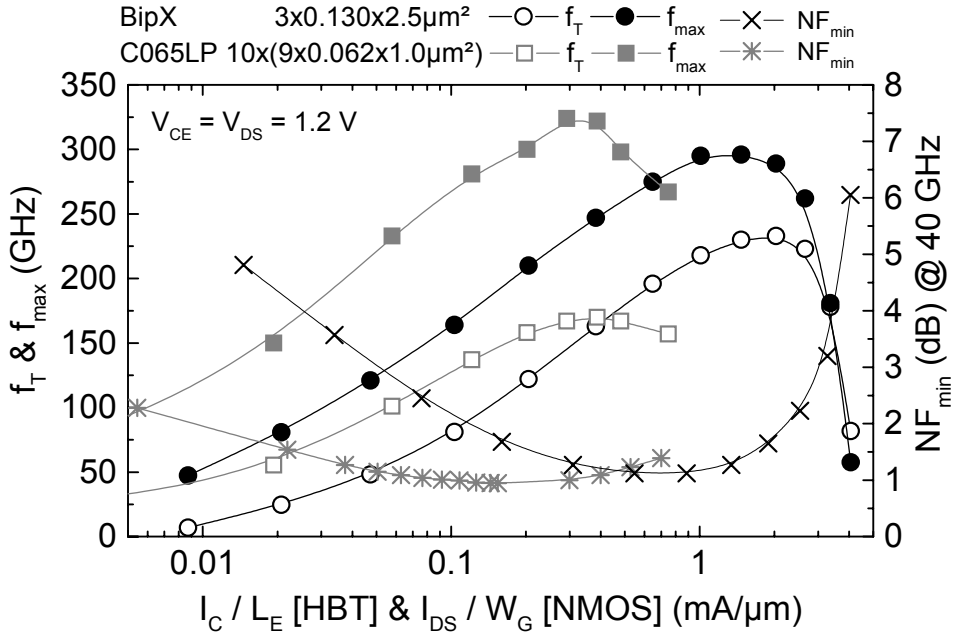

Fig.2. Measured 65nm LP n-MOSFET vs. SiGe HBT f_T, f_{MAX} and NF_{MIN} vs. Collector Current Characteristics. [30]

Fig. 4a, shows that GP bulk and SOI MOSFETs from different foundries exhibit remarkably similar f_T-I_D characteristics which scale almost ideally from one technology node to another [4],[33]. Note that, for the first time, there is no improvement in the peak f_T value between 90nm GP and 65nm LP n-MOSFETs because the physical gate lengths are practically identical. On the contrary, as illustrated in Fig. 4b, the peak f_T current density of SiGe HBTs increases in every new generation [34], and the optimal biasing conditions for HBT-circuits must be revisited, typically increased, in new nodes or at higher frequencies.

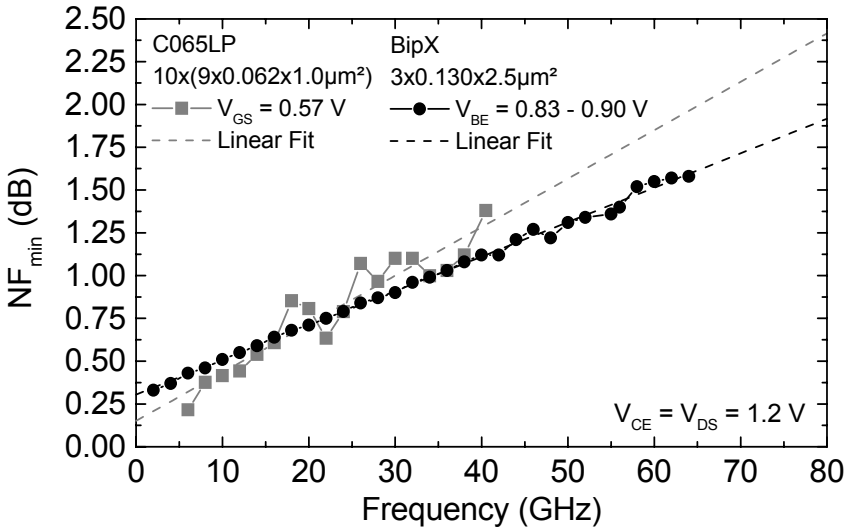

Fig.3. Measured N_{FMIN} as a function of frequency for a SiGe HBT and a 65nm LP n-MOSFET. [30]

Finally, the measured intrinsic voltage gain is plotted in Fig. 5 vs. current density - rather than versus effective gate voltage - for n-MOSFETs across technology nodes and for different gate lengths in the 65nm LP node. These results show that 90nm GP MOSFETs have higher voltage gain than 130nm MOSFETs for all gate lengths, and that high threshold voltage (HVT) 65nm LP devices have less gain than low threshold voltage (LVT) ones. Furthermore, a 130nm MOSFET fabricated in the 65nm LP node has higher gain than a 130nm device fabricated in the 130nm node. Increasing gate length beyond $2\times L_{MIN}$ brings no improvement in analog performance with severe degradation of HF performance [35]. Ironically, the GP LVT 90nm MOSFETs have better analog performance and dissipate less power than the LP 65nm MOSFETs.

3. Inductors, transformers and antennas

Similar to MOSFETs and HBTs, passive components such as antennas, inductors and transformers also follow Moore's law. For example, (1) shows that when the inductor diameter d, average diameter d_{avg}, metal width W, and inter-winding spacing [36] are all reduced by the scaling factor S, the inductance decreases proportionally. It can also be shown that the parasitic capacitance to ground decreases by S^2 and that the self-resonant frequency (*SRF*) and the peak Q frequency (PQF) increase S times while the peak Q remains largely unchanged. This suggests that one can continue to employ lumped inductors and transformers at mm-wave frequencies and thus take advantage of the most natural and most economical way to shrink the size of mm-wave silicon ICs far

beyond what has been accomplished with transmission lines, distributed baluns and power splitters [1],[9],[15].

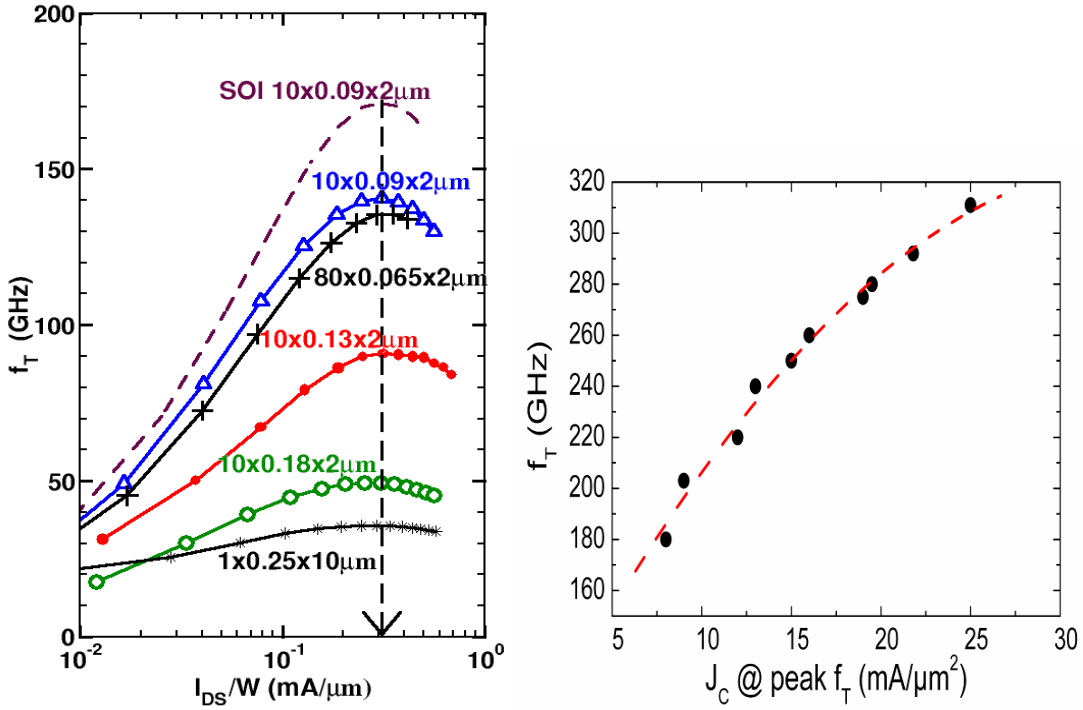

Fig.4. a) Measured f_T vs. drain current density per unit gate width for a) n-MOSFETs in different technology nodes [4] and b) measured peak f_T value of SiGe HBTs as a function of the peak f_T current density per emitter area [34].

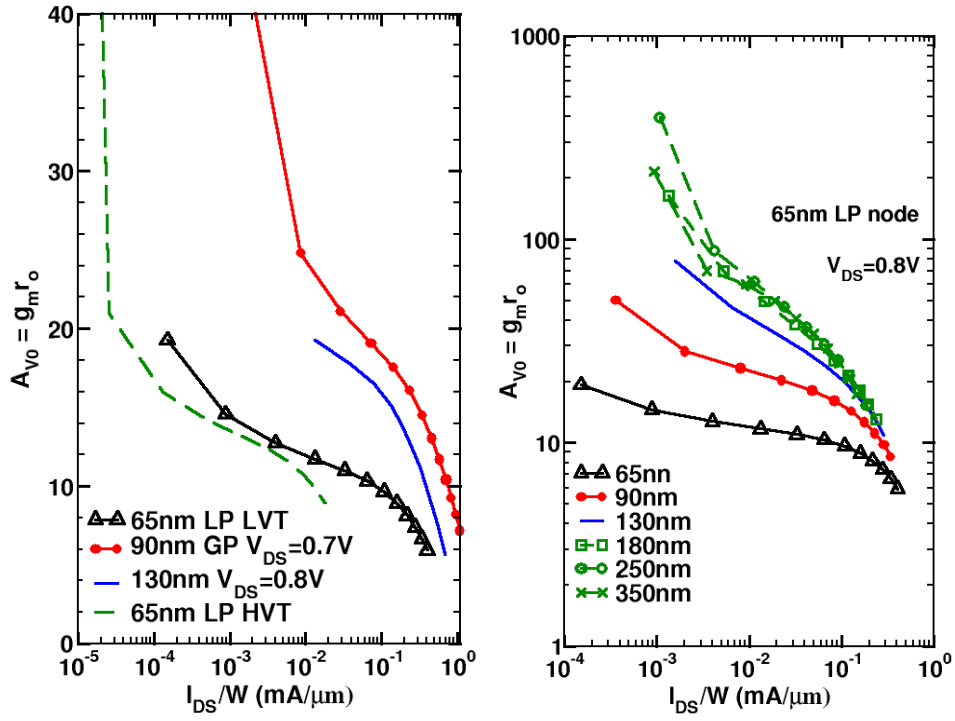

Fig.5. Intrinsic voltage gain a) across technologies and b) for different gate lengths in a 65nm LP CMOS technology as a function of drain current density.

$$L \approx \frac{9.375\mu_0 n^2 d_{avg}^2}{11d - 7d_{avg}} \quad \Rightarrow \quad \frac{L}{S} \approx \frac{9.375\mu_0 n^2 \left[\frac{d_{avg}}{S}\right]^2}{11\frac{d}{S} - 7\frac{d_{avg}}{S}} \tag{1}$$

Fig. 6 reproduces the die photo of a differential dipole antenna designed for 160GHz operation which occupies less than 200μm×200μm and is driven by a differential-to-single-ended converter realized with a vertically stacked transformer. The simulated gain and return loss of the antenna are plotted in Fig.7, while the structure and equivalent circuit of the transformer, extracted from ASITIC y-parameter simulations are shown in Fig.8.

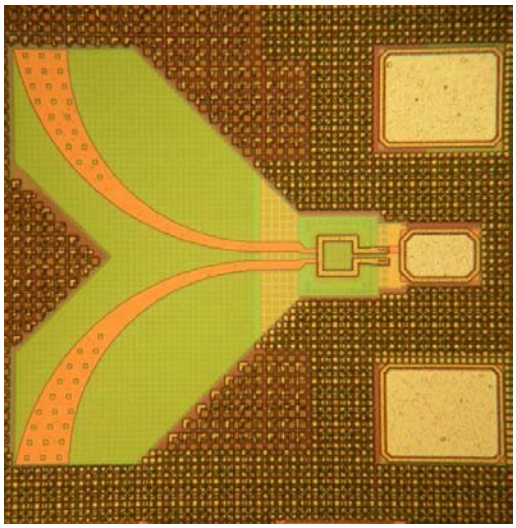

Fig.6. Die photo of 160-GHz dipole antenna with vertically-stacked transformer as single-ended to differential converter.

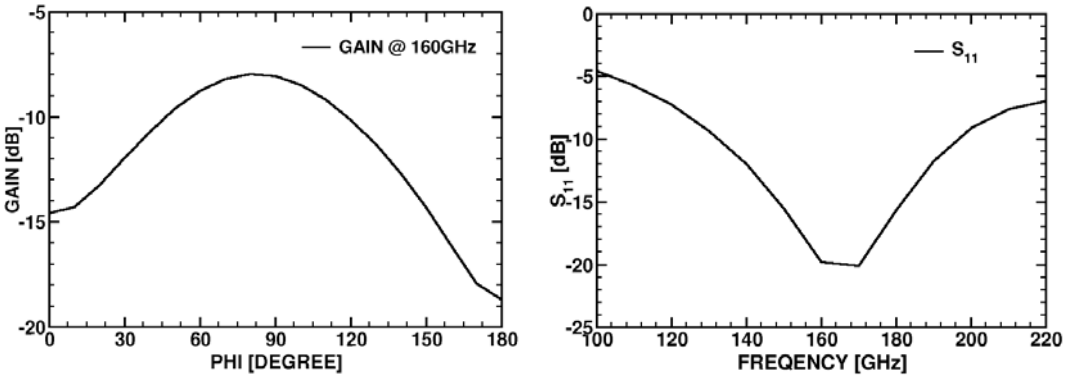

Fig.7. Simulated gain at 160 GHz and simulated return loss of antenna using ANSOFT's HFSS.

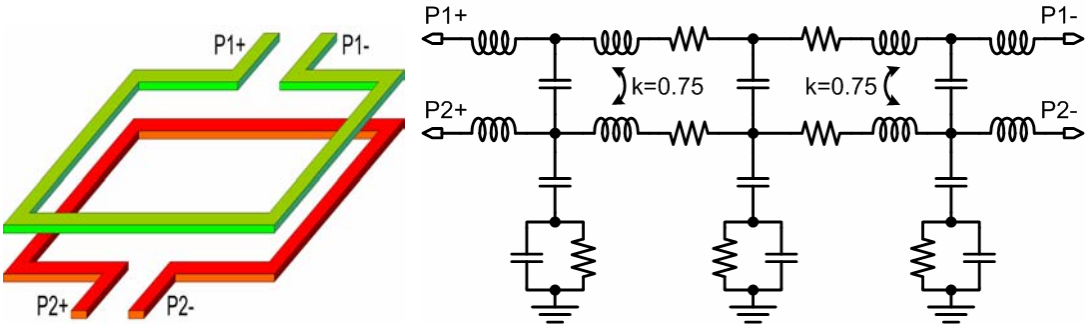

Fig.8.Pictorial view of vertically-stacked transformer and multi-section equivalent circuit model extracted using ASITIC

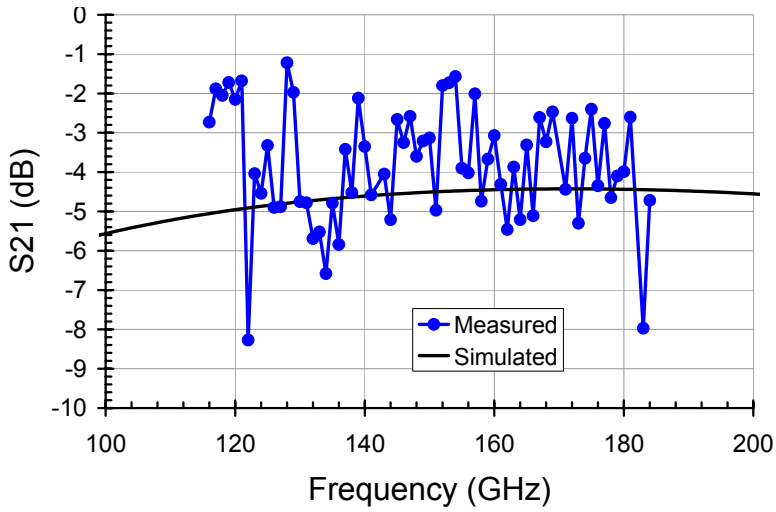

Fig.9. Measured vs. simulated S_{21} of a vertically-stacked transformer.

The transformer was fabricated as a separate test structure in a standard digital back-end with 6 copper layers [28]. Its transmission loss is about 4 dB and was measured on wafer in the 110 to 170 GHz range. Fig. 9 compares measurements with simulations showing good agreement, well within the measurement scatter. While thick and wide metal lines are useful to reduce loss in t-lines and baluns [15],[24],[37],[38], to increase coupling and to reduce the footprint of transformers and vertically-stacked inductors, it is critical that the vertical and lateral spacing between windings is shrunk below 1 μm. This is difficult to accomplish in a process with a thick aluminum top metal.

Finally, should t-lines or inductors be used as matching elements at mm-waves? Are transformers [37] or classical quarter-wavelength couplers and baluns the most effective components for single-ended-to-differential conversion in mm-wave circuits above 60 GHz? The wealth of experimental evidence regarding inductance and Q per layout area, circuit size, and circuit performance [1],[15]-[18],[19]-[21],[24],[27]-[28],[37]-[38], all point to the fact that, just as at lower

frequencies, lumped inductors and transformers lead to lower die size with comparable or better overall circuit performance.

4. Design flow for mm-wave silicon ICs

Compared to analog and RF design flows, the design flow for mm-wave ICs is complicated by the need to model every piece of interconnect longer than 15..20μm as a distributed transmission line. An effective way to contain the modelling effort is to include all interconnect leading to and from an inductor in the inductor itself and to extract the 2π equivalent circuit of the ensemble using ASITIC, as in [39]. At the cell level, the main goal is to minimize footprint by merging the transistor layouts of differential pairs and mixing quads and thus shrink the length and parasitic capacitance of local interconnect. The accurate extraction of RC parasitics at the layout-cell level (i.e. interdigitated transistor or varactor cell, cascode cell, differential pair cell, switching quad cell, cross-coupled pair cell, etc.) is critical for the accurate modelling of the significant gain and noise figure degradation in circuits with nanoscale MOSFETs. The MOSFET series parasitics are notoriously degraded by layout contact and via resistance. This is illustrated in Fig. 10, where the gain of a 90GHz 3-stage cascode amplifier implemented in 65nm LP CMOS [4] is reduced from 15 dB to 8 dB, and its noise figure increases from 5 dB to 7 dB when the parasitics of the transistor layout are included in simulation. All other components are unchanged. Note that there is hardly any shift in $S_{11}(f)$ and $S_{22}(f)$, or in the centre frequency of the $S_{21}(f)$ and $NF(f)$ characteristics, suggesting that the transistor layout parasitics are mostly resistive and not capacitive. Because of the larger R_E and R_B [30] and smaller C_{bc}/C_{be} ratio (i.e. reduced Miller effect) for the same current, circuits realized with HBTs are less sensitive to layout parasitics than those with MOSFETs.

Based on these general observations, a design flow that has been found to work well up to 160 GHz is summarized below:

- Optimize the transistor/varactor emitter length l_E or gate finger width W_f to balance the degradation of f_{MAX} and NF_{MIN} due to R_E/R_S, R_B/R_G and minimize C_{bc}/C_{gd}. In circuits with MOSFETs and AMOS varactors, fix W_f and vary N_f to contain the impact of channel strain variation with W_f.
- Design the circuit at schematic level with R_G added to the MOSFET digital model. The latter is sufficient to turn a "digital" into a good "RF" model. R_S and R_D are normally already included in the digital model.
- Optimize the transistor, cascode, or CMOS inverter cell layout through proper choice of metal stack on drain/collector and source/emitter, by monitoring f_{MAX} and NF_{MIN}. The optimal transistor layout depends on the stage topology: CE/CS, CB/CG, CC/CD, cascode, CMOS inv., etc.
- Include RC-extracted transistor (cascode) layout in schematic.

- Design and model inductors and interconnect in ASITIC based on the desired inductance obtained from schematic-level design with extracted transistors and pad capacitance.
- Add the ground-plane and power-plane metal mesh and the metal fill patterns to the cell and extract the layout of the cell, excluding inductors.
- Add inductor and interconnect models to schematic of RC-extracted cell.
- Add interconnect between cells and model it in ASITIC, ADS or HFSS.

With this approach, the number of iterations between layout and schematic simulations is minimized and first-pass success with at least 10% accuracy is assured, even in the absence of RF foundry models for MOSFETs and varactors.

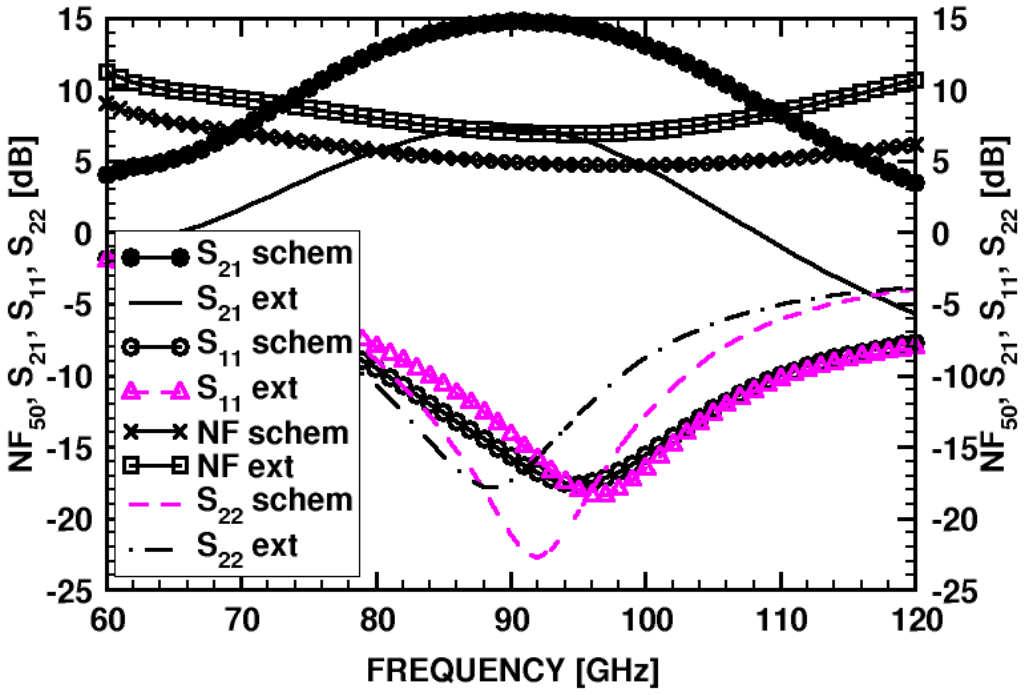

Fig.10. Impact of transistor layout RC-parasitics on 90GHz 65nm LP-CMOS amplifier gain and noise figure degradation.

5. Doppler radar and active imaging transceivers

Fig. 11 illustrates a generic mm-wave transceiver block diagram suitable for multi-gigabit radio, ACC radar, and active imaging applications. Using lumped inductors and transformers as tuning and matching elements, such a system can be realized in a silicon area smaller than 2 mm^2 [4],[18],[28]. Large receiver arrays sharing a fundamental or second harmonic VCO and PLL, as in Fig. 12, are needed for remote sensing. For robust operation over process, temperature and power supply variation, the PLL should be implemented with a static frequency divider chain. To be practical, these SOCs must first overcome the

cross-talk between adjacent transceivers, the leakage from the transmitter to the receiver, large 1/f noise at sub-MHz offsets from the carrier, and large power dissipation, particularly in the VCO and PLL blocks. To contain the power dissipation at acceptable levels, particularly in imagers, all mm-wave building blocks should be powered from 2.5V or lower supplies.

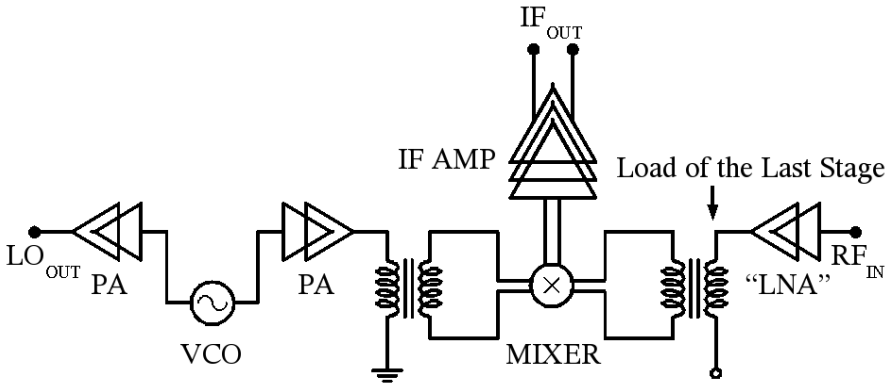

Fig.11. Block diagram of a generic SiGe BiCMOS or 65nm CMOS 80/160GHz transceiver for automotive radar and active imaging applications

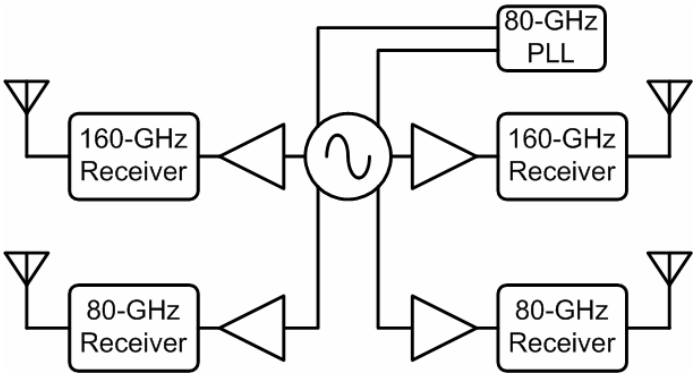

Fig.12. Block diagram of a generic SiGe BiCMOS or CMOS 80/160GHz receiver array for passive imaging applications

The ACC radar has been the first mm-wave application to draw the attention of SiGe technology foundries due to its potentially large volume and relatively stringent requirements for output power and phase noise, which cannot be easily satisfied in CMOS. A system breakout with separate transmitter and receiver dies has been preferred [1], with the antenna placed on the board or in the package. Fig. 13 illustrates a 5V, 77GHz transmitter implemented in 225GHz SiGe HBT technology which consumes 2.8W and features a VCO, a variable-gain amplifier, a 16dBm power amplifier, an auxiliary power amplifier, and a dynamic frequency divider [1]. A companion receiver chip consists of a high-linearity doubly-balanced Gilbert-cell mixer with common-base RF input stage

and t-line baluns at the RF and LO ports for single-ended to differential conversion. Single-chip transceiver arrays with on-die antennas, not applicable to the ACC radar, were also reported [24]. They require sophisticated packaging to increase antenna gain [24], thus offsetting the cost advantage and the rationale of having on-chip antennas.

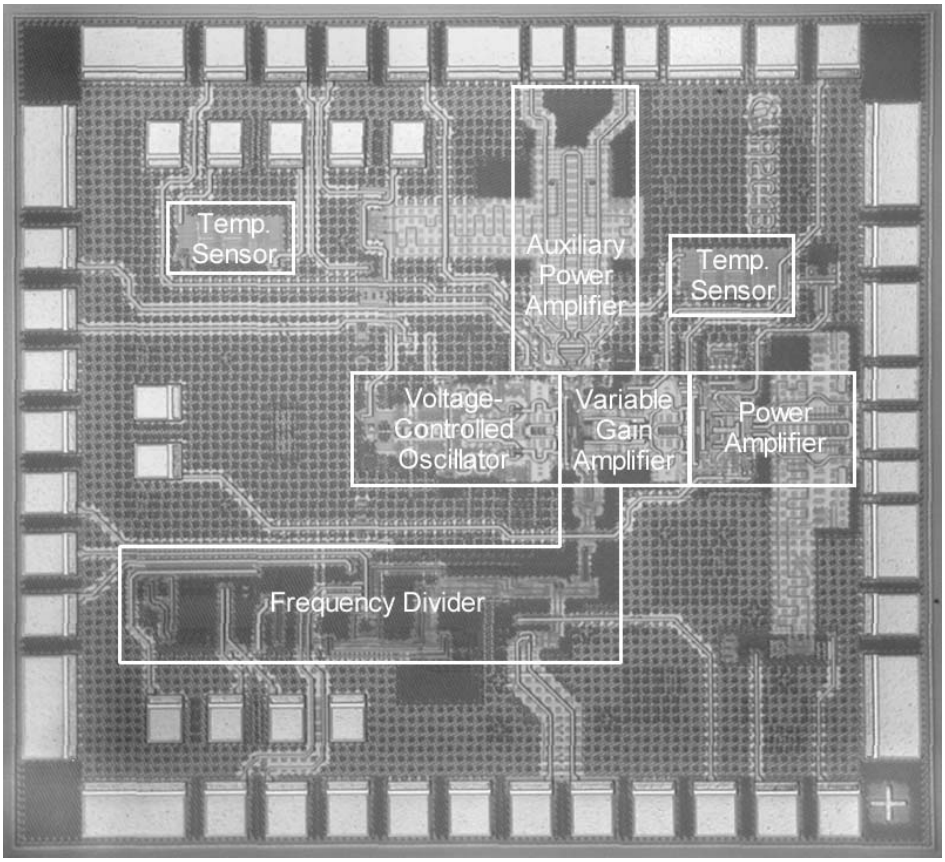

Fig.13. Die photograph of a 77GHz transmitter implemented in SiGe HBT technology courtesy of Infineon Technologies [1].

6. Comparison of SiGe HBT, SiGe BiCMOS and CMOS mm-wave IC building blocks

HBTs and MOSFETs have similar small signal and noise equivalent circuits at mm-wave frequencies. Therefore, the same circuit topologies and circuit design methodologies, relying on constant current density biasing schemes at the characteristic current densities (minimum NF_{MIN} bias, J_{OPT}, peak f_{MAX}, or peak f_T bias) apply to LNAs, PAs, VCOs and CML logic gates implemented with MOSFETs or HBTs [32],[35]. At frequencies above 60 GHz, the input impedance and the noise impedance of MOSFETs and HBTs, or of cascode topologies with HBTs and MOSFETs, described by (2) and (3), become more

resistive due to the parasitic resistances associated with the base/gate and emitter/source regions, and due to the decreasing reactance.

$$Z_{IN}(MOS) = R_S + R_G - j\frac{\omega_T}{\omega g_m}; \qquad Z_{IN}(HBT) = R_E + R_B - j\frac{\omega_T}{\omega g_m} \quad (2),$$

$$R_{SOPT}(MOS) \cong R_S + R_G + k\frac{\omega_T}{\omega g_m}; \; R_{SOPT}(HBT) \cong R_E + R_B + k\frac{\omega_T}{\omega g_m} \quad (3),$$

In (2) and (3), ω_T and g_m already include the impact of R_S or R_E, and are easily obtained from high frequency measurements or simulations, while k is a function of the degree of correlation between the input and output noise currents of the transistor, and is typically close to 0.5. The Miller effect is at least partly accounted for in (2) and (3) through ω_T, especially for cascode stages.

For example, for the 65nm MOSFET and SiGe HBT in Fig. 2, R_S+R_G and R_E+R_B are 3.5 Ω and 14 Ω, respectively. Suppose that these devices were to be sized for noise matching at 77 GHz to 40 Ω [21] and 33 Ω [18], respectively, to account for pad capacitances of 20 fF and 30 fF, respectively. A 16×65nm×1μm MOSFET would be needed, biased for minimum noise at 2.5 mA, with the total series parasitics of 19 Ω, practically half of the optimum noise impedance. Similarly, the corresponding 2×0.13μm×3.75μm HBT will be biased at 8 mA, with total series parasitics of 15 Ω, also about 50% of the optimum noise impedance. These two examples illustrate that transistor parasitics play a primary role at mm-wave frequencies, and that foundries must be able to control them tightly, which appears to be the case in both CMOS and SiGe BiCMOS technologies. In Colpitts VCOs, the increasingly resistive impedance of the transistor is compensated by connecting a high-Q MIM capacitor across the base-emitter or gate-source junction, improving the negative resistance and reducing the phase noise contribution from the resistive parasitics [16],[20].

Next, the experimental performance of 77 GHz LNAs, PAs, frequency dividers and VCOs implemented with HBT-only, MOS-HBT BiCMOS cascodes, and 90nm GP and 65nm LP CMOS transistors will be compared. All these circuits have state-of-the-art performance. The SiGe-HBT circuits were fabricated in a 0.13μm SiGe BiCMOS production process, as well as in variants of this process with several HBT collector profile splits. This allowed drawing a direct correlation between the circuit performance and the HBT f_T and f_{MAX}. The SiGe HBT f_T/f_{MAX} for the technology splits are listed in Table 1. Measurement results are reported for wafer 5, except where indicated. The comparison with CMOS is only carried out for LNAs [4],[21] and VCOs [20] because at the time of

writing, there are no reported CMOS PAs and static frequency dividers operating at 80 GHz or above.

TABLE 1. TECHNOLOGY SPLIT PROCESS PARAMETERS.

Wafer #	f_T (GHz)	f_{MAX} (GHz)	Collector doping	Emitter width
5	250	290	Reference=C	0.13 μm
3	245	280	C+	0.13 μm
7	265	255	C++	0.13 μm
2	260	240	C+++	0.13 μm
6	170	210	Production BiCMOS9	0.13 μm
7	150	160	Production BiCMOS9	0.17 μm

6.1. Amplifiers

In the design of the SiGe-HBT LNA shown in Fig. 14, a 3-stage topology was chosen, which consists of two CE stages followed by a cascode stage [18]. The CE stages allow for 1.2-1.8V operation and minimize the overall noise figure of the LNA, while the cascode stage provides higher gain and is biased from a 1.8-2.5V supply. The input is simultaneously noise and impedance matched using the techniques described in [21],[32]. The LNA consumes a total of 40(60)mW from 1.5(1.8)V and 1.8(2.5)V supplies. The simulated noise figure, gain and input return loss are 5.3dB, 20dB, and -40 dB, respectively. Fig. 15 compares the measured and simulated gain and input return loss for 1.8V and 2.5V supplies at 25 C and 125 C, showing excellent performance, with less than 3dB gain degradation at 77 GHz and 125C, and the input return loss better than -12 dB from 78 GHz to 95 GHz. The 3-dB bandwidth extends from 77GHz to 90GHz with the highest gain of 19dB centered at 86GHz while S_{12} is better than -50 dB. Because a standalone down-converter was not available for W-band noise measurements, only the noise figure of a mixer test structure was measured at this time. This was 12.5 dB at 73 GHz, close to simulations [18], indicating that the simulated 5.3 dB noise figure value of the LNA is also realistic.

The schematics of the 65nm LP CMOS LNA is shown in Fig. 16 and consists of 3-cascode stages with inductive broadbanding [21]. As in the SiGe HBT LNA, the input stage is simultaneously noise and impedance matched. The measured and simulated S parameters, shown in Fig. 17, demonstrate a peak gain of 9 dB at 80 GHz when the amplifier is powered from a 2.2V supply and consumes 40mW. The simulated noise figure is 7dB. The large V_{DD} is imposed by the fact that the LVT, 65nm LP n-MOSFET requires a V_{GS} of 0.9 V (similar to the V_{BE} of a SiGe HBT) at peak f_T bias. Finally, the measured gain of the SiGe HBT and CMOS LNAs are compared in Fig. 18. Even the production SiGe HBT with an

f_T of 170 GHz provides more gain than the 65nm LP CMOS one, while dissipating similar power.

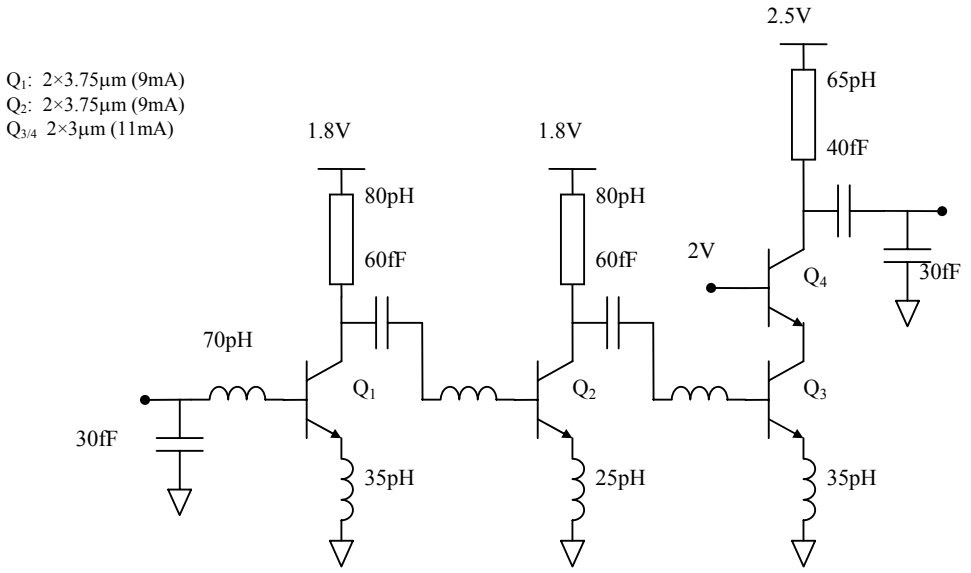

Fig.14. Schematics of 80GHz, SiGe HBT LNA.[18]

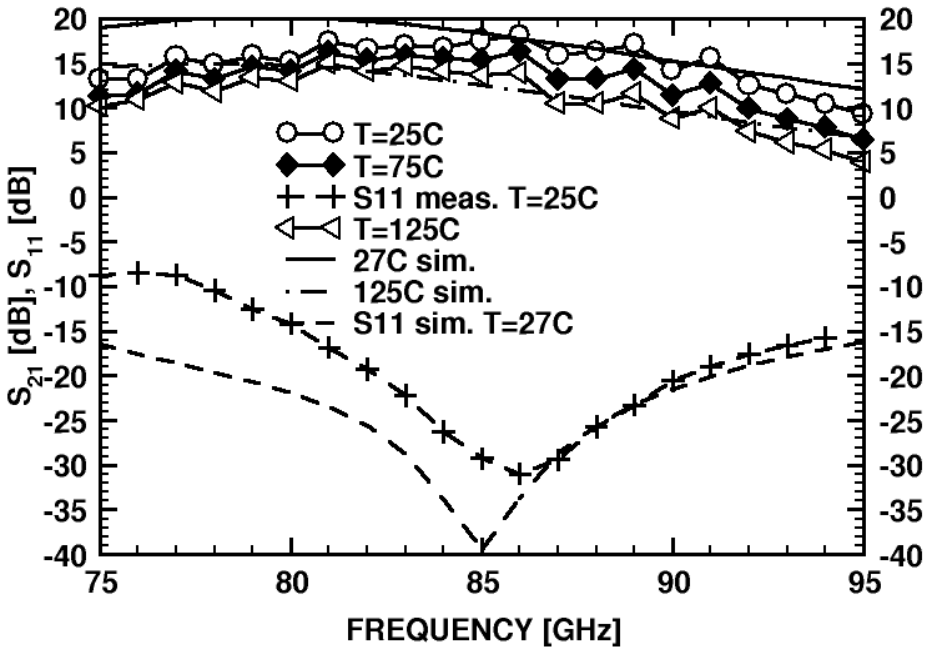

Fig.15. Measured (symbols) vs. simulated (lines) S parameters of 80GHz, SiGe HBT LNA at different temperatures.

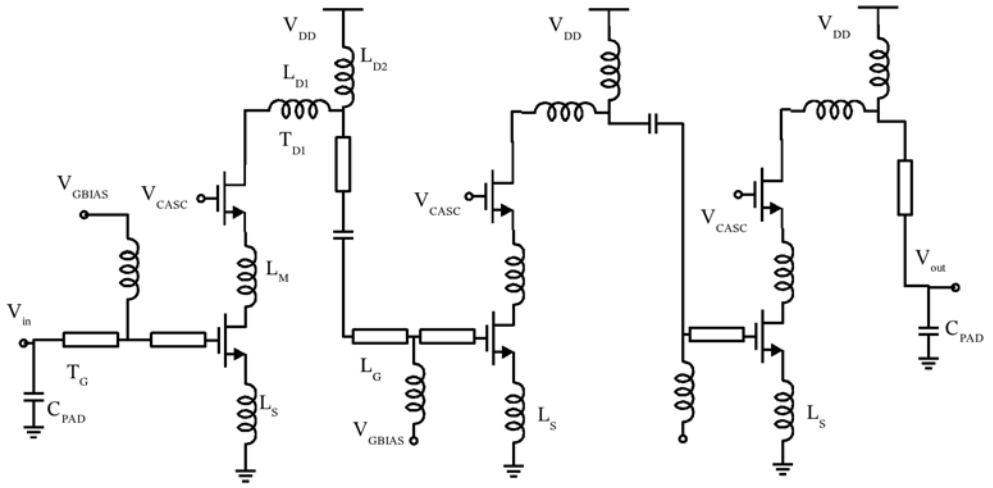

Fig.16. Schematics of 80GHz, 65nm CMOS LNA [4].

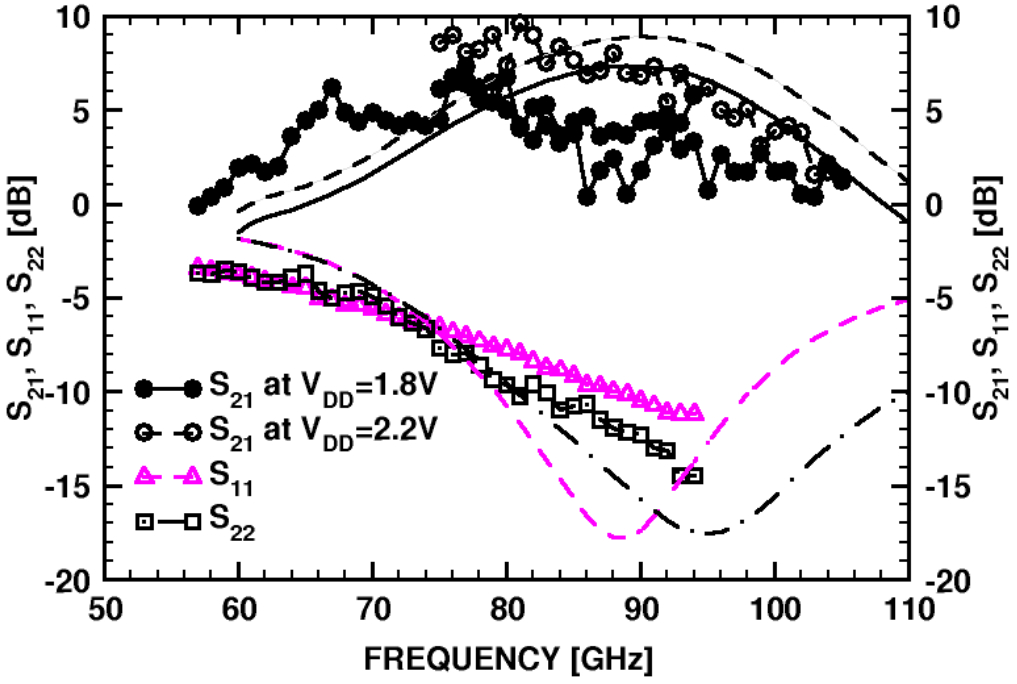

Fig.17. Measured (symbols) vs. simulated (lines) S parameters of 80GHz, 65nm CMOS LNA for different supply voltages.

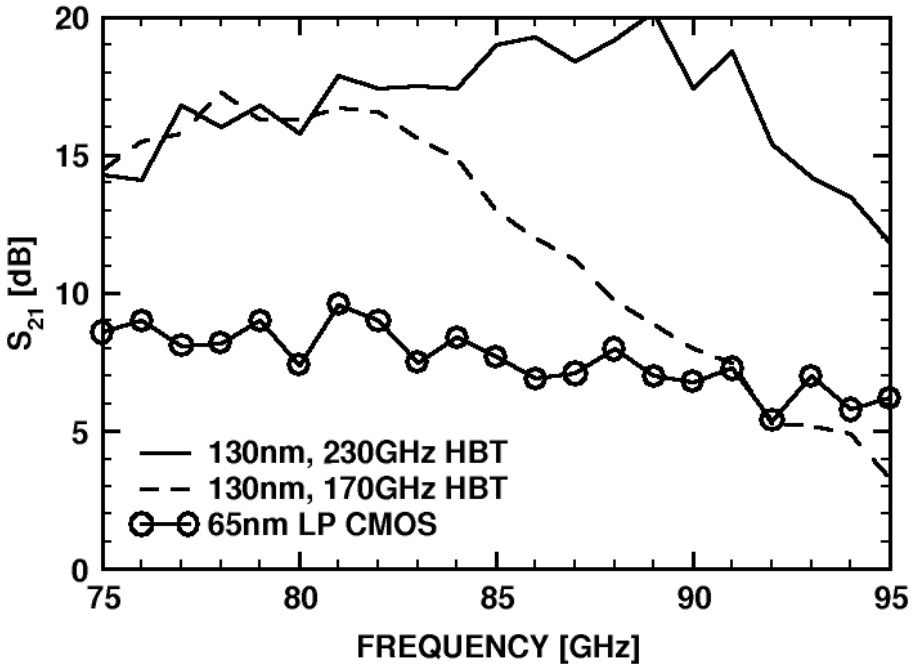

Fig.18. Measured gain of 80GHz SiGe HBT and 65nm LP CMOS 3-stage LNAs.

Fig. 19.a. reproduces the schematics of a single-ended, 3-stage SiGe-HBT power amplifier consisting of a cascode stage - for large gain and powered from 2.5V - followed by two CE stages, for maximum power-added efficiency (PAE) and 1.8V supply [18]. Transistor sizes and currents increase by a factor of 2 from stage to stage toward the output. The CE stages have no inductive degeneration and are biased in class AB mode to maximize the saturated output power. For comparison, Fig. 19.b. describes a single-stage differential output buffer employing 130nm MOS-HBT cascodes and operating in the 85-90 GHz range. The latter draws 80mA from 2.5-3.3V supplies.

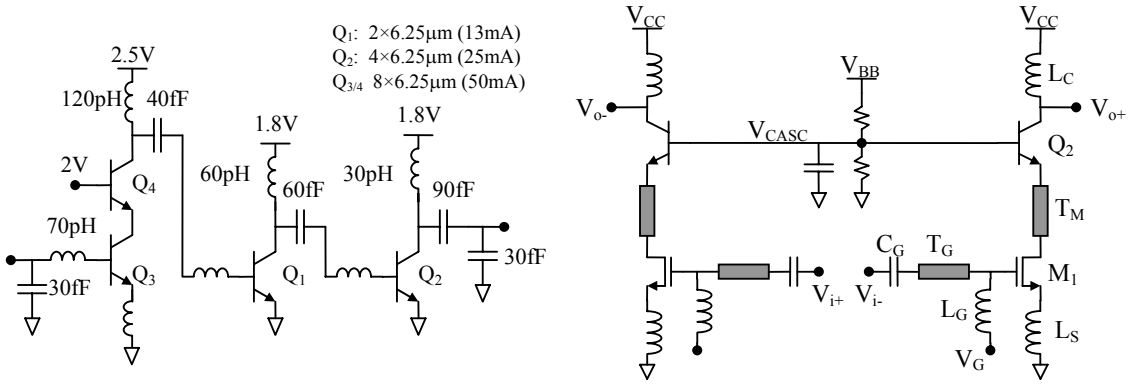

Fig 19. 3-stage SiGe HBT PA schematic and b) schematic of differential single-stage MOS-HBT cascode output buffer for W-band VCOs.

The gain and output power of the first PA were measured from 75GHz to 95GHz over temperature up to 125 C, and over the 5 wafer splits [18]. At 77GHz, the PA achieves S_{21} of 15 dB, saturated output power of +13 dBm, and PAE of 12% (based on 168mW P_{DC}). The measured gain of the single-stage differential output buffer which employs 130nm MOS-HBT cascodes, is plotted in Fig. 20 along with that of the 3-stage PA measured for two wafer splits. The single-stage output buffer exhibits higher gain in the 85-89 GHz range than the 3-stage PA realized with 170GHz HBTs, and delivers +10.5 dBm differentially at 87 GHz. This is the first power amplifier operating above 60 GHz that uses MOSFETs, and it demonstrates once again [29],[35] that, by combining MOSFETs and HBTs at high frequencies, one can obtain better performance than that of the corresponding MOS-only or HBT-only circuits.

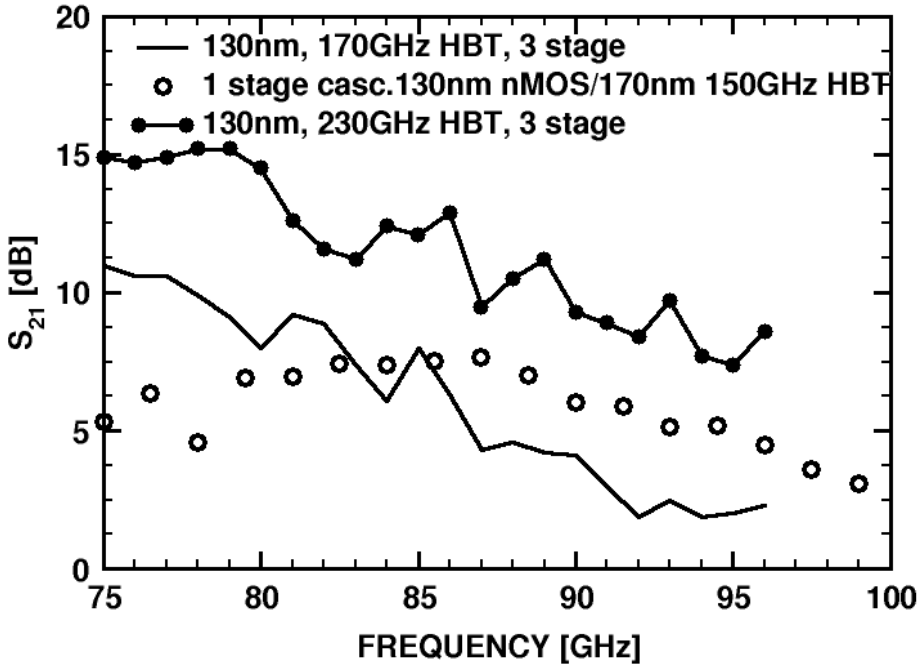

Fig.20. Measured gain of 80GHz SiGe HBT 3-stage PAs and of a 1-stage BiCMOS cascode differential PA.

6.2. Static Frequency Dividers

To verify the viability of a robust, fundamental frequency PLL at 80 GHz, a divide-by-64 static frequency divider chain, based on the low-power, 3.3V SiGe HBT topology in [17] was fabricated. The die photo is reproduced in Fig. 21. The divider was tested over temperature from 25 C to 125 C. The output spectrum, measured for a 77GHz input at 125 C is shown in Fig. 22. The self-oscillation frequency (SOF) was measured on each of the 5 wafer splits and is plotted in Fig. 23 along with the gains of the SiGe HBT LNA, SiGe-HBT PA

and with the downconversion gain of a SiGe-HBT common-base, Gilbert-cell, mixer [18], as a function of the SiGe HBT f_{MAX} (a different f_{MAX} for each wafer). Remarkably, but not surprisingly, in all cases, the best circuit performance is obtained for the wafer split with the highest f_{MAX}. Since only the SIC implant was changed in these wafer splits, the f_{MAX} on each wafer degrades as the f_T is improved. There is thus no ambiguity that f_{MAX} rather than f_T is the more important transistor figure of merit for mm-wave ICs. In a separate experiment to be described elsewhere, the noise figure of the 77GHz mixer also improves with the HBT f_{MAX}.

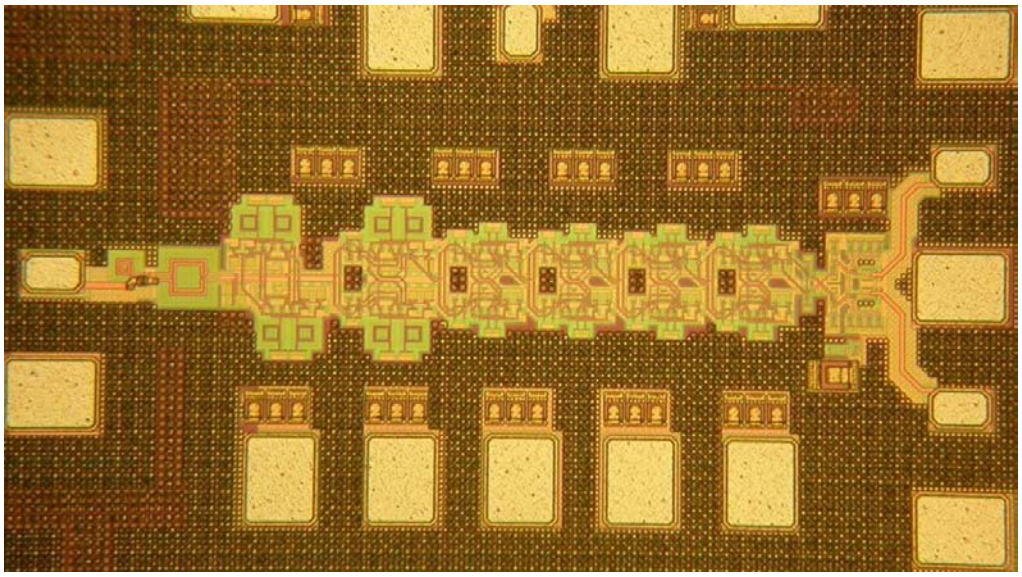

Fig.21. Die photo of 100GHz divide-by-64 chain.

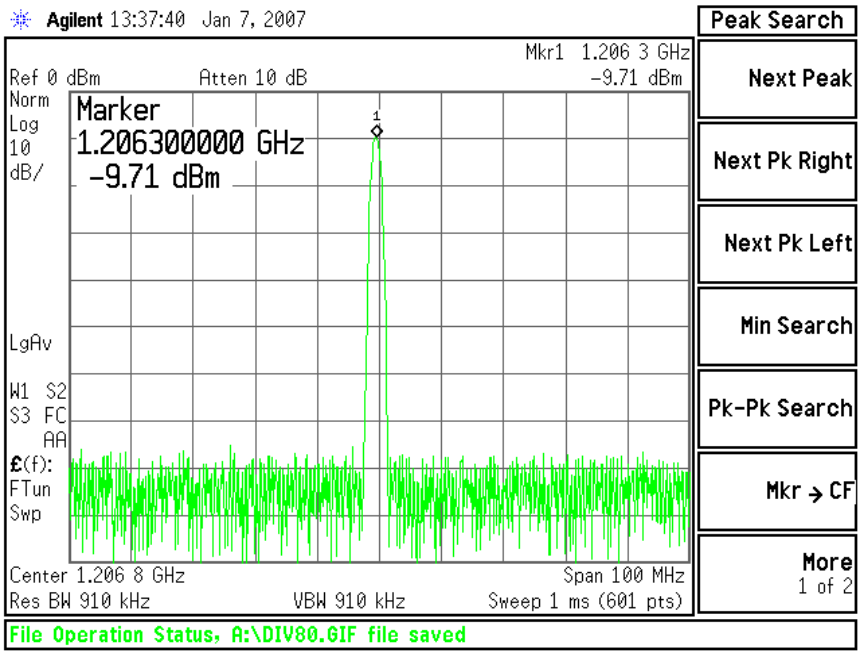

Fig.22. Measured output of divide-by-64 chain for a 77GHz input at 125 C.

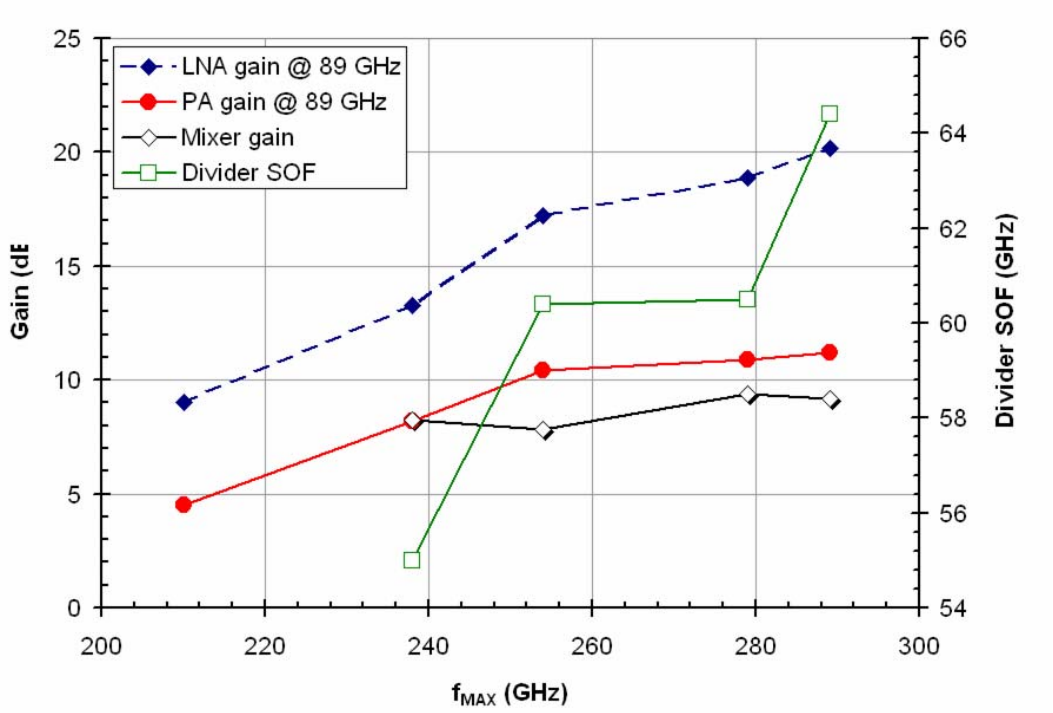

Fig.23. Measured 80GHz SiGe HBT LNA, PA and static frequency divider SOF across wafer splits as a function of the f_{MAX} of SiGe HBT on each wafer.

6.3. VCOs

Record low-phase-noise Colpitts VCOs (Fig. 24) were implemented with SiGe HBTs [16] (Fig. 24) and 90nm GP MOSFETs [20] (Fig. 25) for operation in the 77GHz to 105GHz range. The oscillation frequency (f_{osc}) of the VCO is given by (4). In line with the VCO design methodology outlined in [32], the tank inductance (L_B) is chosen as the smallest realizable inductance with hi-Q, or about 25pH for the HBT, and 50pH for the CMOS technologies. Thus, C_{EFF} is fixed by the desired oscillation frequency. In reality, C_π (or C_{GS}) is much greater than C_{VAR}, and consequently, $C_{EFF} \approx C_{VAR}$ for design purposes.

$$f_{osc} = \frac{1}{2\pi\sqrt{L_B C_{EFF}}} \qquad C_{EFF} = \frac{C_{VAR}(C_1 + C_\pi)}{C_{VAR} + C_1 + C_\pi} \tag{4}$$

The negative resistance provided by Q_1, given by (5), must be large enough to overcome losses in the tank and the base/gate and emitter/source resistance. In the W-band, the finite Q of the varactor (C_{VAR}) and of the base/gate inductance (L_B) adds substantial losses to the tank.

$$R_{NEG} \cong R_B + R_E + \frac{\omega_{osc} L_B}{Q_{LB}} + \frac{1}{\omega_{osc} Q_{CVAR} C_{VAR}} - \frac{g_m}{\omega_{osc}^2 (C_\pi + C_1) C_{VAR}} \quad (4)$$

Capacitor C_1 is important in minimizing the oscillator phase noise, vital in radar applications.

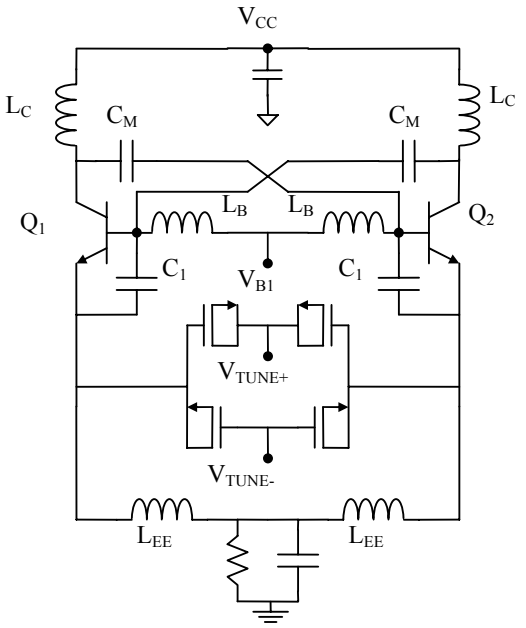

Fig.24. Schematics of 100GHz SiGe BiCMOS VCOs [16].

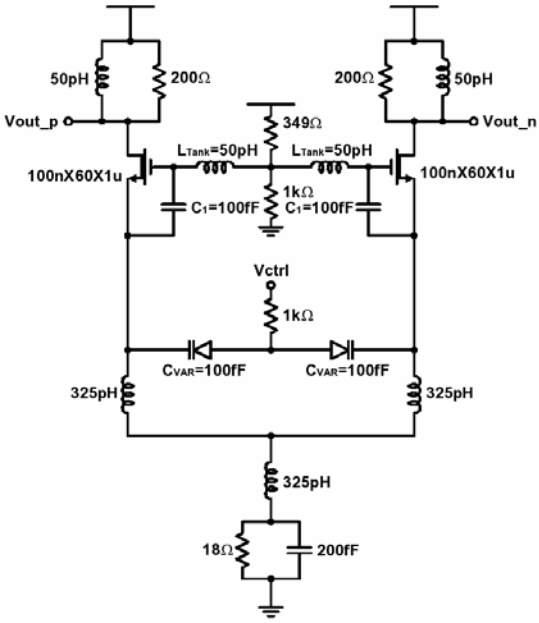

Fig.25. Schematics of 79GHz 90nm GP CMOS VCO [20].

Record phase noise values of -101.3 and -100.2 dBc/Hz, respectively, were measured at 1MHz offset from the 105 GHz SiGe HBT VCO carrier (Fig. 26) and from the 79GHz carrier of the CMOS VCO, as needed in imaging and ACC radar applications. However, the output power is at least 18 dB higher for the SiGe HBT VCO while its power consumption is only 4 times larger: 120mW vs. 30mW. The measured tuning characteristics of the CMOS VCO are very linear, spanning 73 to 79 GHz. The fact that the ITRS FoM for VCOs excludes output power explains why CMOS VCOs rate very highly using this figure of merit. However, in many applications, a mm-wave VCO with low output power would require amplification before becoming useful. A better design strategy is to dissipate greater power in the VCO core, which reduces the overall VCO complexity by eliminating amplifier stages. Furthermore, increased core power dissipation can ultimately improve phase noise, whereas amplifying stages do nothing to improve phase noise.

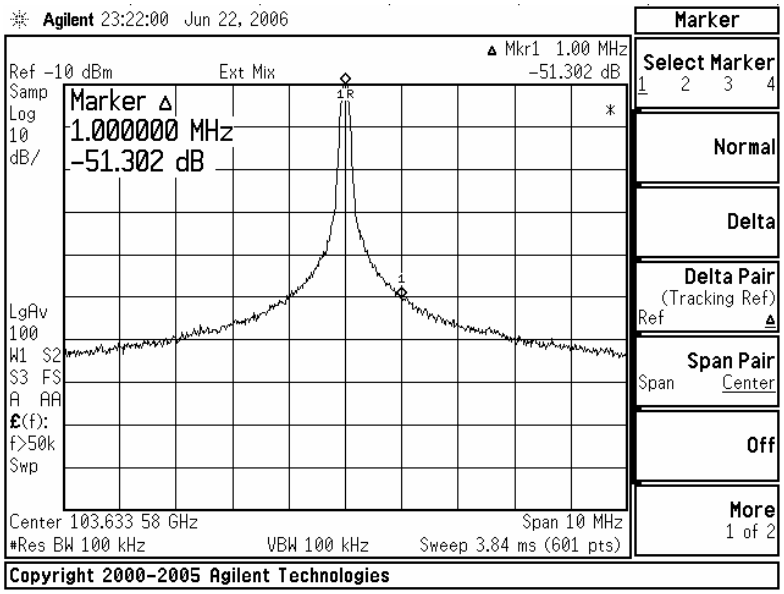

Fig.26. Measured Phase Noise of 105GHz SiGe HBT VCO [16].

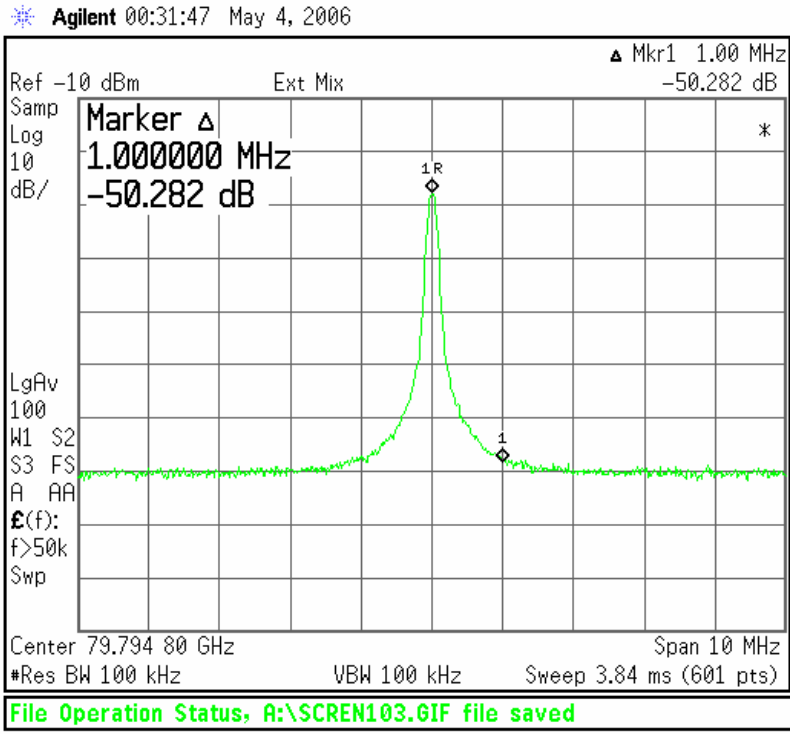

Fig.27. Measured Phase Noise of 79GHz 90nm GP CMOS VCO [20].

7. Conclusions

As a result of the larger breakdown voltage, transconductance, and f_T, and because of their reduced sensitivity to layout parasitics and temperature variation when compared to 65nm CMOS, SiGe HBTs and SiGe BiCMOS

technologies have established a clear advantage and a strong foothold at mm-wave frequencies. They are set to seriously challenge the supremacy of III-V transistors in all but the lowest noise astronomy applications. While showing good promise for WLAN applications at 60 GHz, 90nm GP and 65 nm LP CMOS technologies do not have adequate performance for most IC building blocks required in 77 GHz ACC systems. However, this situation may change in the 45nm node. By applying constant-field scaling rules to inductors and transformers, and design methodologies that have proven successful at GHz-frequencies, it is now possible to integrate 80GHz and 160GHz transceiver arrays on a silicon die and thus bring economies of scales, typical of silicon, to a variety of sensors for security, remote sensing, imaging and automotive radar applications at and beyond 80 GHz.

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