In the clouds:

Towards 1Tb/s per carrier

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University of Toronto

University of Southern California, October 12, 2012

Credits

Graduate students

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- Peter Asbeck
- Gabriel Rebeiz
- Jim Buckwalter
- Larry Larson

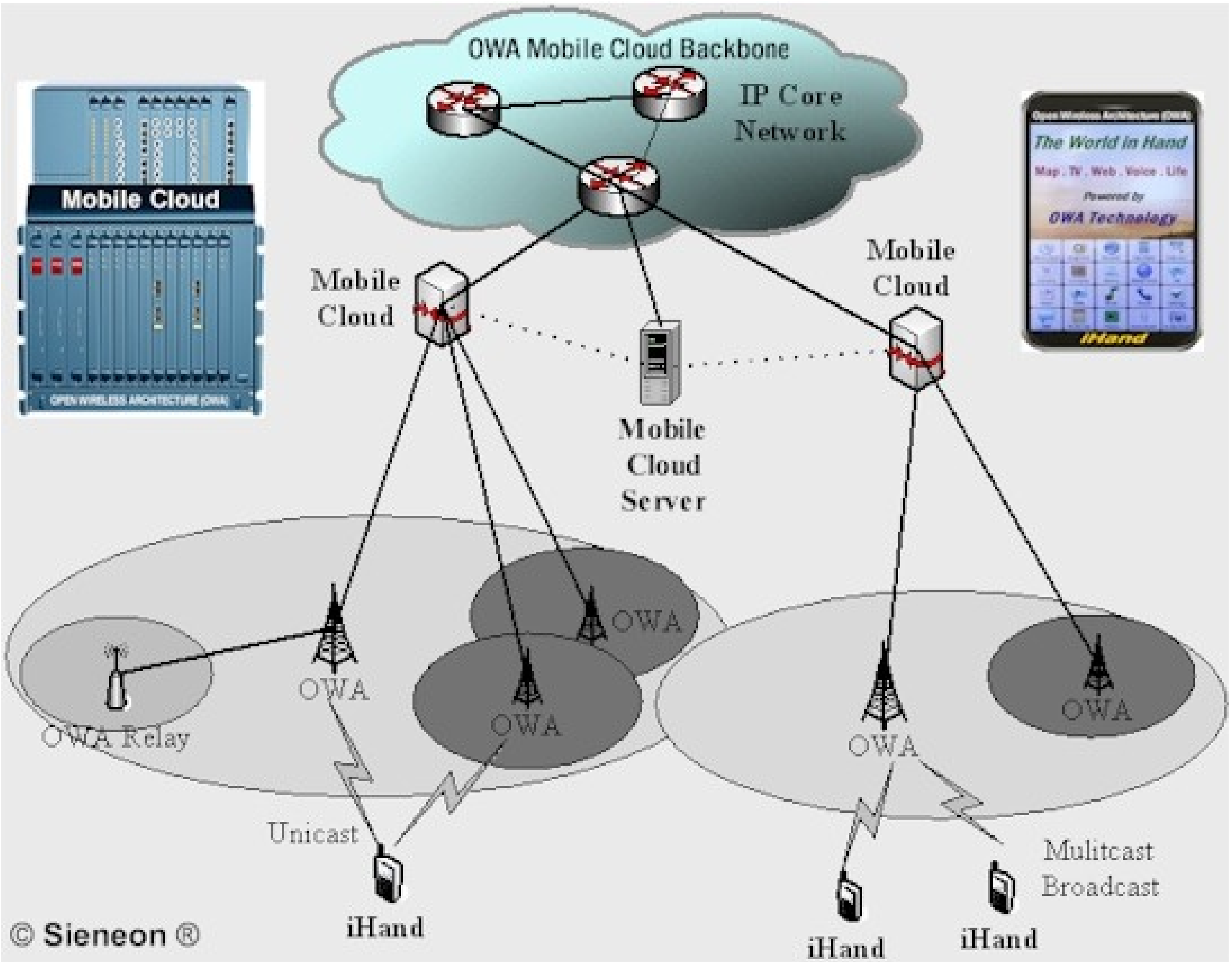
- NSERC, OCE
- Robert Bosch GmbH, DARPA, Ciena, Gennum for funding
- STMicroelectronics, Darpa, Ciena for chip donations

Outline

- Why?
- How?
  - System
  - Antenna
  - Baseband
  - Radio transceiver
- When

We are addicted …

What's in a cloud?



- wireless links
- optical fiber links
- data centers

What's in a data center?

- Optical fiber links
- Coaxial cable links
- Routers
- Boards
- Backplanes

Facebook pictures...

- 40 Million pictures uploaded per day to Facebook

  > 10^{15} bits/day => 15 Gb/s

- Worldwide: 2049 data centers

  consume 30 Billion Watts = 30 nuclear power stations

Evolution of CMOS since 2000

- 130 nm, f_T =80 GHz: V_{DD}=1.2 V
- 2002 => 90 nm, f_T =120 GHz: V_{DD}=1.2 V
  - Strained channel, SiGe S/D
- 2004 => 65 nm, f_T =180 GHz: V_{DD}=1.1-1.2 V
  - More strain
- 2006 => 45 nm, f_T =240 GHz: V_{DD}=1.0-1.2 V
  - High-K MG, more strain
- 2008 => 32 nm, f_T = 360? GHz: V_{DD}=0.9-1.2 V
  - High-K MG, more strain
- 2011 => 22 nm, f_T = 500?? GHz: V_{DD}= 0.9 V
  - Tri-gate, High-K MG, more strain

Some observations

$$E \propto f \cdot C \cdot V_{DD}^2$$

- Moore's law is alive!
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  - Clock frequency should improve=> **Hint, hint** digital designers

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Millimeter & sub-millimeter wave circuits are OK!

Why can't we reduce V_{DD}?

- Because the subthreshold slope, *S*, does not scale
- *S* determined by the Fermi-Dirac distribution function

$$S\left[V/decade\right]=\frac{kT}{q}\cdot\ln\left(10\right)$$

Valid in

- 3-D (Fin)FETs, bipolar transistors
- 2-D crystal FETs (graphene, MoS_2)
- 1-D FETs (nanowire, carbon nanotube)

So what are we to do?

$$S[V/decade] = \frac{kT}{q} \cdot \ln(10)$$

k and *q* are constants, *T* is a variable

Solutions

- Refrigeration: 77 K (liquid nitrogen), 4 K (space station?)
  - Not in your hand!
  - Possible in the data center
- New physics:
  - Tunnel FETs? Maybe, but S is V_{gs}-dependent.

More immediate solutions in…

- Wireless, wireline, fiberoptic system architectures that
  - Increase data rate >1 Tb/s carrier (imperative in fiber links)
  - Increase efficiency per bit
- Faster, more efficient circuit topologies
  - CMOS logic at 50-100 Gb/s to save power?
  - Stacked CMOS logic for large swing drivers?
- Can we push the carrier frequency to 300 GHz?

Energy Efficiency of Communication Links

	4G WiMAX	60 GHz LOS Radio	Wireline IEE 802.3.an	Fiber SerDes VCSEL	Fiber DP-QPSK/BPSK
Data Rate	≤1 Gbps	5.3 Gbps	10 Gbps	10 Gbps	50 Gbps
Power	1.76 W	350 mW	2 W	2.5 W	25 W
Distance		2 m	100 m	20 km	3500 km
Energy/bit	1.6 nJ/b	66 pJ/b	200pJ/b	250 pJ/b	500pJ/b
Energy/bit/m	↑	33 pJ/b/m	2 pJ/b/m	12.5 fJ/b/m	0.14 fJ/b/m
Reference	[Krishnamurthy, •RFIC 2010]	[Laskin, •RFIC 2011]	[Gupta, ISSCC 2012]	[Voinigescu, CICC 2001]	[Crivelli, ISSCC 2012]

Energy Efficiency of Communication Links

Optical: 10 fJ/b/m

5000 km

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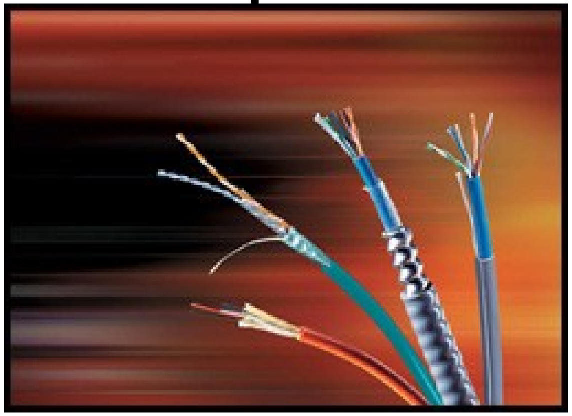
Source: Belden Inc.

Wireline: 2 pJ/b/m

100 m



Source: Belden Inc.

Energy Efficiency of Communication Links

Wireless> 30 pJ/b/m

10m

Source: Samsung

Optical: 10 fJ/b/m

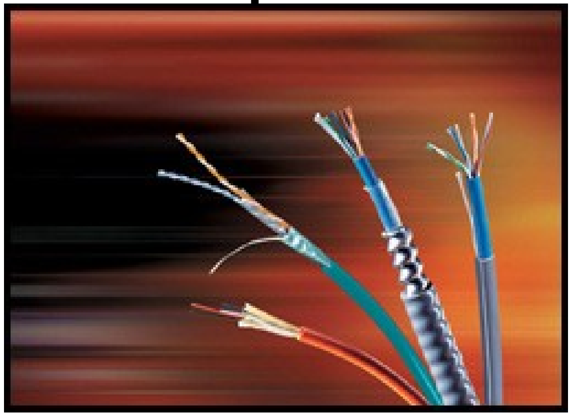
5000 km

Source: Belden Inc.

Wireless is the most inefficient, yet most popular!

Wireline: 2 pJ/b/m

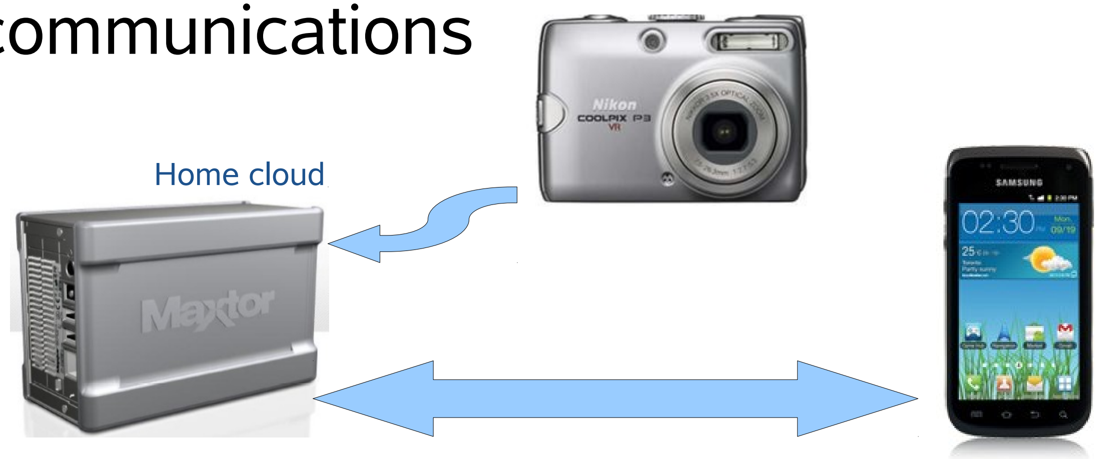
100 m



Source: Belden Inc.

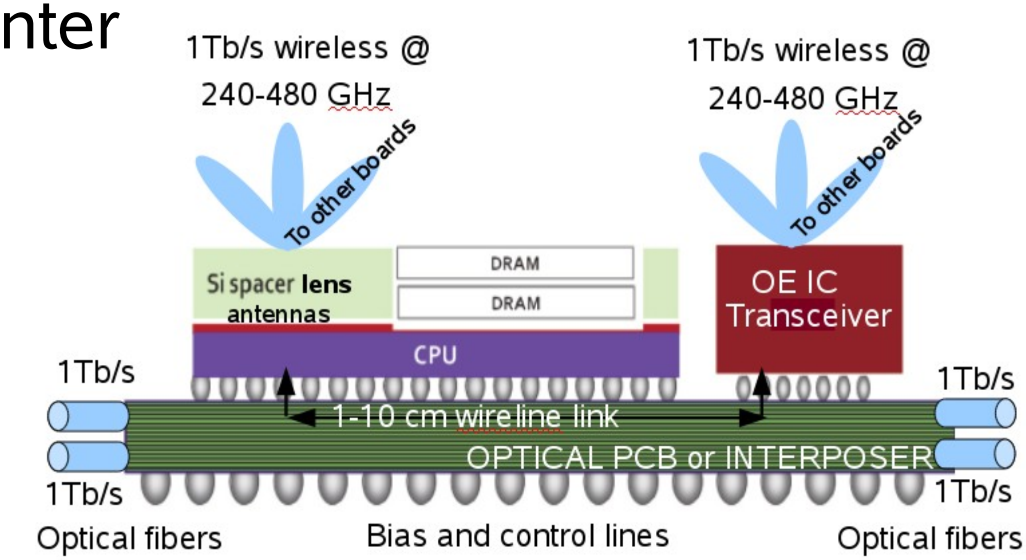
Why Tb/s wireless?

- Near field communications

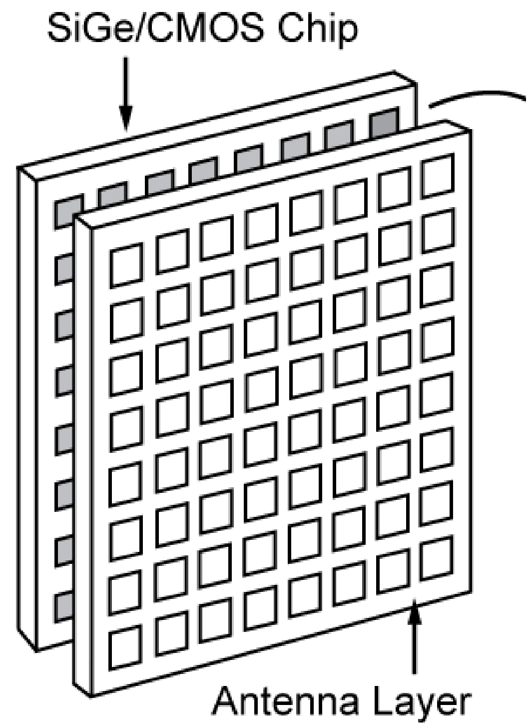


- Short-range reconfigurable wireless data transmission in the data center

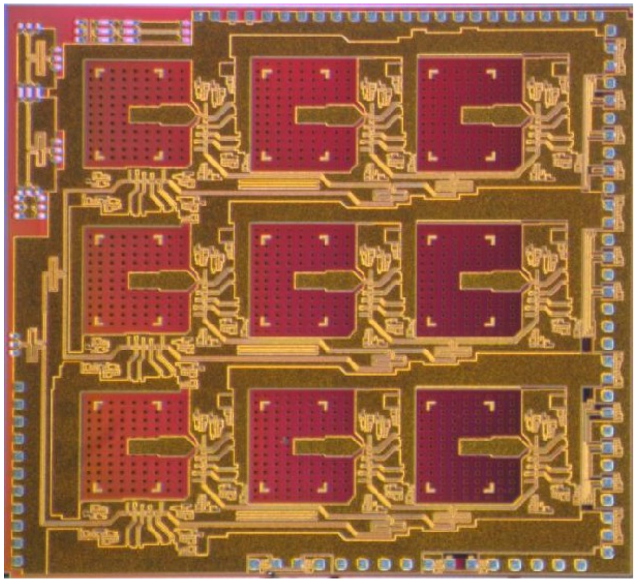
- Board-to-board



Why 200-300 GHz?



- Silicon transistors with f_{MAX}>400 GHz
- 100 GHz of bandwidth with no absorbtion
- Small antenna size with good gain
- Lower power LNA, mixer, receiver
- But...
  - higher power PLL,
  - reduced P_{out},
  - shorter range ~$1/f^2$



Source: G. Rebeiz UCSD

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Scalable Digital Radio Transmitters

- Can we improve efficiency by increasing the modulation rate per carrier at fixed P_{OUT}?

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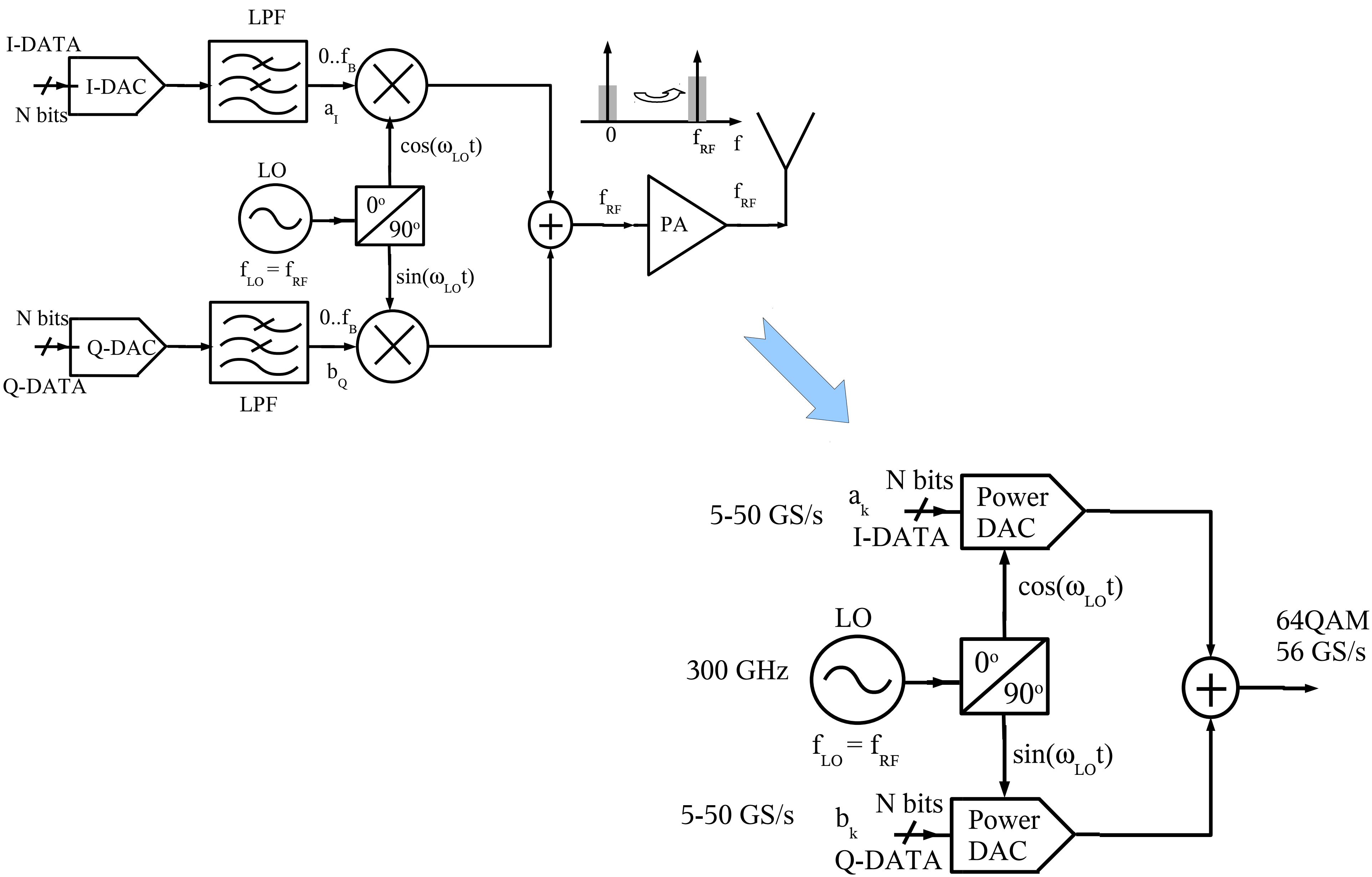
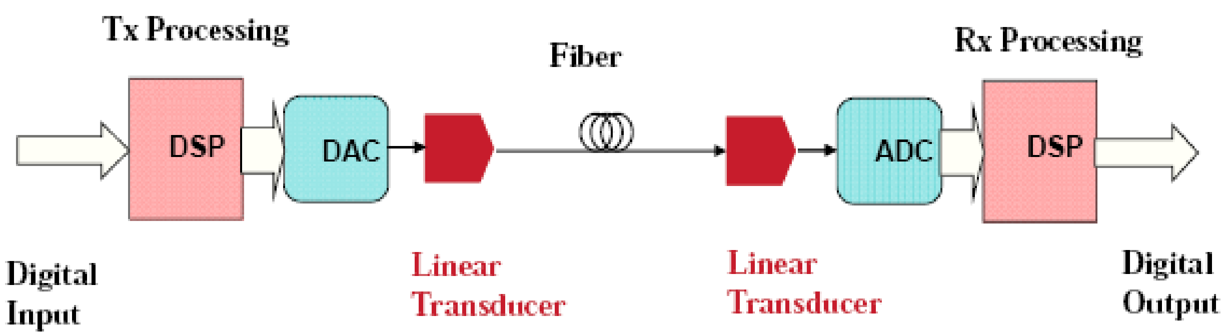
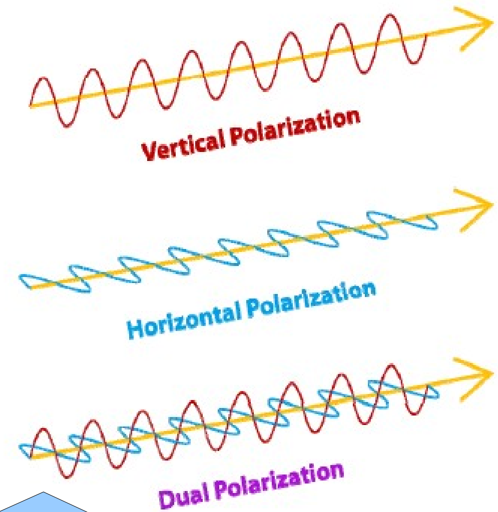
- Example: 0.3 Tb/s with 1 W PA => 3.3 pJ/b
    - But 0.3 Tb/s with 64 QAM modulation requires 50-Gb/s serial baseband lanes,
    - difficult to realize efficiently with up-conversion transmitter architecture

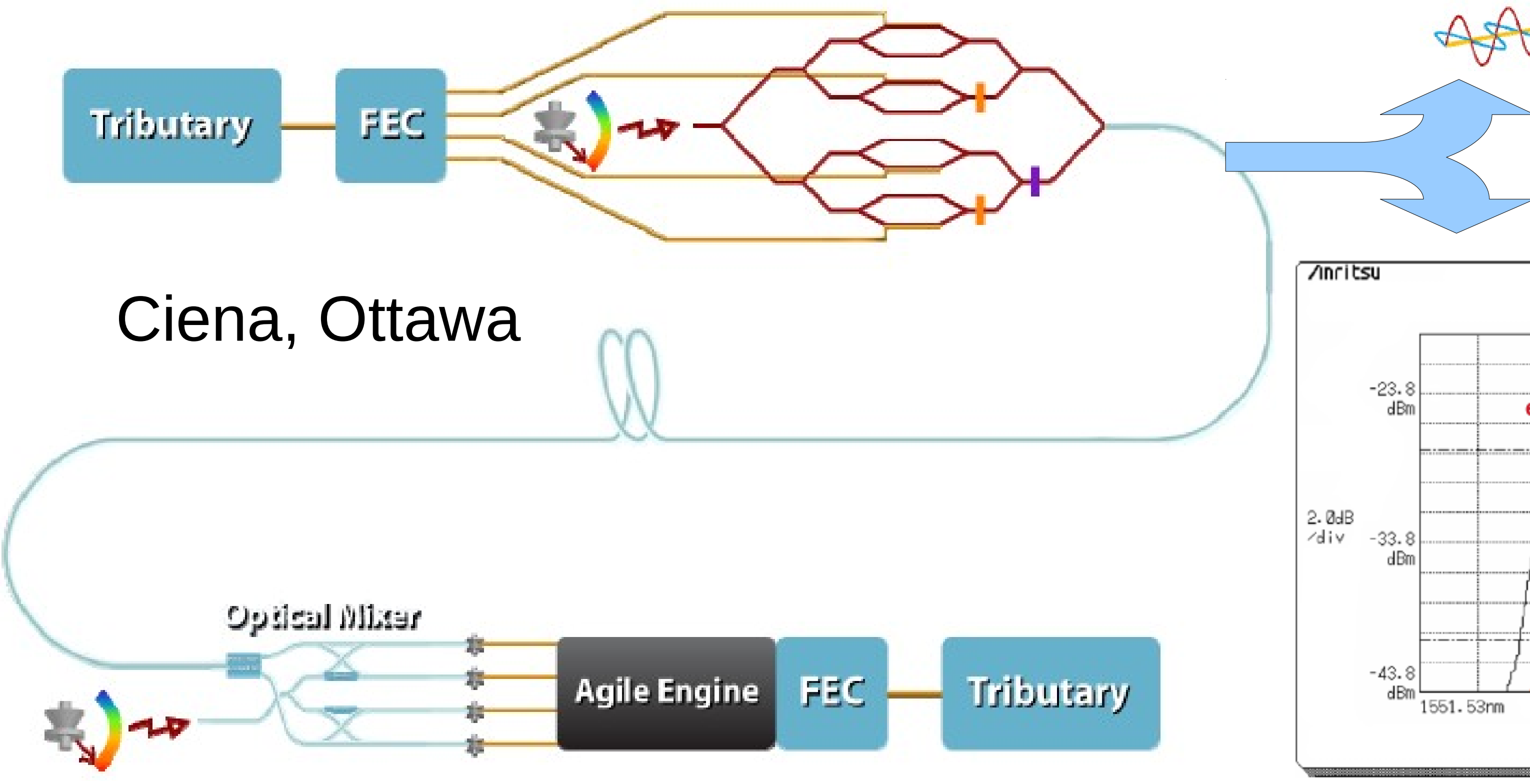
Potential Solution: Direct Modulation TX Radio



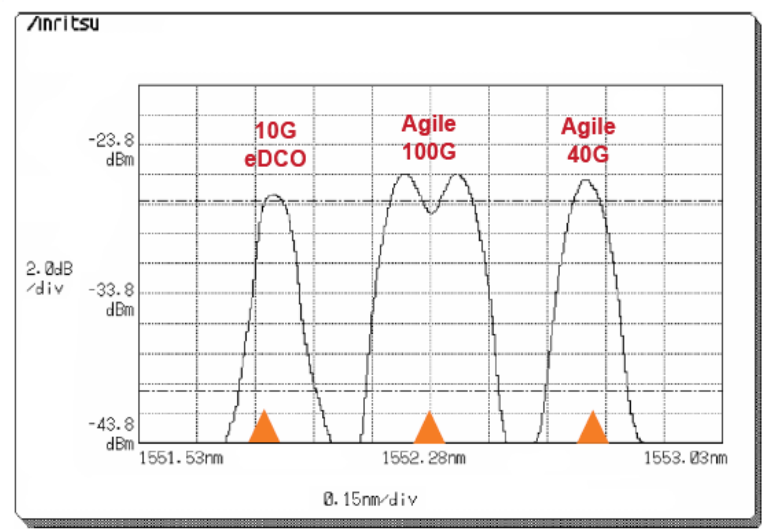
Like Coherent Fiberoptics links: 110 Gb/s TX-RX



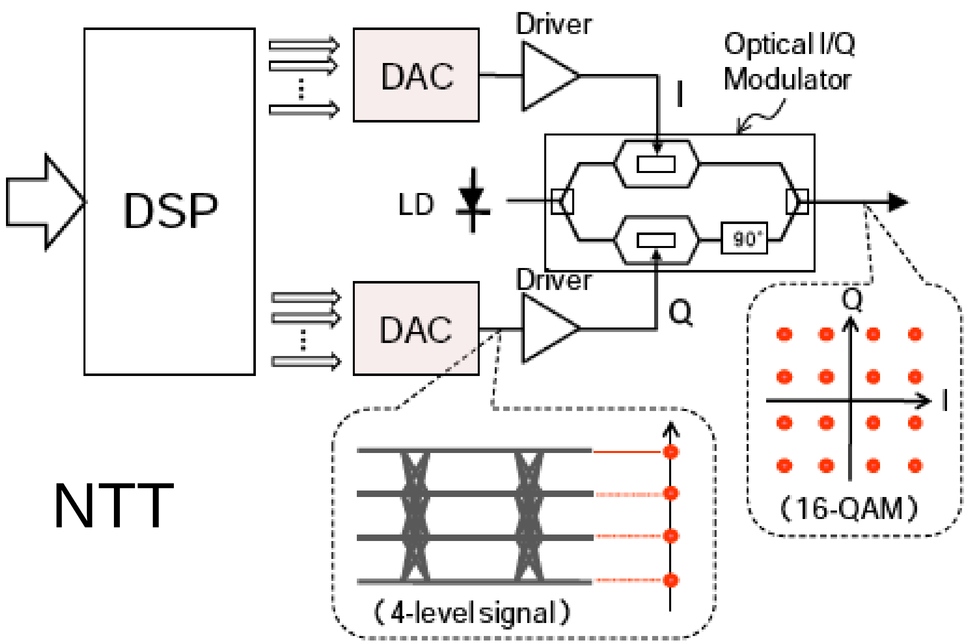




Ciena, Ottawa

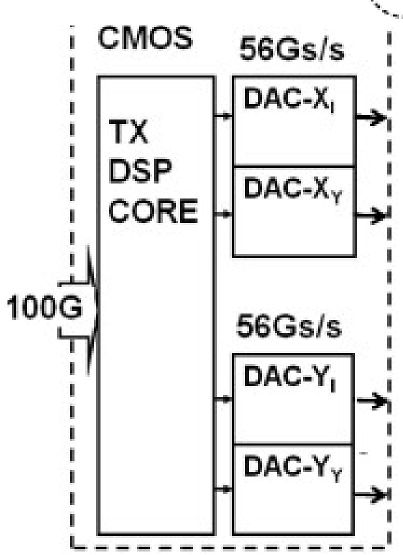


200+ Gb/s Dual-Polarization TX/RX (ii)



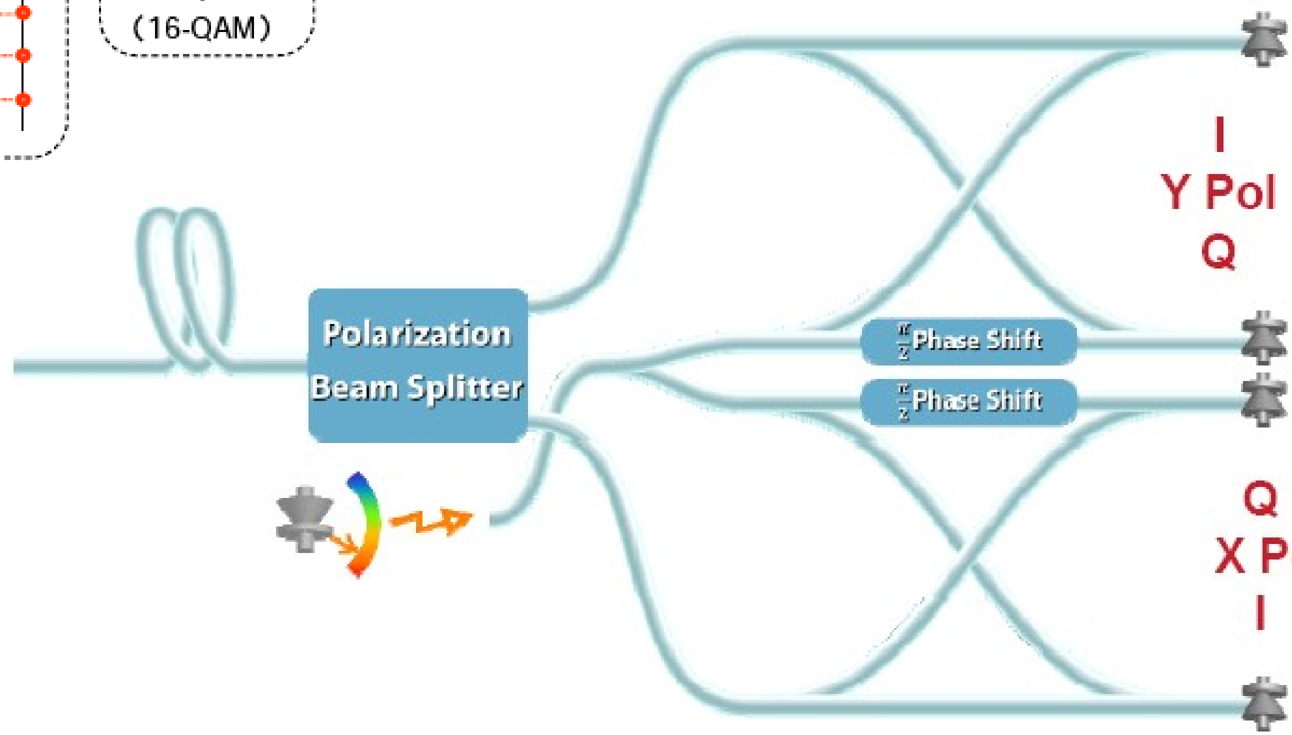
Direct QAM Modulation transmitter

NTT



Ciena

Coherent Detector



How can we get to 1 Tb/s per carrier?

- Fiber: Dual-polarization, 16 QAM at 125 Gbaud
  - 8 baseband lanes at 125 Gb/s
  - Power consumption is not that critical here....
  - Need phase equalization in receiver
  - Need large swing (>5V) 6-bit 125 GS/sec DACs

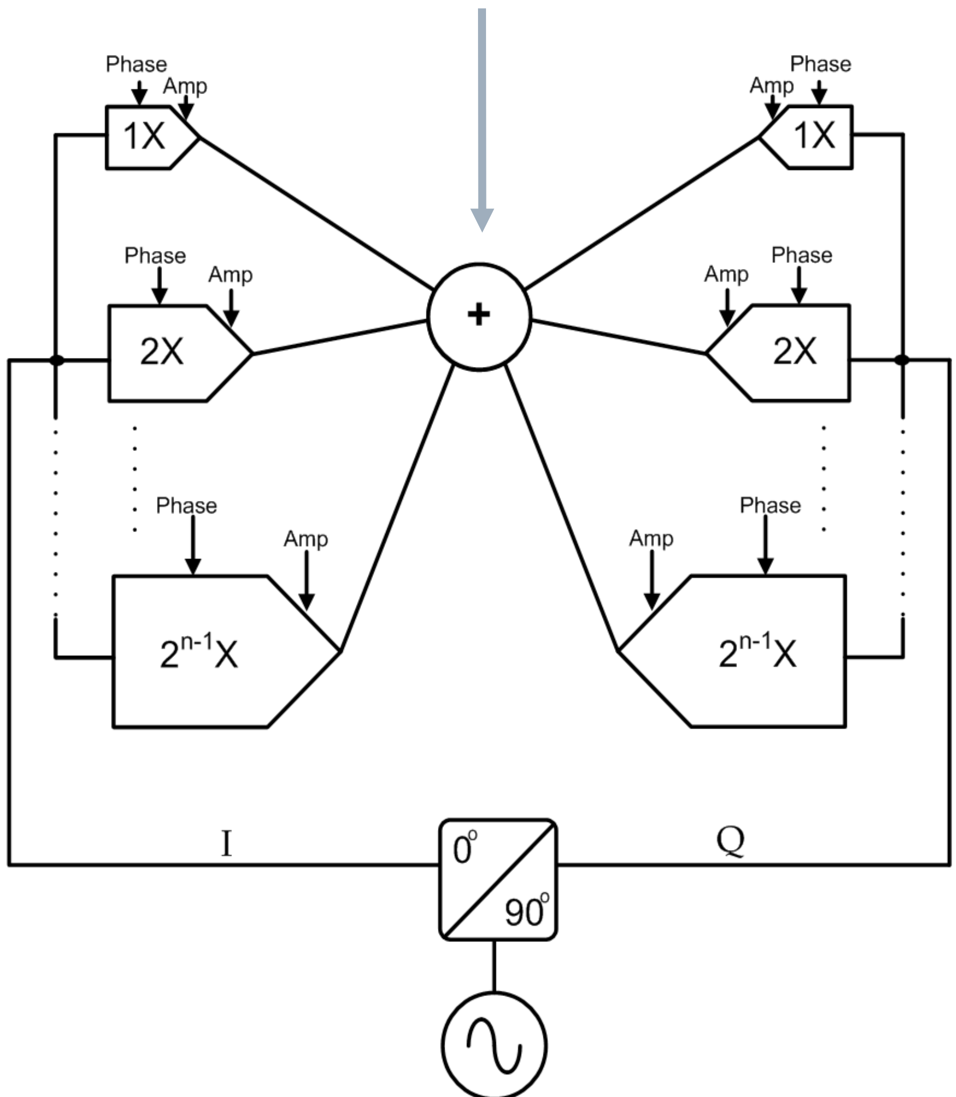
- Wireless: 256 QAM at 125 Gbaud
  - Power consumption is critical
  - Need amplitude and phase equalization in receiver

Direct Modulation TX Radio

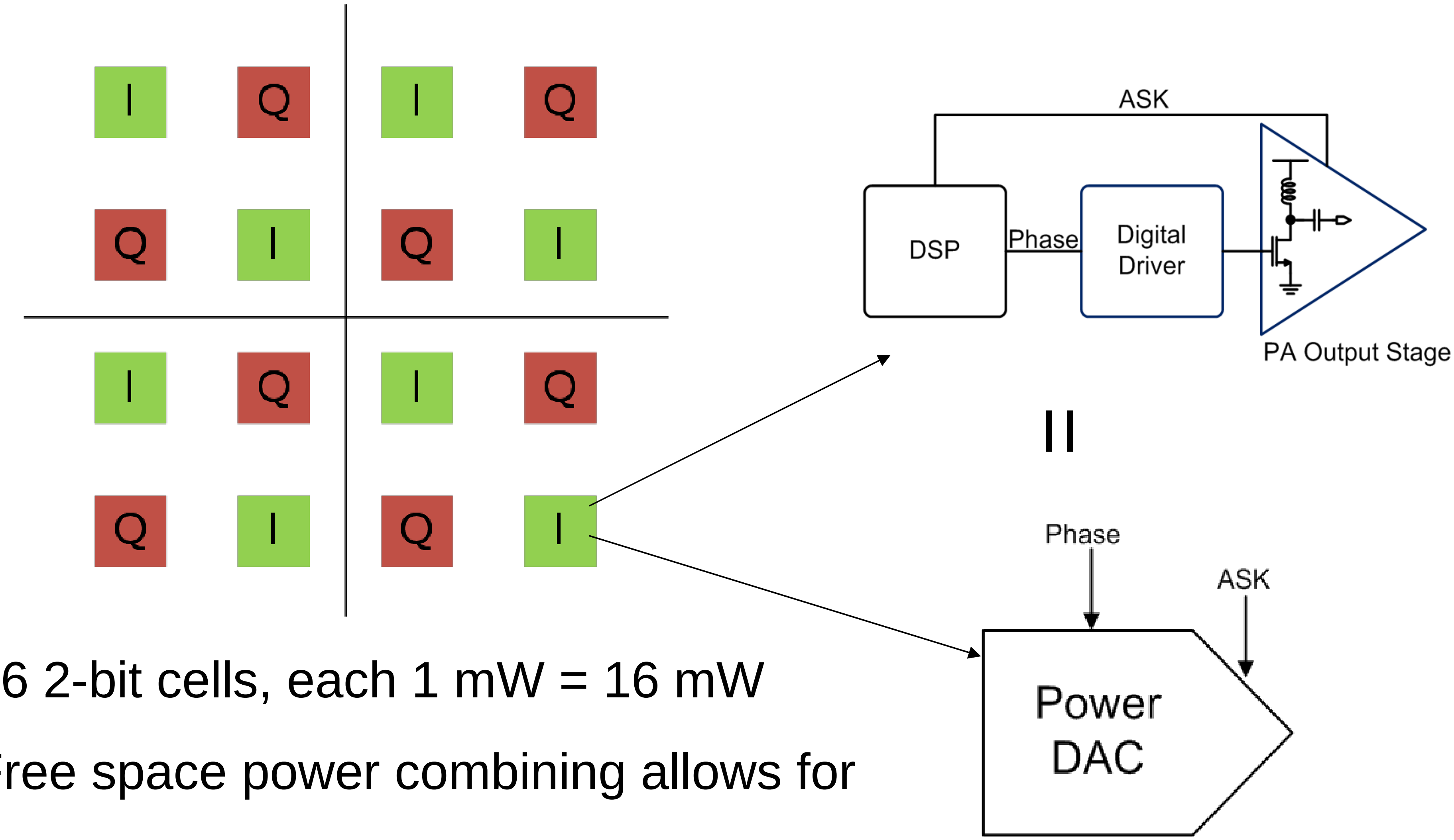
- 2-bit polar-modulated, binary weighted PA cells driven in quadrature
- No back-off needed for linearity
- Phase/Amp bits @ 1-100 Gbps

[A. Balteanu et al. IMS 2012]

•On chip free-space power combiner

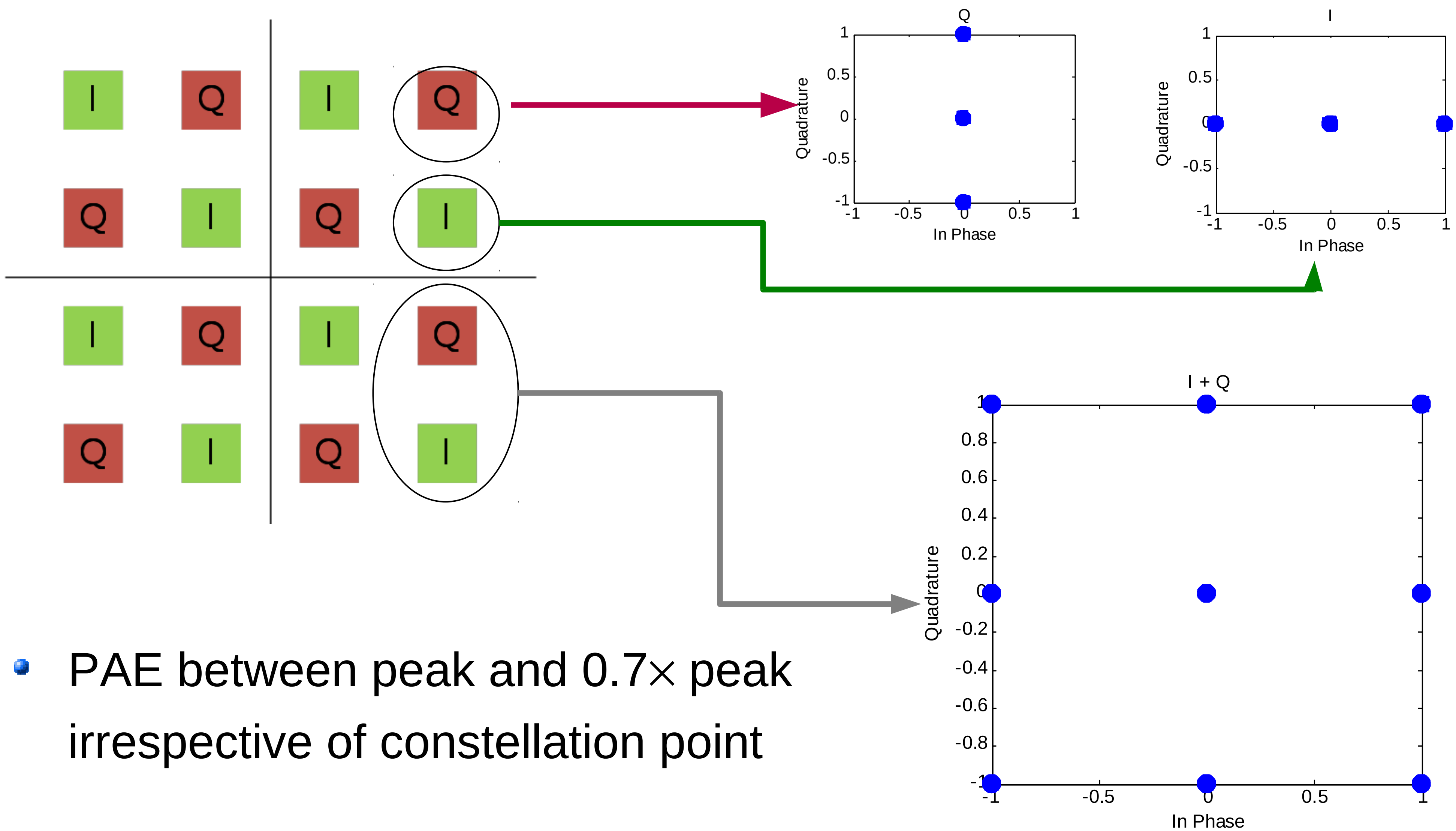


IQ DAC TX with Antenna Level Segmentation



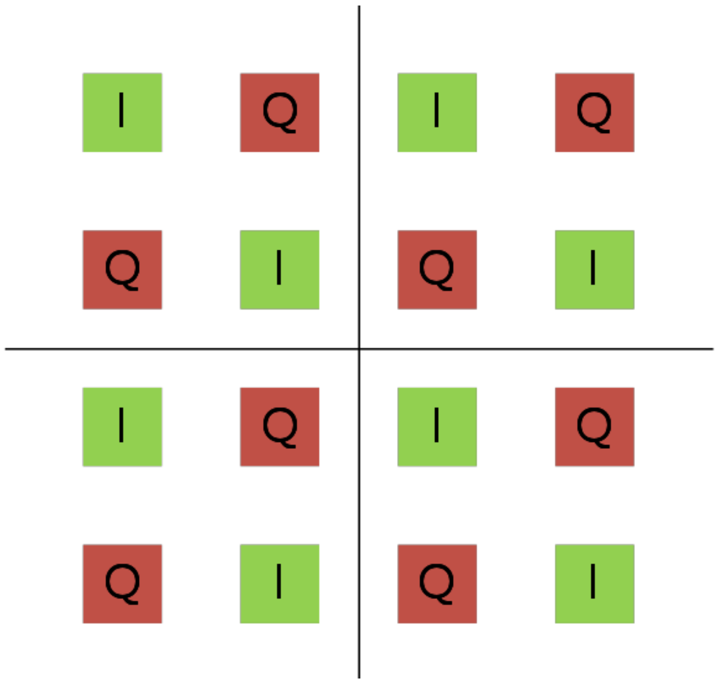
- 16 2-bit cells, each 1 mW = 16 mW
- Free space power combining allows for antenna segmentation
- Reconfigurable modulation format

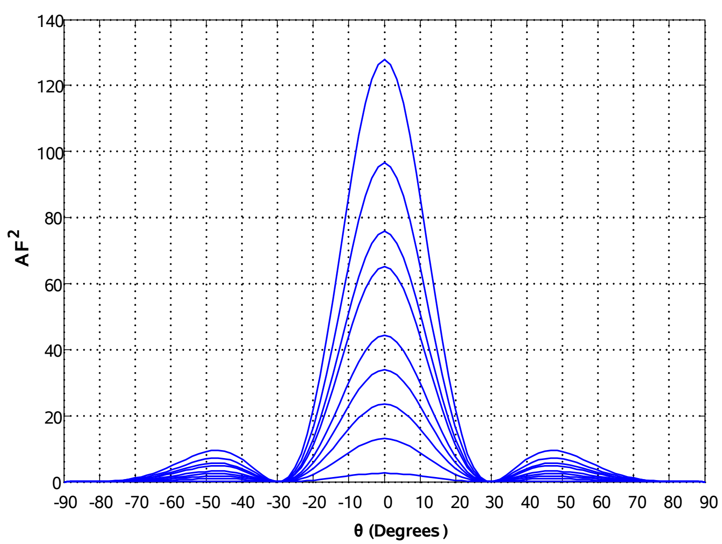
IQ DAC TX Constellation

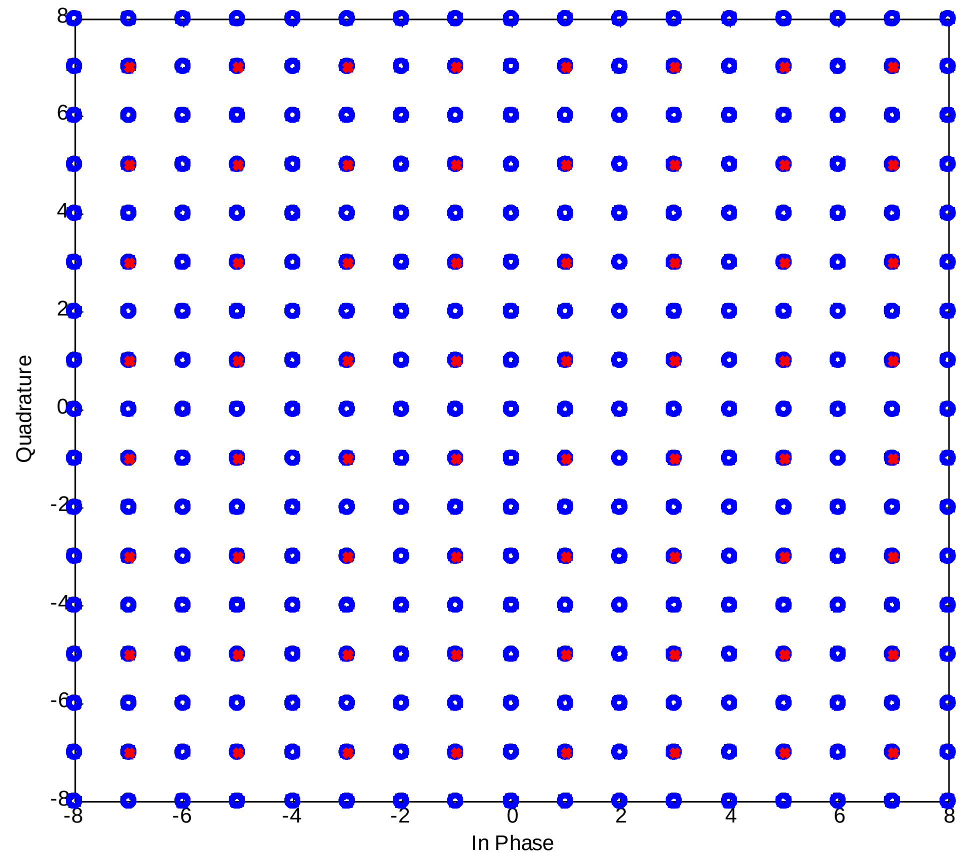


- PAE between peak and 0.7× peak irrespective of constellation point

Full 8I + 8Q Constellation







64 QAM Constellation Points

8I + 8Q -> 289 Constellation Points >2^8
2 extra bits

Wish list for sub-millimetre wave radio

- 100 Gb/s standard CMOS baseband lanes
  - Efficiency scalable with data rate
- P_{TX} = 10 dBm
- PLL with PN < -90 dBc/Hz in band at 300 GHz
- NF < 12 dB
- P_{DC} < 1W
- BW = 25-30%
- Antenna gain > 20 dB (lens)
- Distance: 10’s cm

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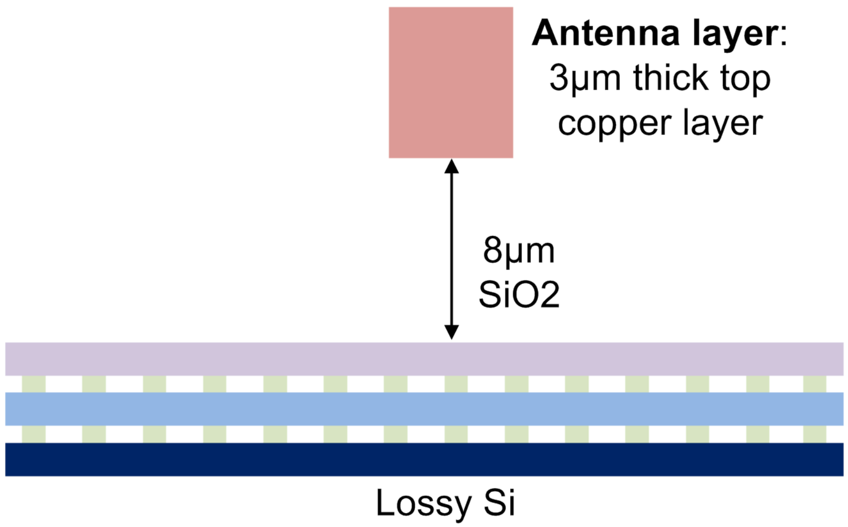
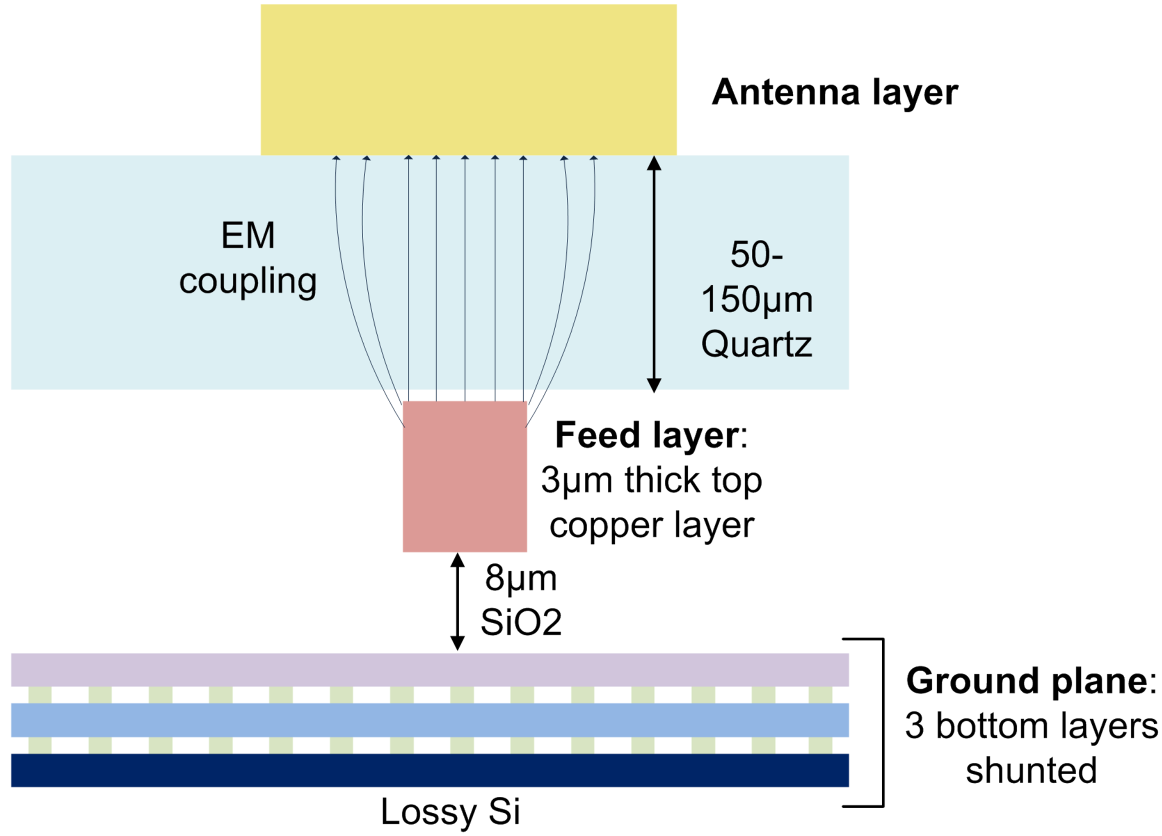
Antenna Integration

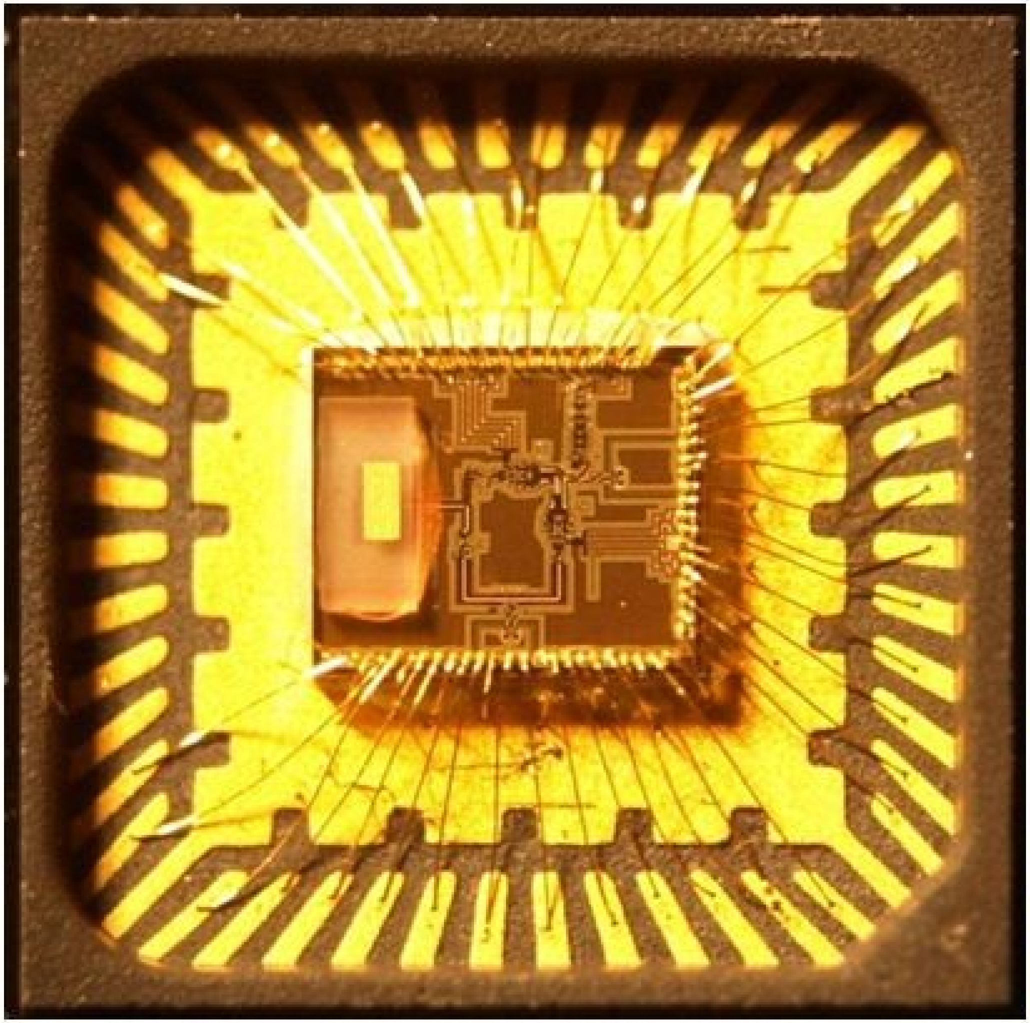


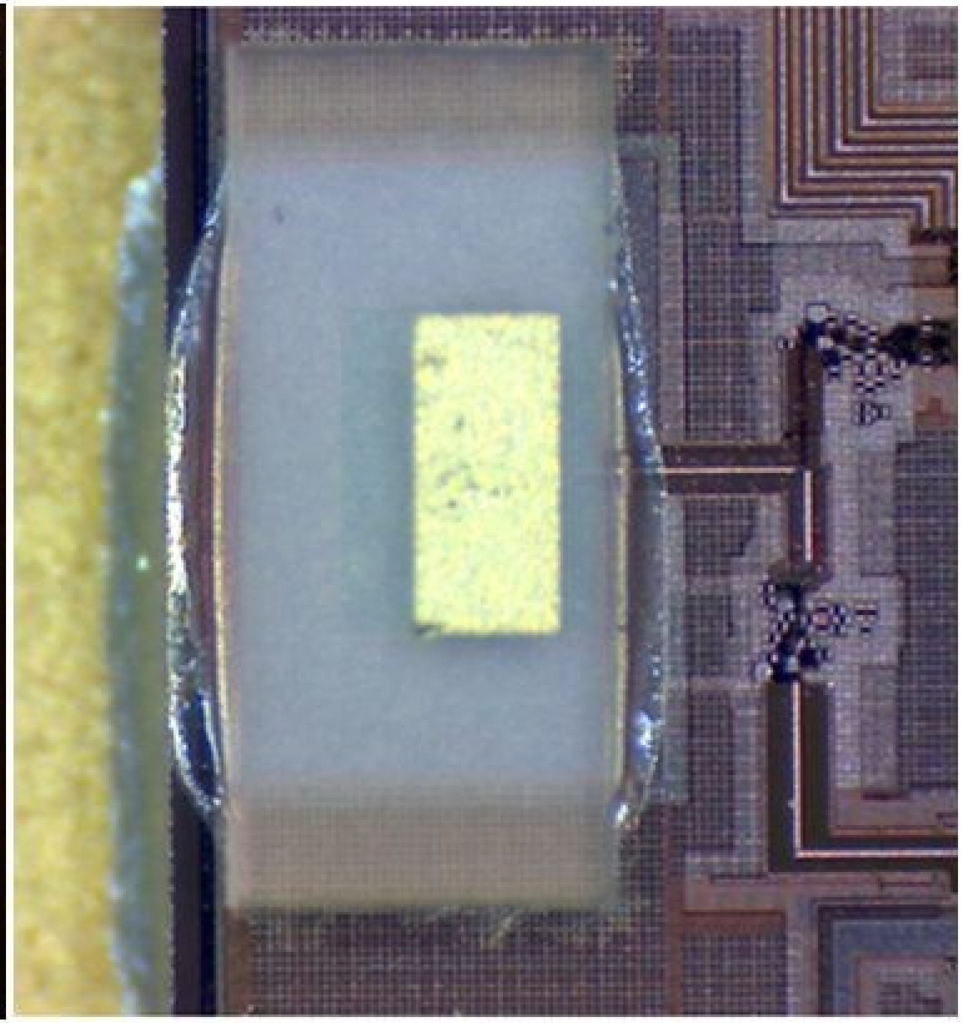
On-chip



Above IC
[J. Hasch et al, March 2010]

120/160 GHz Transceiver Packaging



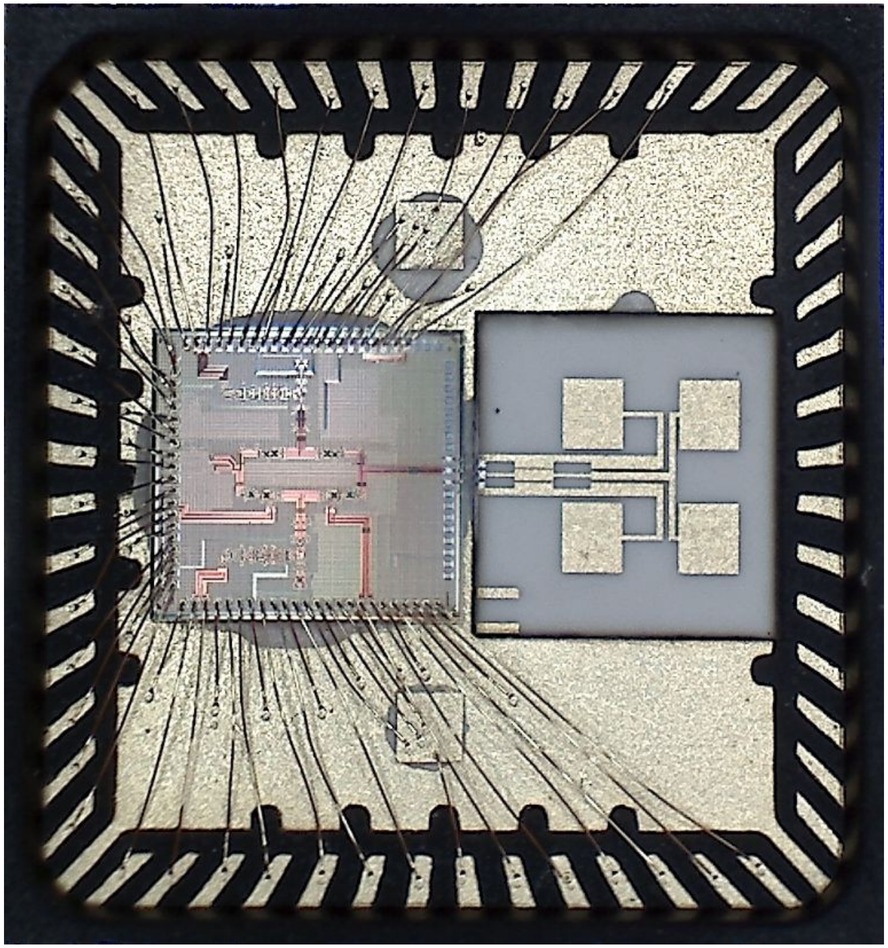


Chip: 2.2mm×2.6mm

Package: 7mm×7mm

[I. Sarkas Trans MTT, March 2012]

142-152 GHz Antenna and die in QFN package



Package: 7mm×7mm

EU SUCCESS Project

- Antenna design by Stefan Beer, Karlsruhe Institute of Technology
- Packaging by Robert Bosch GmbH
- Fundamental frequency transceiver with self-test

[I. Sarkas CSICS 2012]

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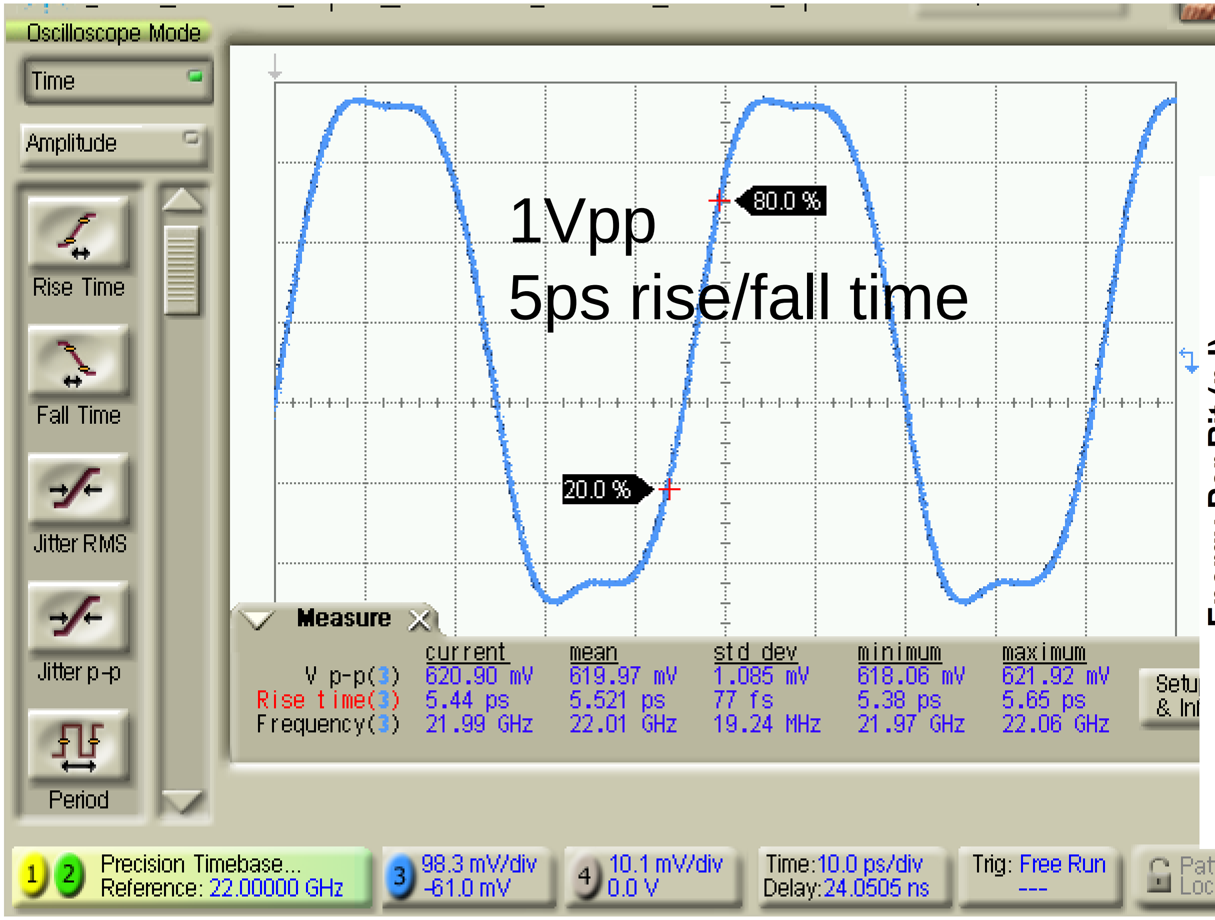
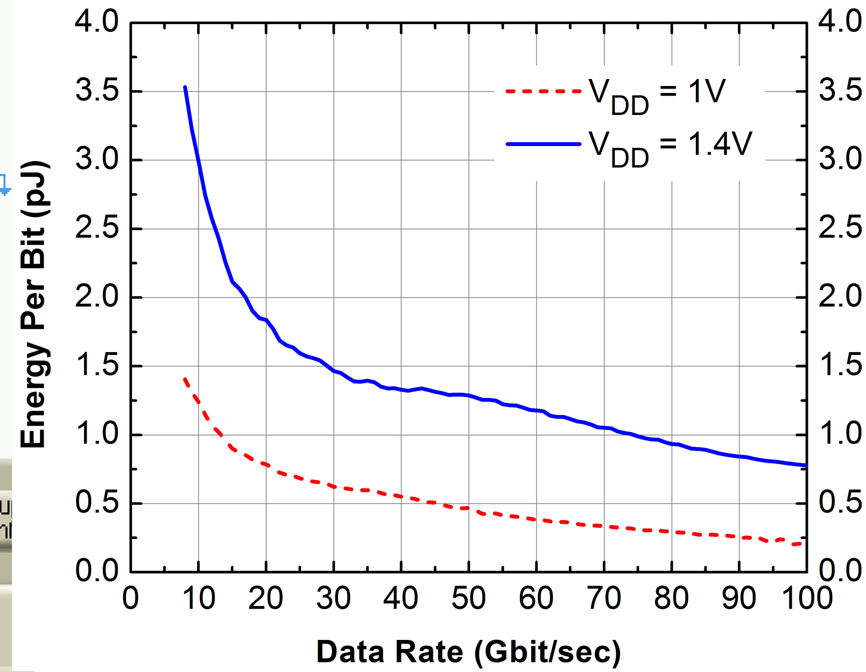
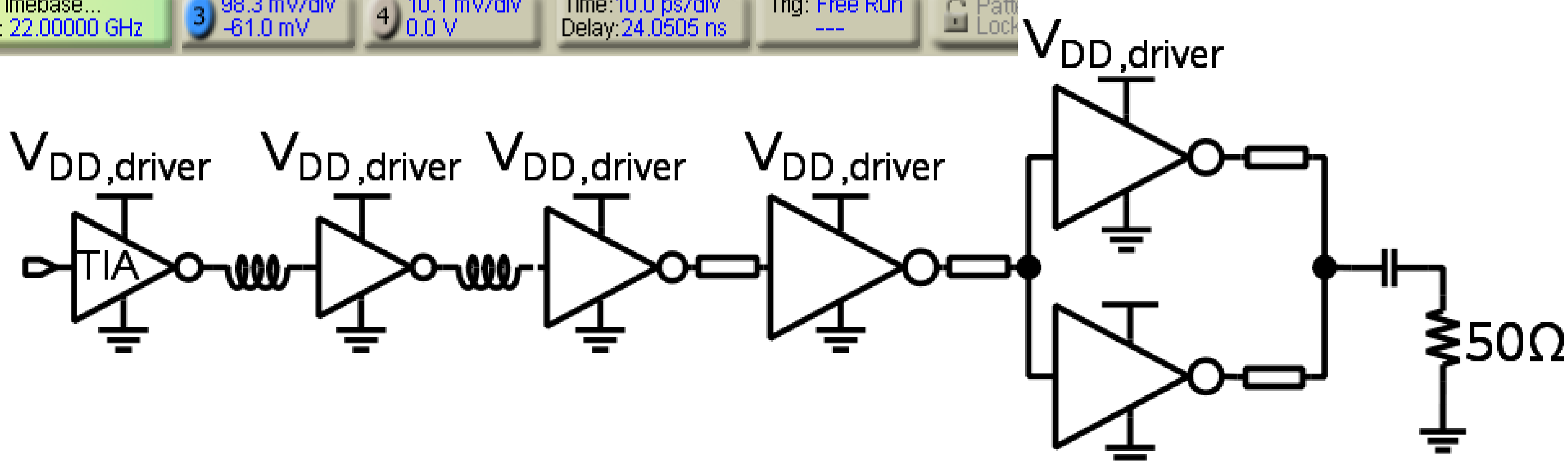
Rise/fall time, efficiency/bit in 45-nm SOI

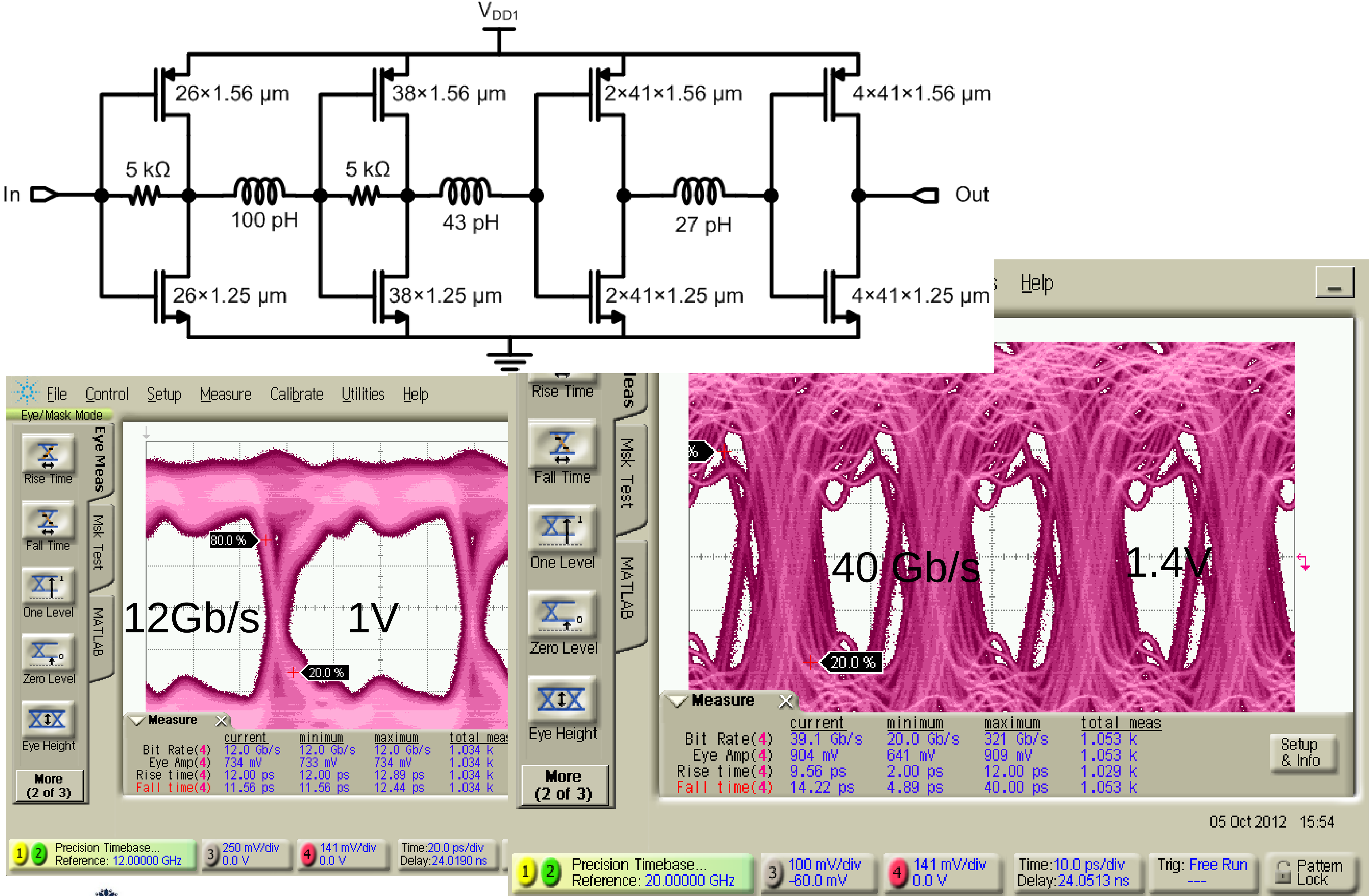


[I. Sarkas, ISSCC 2012]



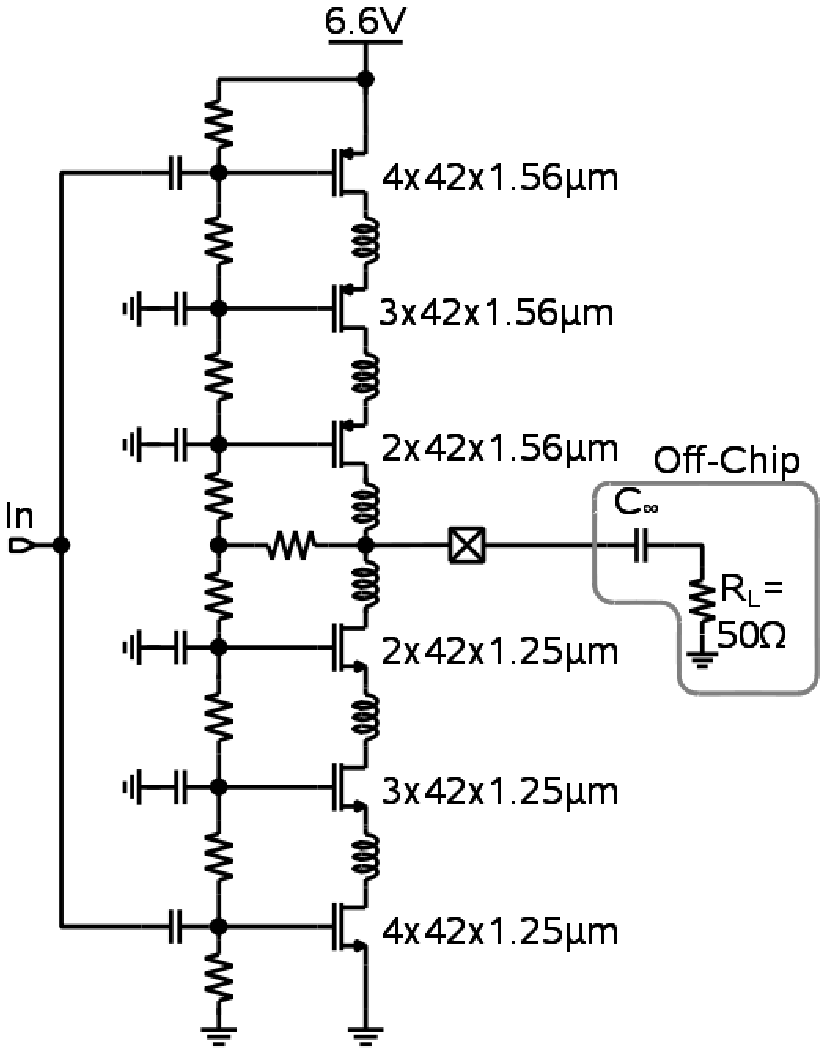


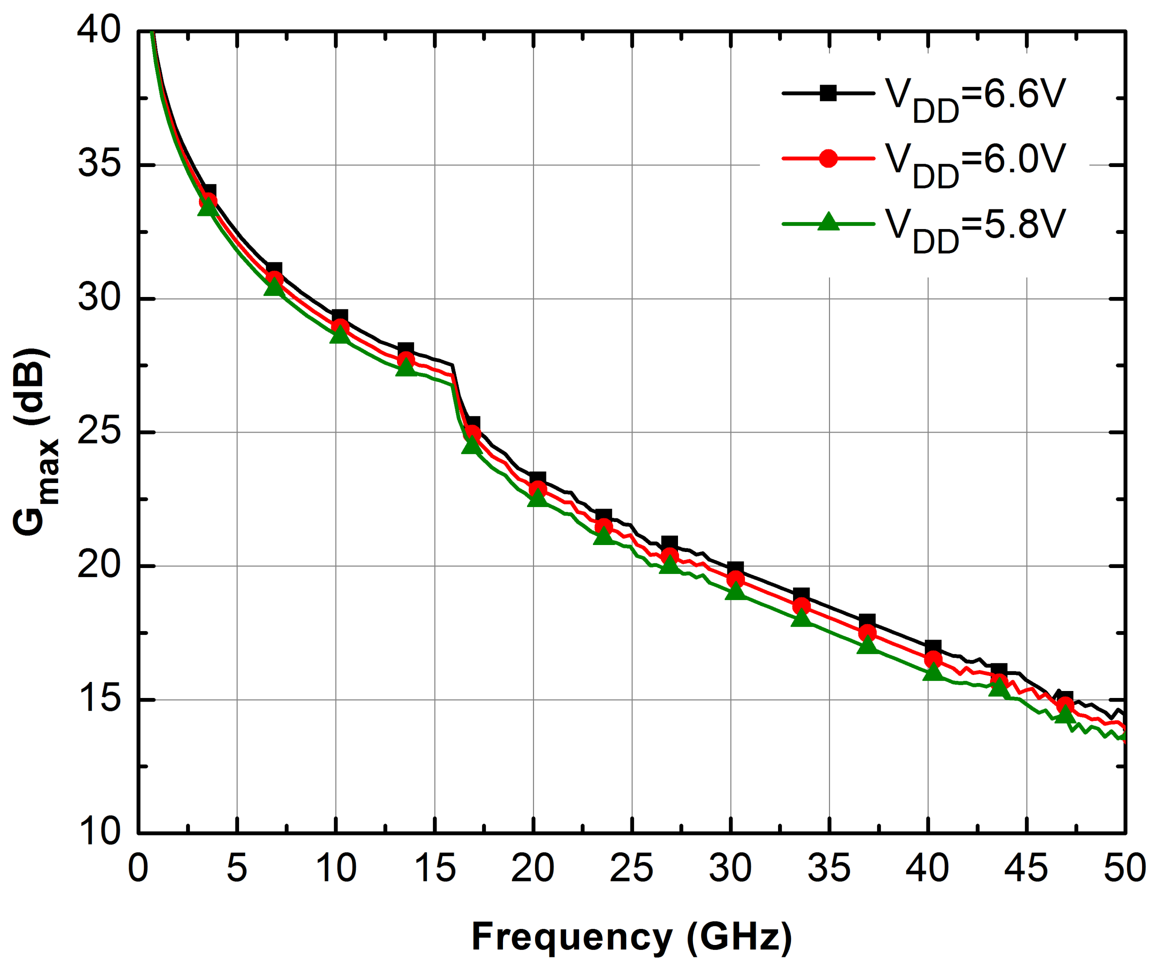
40+ Gb/s inductively-peaked CMOS logic



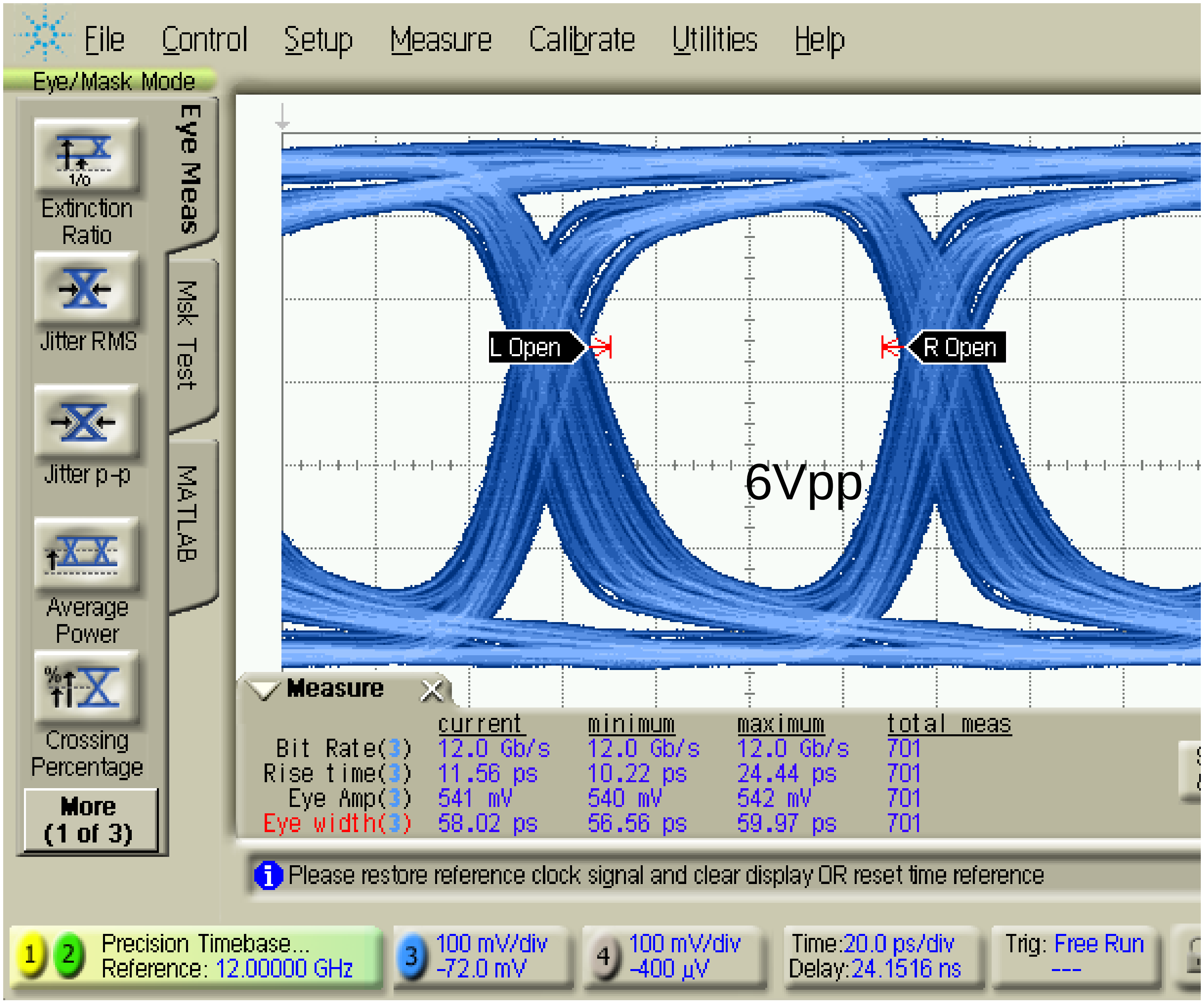
Broadband, large swing stacked CMOS LOGIC

[I. Sarkas, ISSCC 2012]





Eye diagrams at 12 Gb/s



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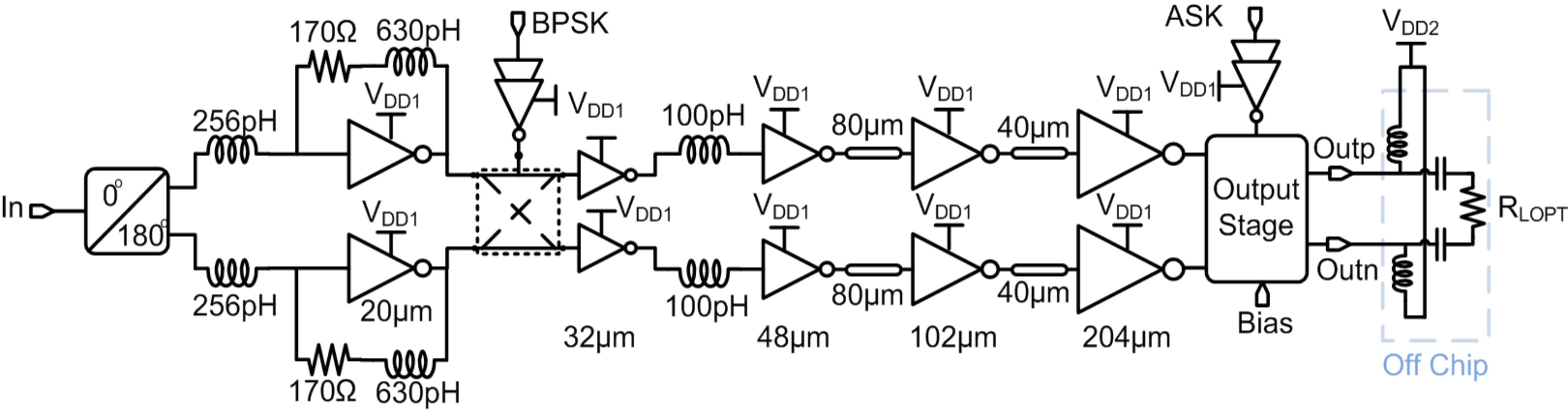
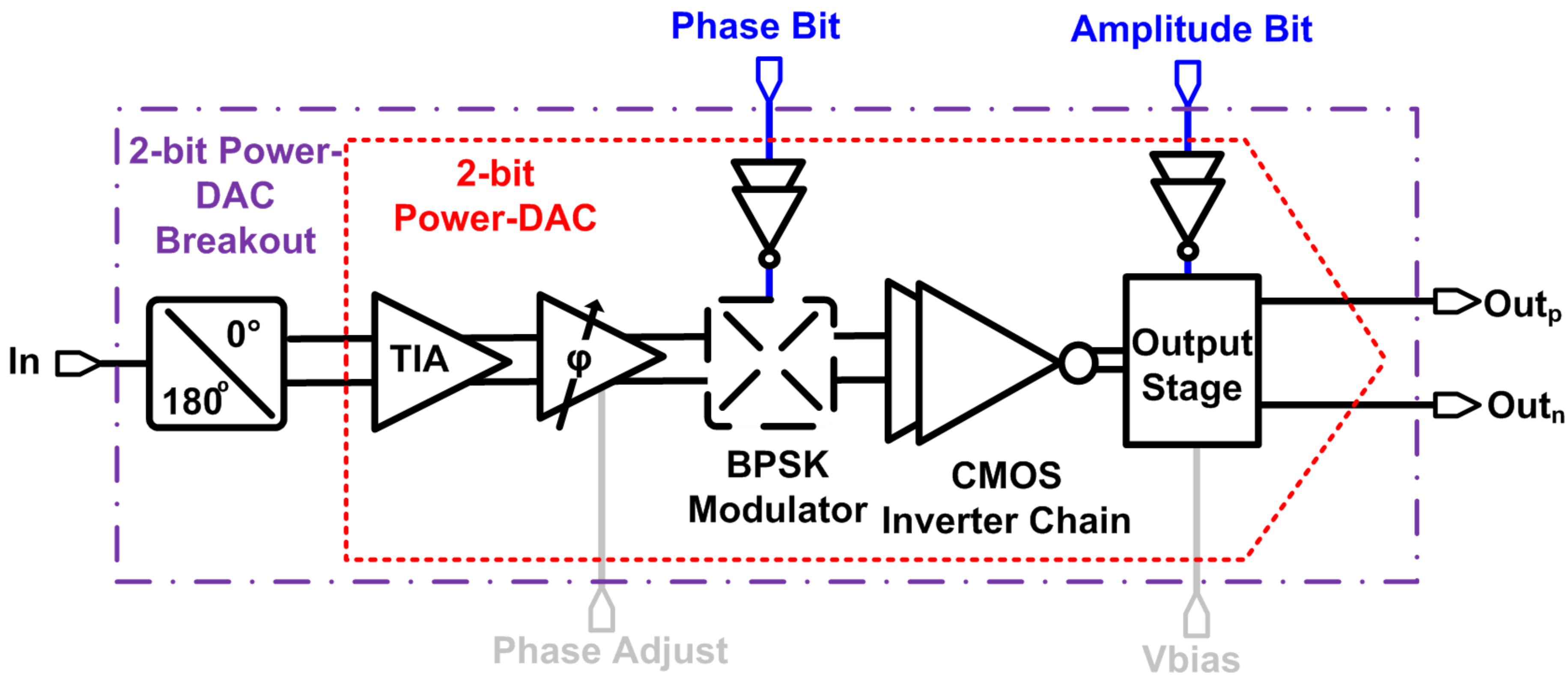
1.5-bit DAC Cell with stacked-CMOS inv.



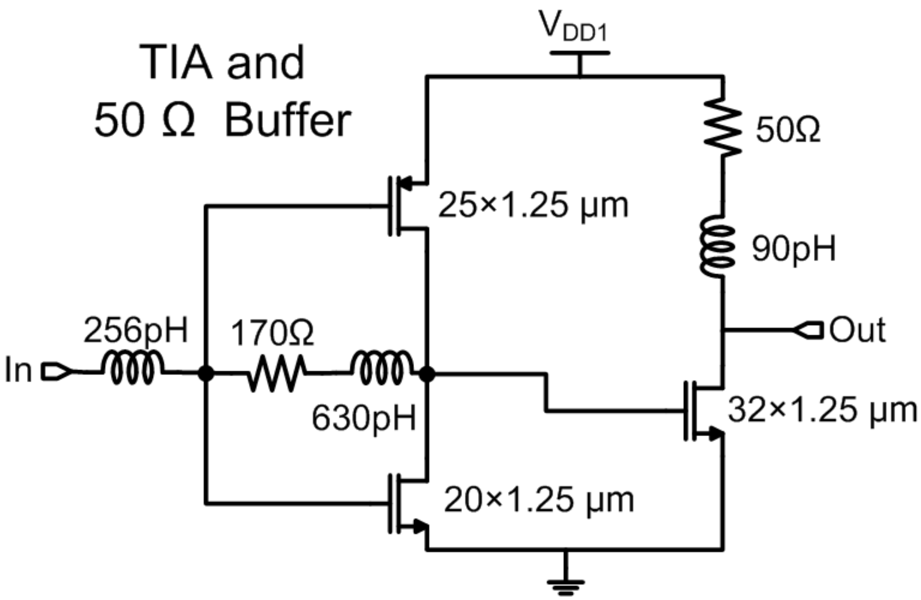
- Input balun for single ended to differential conversion
  - the only tuned component in chain
  - needed for testing
- Input CMOS TIAs for broadband matching
- CMOS Inverter based class-D driver chain

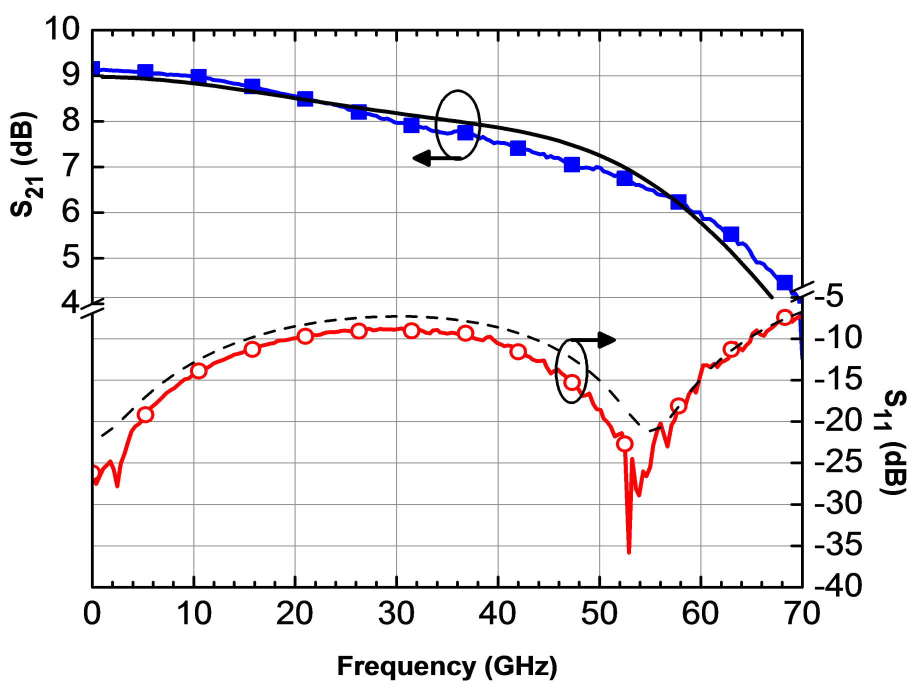
Power-DAC Cell with N-MOS output stage

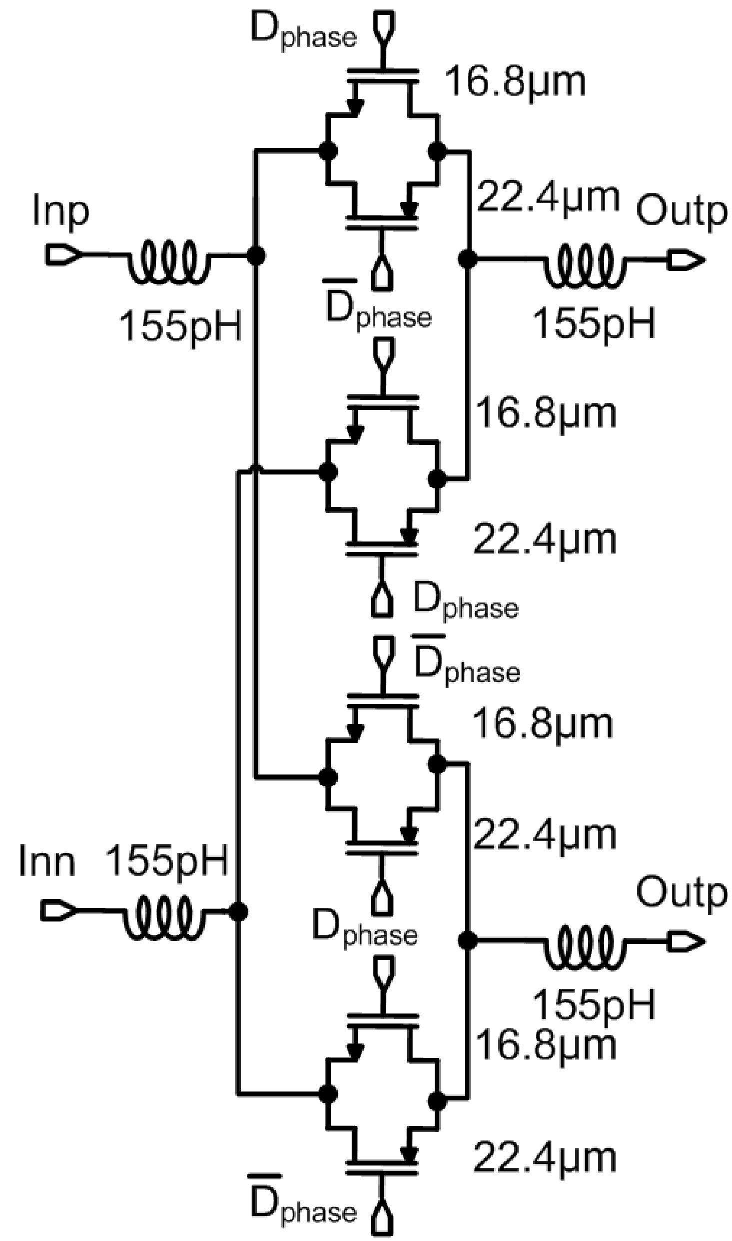


- DC – 50 GHz in 45-nm SOI
- CMOS inverter based. Purely digital
- Scalable to 240 GHz using tuned LO path

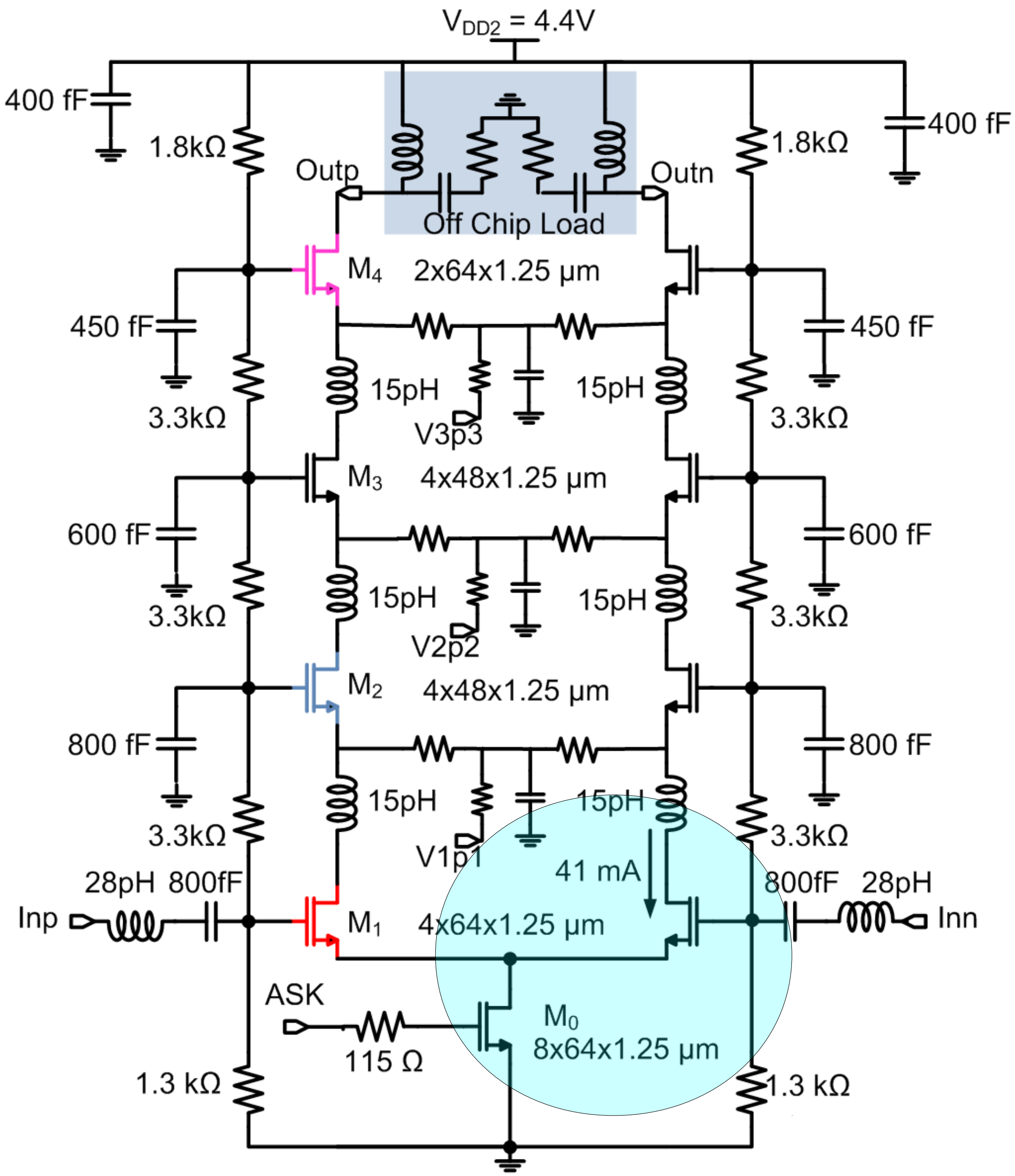
TIA, BPSK Modulator

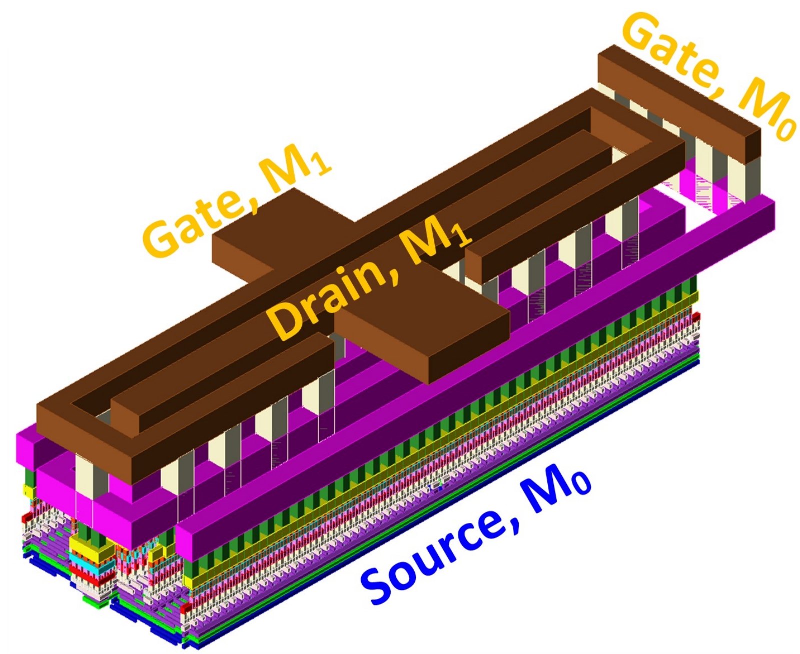




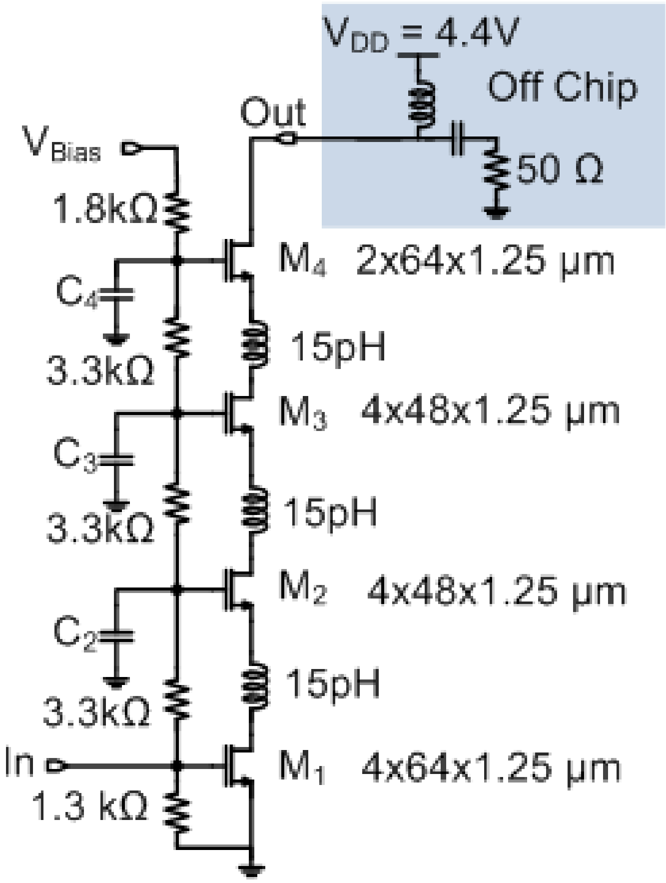


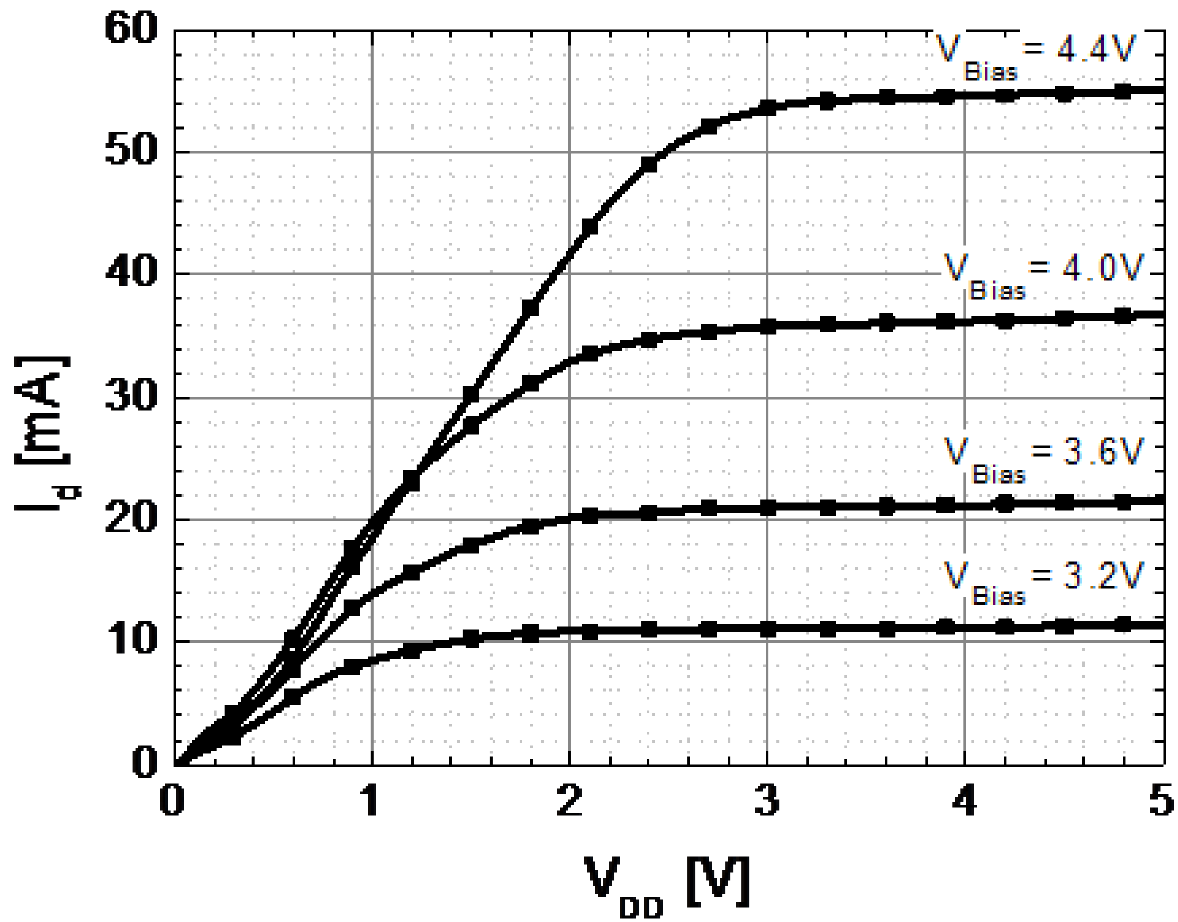
Differential output stage with On-Off switch



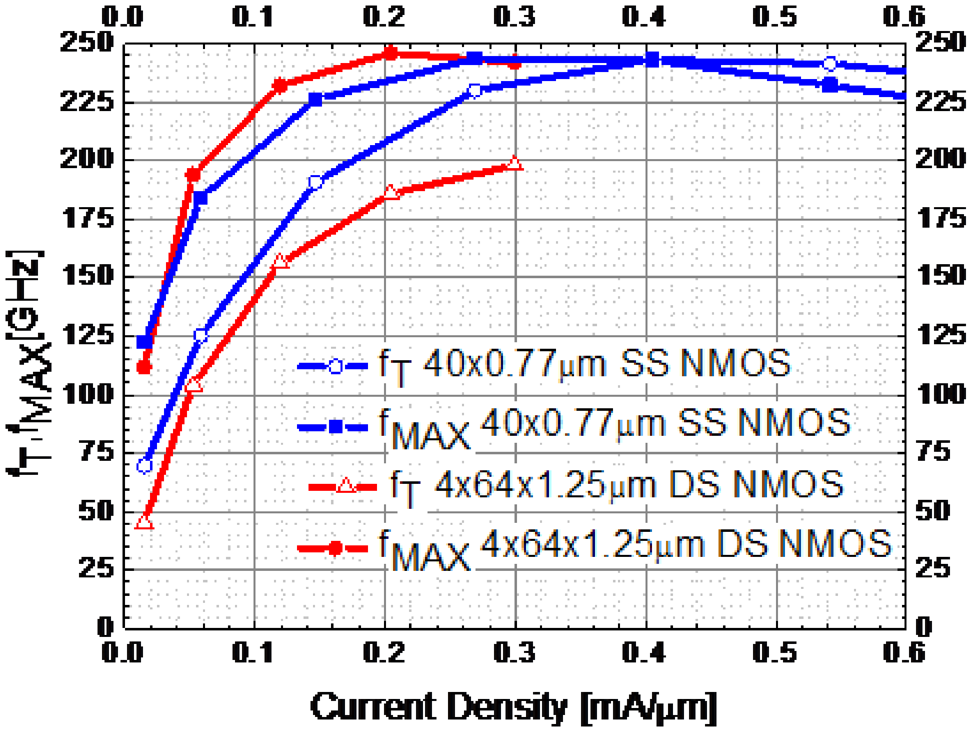


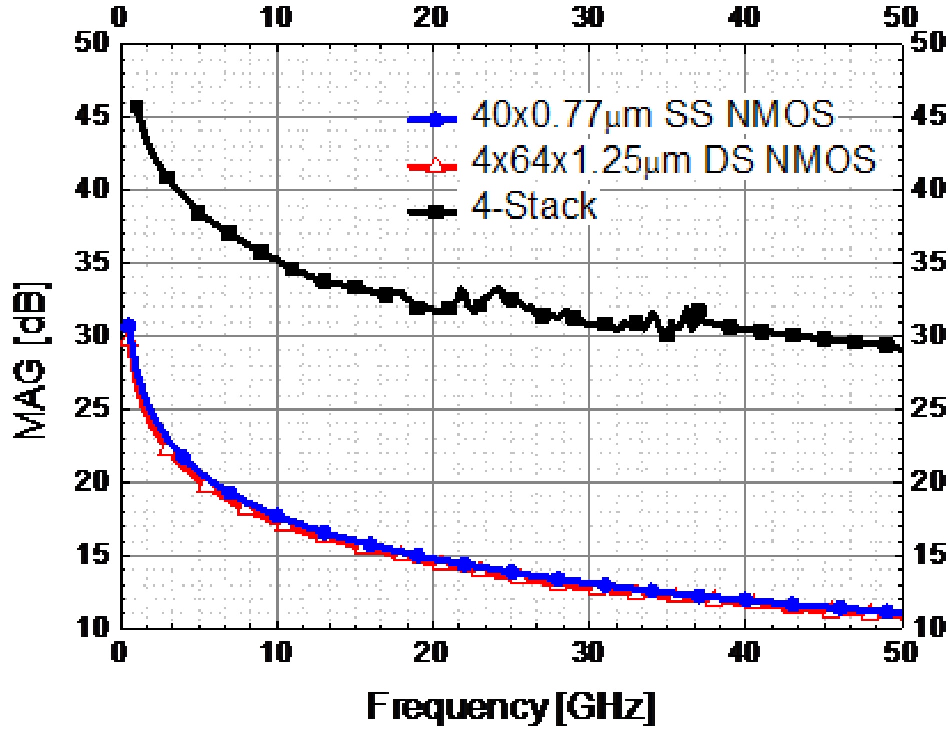
4-Stacked n-MOS Cascode



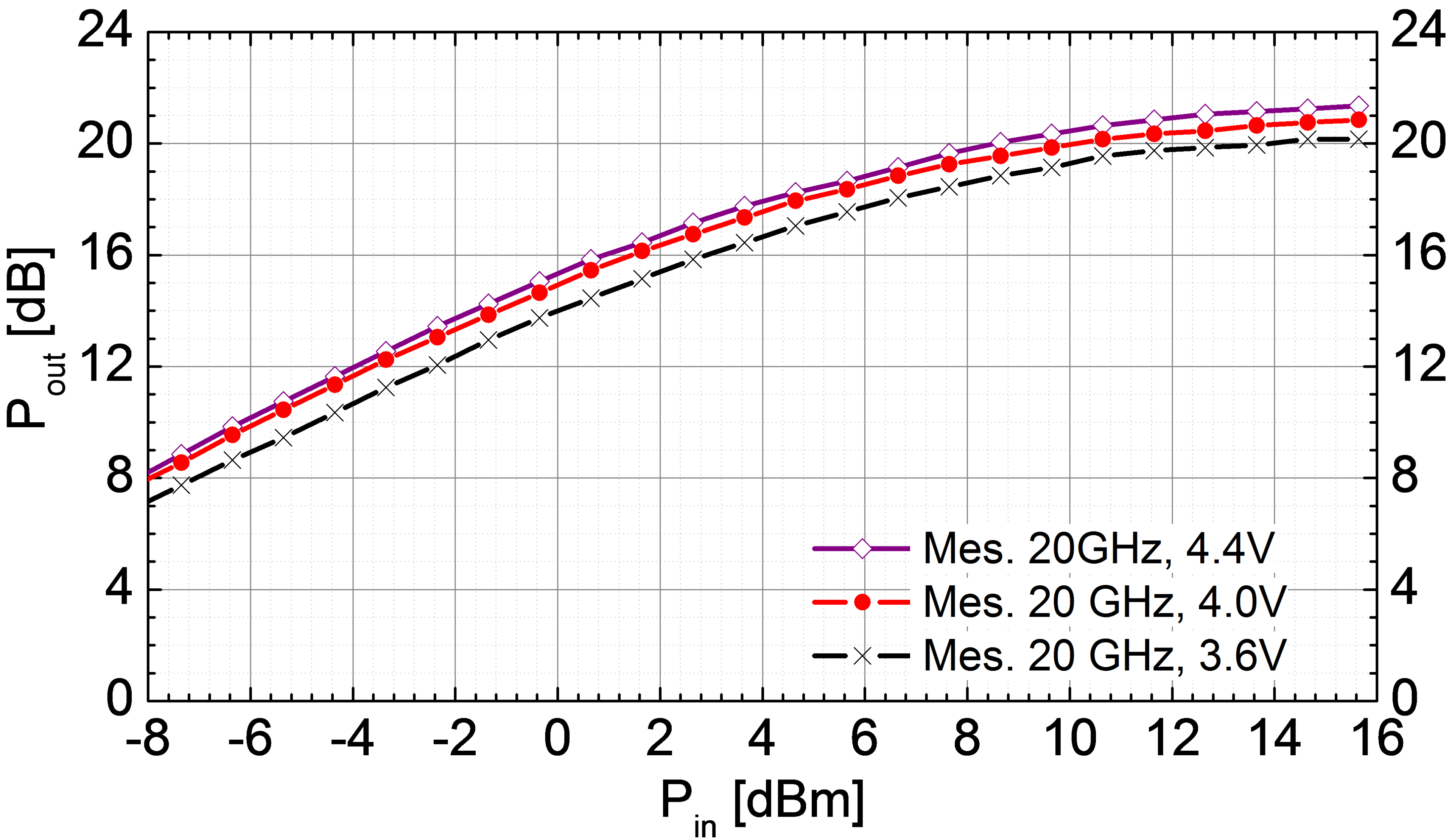


4-Stacked n-MOS Cascode (ii)

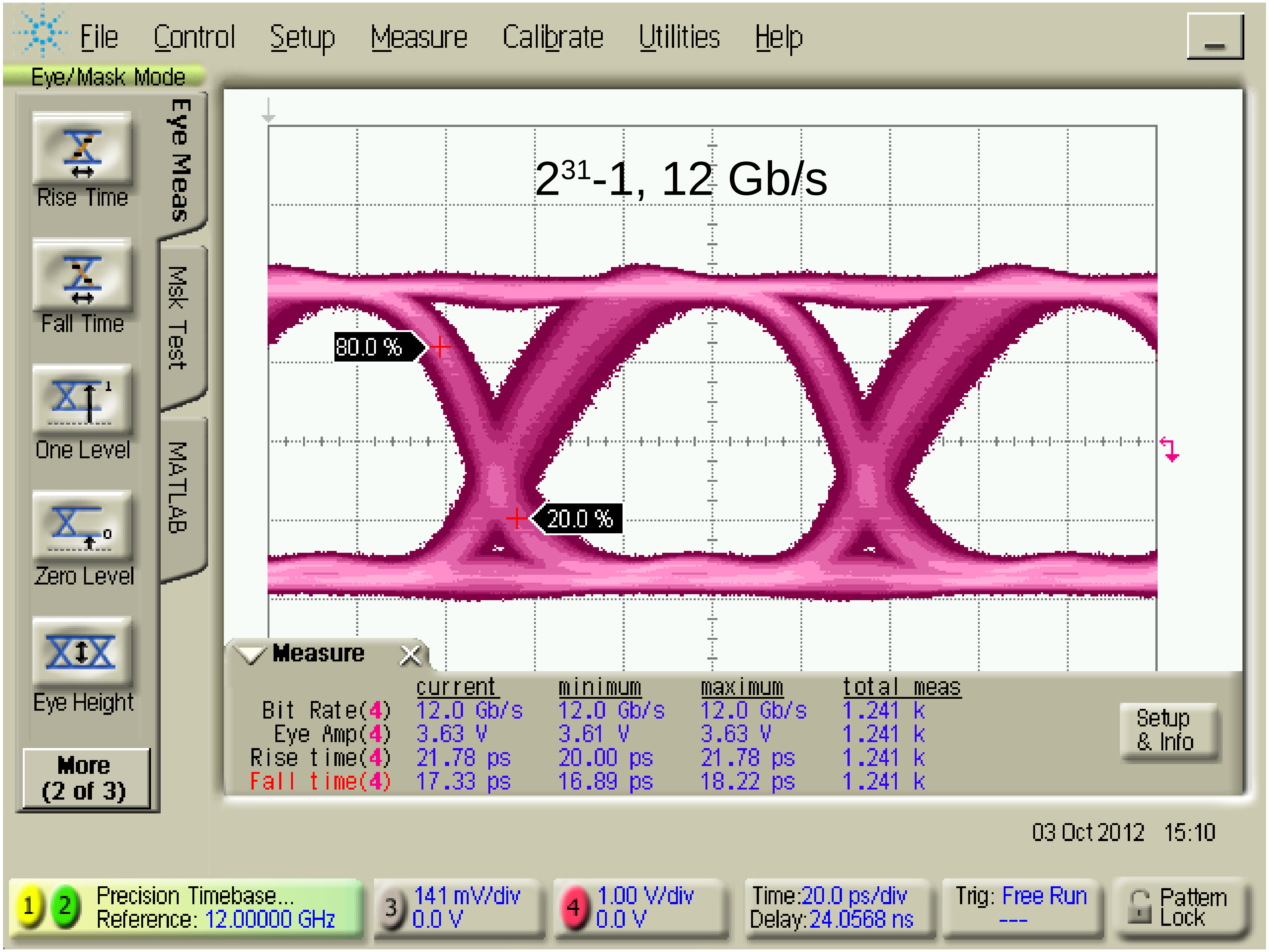




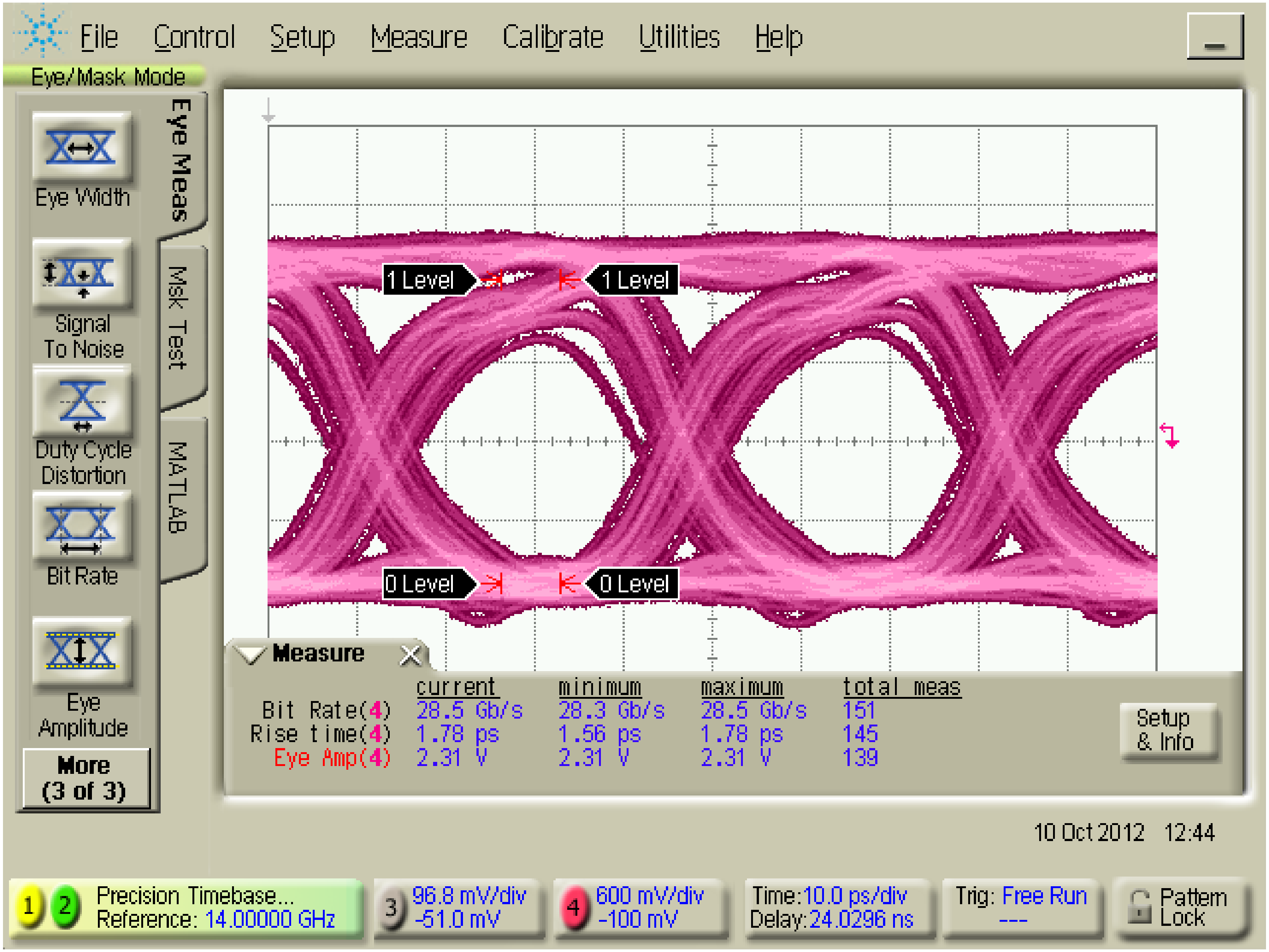
4-Stacked n-MOS Cascode (iii)



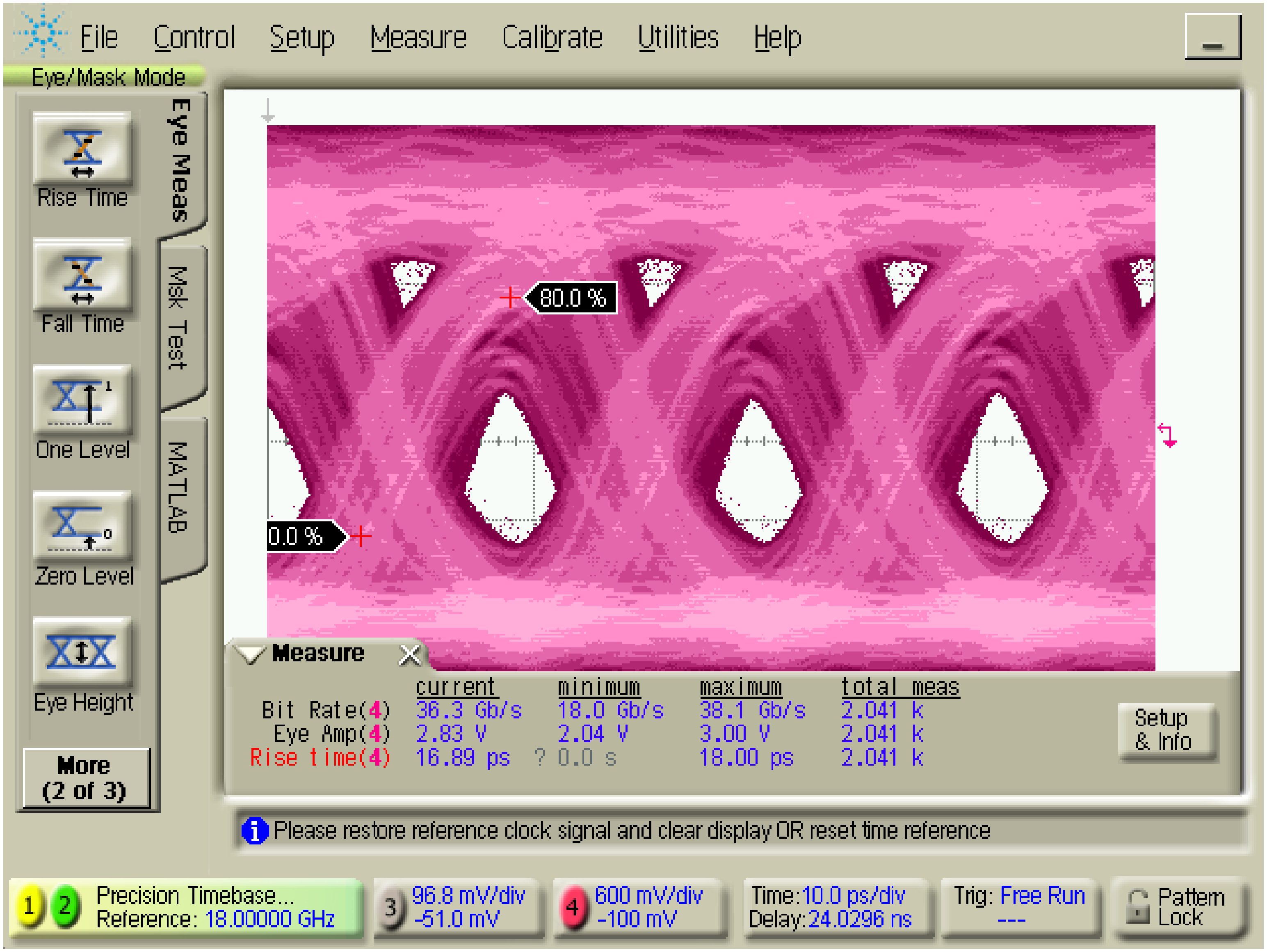
4-Stacked n-MOS Cascode (iv)



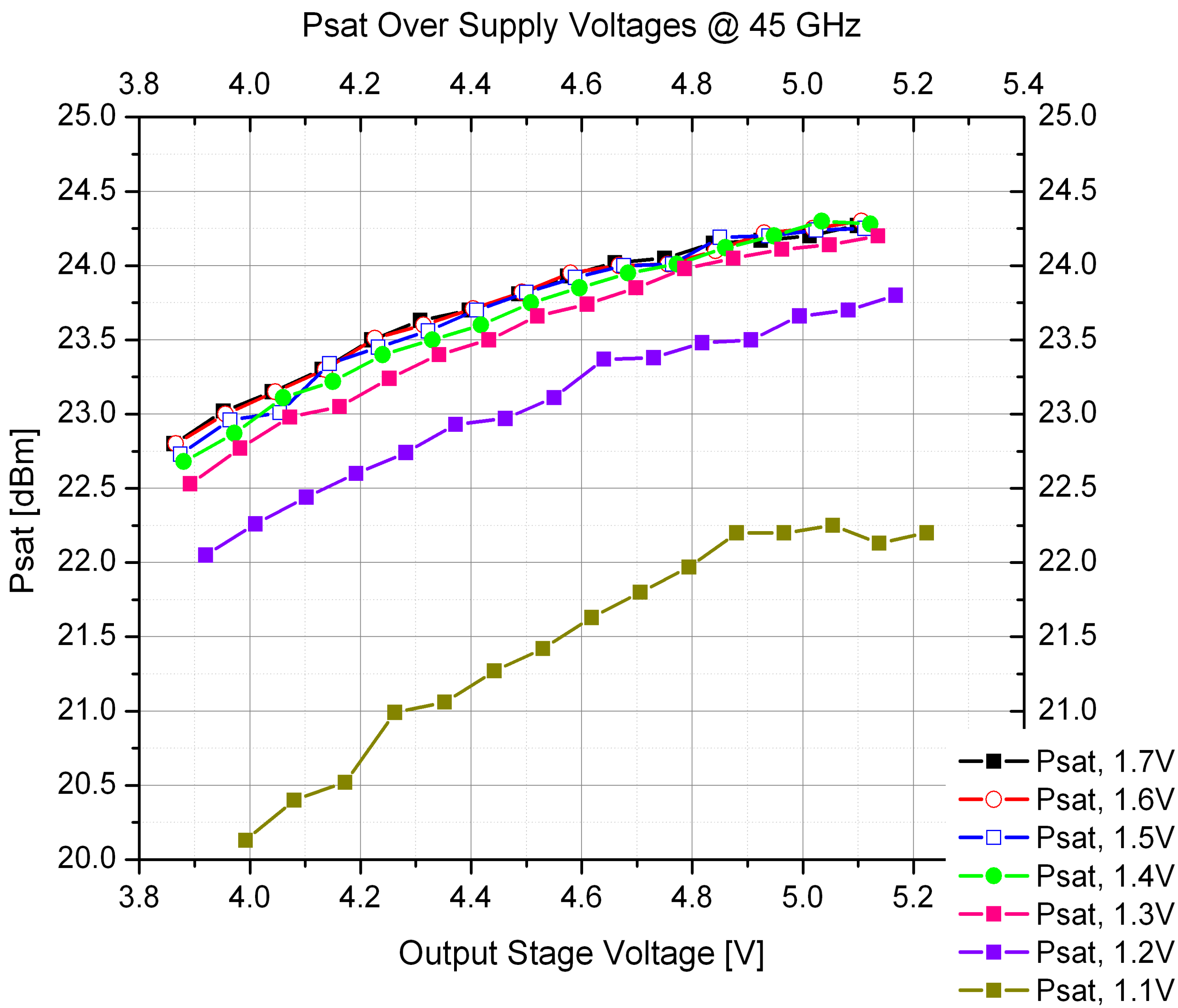
DAC Cell: 28 Gb/s Eyes



DAC Cell: 36 Gb/s Eyes



45-GHz IQ DAC Cell: Eyes, P_{SAT}



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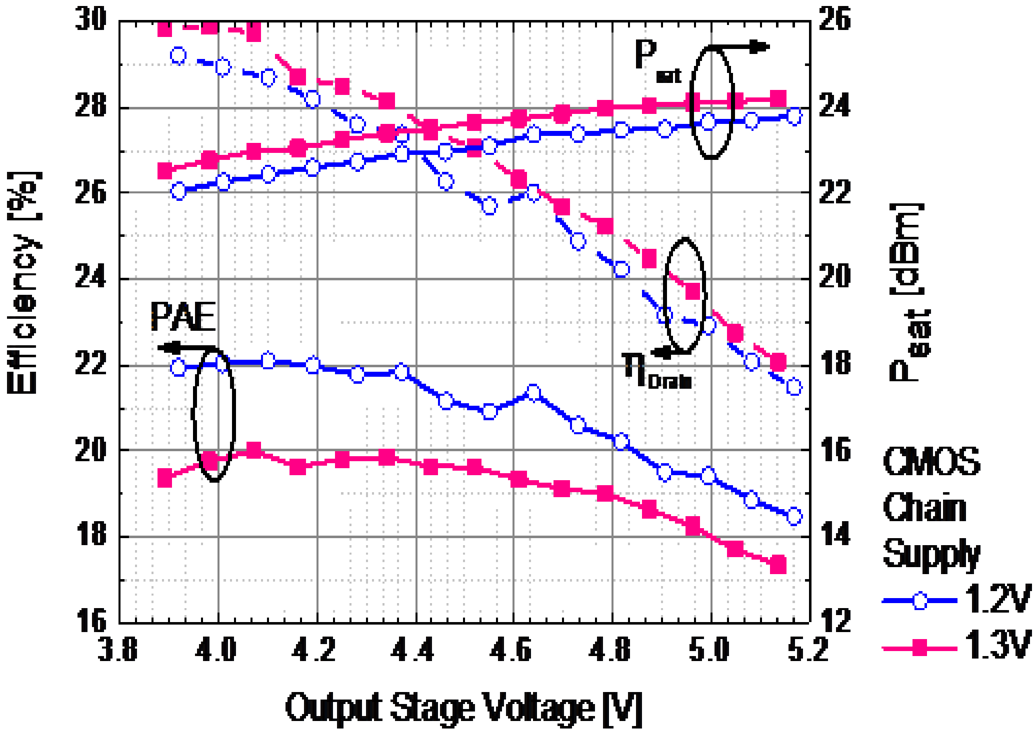
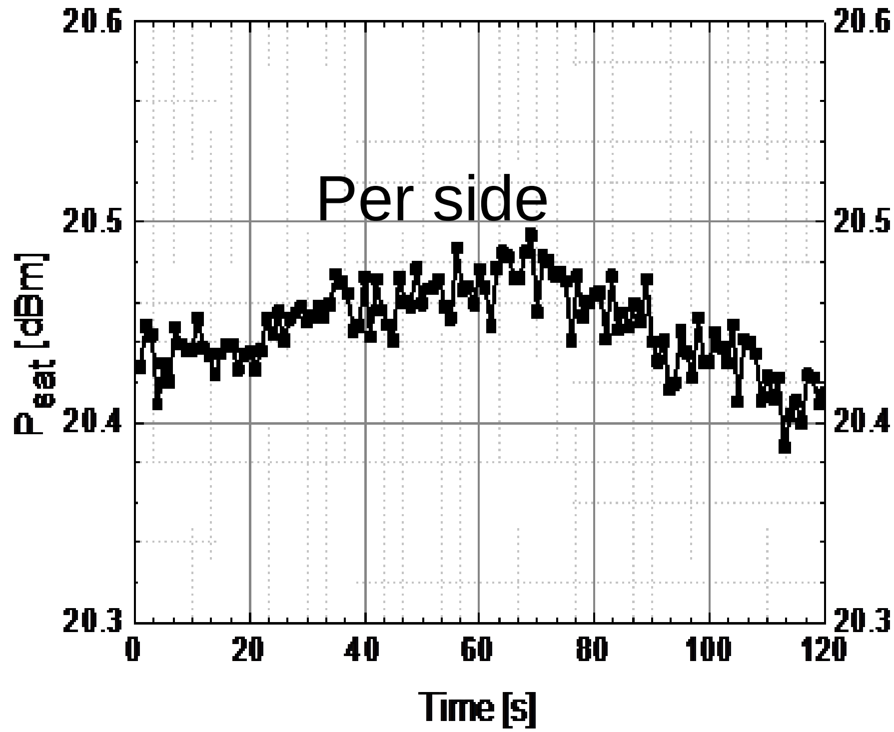
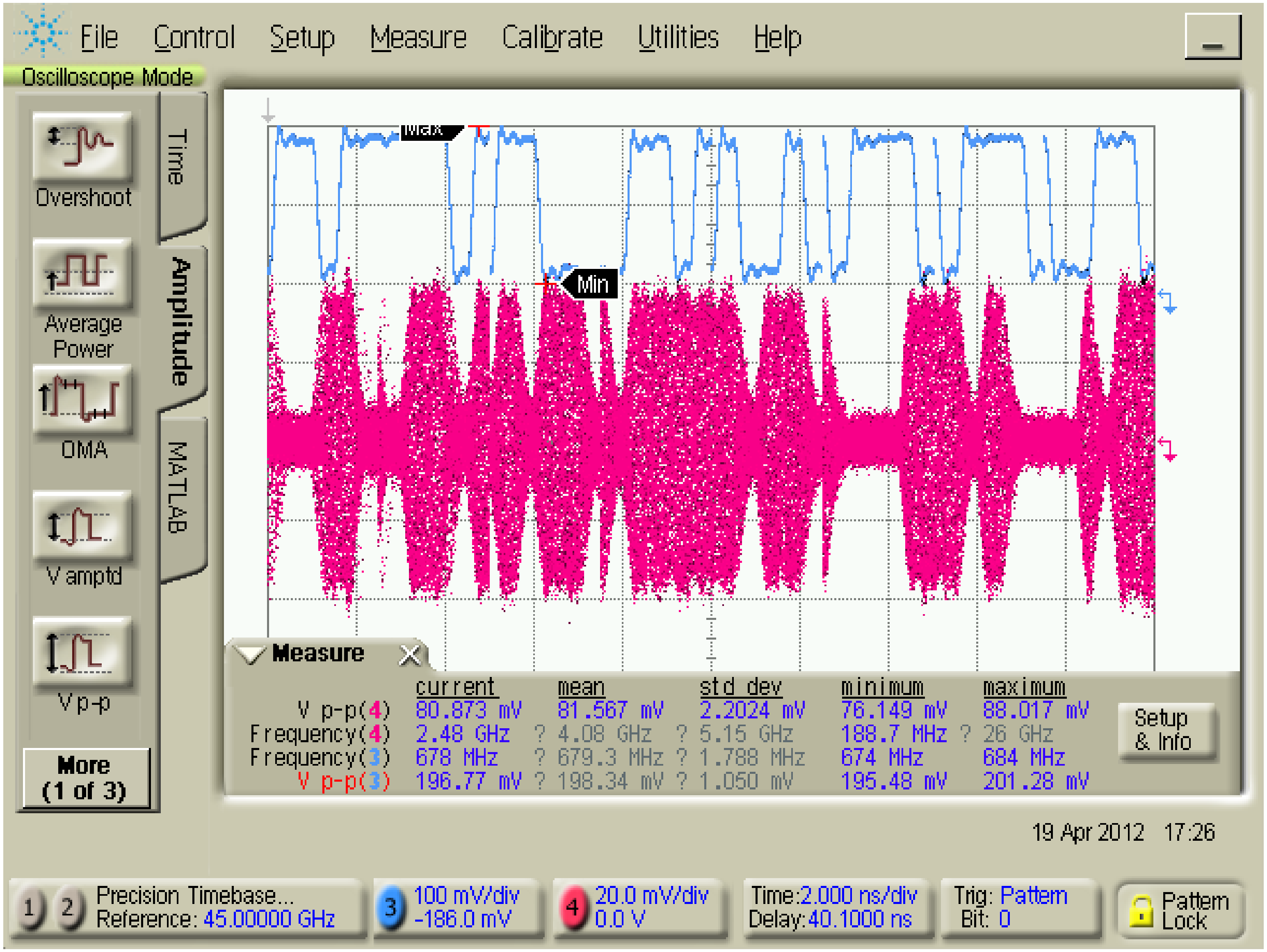
Pout of 45-GHz DAC cell vs. time



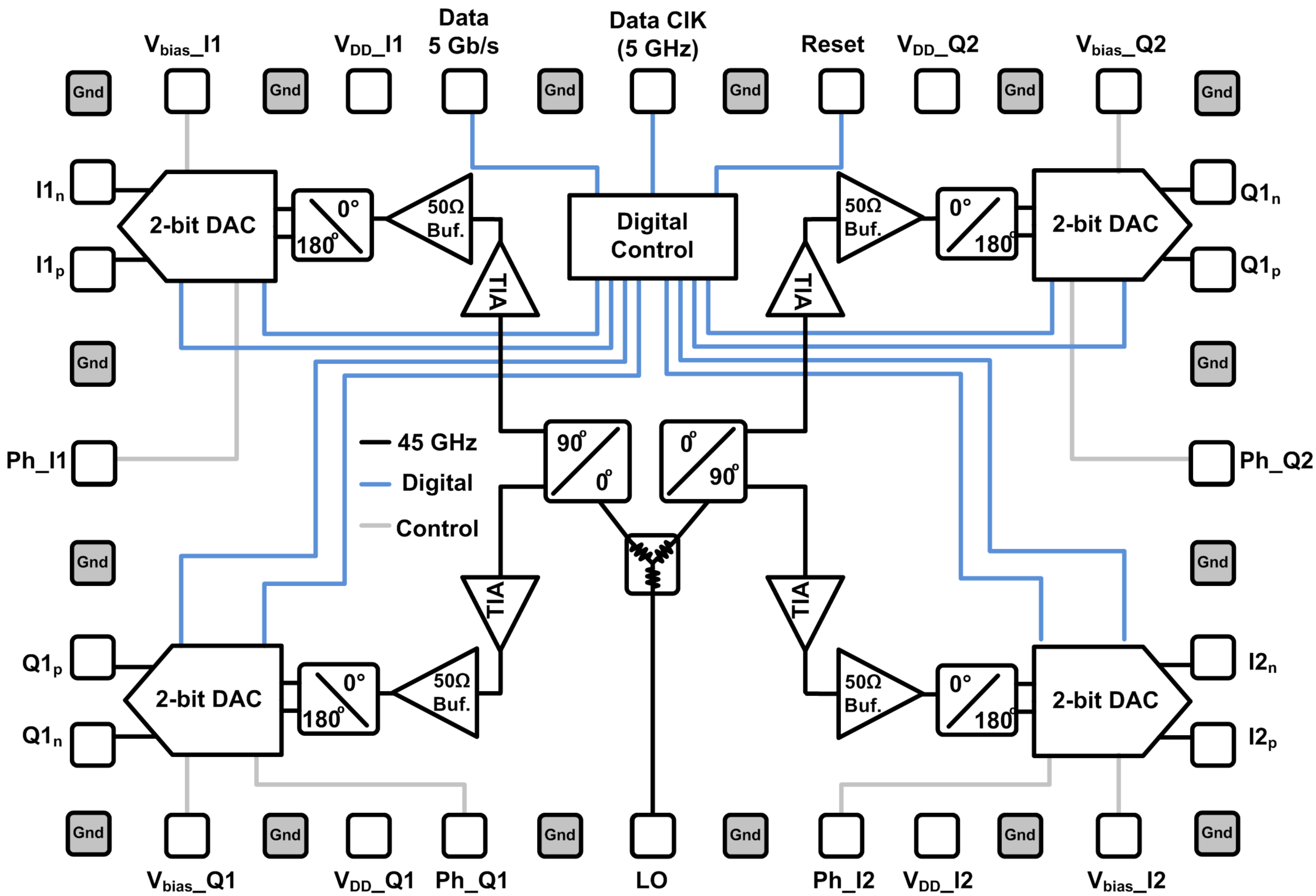


- P_{sat} =23 dBm, η_{Drain}=30%, PAE=20%, 4.1V/1.3V
- P_{sat} =24.3 dBm, η_{Drain} =22%, PAE=16.3%. 5.1V/1.4V

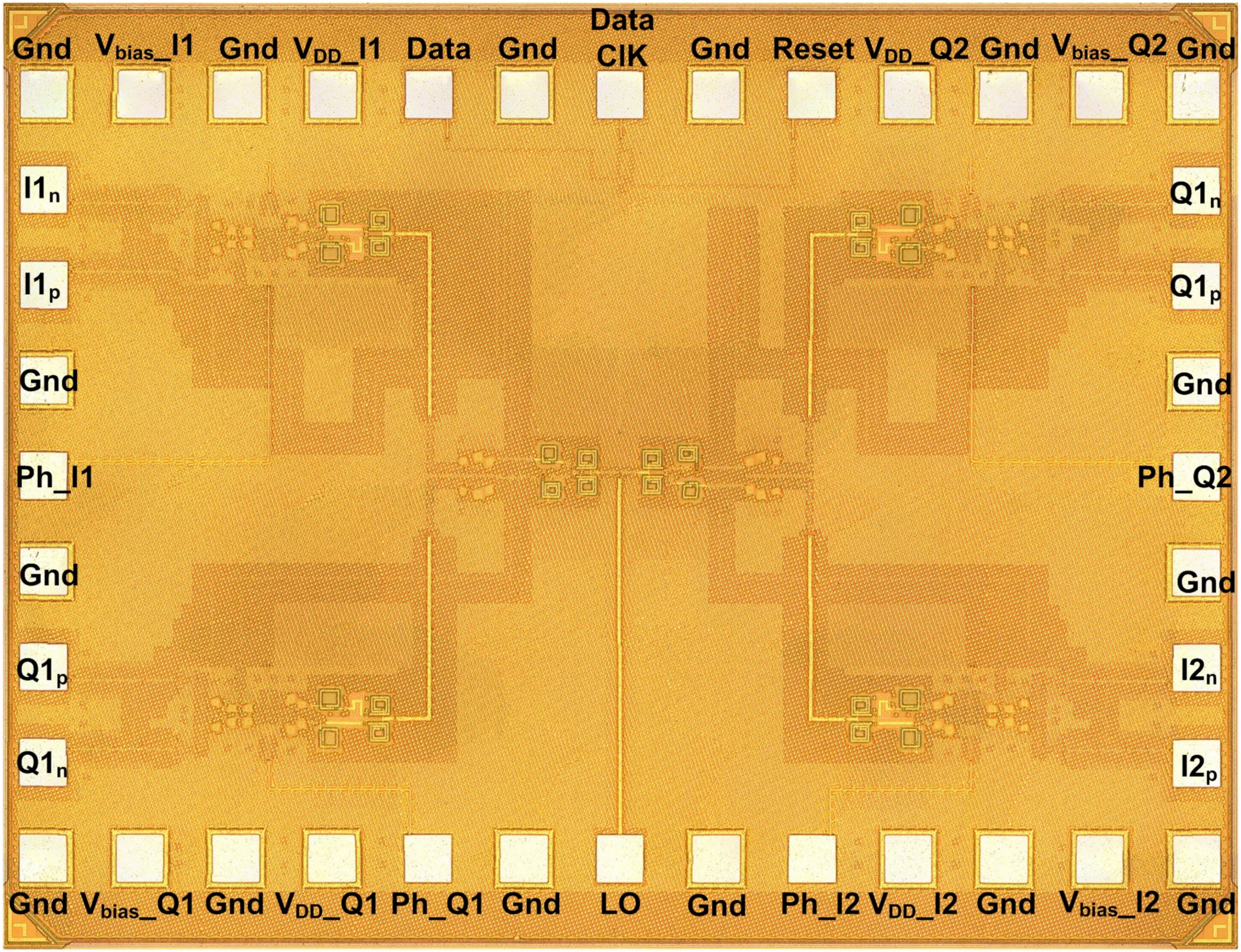
2-Gb/s ASK+ 2-Gbs BPSK Mod of 45-GHz Carrier



45-GHz 8-bit IQ DAC chiplet

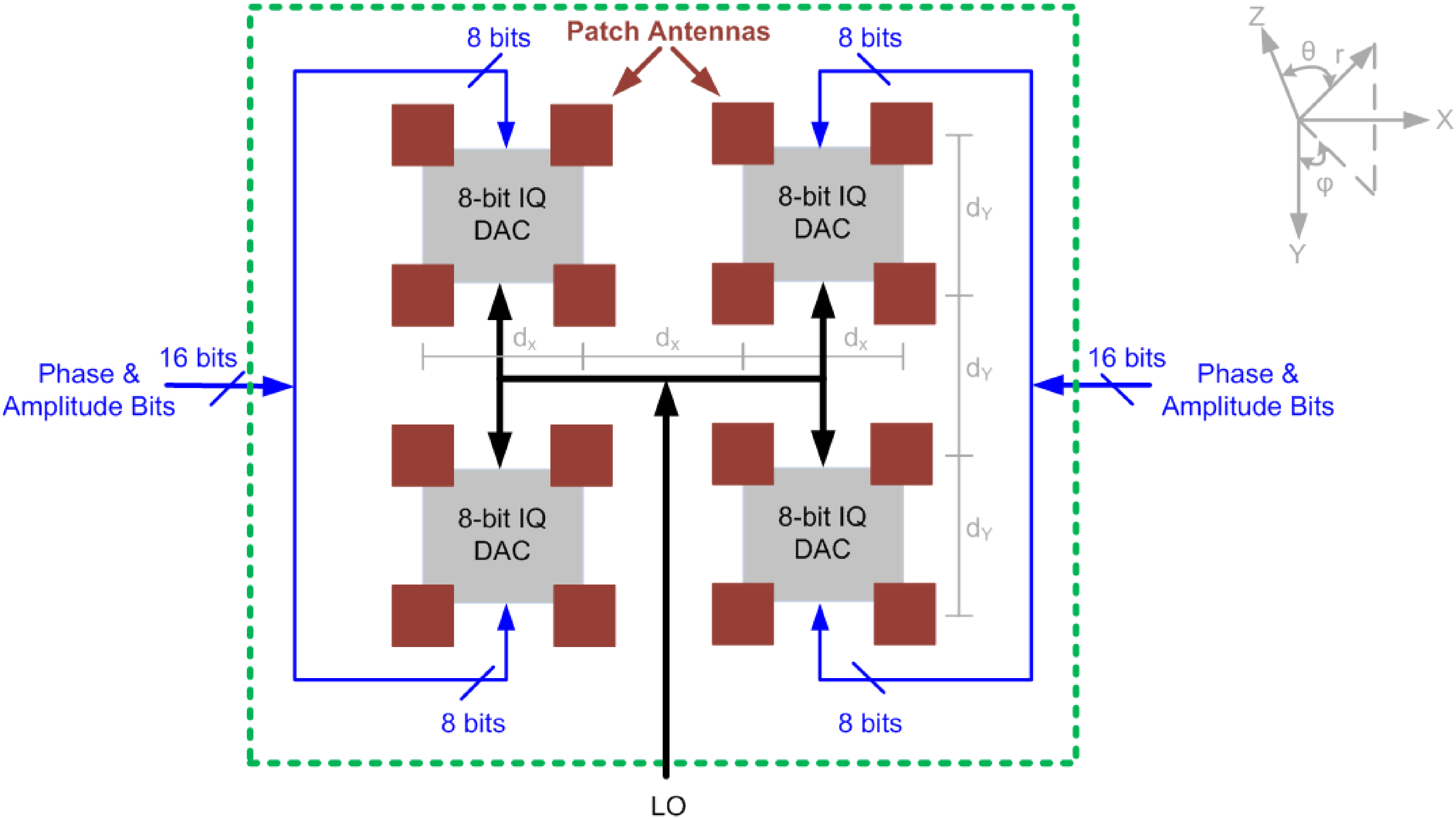


Die photo



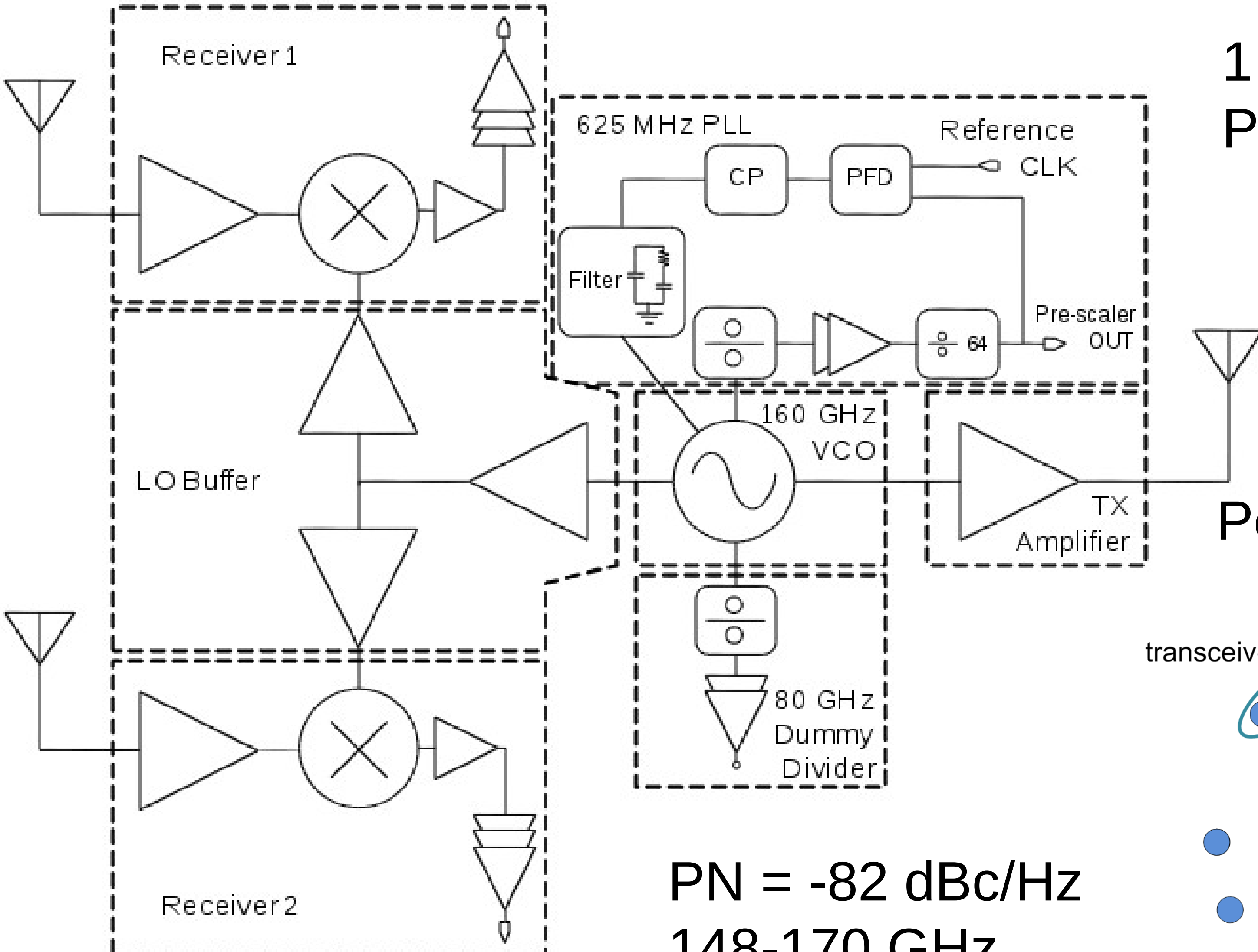
Gnd
Vbias_I1
Gnd
VDD_I1
Data
Gnd
Data ClK
Gnd
Reset
VDD_Q2
Gnd
Vbias_Q2
Gnd
I1n
I1p
Gnd
Ph_I1
Gnd
Q1p
Q1n
Q1n
Q1p
Gnd
Ph_Q2
Gnd
I2n
I2p
Gnd
Vbias_Q1
Gnd
VDD_Q1
Ph_Q1
Gnd
LO
Gnd
Ph_I2
VDD_I2
Gnd
Vbias_I2
Gnd

45-GHz 32-bit IQ-DAC board



- > 34 dBm, to be designed and packaged by UCSD

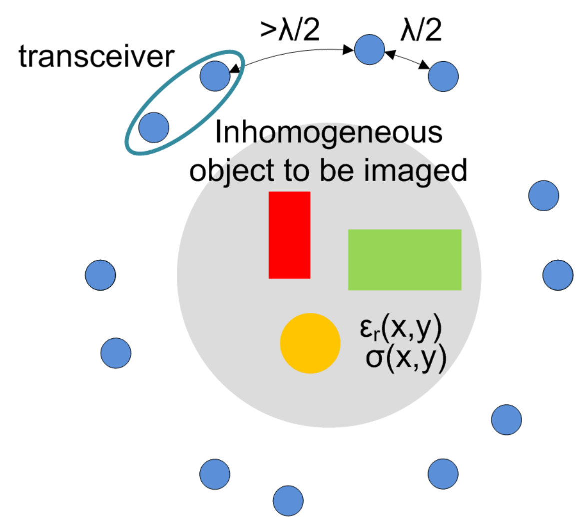
Dual Receive Channel Transceiver



1.5/2.5/3/3.6V

P_D = 1.8 W

Pout = 1 dBm



PN = -82 dBc/Hz

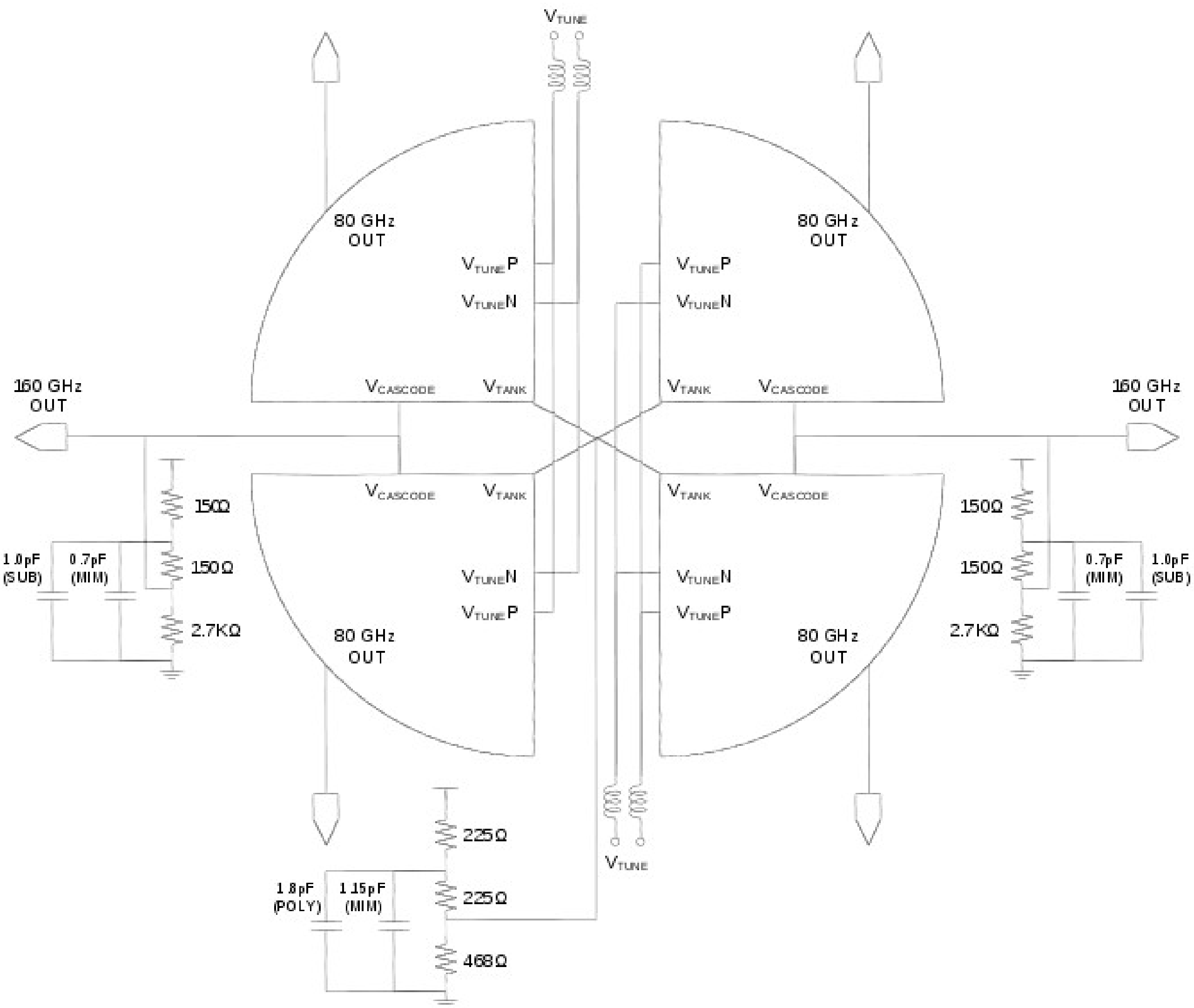
148-170 GHz

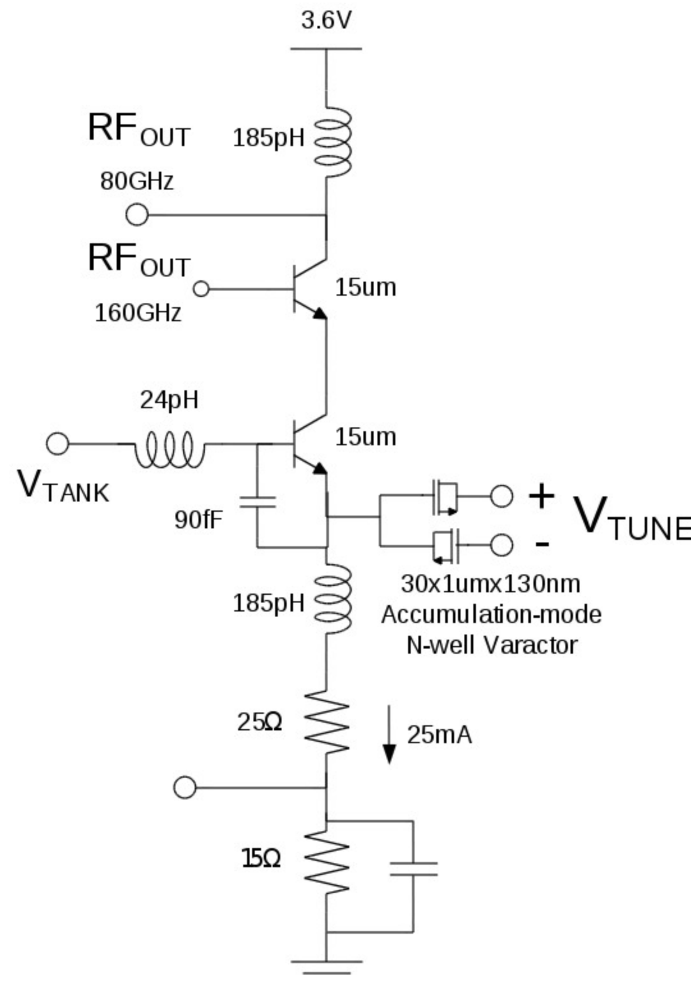
RX Gain = 27 dB

NF = 12 dB

I. Sarkas et al., MIKON-2012

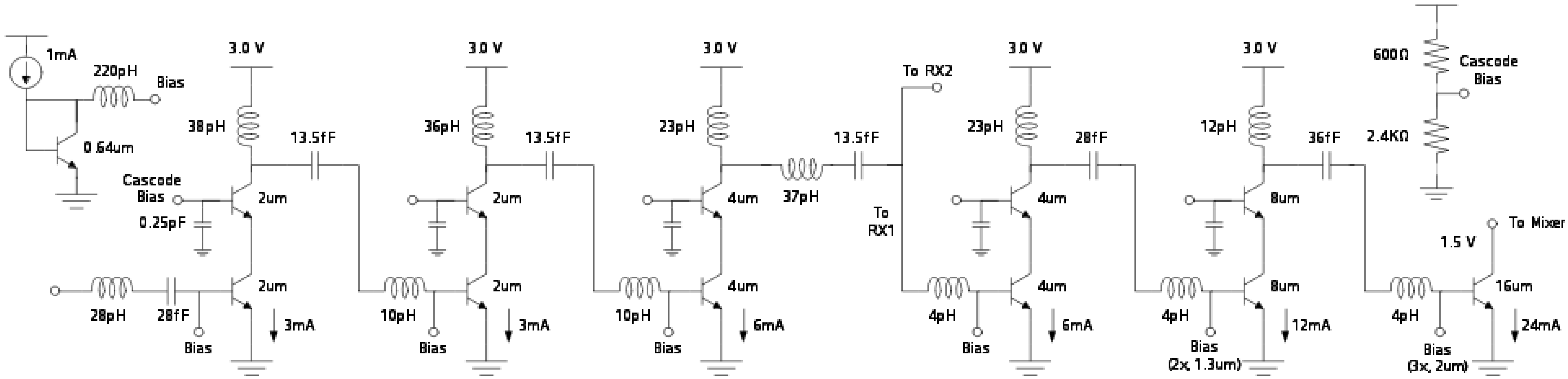
Push-Push 148-170 GHz VCO



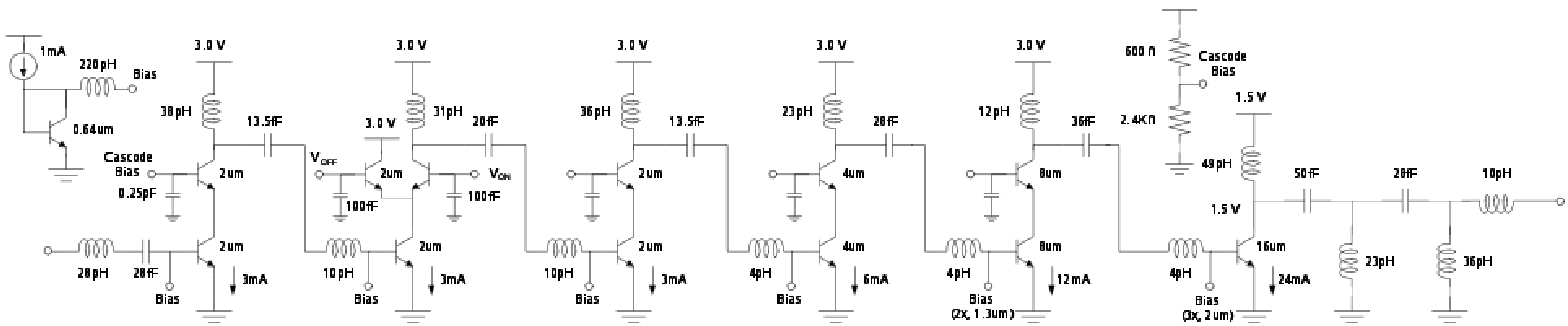


P_{DC} = 360 mW, P_{OUT} = -10 dBm, PN = -82 dBc/Hz at 1 MHz offset

148-170 GHz LO Tree and TX Amplifiers



P_D = 126 mW

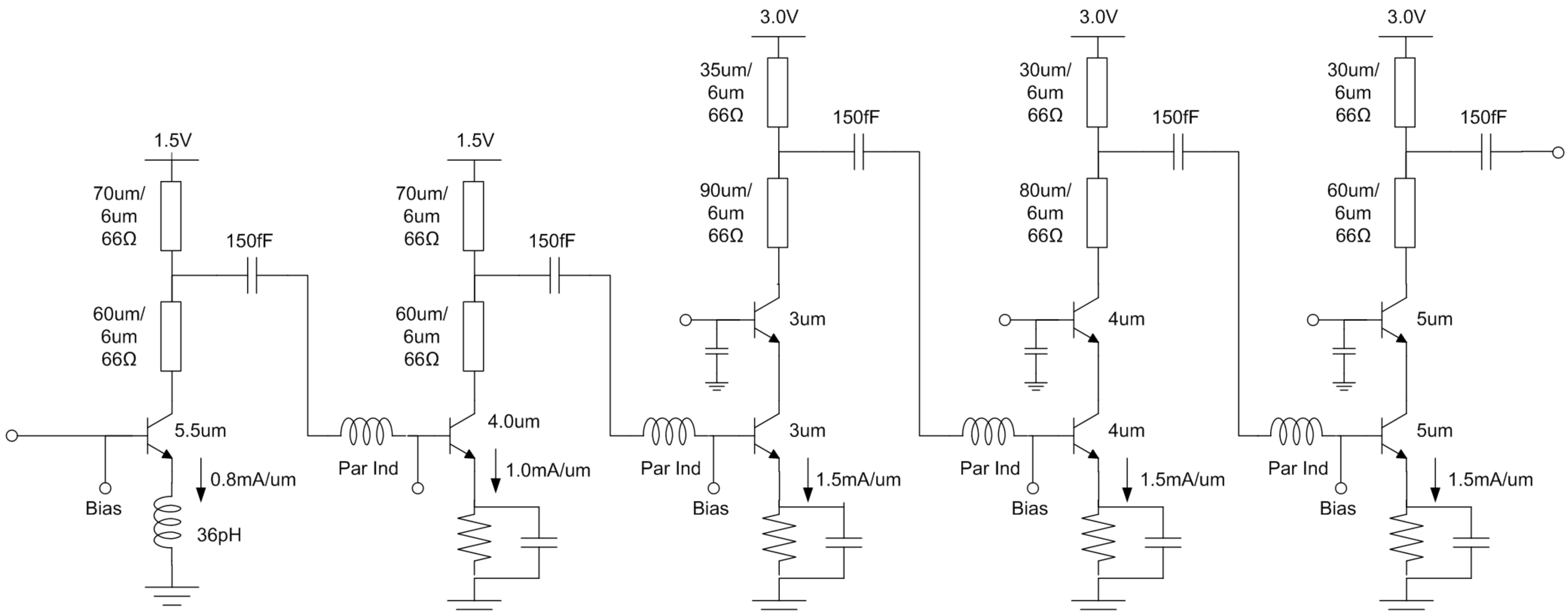


Amplitude Modulator

P_{out} > 2 dBm

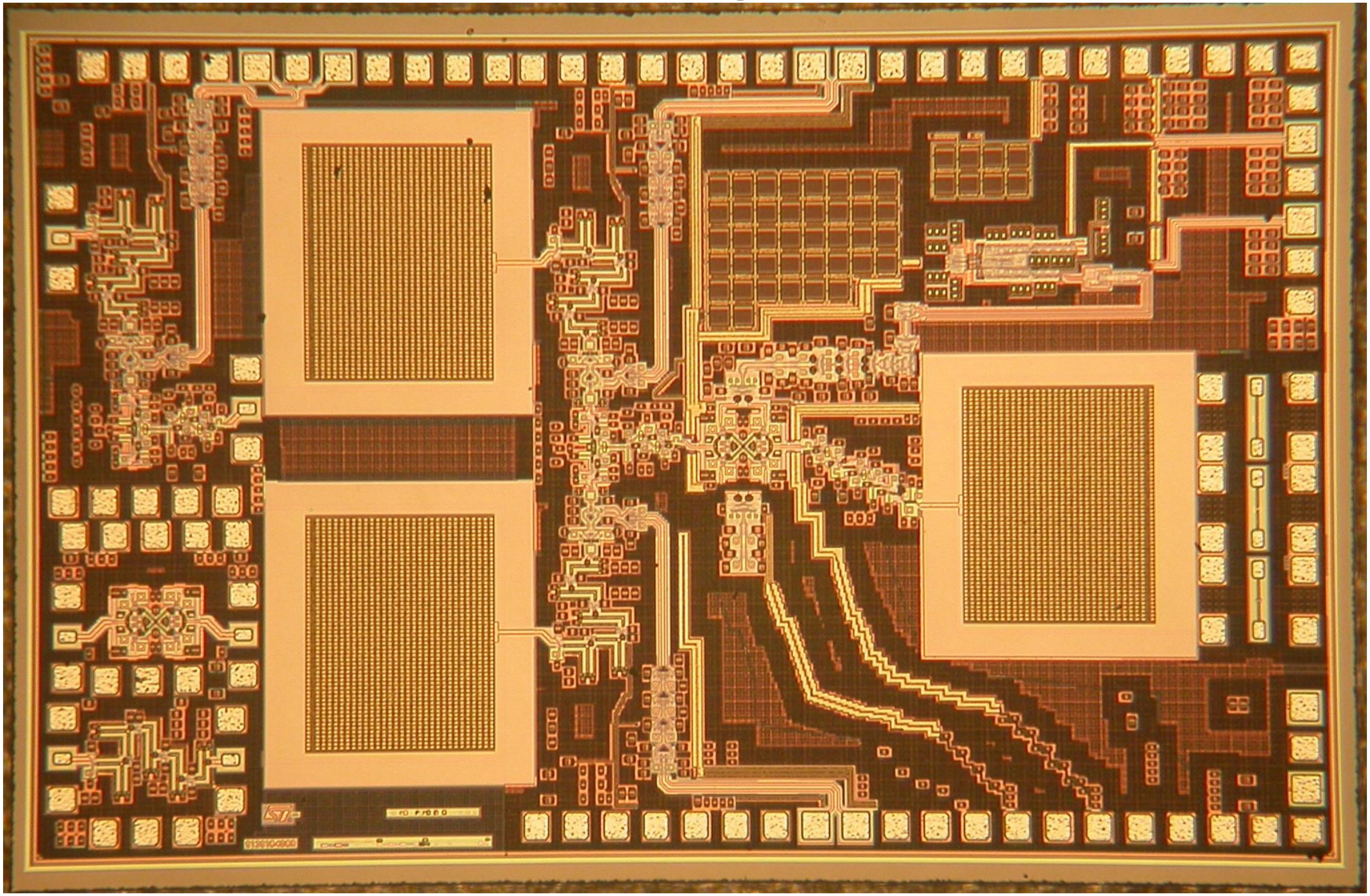
P_D = 117 mW

148-170 GHz Low Noise Amplifier



P_D = 67 mW, Gain= 20 dB, NF < 12 dB.

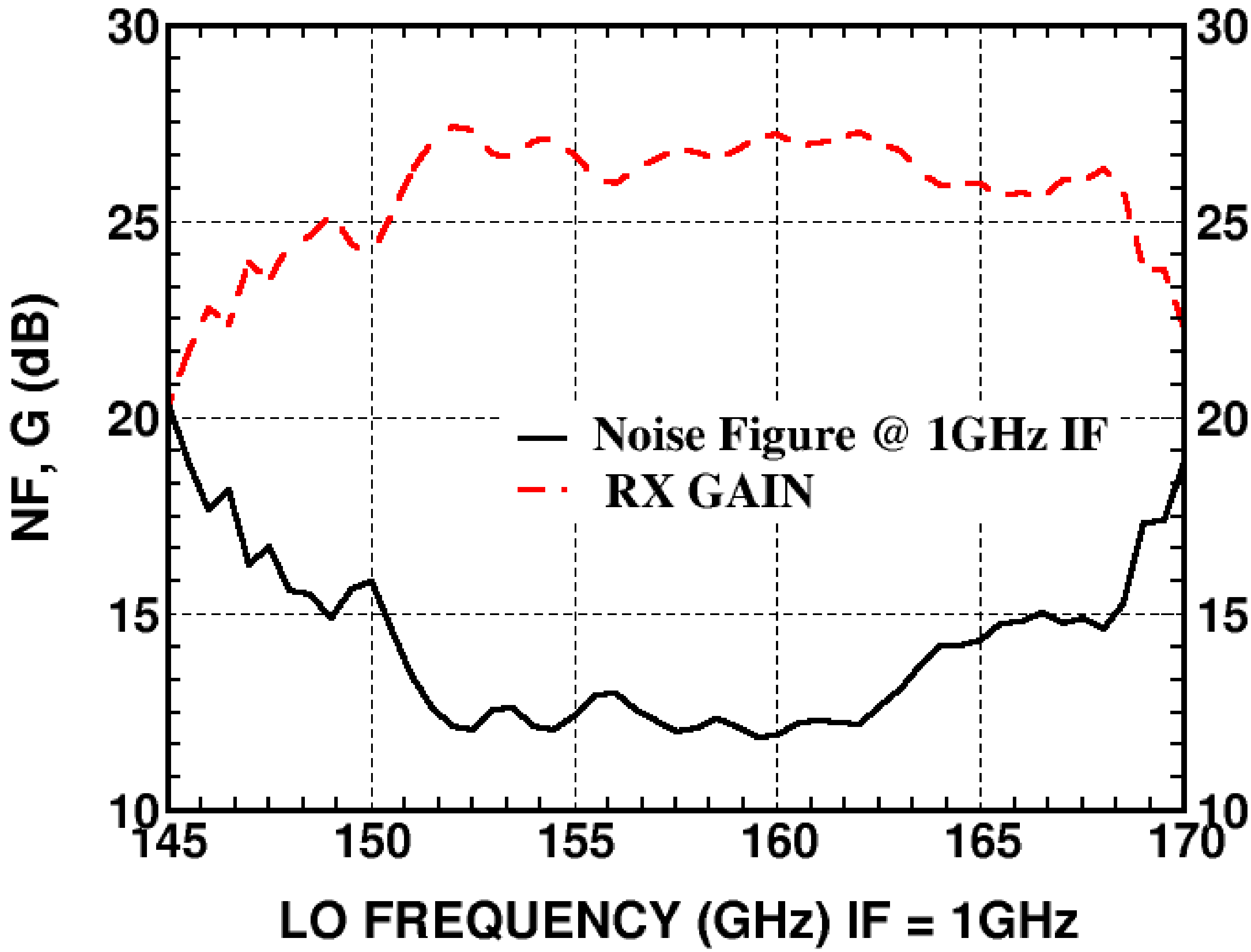
Die photograph



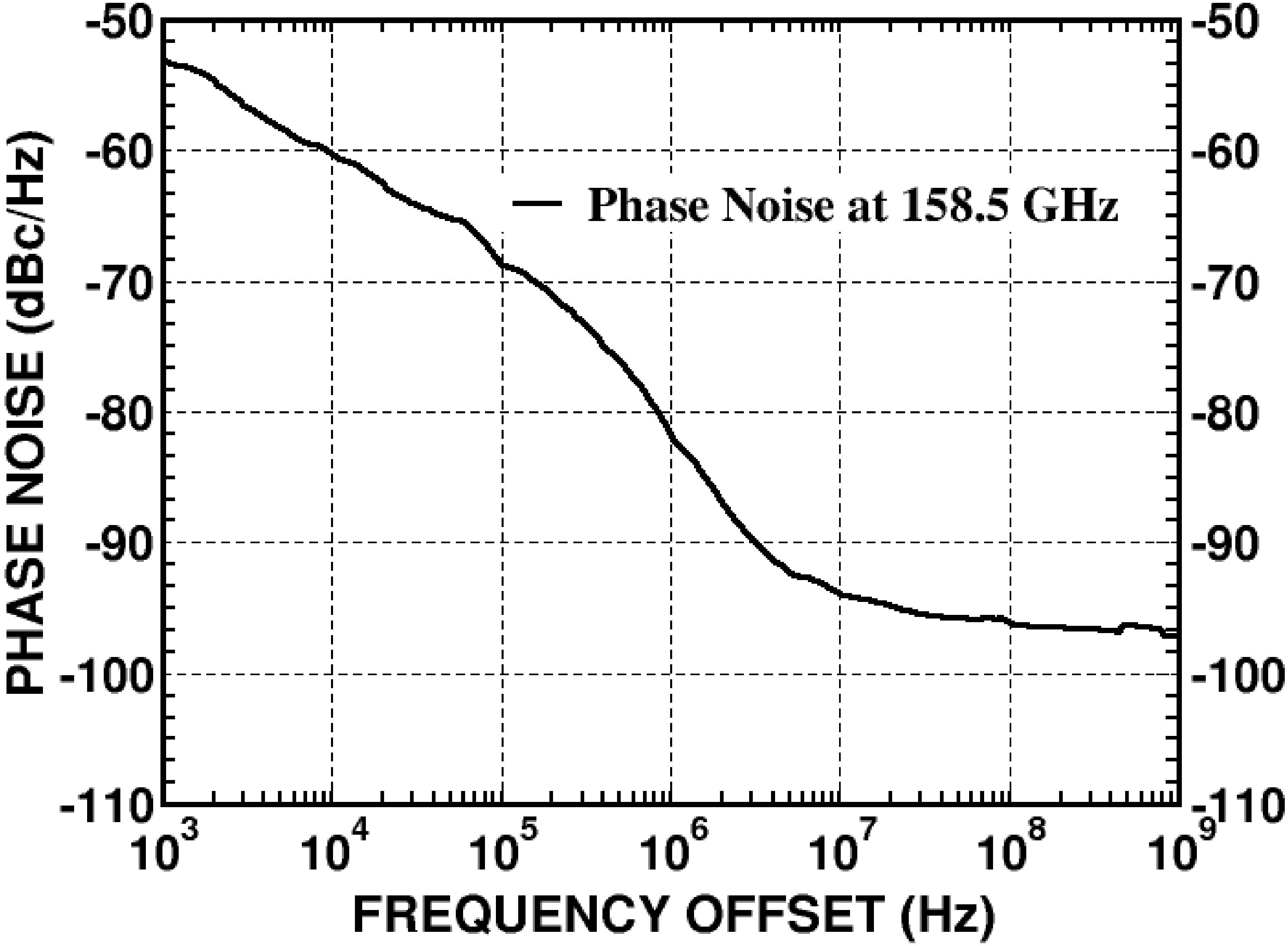
Chip: 2.1mm×2.9mm

130-nm BiCMOS9MW: SiGe HBT f_T= 230 GHz, f_{MAX} = 280 GHz

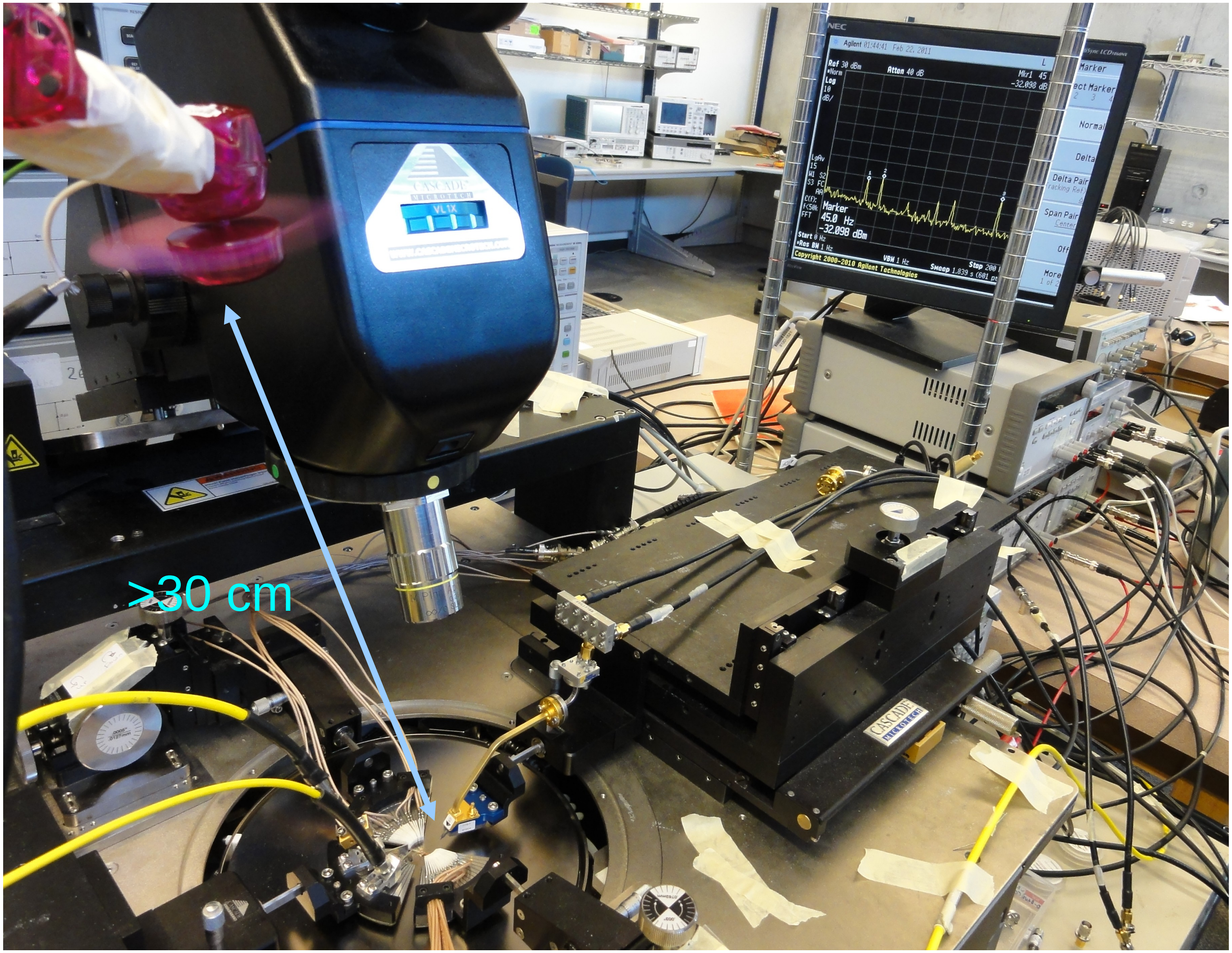
RX Breakout Gain and Noise Figure



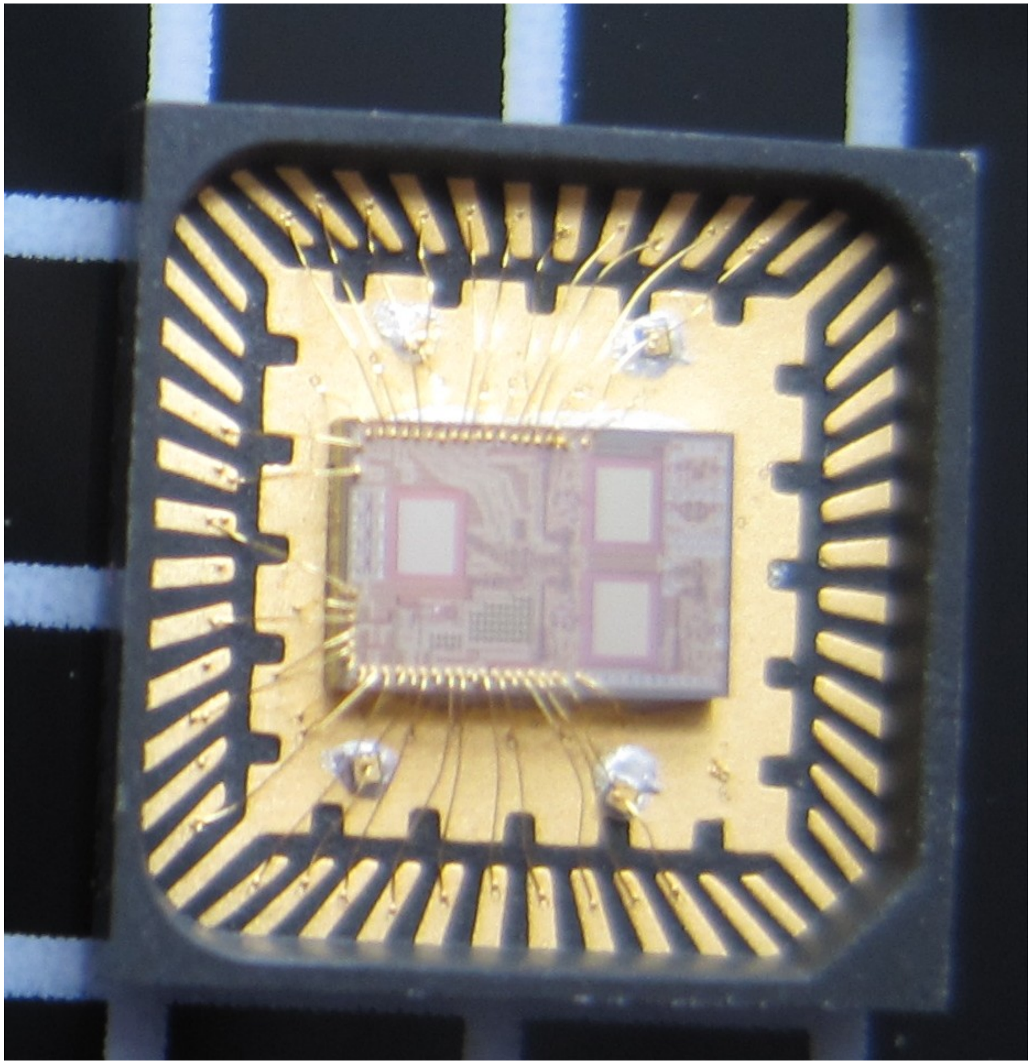
Transceiver PLL Phase Noise

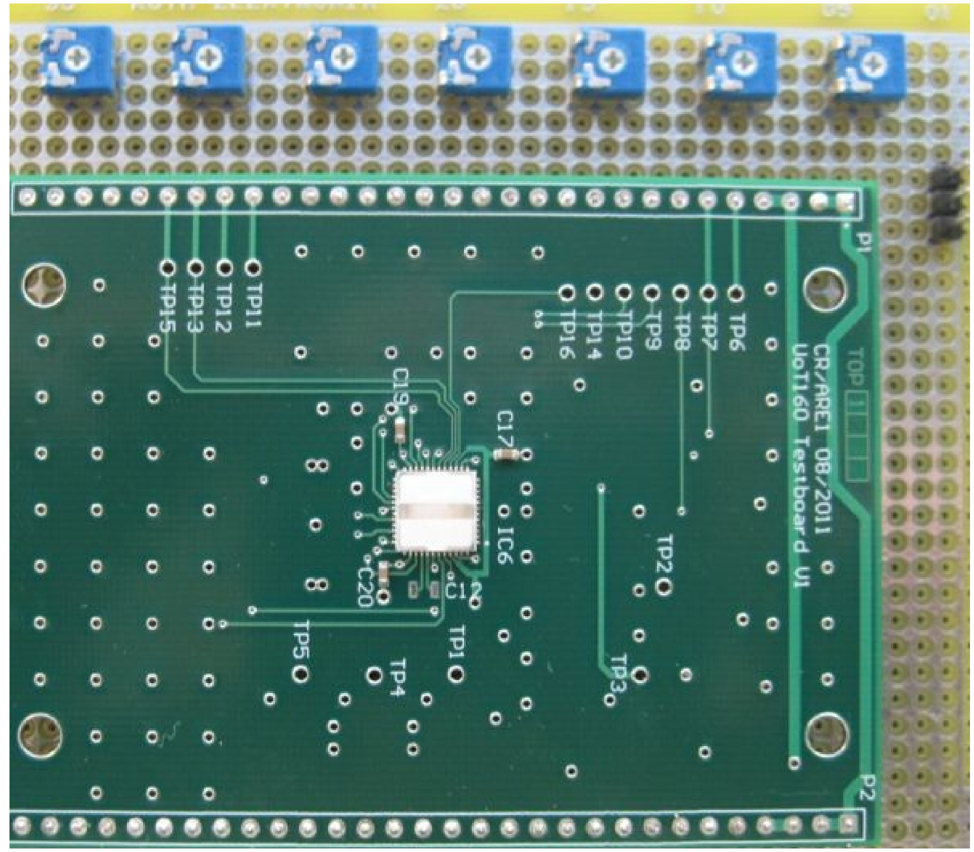


On-die Doppler Test



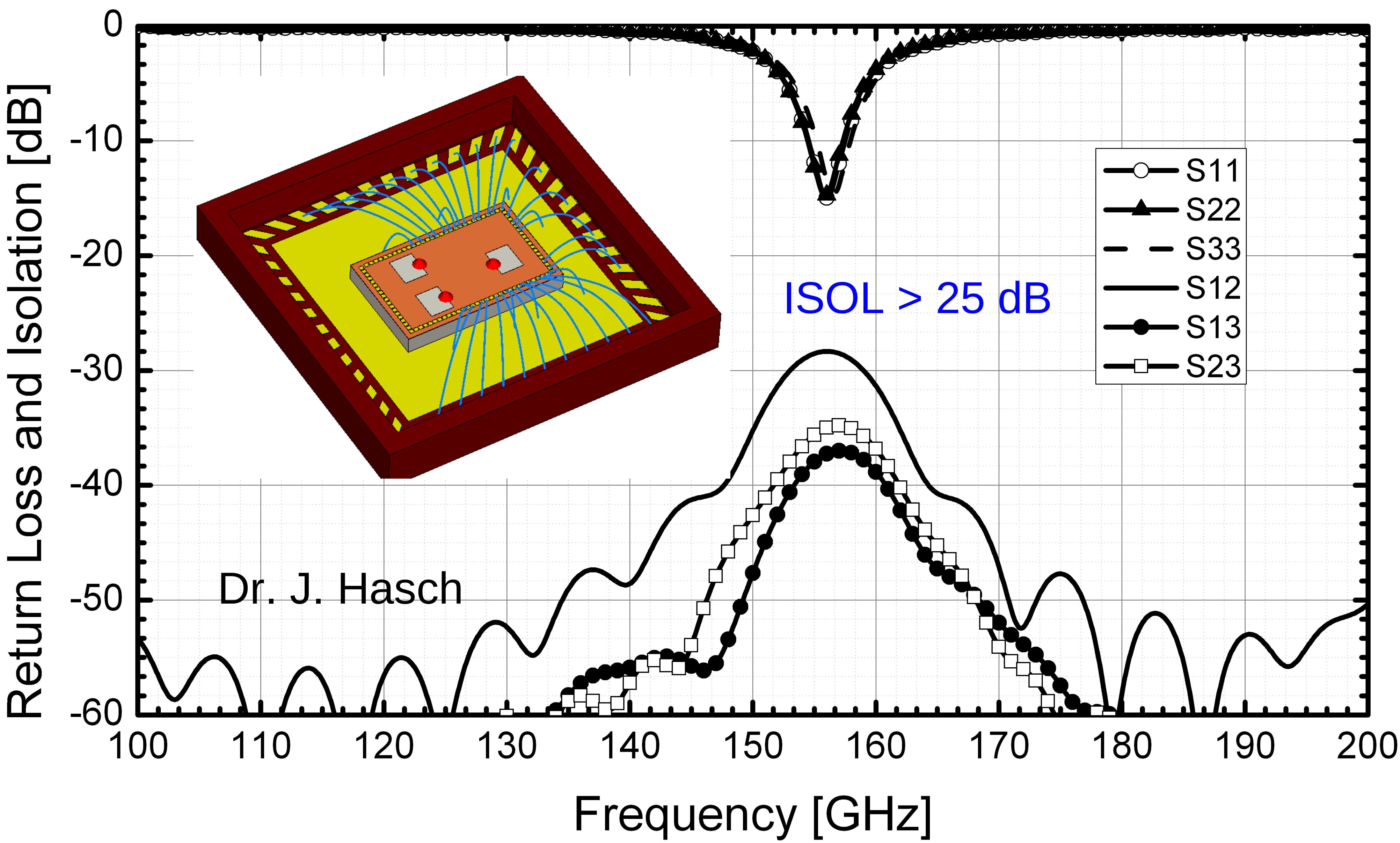
Packaging



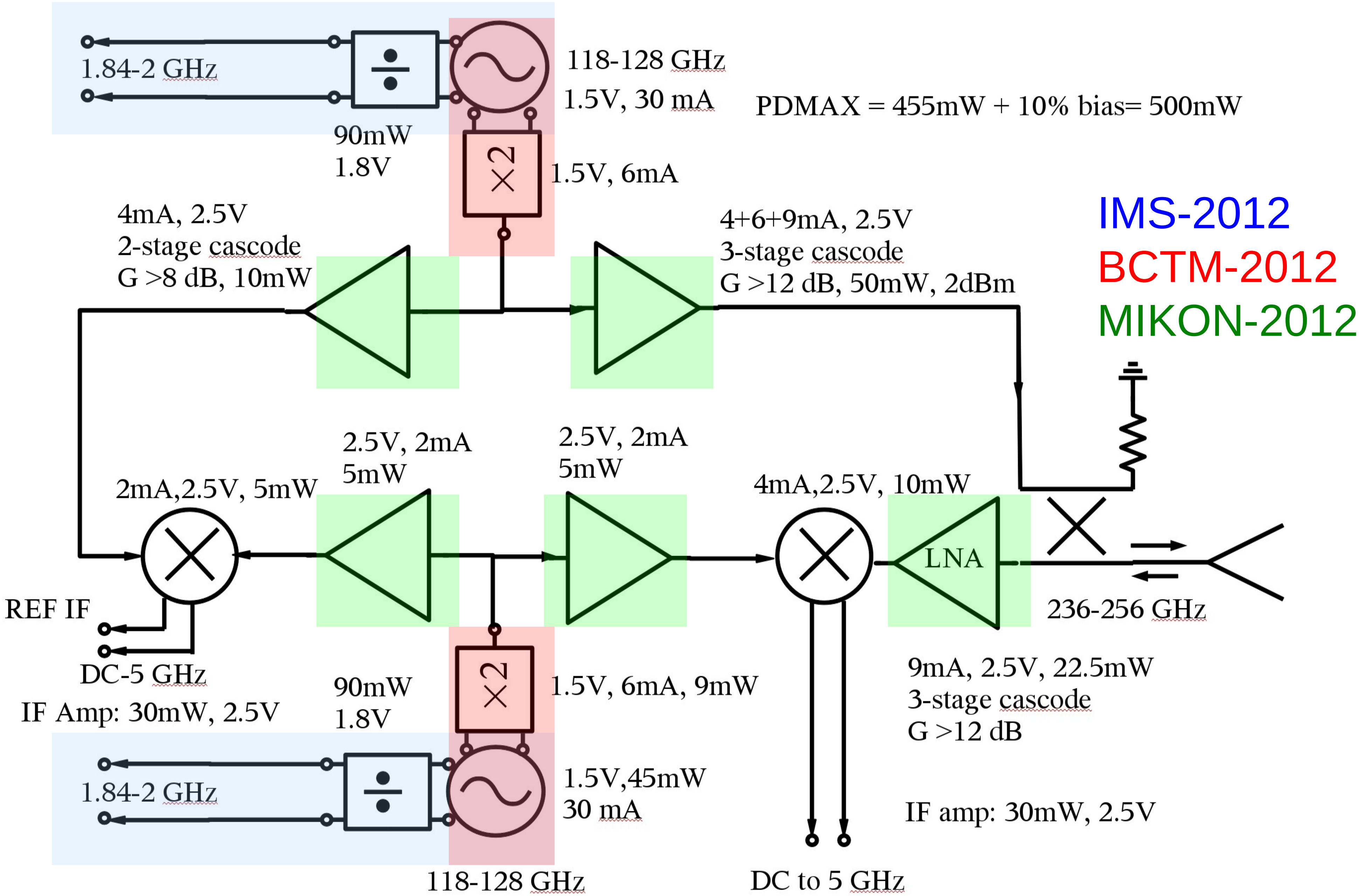


Dr. J. Hasch

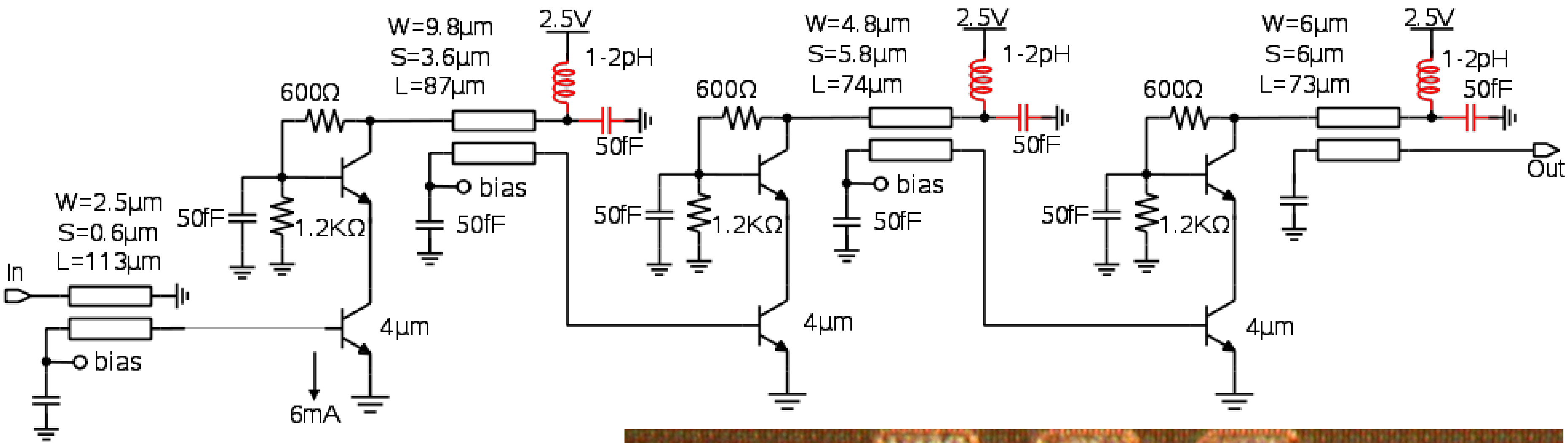
In-package Antennas Simulation

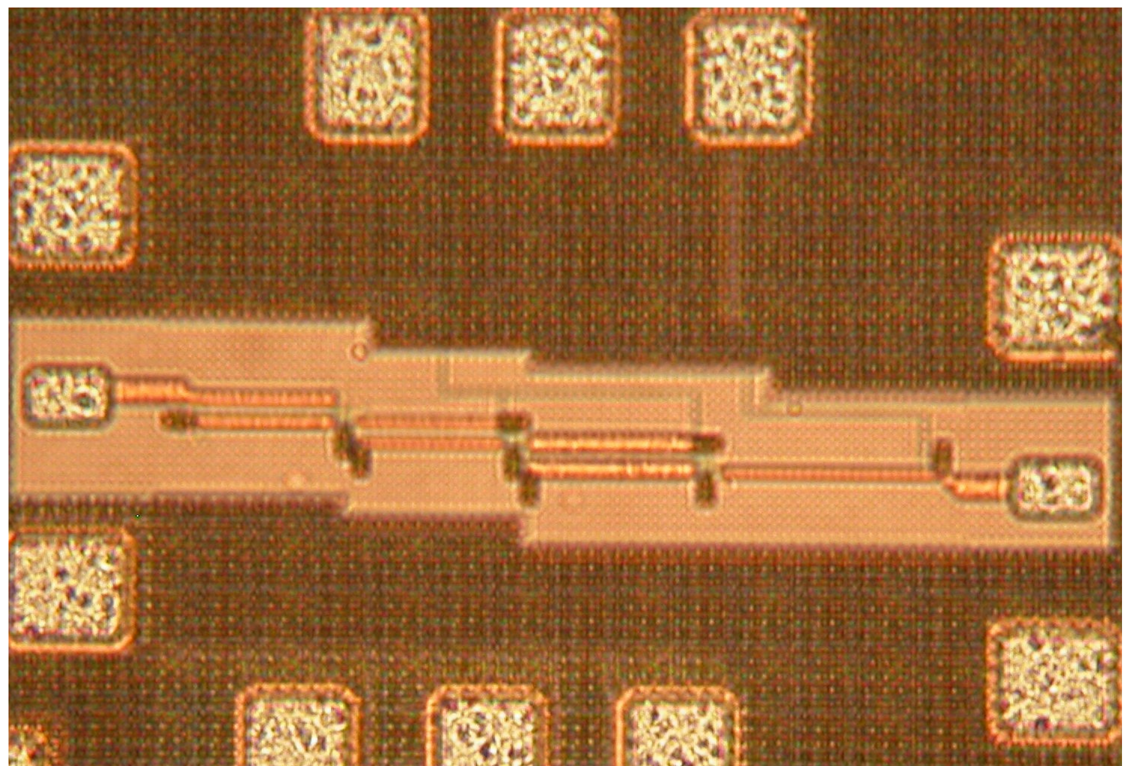


240-GHz Transceiver Blocks



240-GHz Amplifier



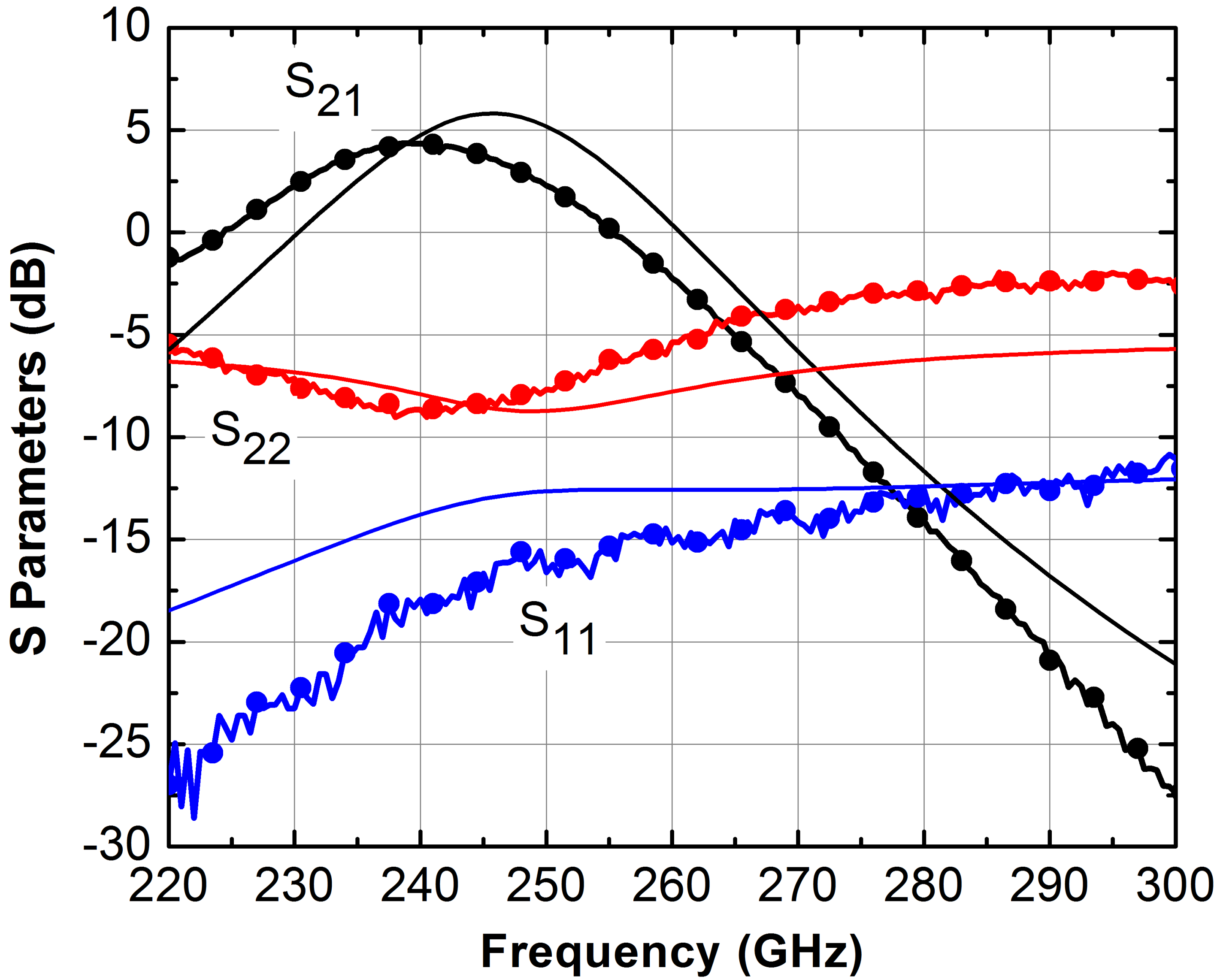


P_D = 37.5 mW

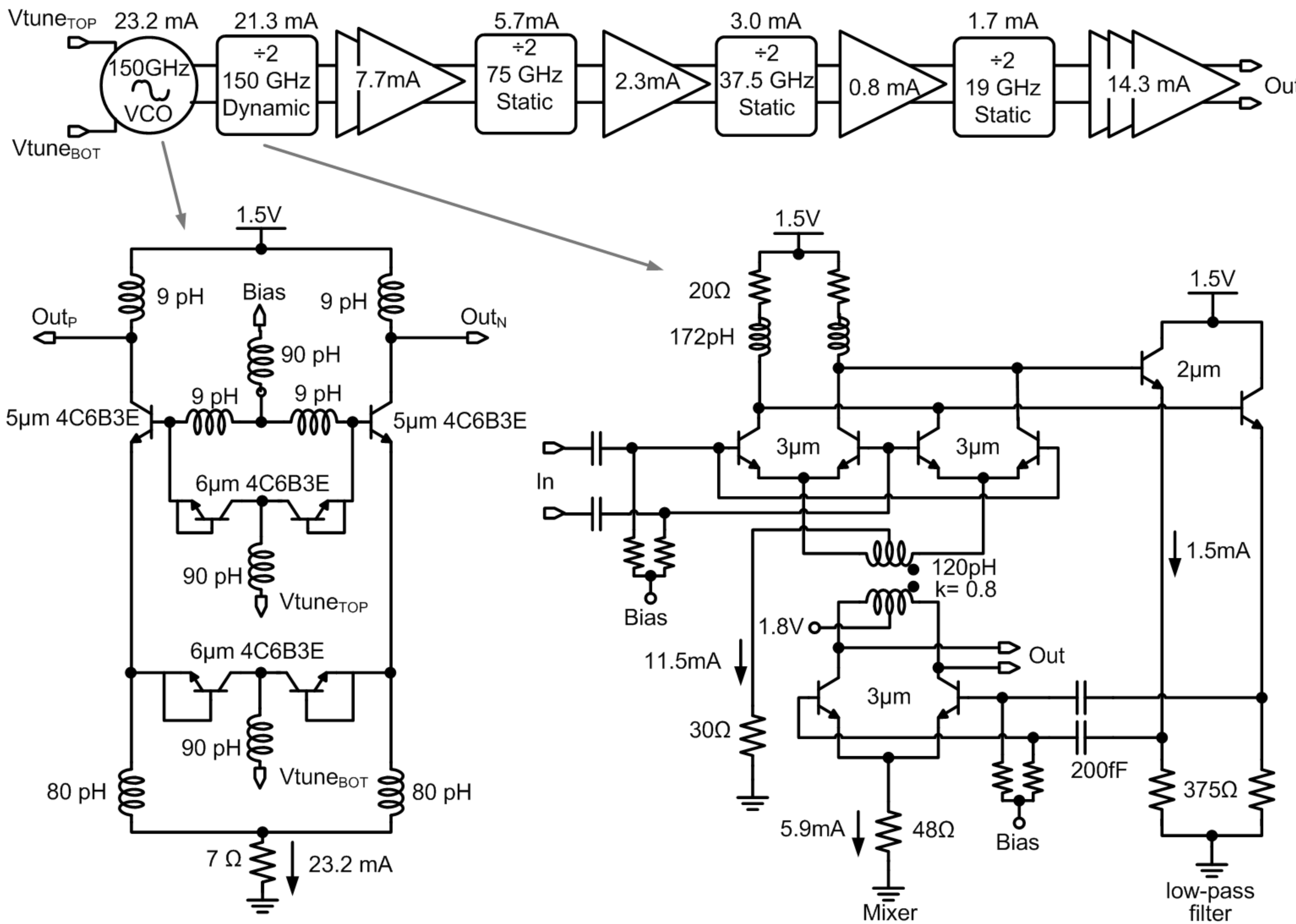
G = 4.5 dB @ 240 GHz

I. Sarkas et al, MIKON 2012

240-GHz Amplifier

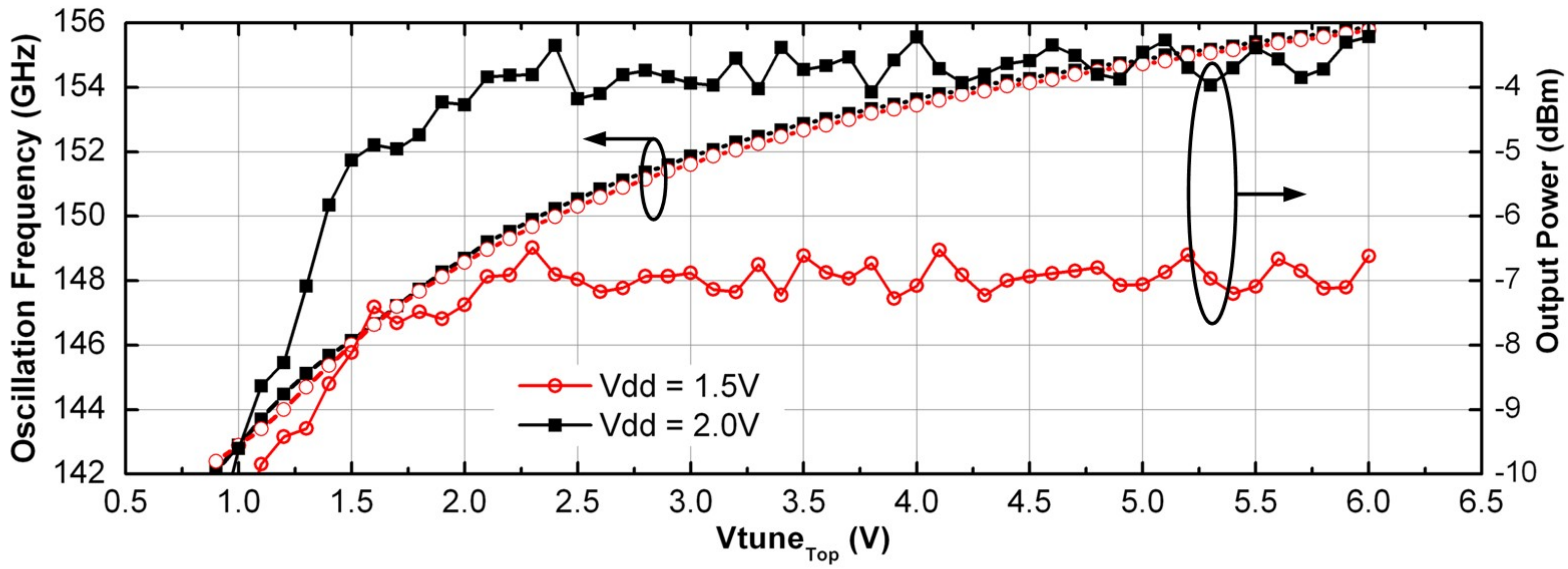


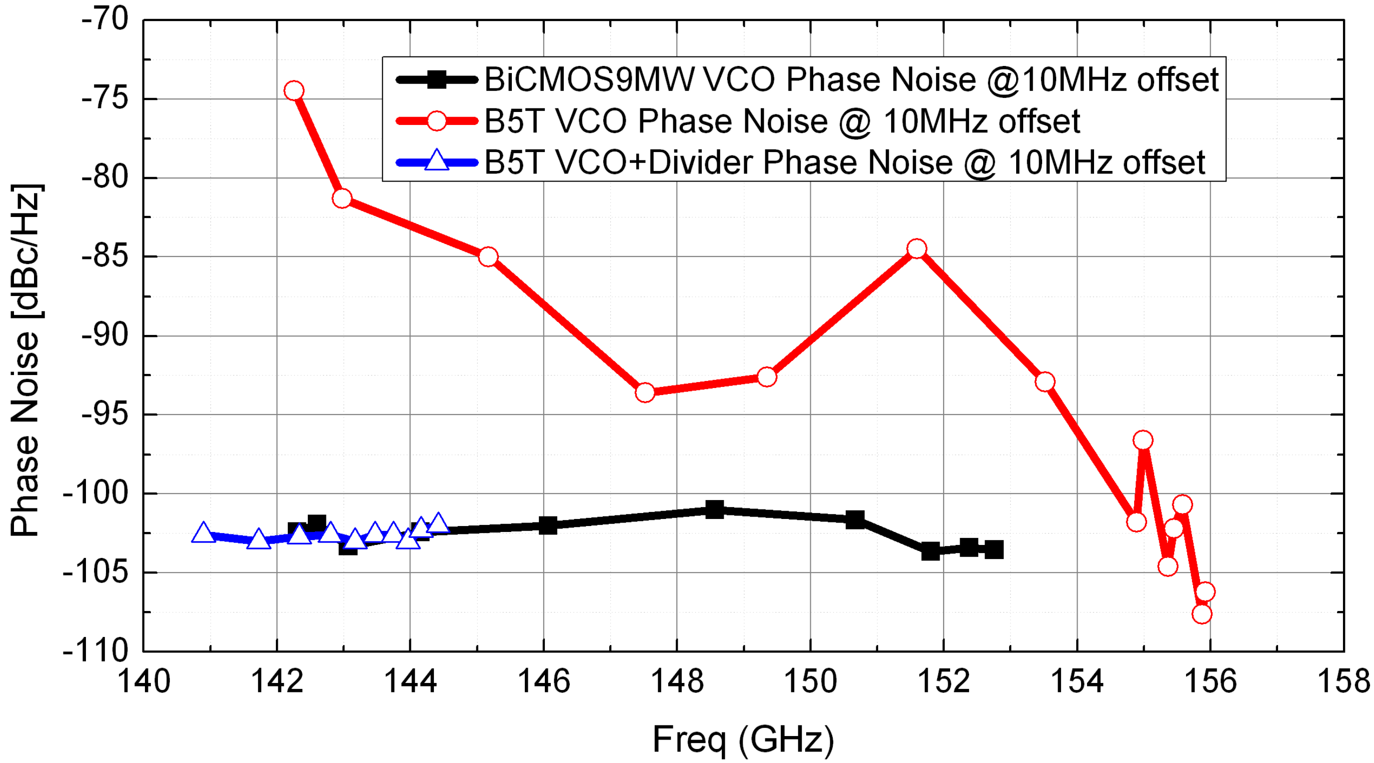
150-GHz VCO-prescaler



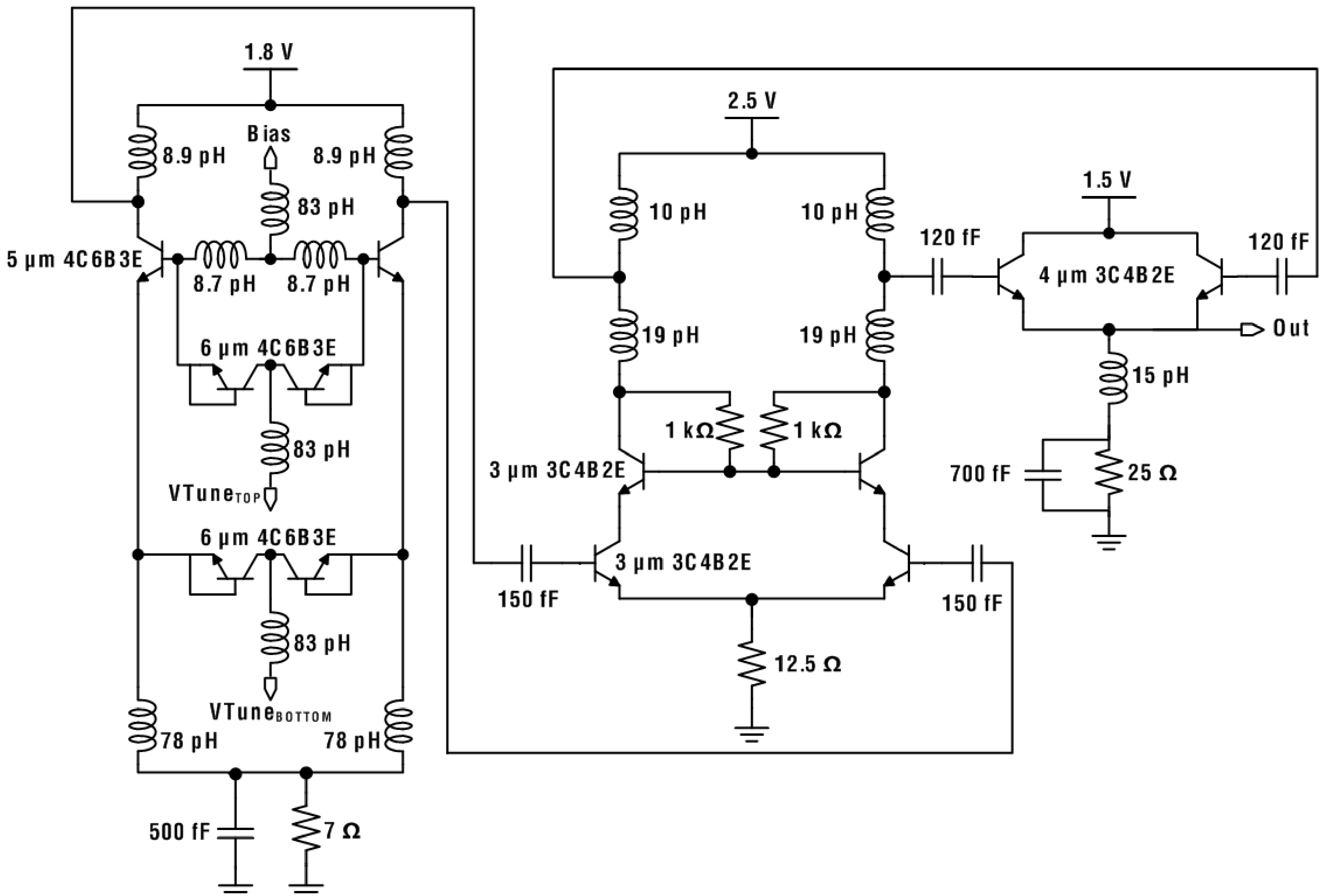
[A. Balteanu et al IMS 2012]

Measurements



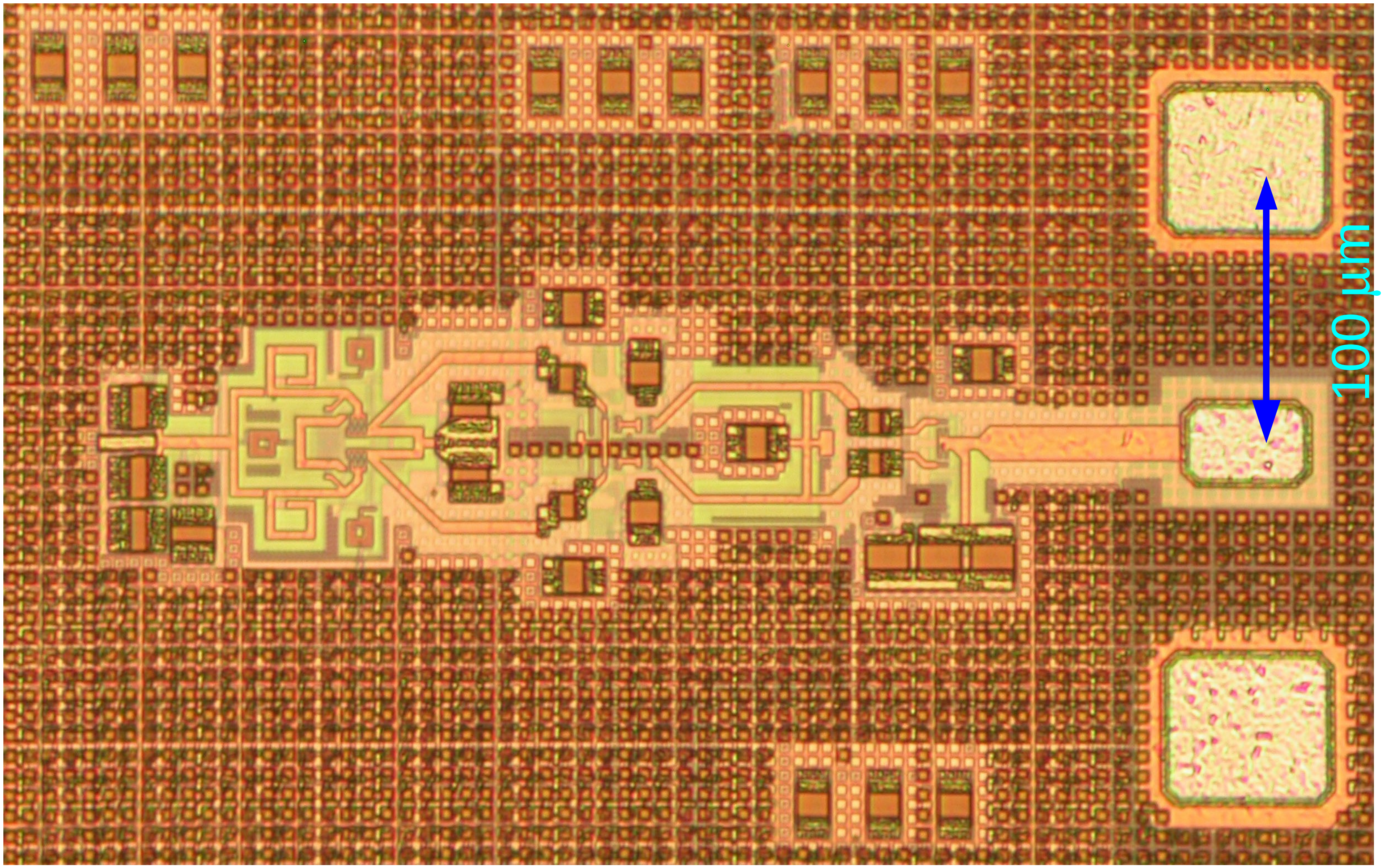


300-GHz VCO-Doubler

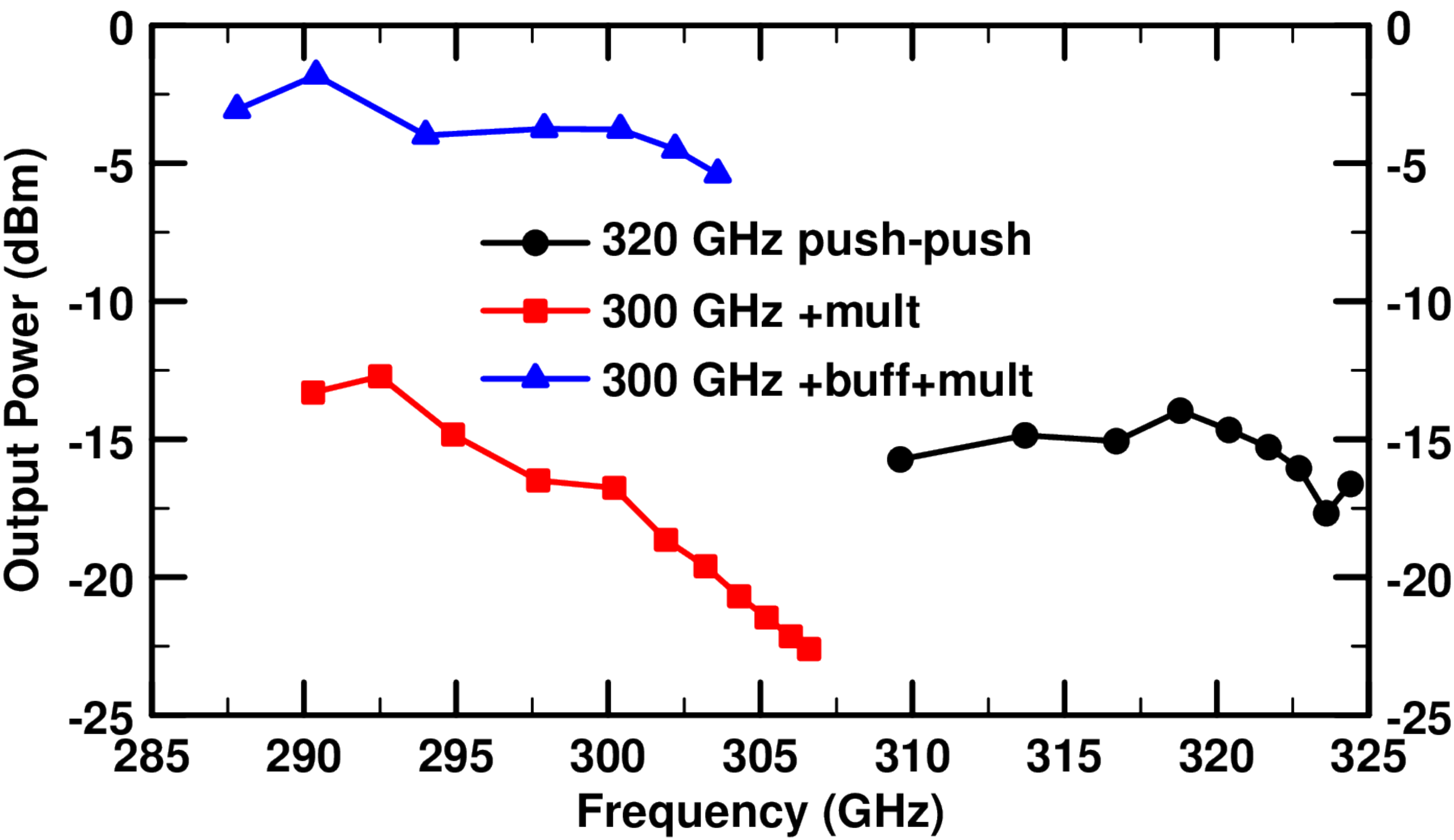


A. Tomkins et al., BCTM 2012

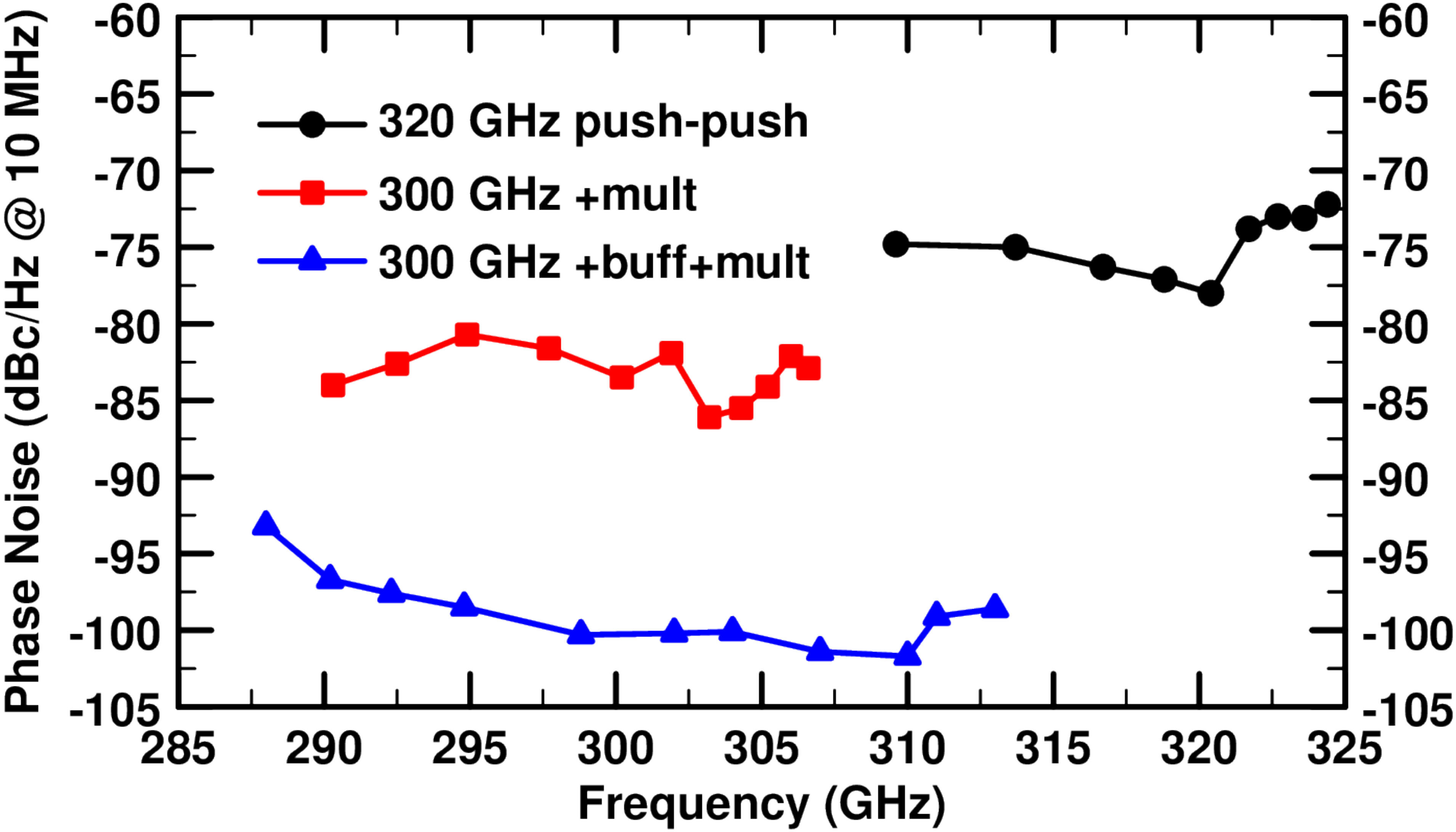
Layout



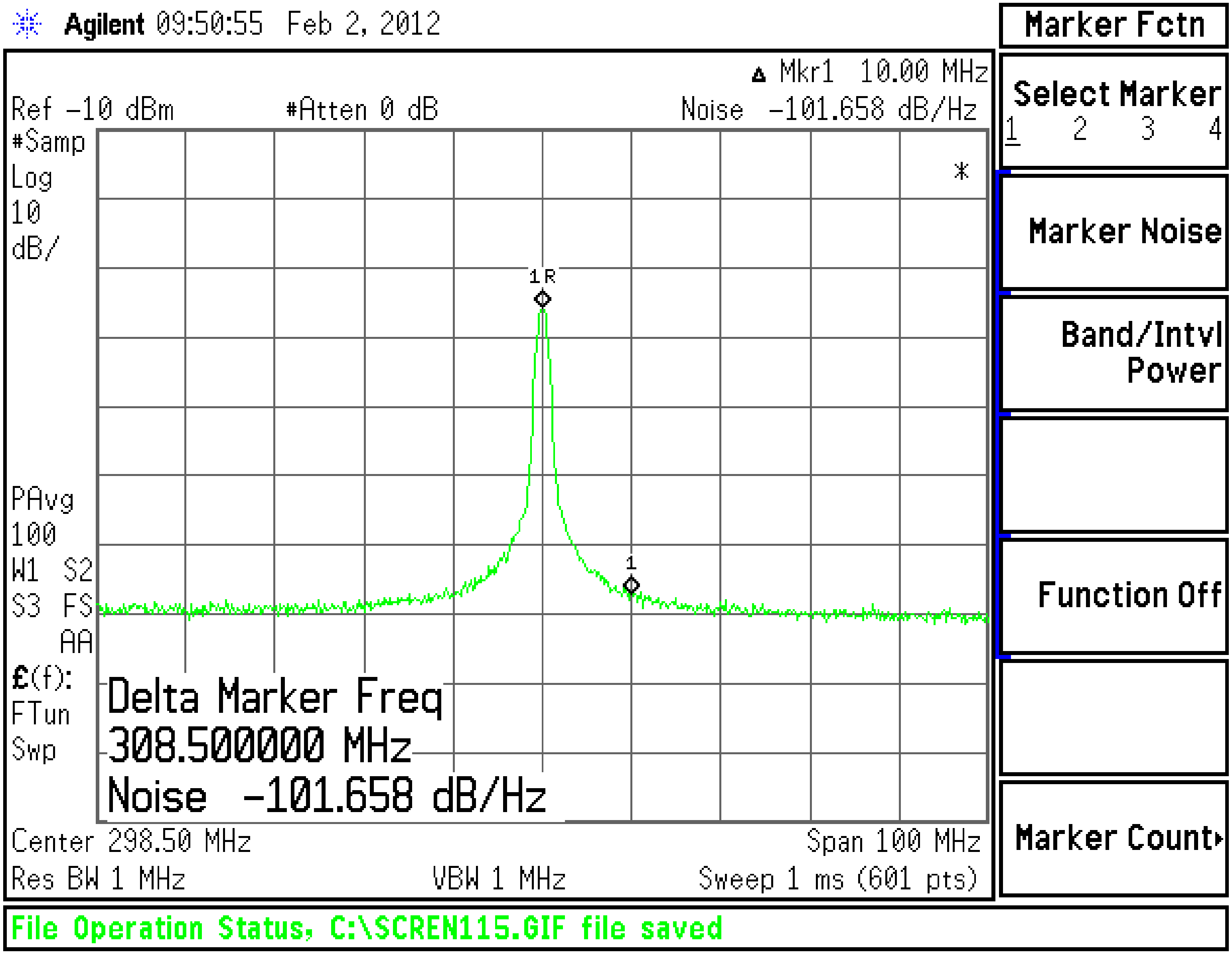
300-GHz Signal Source Comparison



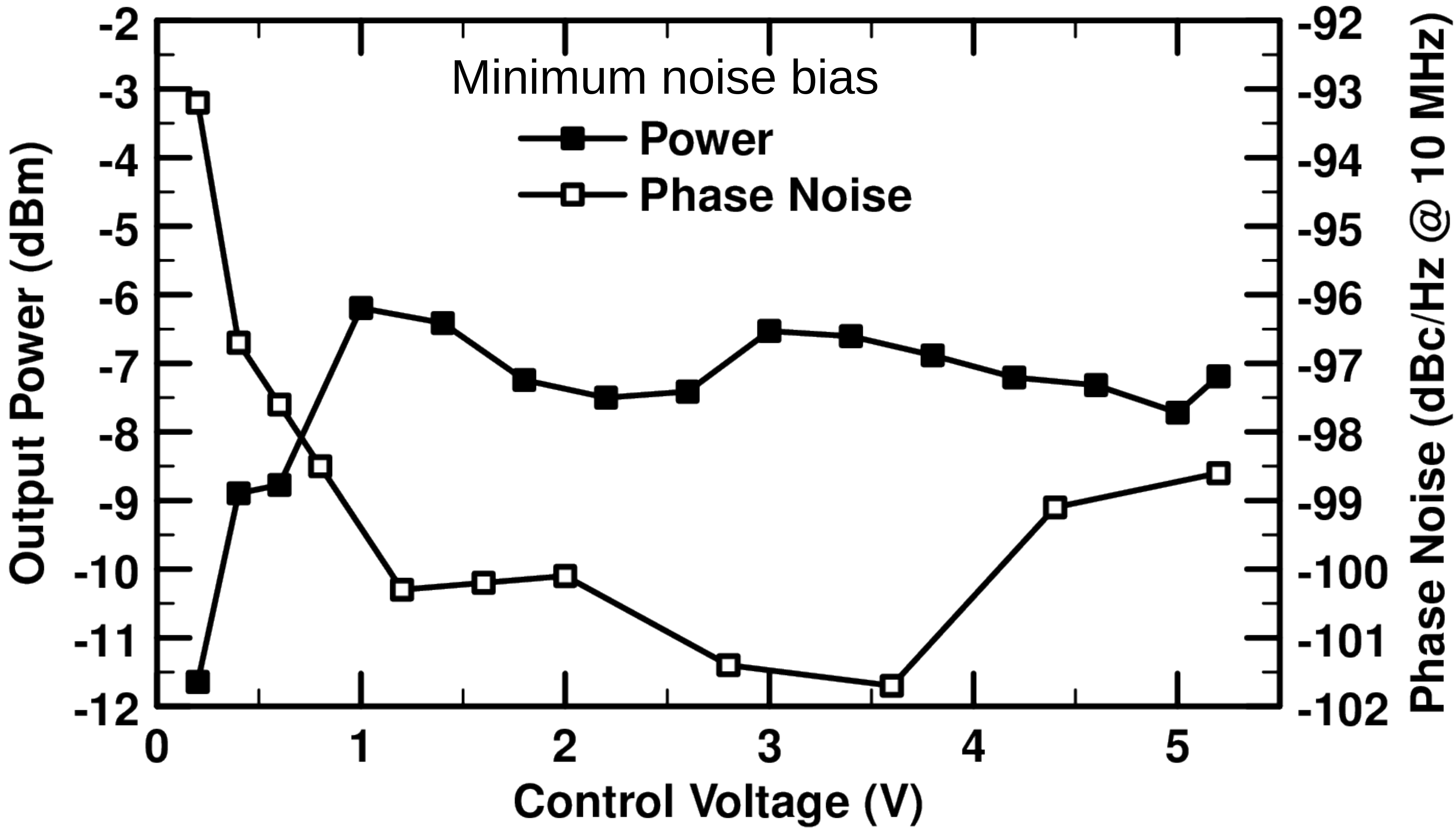
300-GHz Signal Source Comparison (ii)



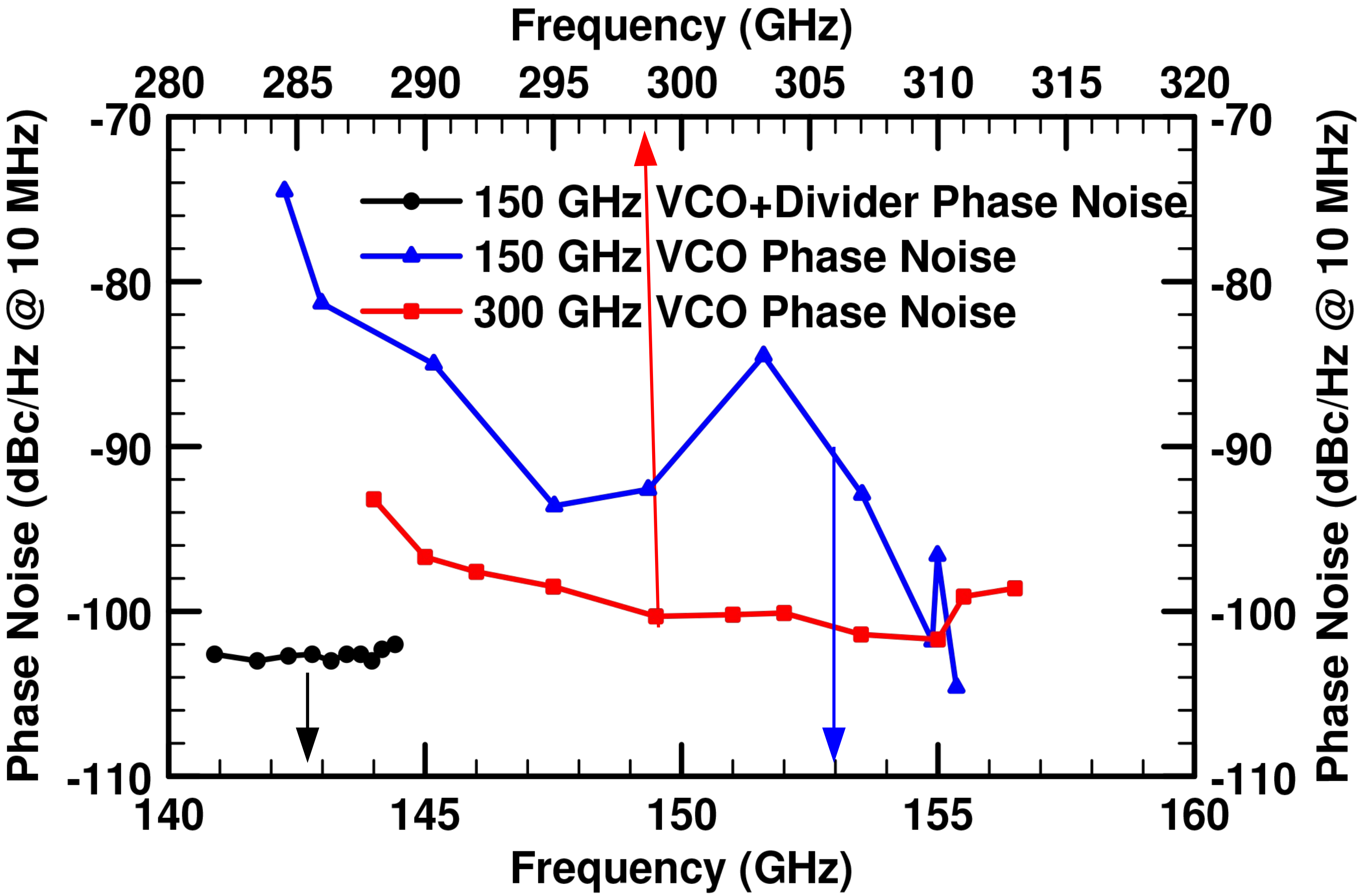
Phase Noise of VCO-doubler at 309 GHz



Measured Pout and Phase Noise 300-GHz VCO+buffer+doubler



300-GHz vs. 150-GHz Phase Noise

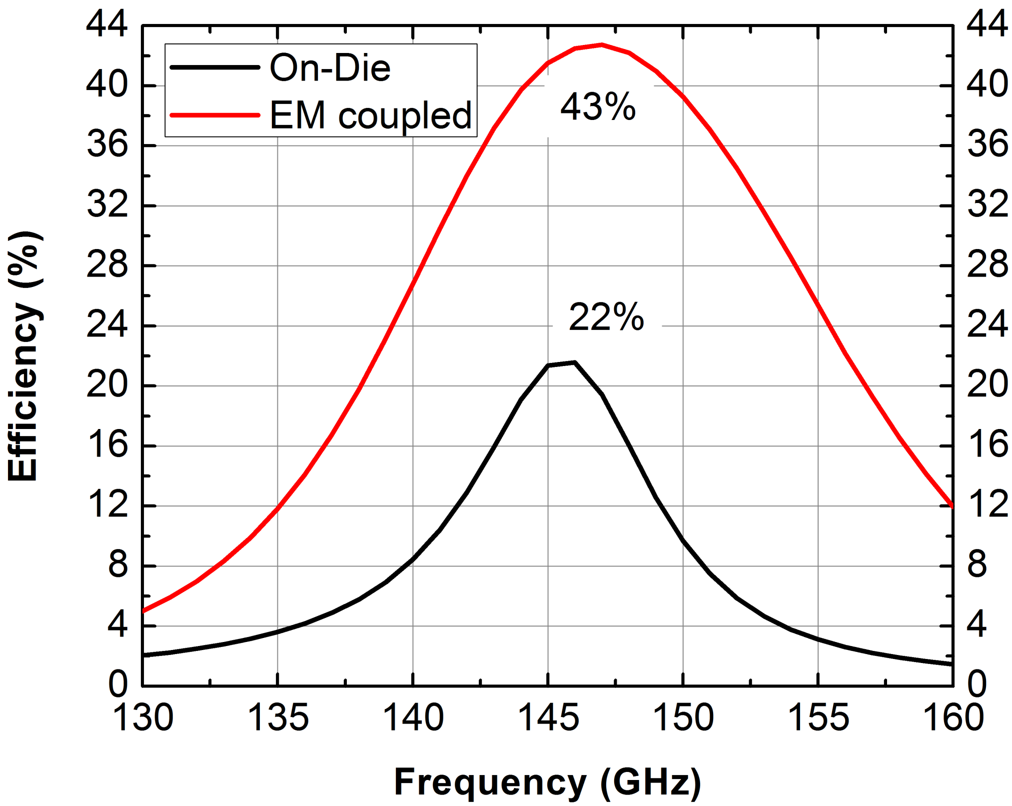


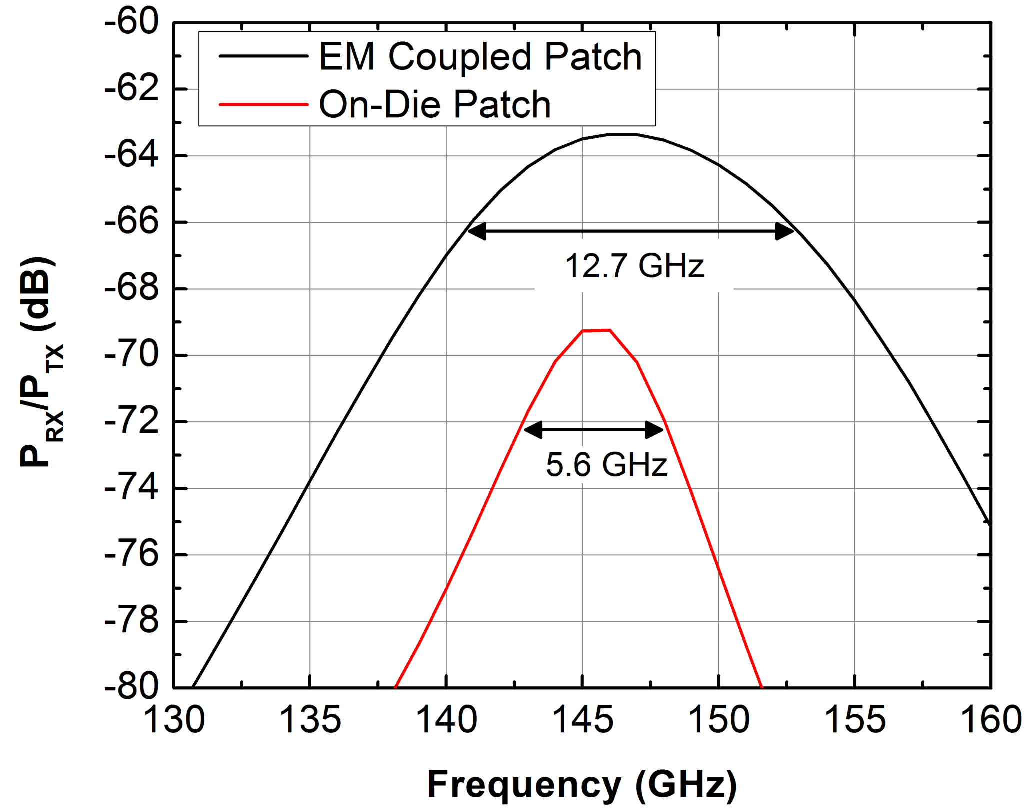
SAME VCO in BOTH!

Conclusions

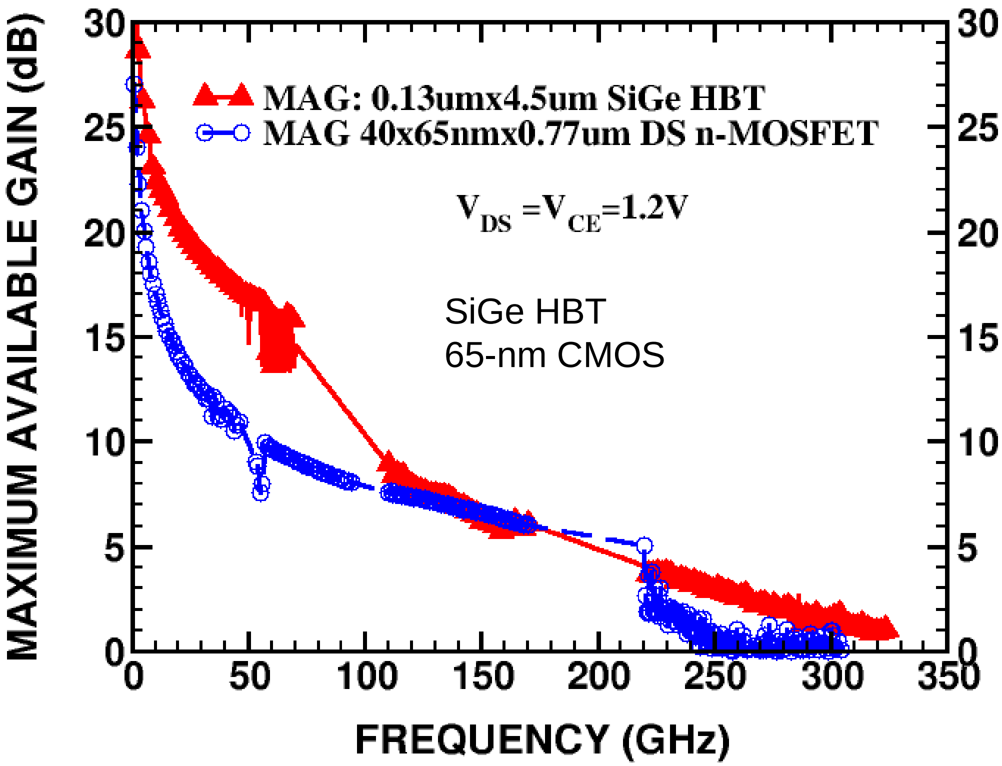
- Why?
  - Because we can!
  - “Cloud” unsustainable without 10x speed and 100x efficiency improvement
  - Need 1Tb/s for near field and intra data center comms
- How?
  - 50-100 Gb/s inductively peaked CMOS logic
  - Mm-wave Power-DAC Transmittter
  - H-Band SoCs with on-die antennas
  - Low-cost QFN package

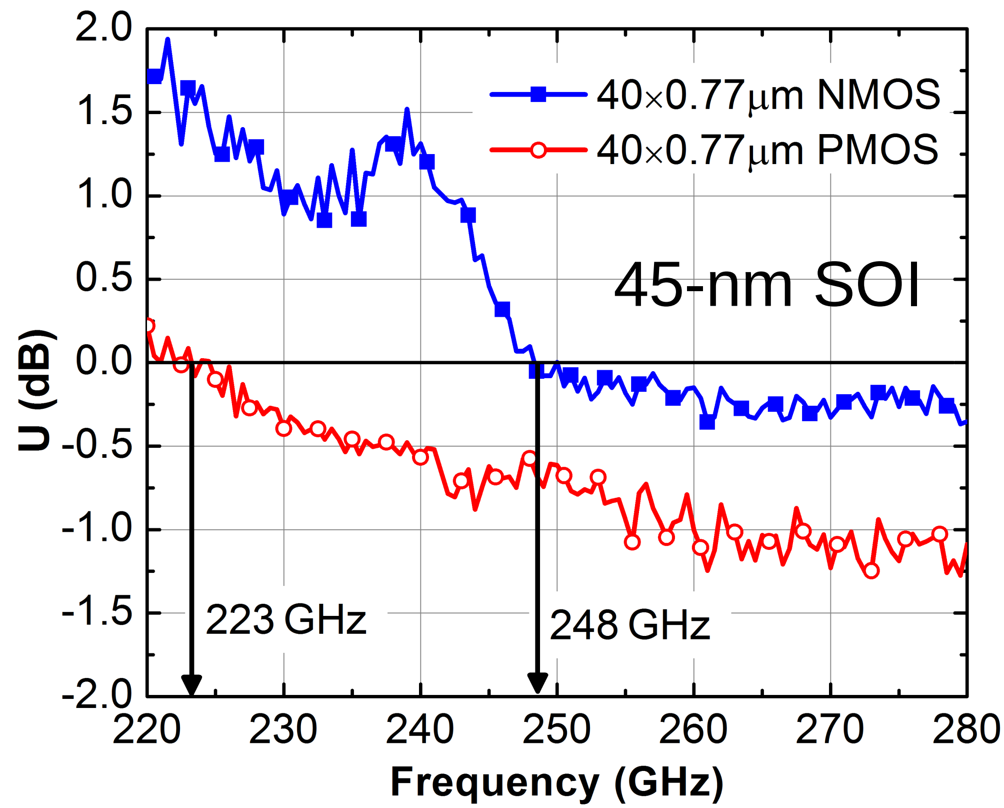
Antenna Efficiency & Bandwidth



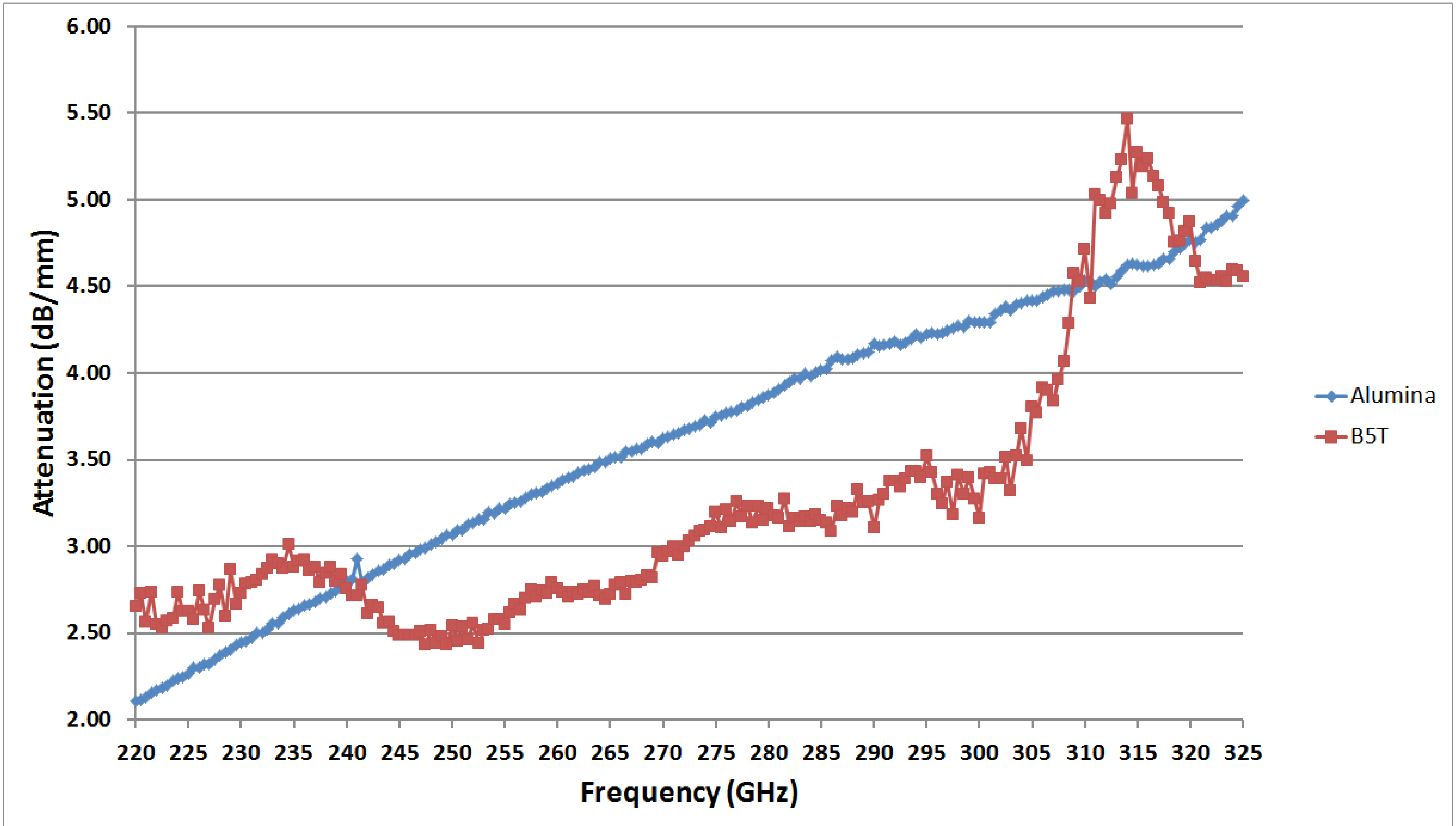


Si Transistor Performance at H-Band





SiGe vs. Alumina µstrip-lines: H-Band



50-GS/s 6-bit Fully Segmented RZ-DAC 3Vpp swing per side

A. Balteanu et al. IMS 2012

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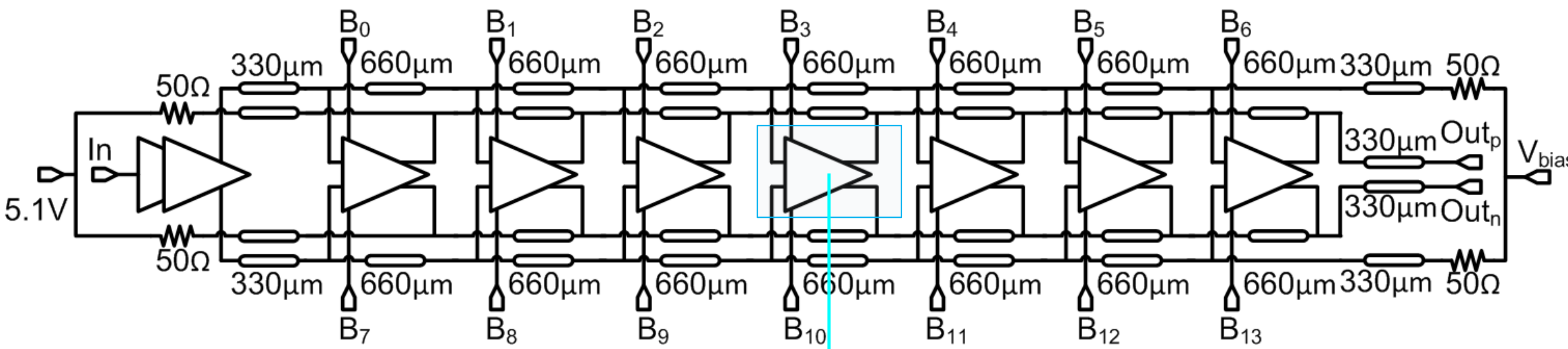
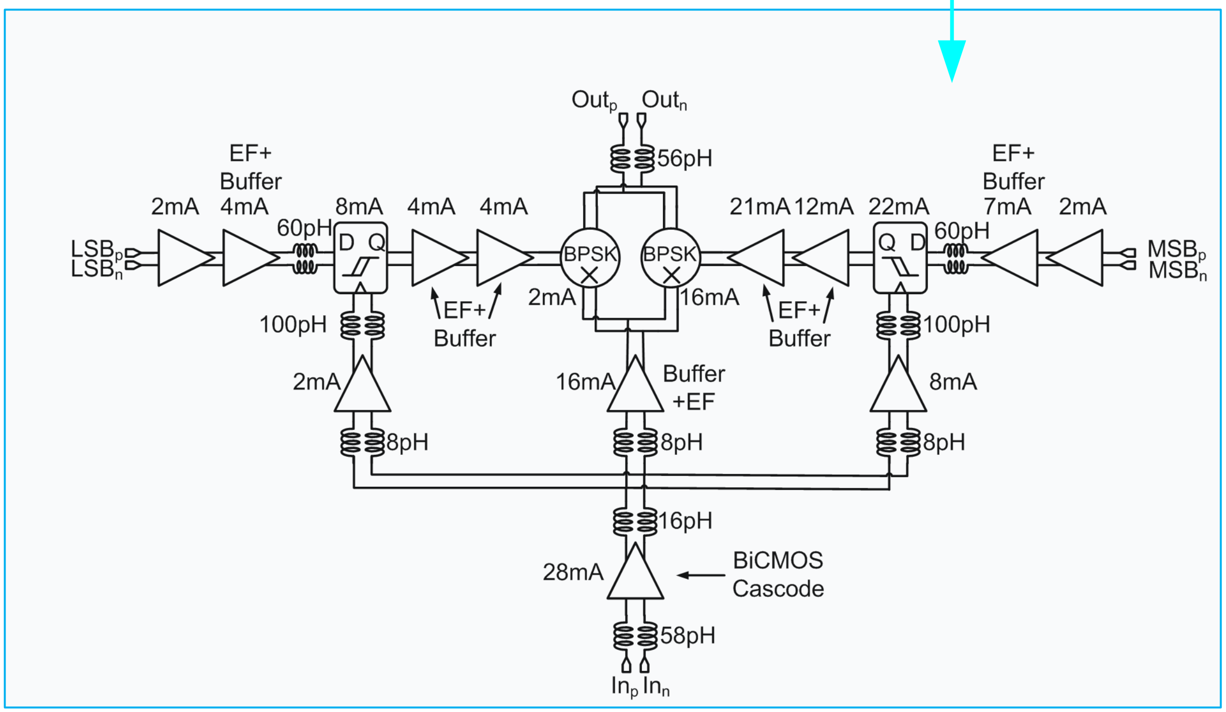
Block Diagram

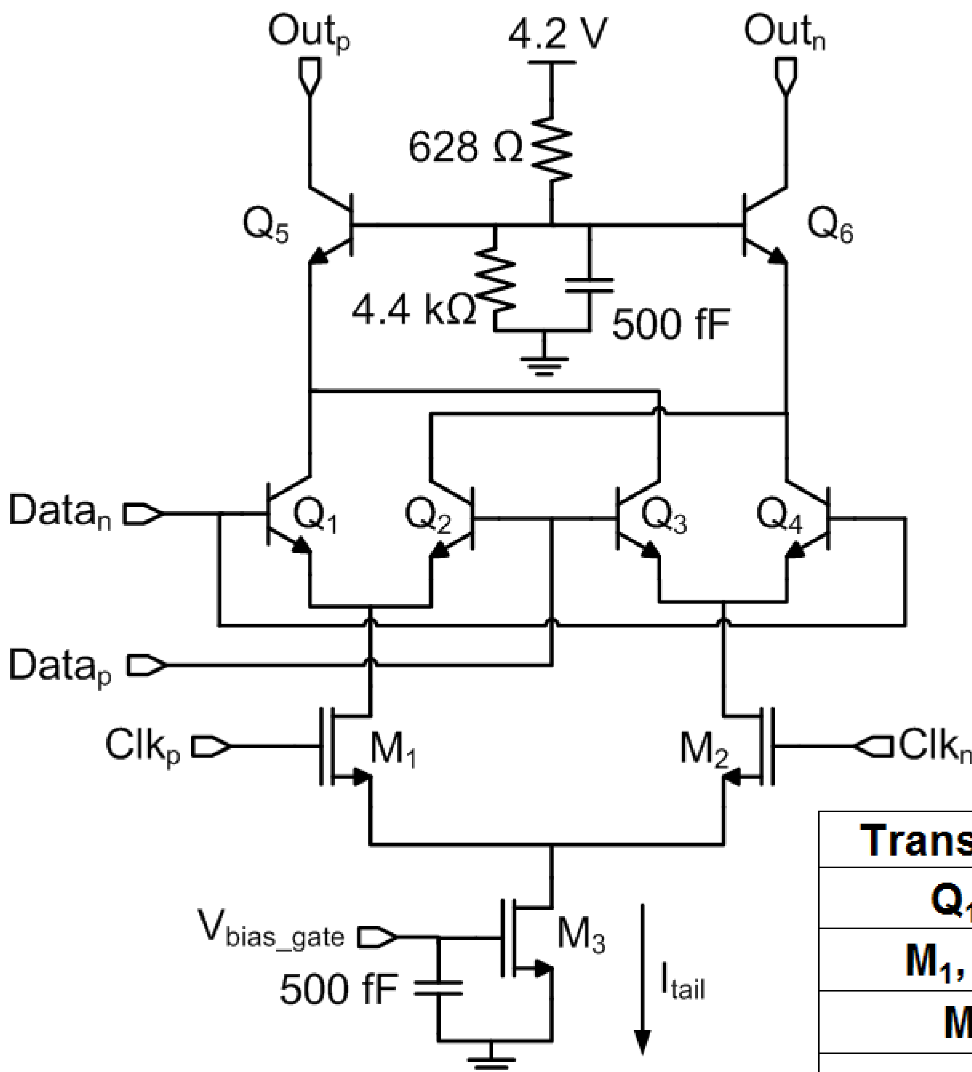




P_{DC} = 5W
Output stage = 1.2W
14 CML bit streams at 50 Gb/s => 3.8W

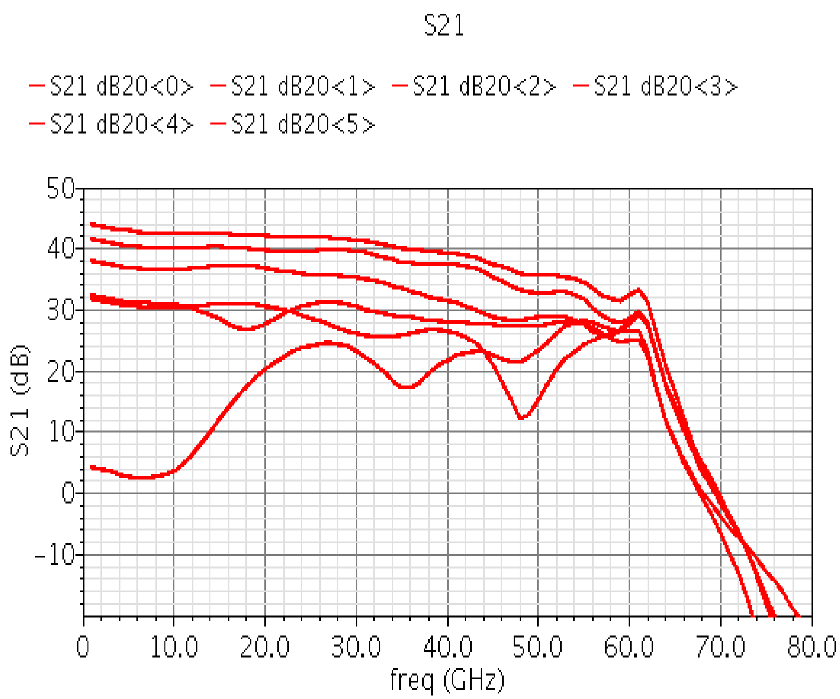
- Distributed Segmentation: 7 MSBs and 7 LSBs in 8:1 size ratio
- Each bit retimed at up to 50 GHz

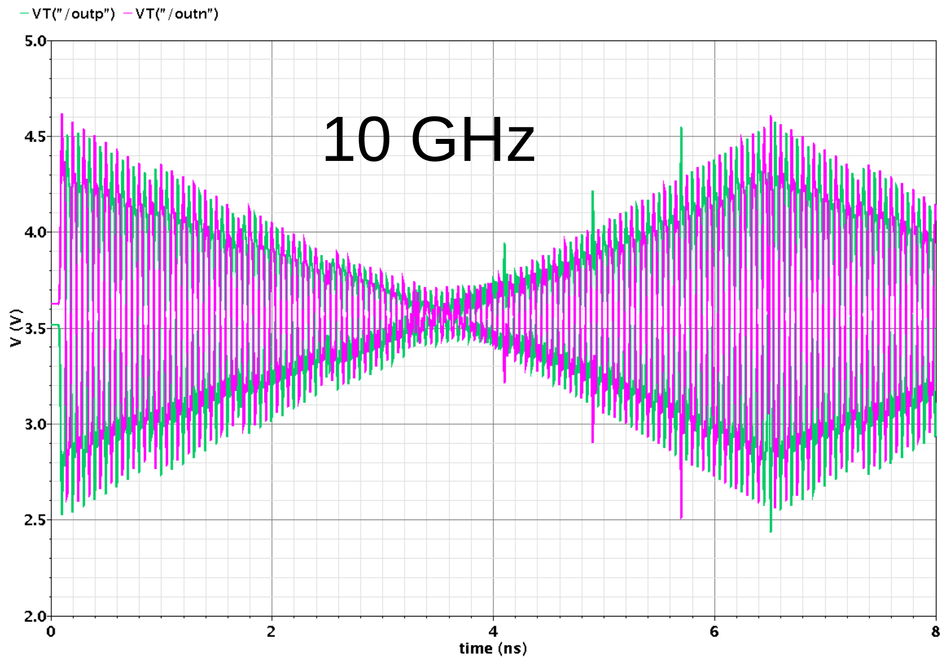
BPSK Cell Schematics

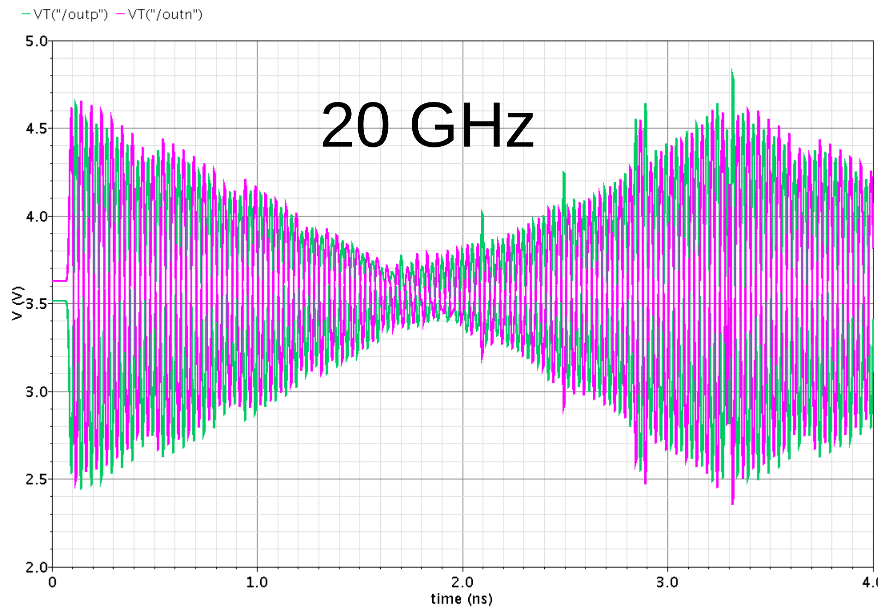


Transistor	LSB	MSB
$Q_{1\text{-}6}$	1 µm	4×2 µm
M_1, M_2	3×2 µm	24×2 µm
M_3	5×4 µm	40×4 µm
I_{tail}	2 mA	16 mA

Distributed Power DAC Simulations (V2)







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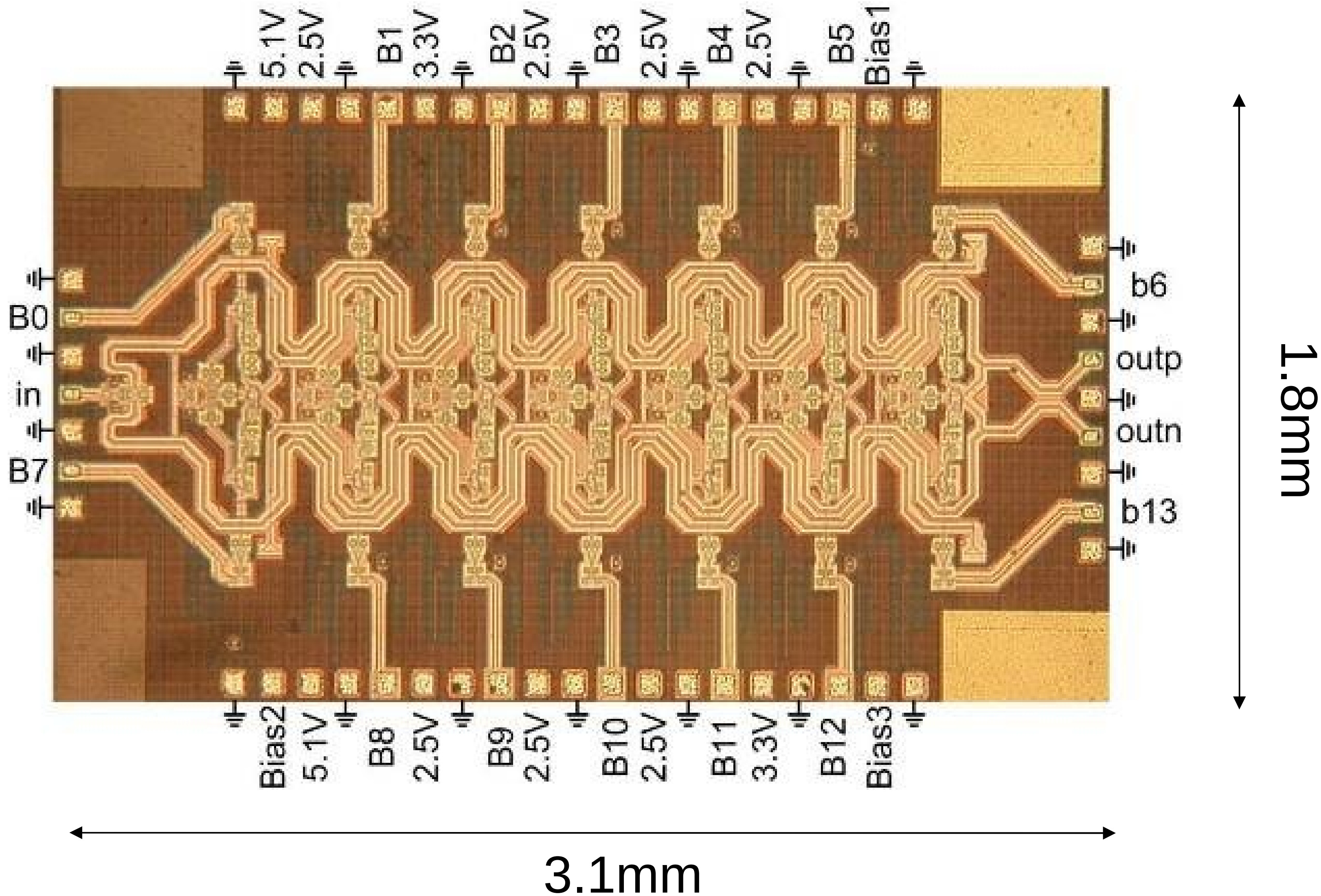
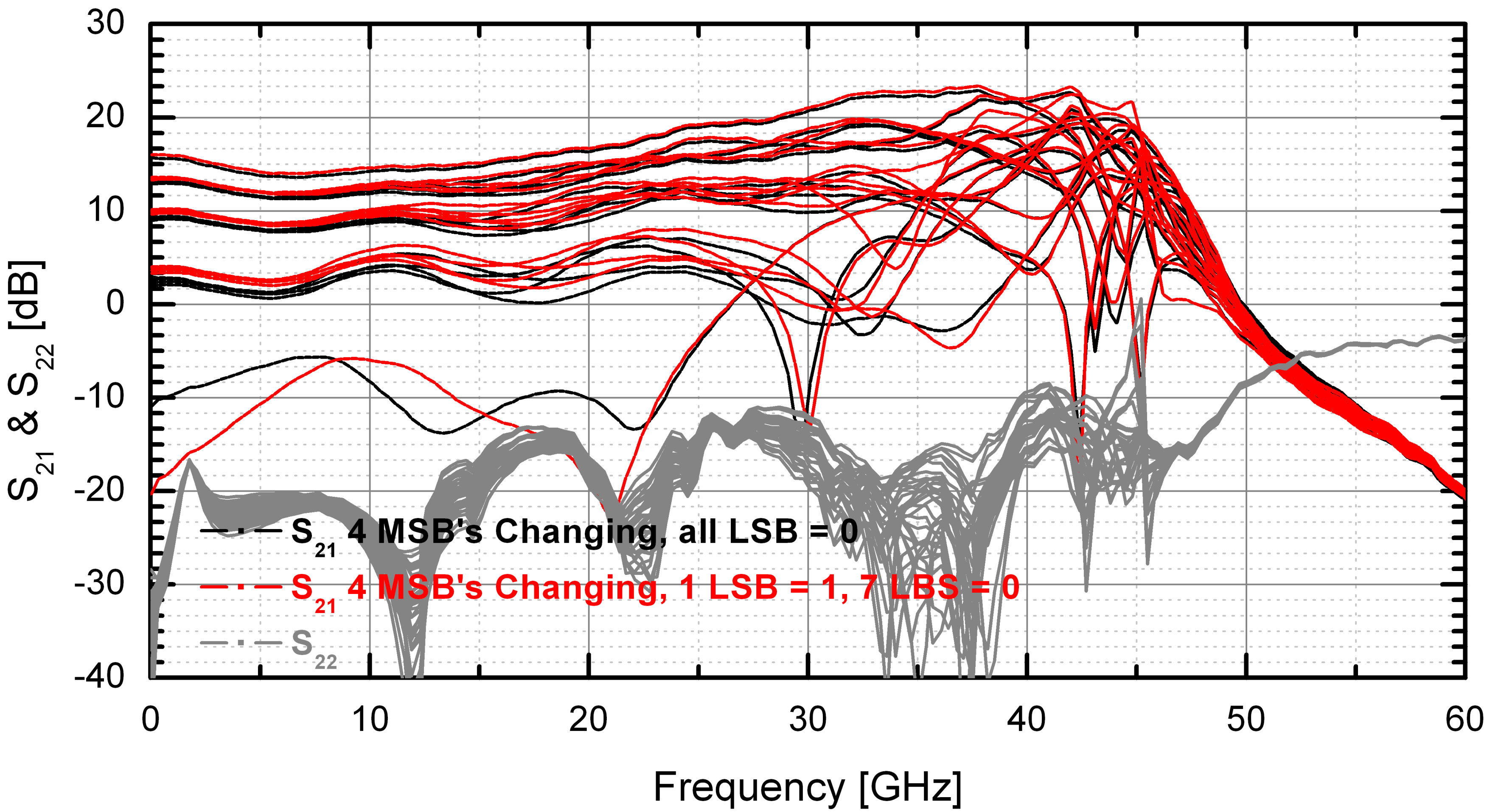
Die Photo (V1)



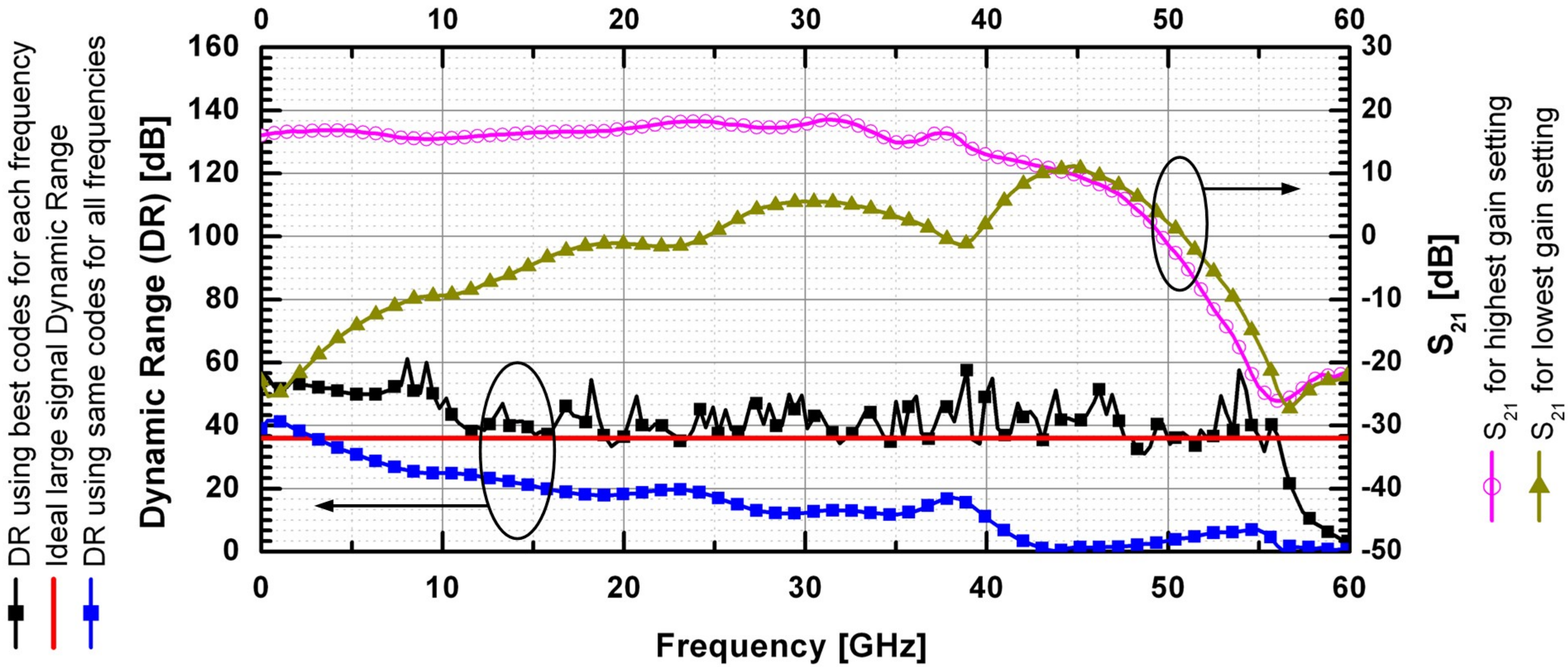
ST's 130-nm SiGe BiCMOS Production Process

f_T/f_{MAX} = 230/280 GHz

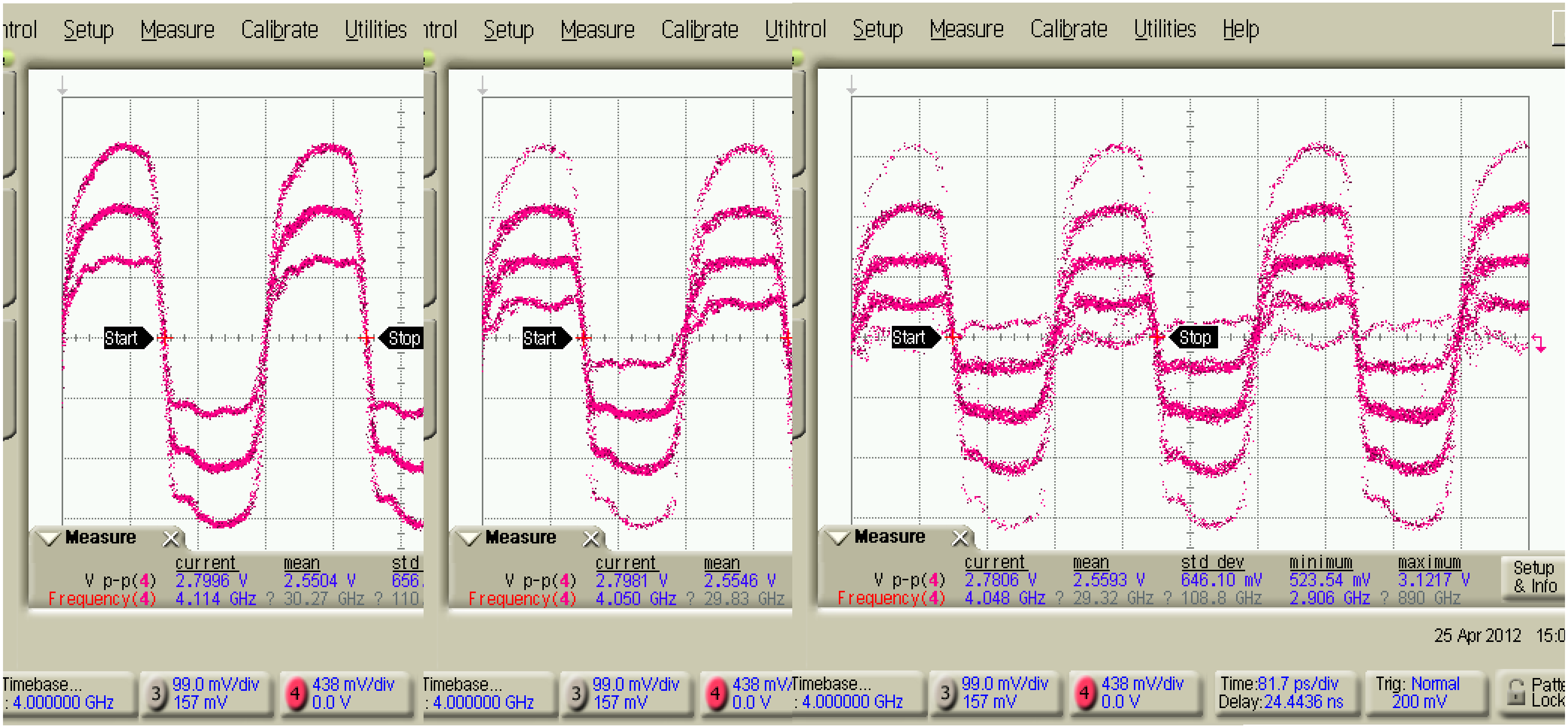
Measured S-parameters (V1)



Dynamic Range from S-parameters (V1)

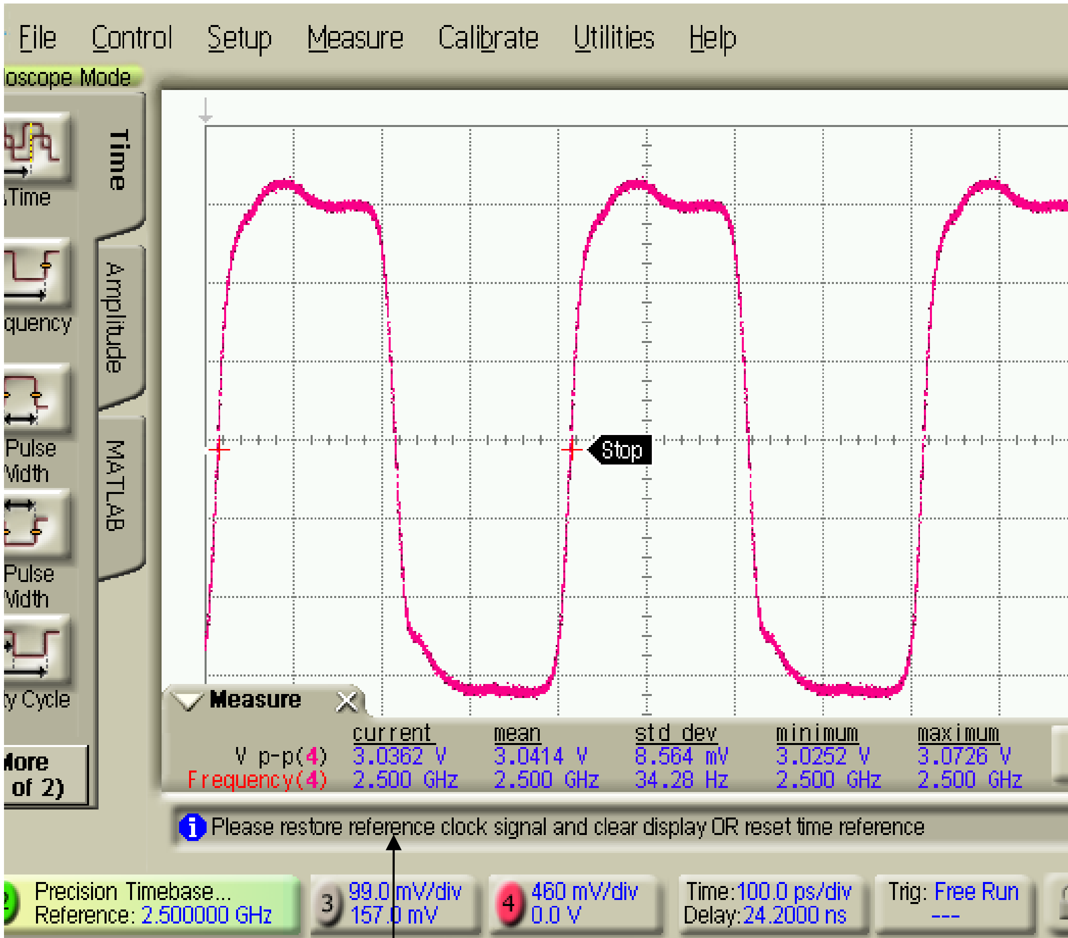


4 GHz large signal: one MSB at a time (V2)

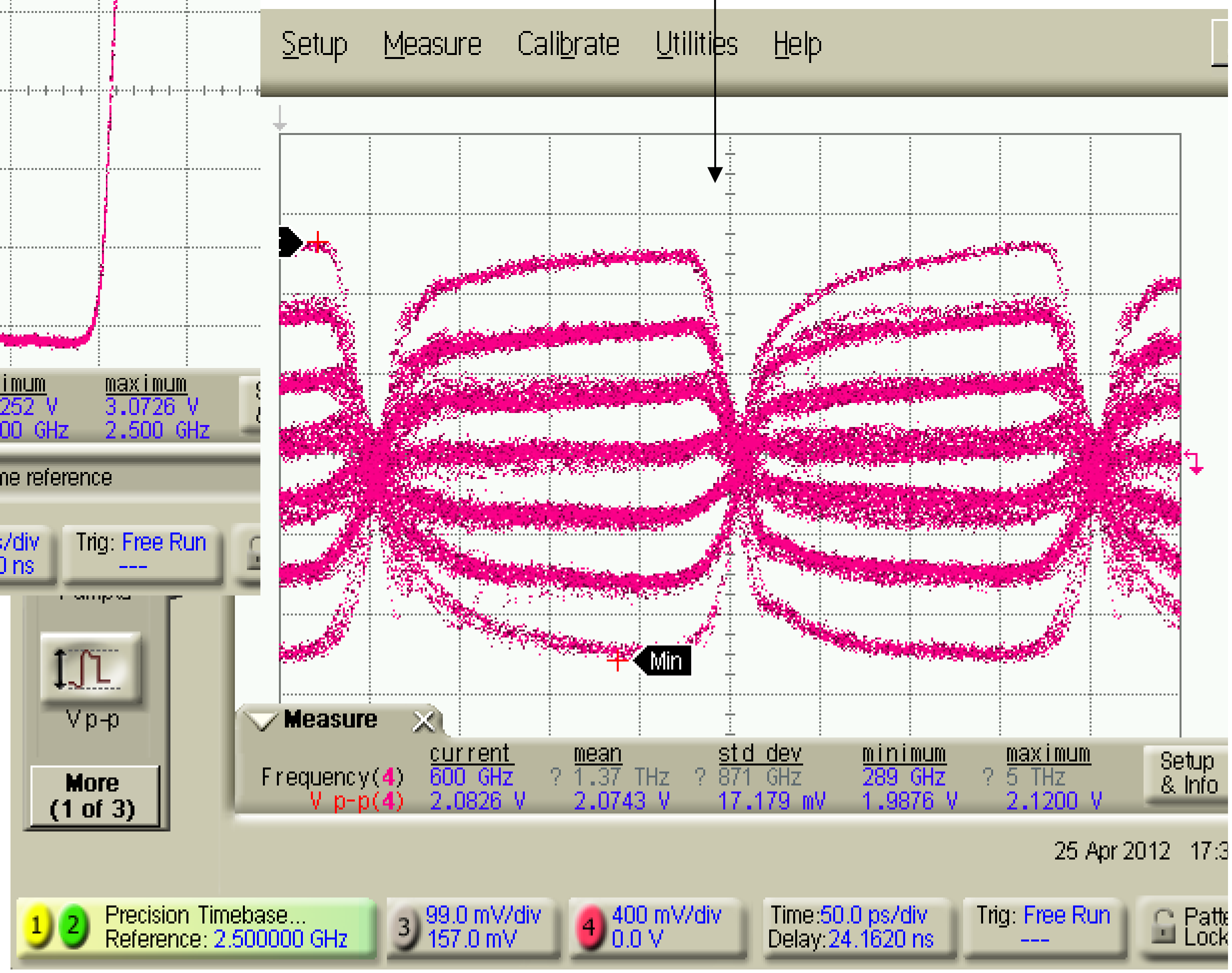


2.8Vpp per side, no de-embedding

2.5 GHz large signal swing (V2)



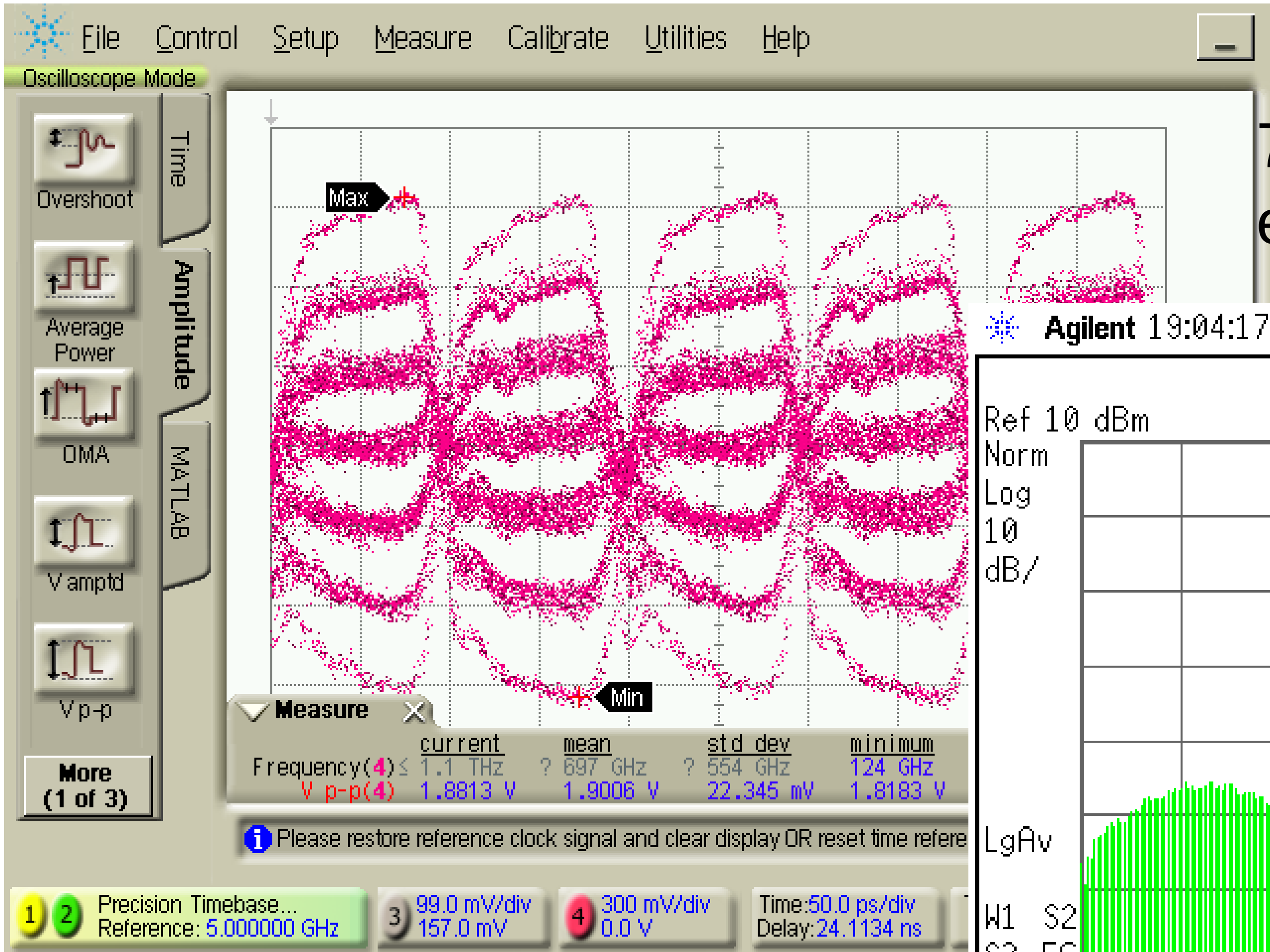
7 MSBs switching at 2.5Gb/s each



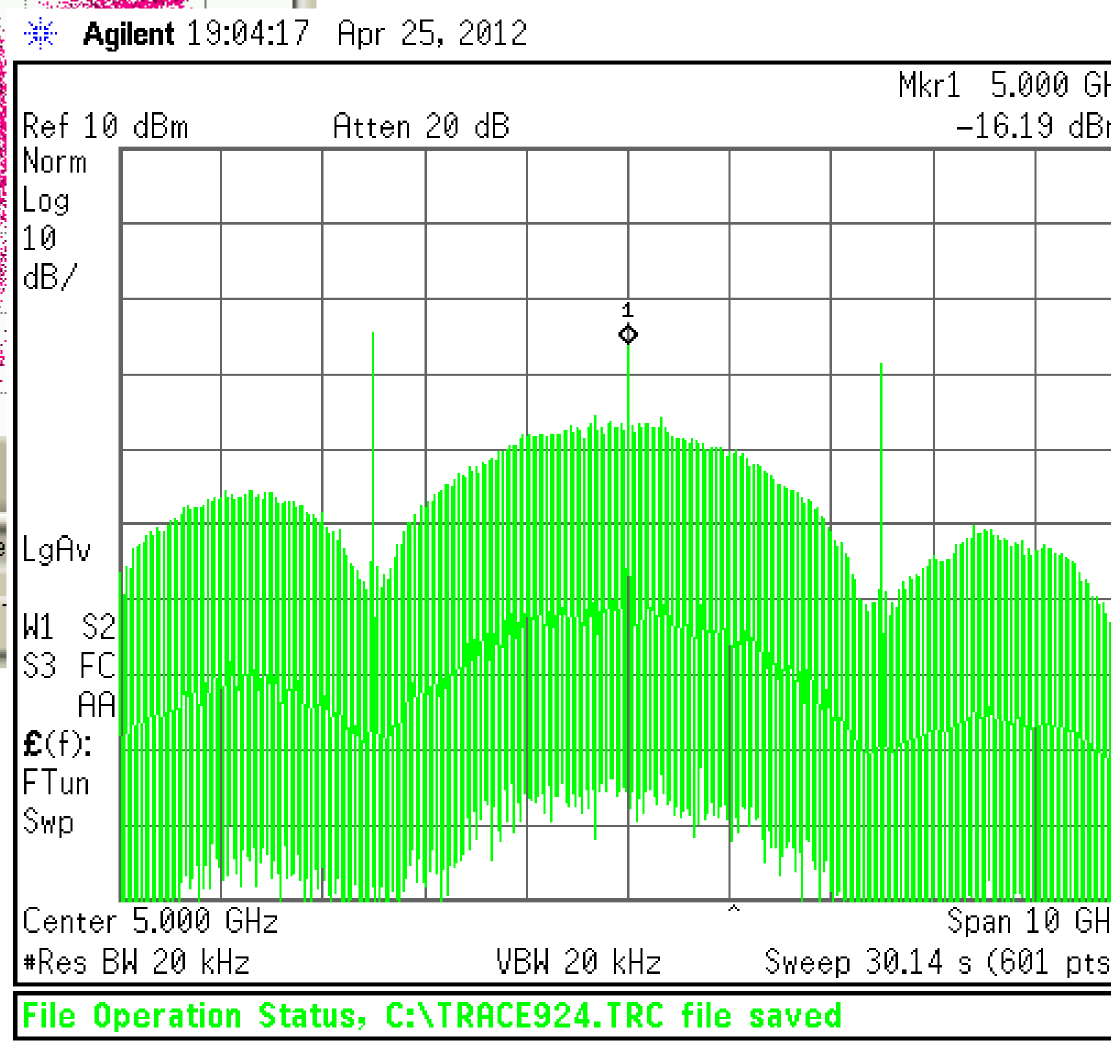
$3V_{pp}$ per side, all 1's

No de-embedding

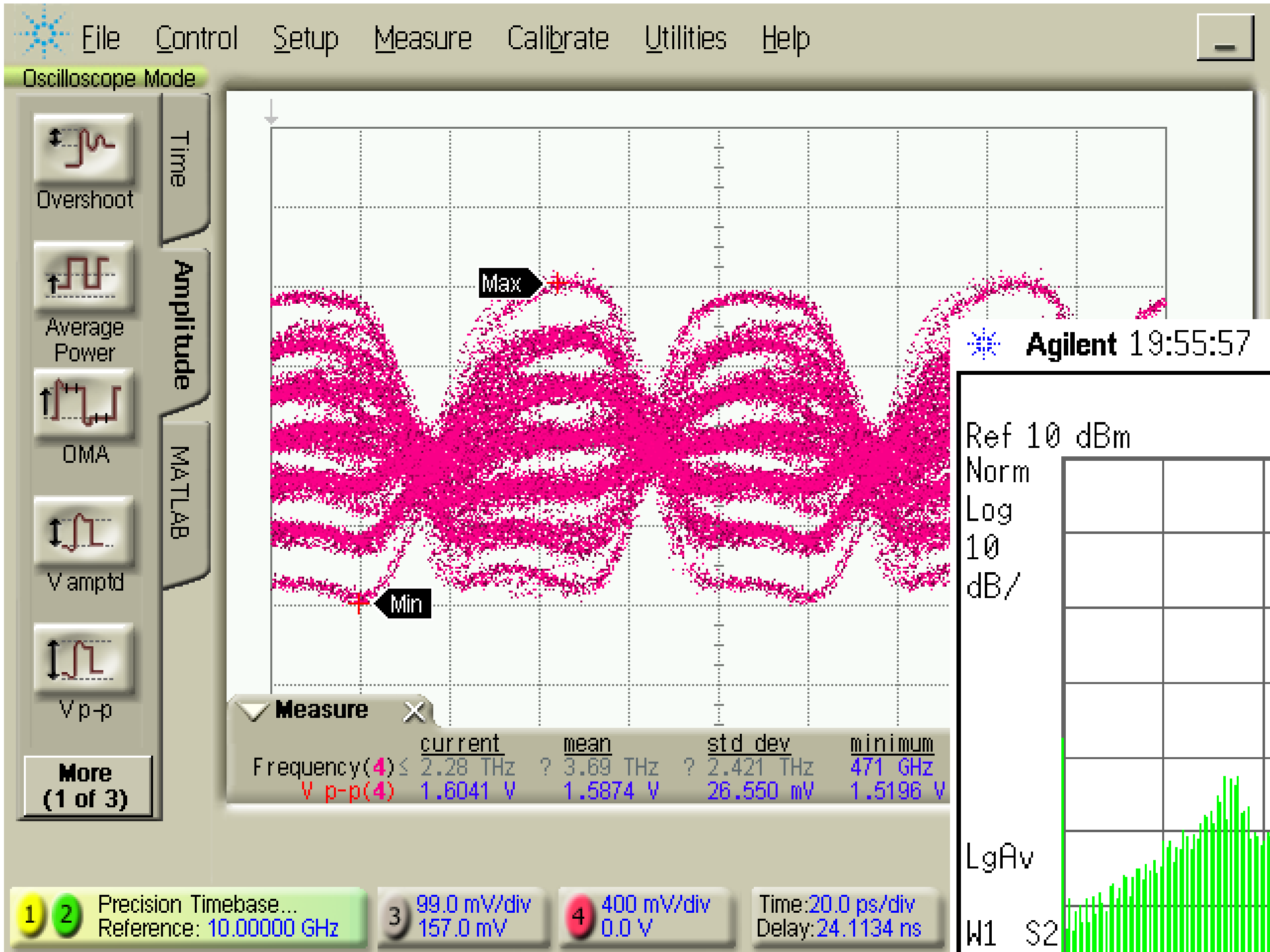
5 GHz large signal swing, spectra (V2)



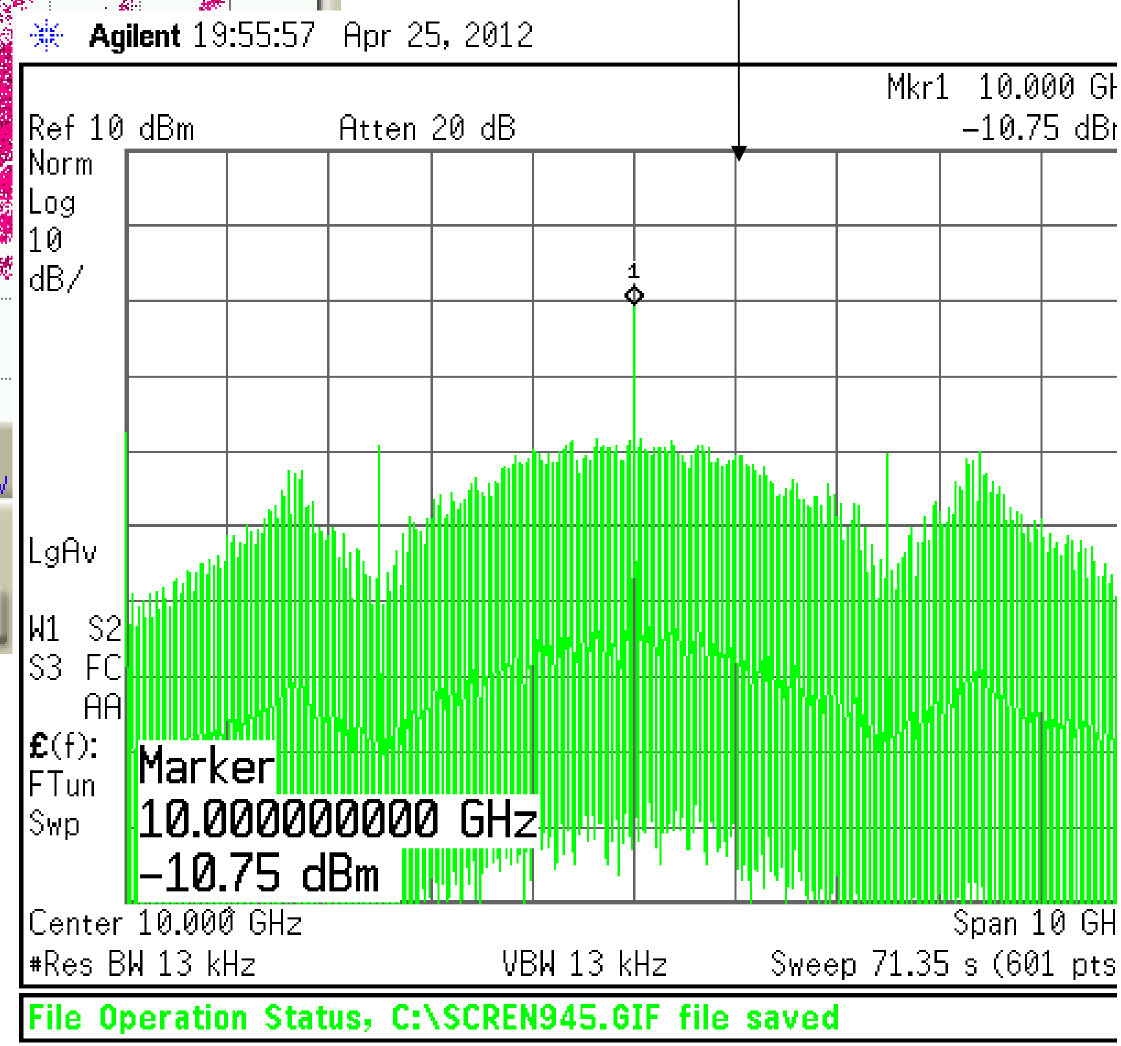
7 MSBs switching at 2.5Gb/s each



10 GHz large signal swing, spectra (V2)

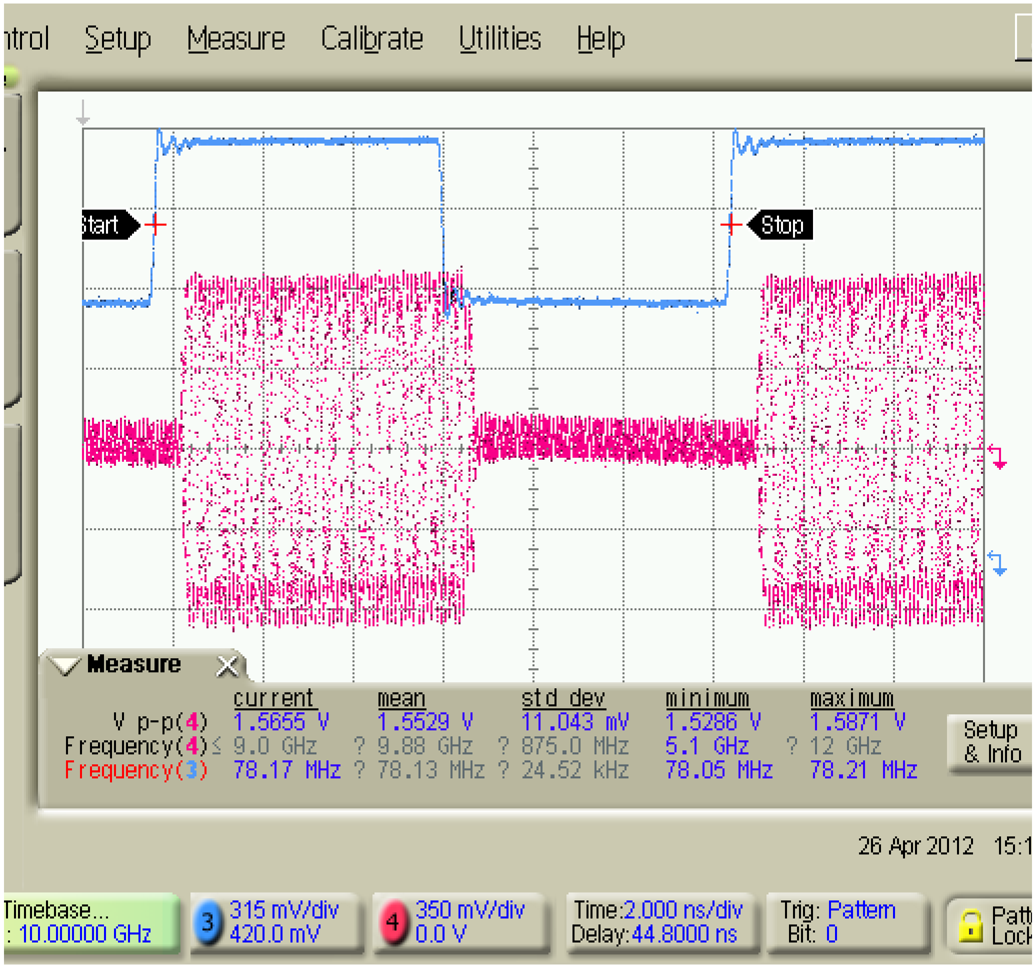


7 MSBs and 5 LSBs switching at 2.5Gb/s each

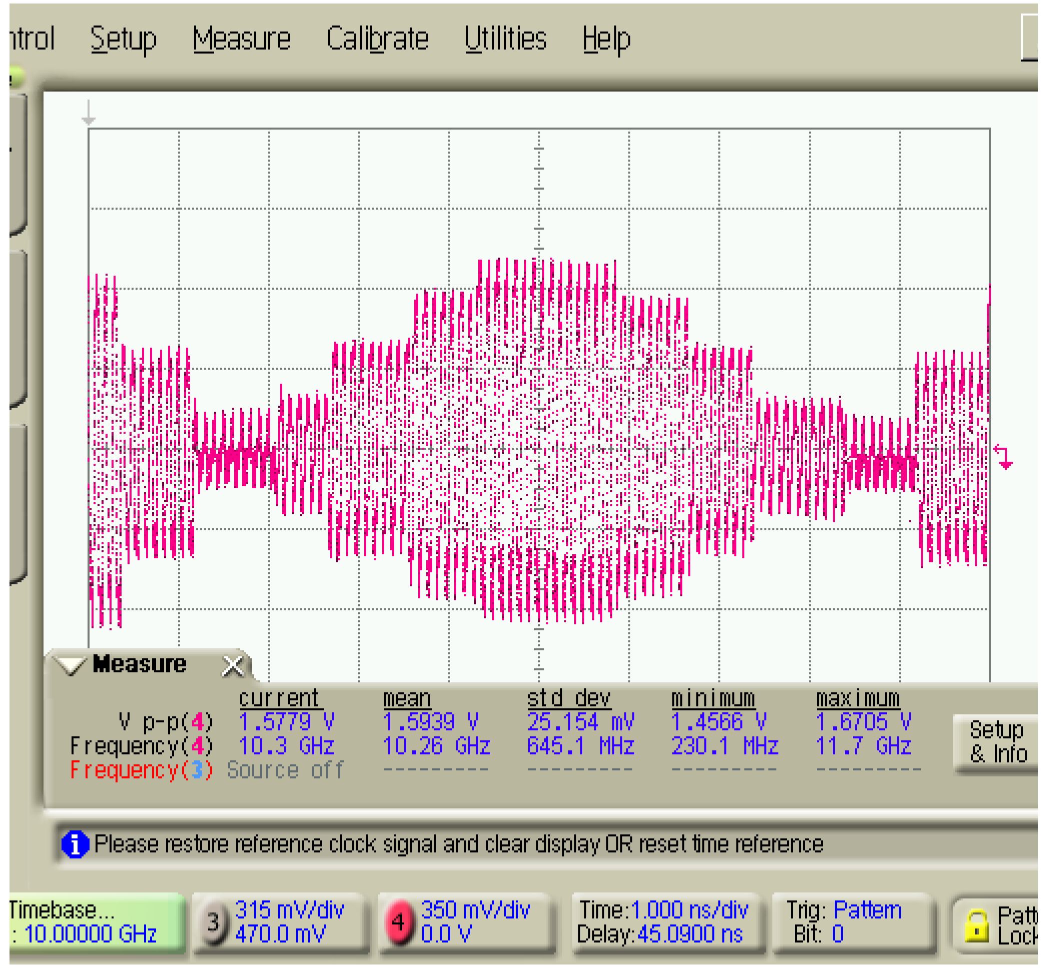


7 MSBs switching at 2.5Gb/s

10 GHz large signal patterns (V2)



On-Off



Sine

20 GHz large signal swing, spectra (V2)

7 MSBs + 5 LSBs switching at 2.5 Gb/s each