ANALYSIS AND DESIGN OF W-BAND PHASE SHIFTERS

BY

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Abstract

This thesis describes 80 – 94 GHz and 70 – 77 GHz interpolating phase shifters and the corresponding transmitter and receiver ICs, fabricated in 65-nm CMOS and SiGe BiCMOS technologies, respectively. Lumped inductors and transformers are employed to realize small-form factor 90° hybrids as needed in high density phased arrays. The CMOS transmitter exhibits absolute phase and amplitude errors of 4° and 4 dB, respectively, at 90 GHz, when the phase is varied from 0° to 360° in steps of 22.5°. The absolute phase error in the SiGe BiCMOS receiver is less than 5°, with a maximum gain imbalance below 3 dB at 74 GHz. The peak gain and power consumption are 3.8 dB and 142 mW from 1.2 V supply for the CMOS transmitter, and 17 dB and 128 mW from 1.5 V and 2.5 V supplies for the SiGe BiCMOS receiver.
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The scaling of CMOS and SiGe BiCMOS technologies into the nanometer regime pushed their cut-off frequencies well above 200GHz. This fact allowed engineers to develop wireless transceivers that operate deep inside the mm-wave frequency range. This range offers plenty of opportunities for new application such as high data rate wireless communications, commercial radars and imagers. Among the numerous examples of proposed systems in the literature, as of now, there are at least two fully developed products, a SiGe HBT 77GHz automotive radar [1] and a CMOS 60GHz wireless communication transceiver array [2].

The advantage of the compact size of mm-wave transceivers and antennas, as compared with their lower frequency versions, could be further exploited in order to realize phased arrays. Phased arrays are formed by combining the inputs and outputs of multiple transmitters and receivers, resulting in a combined antenna pattern. Most importantly, the array pattern can be electronically steered if a phase shifter is inserted in the transmitter and receiver chain.

Phased arrays and electronic beam steering have been traditionally utilized in radar systems [3], where it is necessary to illuminate a distant target with a very narrow beam of high power in order to determine its position accurately. Recently, new applications have been explored, including short range wireless data communications [2], satellite communications [4] and automotive radar [1, 5].

Another interesting application which is of particular importance for this thesis is spatial power combining [3, 6], where the output power of several transmitters in a phased array configuration can be combined in free space. The need for spatial power combining is exacerbated in the case of mm-wave transceivers in nanoscale CMOS, where the need for low supply operation poses fundamental limitations in the maximum available output power. The problem can be alleviated if the output power of several low output power transmitters is combined.
1.1. Phased Arrays

Consider the system of Figure 1.1a. The signals from the antennas can be combined by appropriately spacing them and arranging the corresponding phase shifts. The resulting antenna can have various properties, depending on the system; most importantly, the main lobe of the antenna can be electronically steered in a desired direction. The same idea applies to both receiving and transmitting arrays.

A simple array case is when the phase shifts in the one dimensional, linear, $N$-element array of Figure 1.1a are progressively increased as: $0$, $\Delta \phi$, $2\Delta \phi$, $\ldots$, $N\Delta \phi$. Assuming that the elements are ideal isotropic antennas, the rotationally-symmetric radiation pattern of the resulting system is given by [7]:

$$F = \sum_{n=1}^{N} e^{j(n-1)\psi} \approx \frac{\sin\left(\frac{N}{2} \psi\right)}{\psi}$$

where $k = 2\pi/\lambda$, $d$ is the antenna spacing and $\theta$ is the angle perpendicular to the array axis. The radiation pattern maximum occurs at:

$$\theta_m = \cos^{-1}\left(\frac{\lambda \Delta \phi}{2\pi d}\right)$$

Figure 1.2a illustrates the antenna array directivity patterns when $\Delta \phi = 0^\circ, 45^\circ, 90^\circ$. The patterns correspond to a linear array of $N = 15$ isotropic radiators, placed on the $z$-axis, where the inter-element spacing is $d = \lambda/4$. As seen in the figure, the radiation pattern can be changed based on the applied phase shift. As a result, it is possible to receive or transmit from a desired direction that is chosen by setting the appropriate phase shift to the phase shifters. The same principle with slightly more complicated mathematics [7] applies in the case of a two dimen-
1.1 Phased Arrays

\[ \Delta \phi = 0^\circ \]
\[ \Delta \phi = 45^\circ \]
\[ \Delta \phi = 90^\circ \]

(a) 1-D Array directivity patterns. The linear array lies on the z-axis.

\[ \Delta \phi_{xy} = 0^\circ \]
\[ \Delta \phi_{xy} = 45^\circ \]
\[ \Delta \phi_{xy} = -45^\circ \]

(b) 2-D Array directivity patterns. The array lies on the xy-plane.

Figure 1.2: One and two dimensional array directivity patterns.

There are two fundamental limitations in the phased array implementation of figure 1.1a. First, the constant-phase phase shifters presented in the previous section can, at most, generate a phase shift between 0° and 360°. However, the most common array topologies require a progressive phase shift between the elements of the form 0, \( \Delta \phi \), \( 2\Delta \phi \), \ldots \( N\Delta \phi \). As a result, the phase shift of the elements that exceed 360° must be truncated by \( k \cdot 360^\circ \) in order to be brought back into the 0° − 360° range. Second, as can be seen in equation (1.2), the radiation pattern maximum depends on the wavelength \( \lambda \) when \( d \) is constant. Therefore, for a constant \( \Delta \phi \) over frequency, the array pattern will not be constant over the bandwidth of operation. These two limitations result in an overall constraint over the bandwidth of operation of the array. Moreover, this bandwidth constraint gets more severe as the number of elements in the array increases [4].

In case the bandwidth limitation needs to be avoided, or in case the number of elements is very large and the bandwidth constraint cannot be met, the architecture of Figure 1.1b could be considered. If the constant-phase phase shifters are replaced with true time delay phase...
shifters, equation 1.2 becomes:

\[ \theta_m = \cos^{-1} \left( \frac{\lambda 2\pi f \Delta \tau}{2\pi d} \right) = \cos^{-1} \left( \frac{c \Delta \tau}{d} \right) \]  

(1.3)

Therefore, when the constant-phase phase shift is replaced with a fixed time delay, the pattern maximum does not depend on the frequency of operation and the bandwidth limitation problem is alleviated. Nevertheless, the phase truncation issue is now converted to a time delay truncation issue since it is very expensive to realize a phase shifter that can create very long time delays.

### 1.2. Objective of Thesis

There are two mm-wave bands that are particularly interesting for radar and imaging applications. First, the 76 – 77GHz band allocated for collision avoidance automotive radar \([1, 8]\) and the 94GHz band allocated for radar and imaging of concealed weapons. Both applications would ultimately require a phased-array for proper operation.

It is obvious from phased array theory, that was briefly presented in section 1.1, that a phase shifter is an essential component if electronic beam steering is required. The purpose of this thesis is to develop phase shifters for these two applications and in two different integrated circuit process technologies. Moreover, by utilizing these two phase shifters, a 94GHz 65-nm CMOS transmitter and a 77GHz SiGe BiCMOS receiver with phase shifting are developed. Both the receiver and transmitter can be integrated in an array configuration as illustrated in figure 1.3.

There are two main design objectives for the phase shifters, apart from their frequency
1.3 Technology Overview and mm-wave Circuit Design Aspects

Two technologies were utilized for the circuits developed in this work, both provided by STMicroelectronics. A 130-nm SiGe BiCMOS [9] process and a 65-nm CMOS process.

STMicroelectronics’ 130-nm SiGe BiCMOS (BICMOS9MW) is a dedicated, all-copper, millimeter-wave process. It features two thick metal metallization layers, intended for low-loss transmission lines and inductors, and high quality factor Alucap MIM (Metal-Insulator-Metal) capacitors. The HBT transistors achieve $f_T$ of 240GHz and $f_{MAX}$ 270 GHz. The current density that yields the maximum power gain at each frequency is 1.4mA per micron of emitter length. The measured HBT Maximum Available Gain (MAG) at 77GHz is above 9dB. The 130-nm n-MOSFET devices feature $f_T/f_{MAX}$ of 85/95 GHz when biased at 0.3 mA per micron of gate width, and the $V_{DS}$ voltage is 1.2V

STMicroelectronics’ standard 65-nm CMOS process features 7-layer Cu back-end, as well as MIM capacitors. Both LP and GP transistors are available on the same die. However, because GP transistors exhibit 20-30% higher $g_m$ and $f_T$, and lower $V_T$, they were used exclusively in all circuits. The General Purpose (GP) NMOS transistors exhibit peak $f_T$ of 180GHz when biased at 0.3mA to 0.35mA per gate width, with $V_{DS} = 0.7$V, while their MAG is 8dB at 94GHz.

In the circuits presented in this thesis, all transistors are biased at their peak $f_{MAX}$ current densities in order to obtain as much gain as possible out of them [10, 11]. The only exception is the first two 77GHz low noise amplifier stages that are biased at slightly lower current for optimum noise figure. In all NMOS transistors, the finger width is 1\( \mu \)m while the drawn emitter width of all HBTs is 0.13\( \mu \)m. In addition, all passive components are realized using lumped inductors and transformers as described in [11, 12].
Chapter 2

2.1. Introduction

This chapter reviews the theory of high-frequency phase shifters. It starts with a formal definition of the phase shifter as a circuit building block. Then, the different microwave phase shifter topologies that can be realized in standard integrated circuit form are presented and analyzed. An attempt is made to present the main advantages and disadvantages of each topology. Phase shifter topologies involving ferrites, Surface Acoustic Wave devices, exotic dielectrics and optics will not be analyzed in this work.

Almost all topologies were first proposed and analyzed between 1955 – 1975. During this period the Cold War was at its peak and there was a demand of accurate, long range (i.e. high power) radars. This demand drove the microwave engineers to innovate, notably in digitally controlled phase shifters, utilizing mainly PIN diodes [13–16]. The interest in microwave and mm-wave phase shifters was revived recently due to the application of phased arrays in commercial radars (i.e. 24GHz and 77GHz automotive radars), radios (60GHz radios) as well as low cost military (Q, X, K, Ka and Ku band) radars.

2.2. Definition and Categorization

Throughout this work, an ideal phase shifter will be defined through its scattering parameter matrix as:

\[
S = \begin{bmatrix}
0 & A e^{-j\phi} \\
A e^{-j\phi} & 0
\end{bmatrix}
\]  

(2.1)

where \(A\) is the gain of the phase shifter and \(\phi\) is the applied phase shift. The purpose of the phase shifter is to change the phase of the signal applied at its input in a known and well defined manner. If \(\phi\) is constant then the phase shifter is a Fixed Phase Shifter [17]. If \(\phi\) can be varied though an external control signal then the phase shifter is a Tunable Phase Shifter. Ideally,
the gain of a tunable phase shifter remains constant when the phase shift varies. Nevertheless, based on the application, small variations of the gain can be tolerated. It should be noted that the generic definition (2.1) applies only to reciprocal phase shifters. There are certain types of non-reciprocal shifters that can be represented by a slight modification of (2.1).

Based on how the phase shift can be controlled, two major categories can be distinguished:

- Continuous phase shifters. These shifters can vary the phase of the input signal in a certain range \([\phi_{\text{min}}, \phi_{\text{max}}]\) in a continuous way. I.e. every phase within the range \([\phi_{\text{min}}, \phi_{\text{max}}]\) can be obtained when the control voltages are set appropriately.

- Digital phase shifters. These shifters can only apply certain phase shift values \(\phi_1, \phi_2, \cdots, \phi_n\) to the input signal. Usually, the phase shift is controlled by setting the corresponding control bits.

There are two other major phase shifter categories that are not immediately apparent from equation (2.1). The equation can be modified so that it expresses the scattering parameter matrix over frequency:

\[
S(\omega) = \begin{bmatrix}
0 & A(\omega) e^{-j\phi(\omega)} \\
A(\omega) e^{-j\phi(\omega)} & 0
\end{bmatrix}
\]  

(2.2)

As a result, based on the frequency variation of the phase shift, the following two categories could be specified:

- Constant phase type phase shifters. These shifters apply a constant phase shift over frequency to the input signal, i.e. \(\phi(\omega) = \phi_0\) (Figure 2.1a).
2.3 Digital Phase Shifters

- Constant time delay type phase shifters (or True Time Delay (TTD) phase shifters). These phase shifters apply a constant time delay to the input signal: \( \phi(\omega) = \omega \cdot \Delta t \). I.e, the phase varied linearly with respect to frequency (Figure 2.1b).

In both categories, the gain is required to remain constant over frequency: \( A(\omega) = A_0 \). Since \( \phi = \omega \Delta t \), the two phase shifter types are equivalent over a narrow bandwidth. As presented in the introduction, constant time delay phase shifting is highly desirable for phased arrays, which constitutes the major application of phase shifters.

2.3. Digital Phase Shifters

This section discusses and compares different digital phase shifter architectures. First the various methods of creating a phase shift bit are presented. Then, two ways of creating a multi-bit phase shifter will be shown.

2.3.1. Switched Line Phase Shifter

In the Switched Line Phase Shifter, it is possible to switch between two different time delays, realized with transmission lines, as illustrated in Figure 2.2. The time delay of a transmission line of length \( l_0 \) is \( \tau_D = \frac{2\pi l_0}{v_p} \), where \( v_p \) is the phase velocity of the guided wave. As a result, the time delay of the two states is given by

\[
\Delta \tau = \frac{2\pi l}{v_p}
\]

(2.3)

where \( l \) is the length difference between the two transmission lines.

The major advantage of the switched line phase shifter is that it can realize variable time
Phase Shifter Architectures

2.3.2. Reflection Type Phase Shifter

A reflection type phase shifter takes advantage of the directional properties of a 3-dB hybrid coupler as shown in Fig 2.3a or of a circulator as depicted in Figure 2.3b. In the hybrid coupler case, the signal enters at the input port and splits into two equal parts. These two parts, based on the state of the switch, are either reflected back and recombine at the output port or travel on the $l/2$ transmission line and are then reflected back, traveling further $l/2$ length before being recombined. Since the total traveled length is $l$, the time delay that the signal is subject to is provided by equation (2.3).

The advantages and disadvantages of this phase shifter are similar to the switched line case. However, there is additional loss stemming from the hybrid coupler or the circulator. The advantage of using a hybrid or circulator is the fact that the input and output ports are better matched to the desired impedance since these structures have high isolation between their ports.
2.3 Digital Phase Shifters

2.3.3. Loaded Line Phase Shifter

The loaded line phase shifter is composed of a quarter wavelength transmission line which has its both ends terminated to either an inductive or a capacitive load, as shown in Figure 2.4. The resulting network can be easily analyzed using the ABCD transmission matrix formulation:

\[
T = \begin{bmatrix} 1 & 0 \\ jB & 1 \end{bmatrix} \cdot \begin{bmatrix} 0 & jZ_0 \\ jZ_0 & 0 \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ jB & 1 \end{bmatrix} = \begin{bmatrix} -BZ_0 & jZ_0 \\ j(1-B^2Z_0^2)/Z_0 & -BZ_0 \end{bmatrix}
\] (2.4)

Converting to S-parameters, the phase shift between the two states can be calculated as:

\[
\Delta \phi = 2 \tan^{-1}\left(\frac{1}{BZ_0 - \frac{BZ_0}{2}}\right)
\] (2.5)

The magnitude of the input reflection is given by:

\[
|S_{11}| = \sqrt{1 - \frac{1}{1 + (BZ_0)^4/4}}
\] (2.6)

It is clear from equation (2.6) that in the input matching of the phase shifter is never perfect and depends on the desired phase shift. Moreover, the higher the desired phase shift, the poorer the input matching is going to be. This fact renders the loaded line phase shifter useful only for small phase shifts.

2.3.4. High Pass - Low Pass Type Phase Shifter

Consider the Π networks shown in Figures 2.5a–2.5b and the T networks illustrated in Figures 2.5c–2.5d. These three-element networks can create a phase shift of \(-90 < \phi < 90\) at a particular frequency \(\omega_0\) while remaining matched to \(Z_0\), which is necessary cascading several
of these networks. The design equations are provided below [18]:

For the low-pass Π network, $-90 < \phi < 0$ (Figure 2.5a):

\[
L = \frac{Z_0 \sin |\phi|}{\omega_0} \quad (2.7)
\]

\[
C = \frac{\tan |\phi/2|}{\omega_0 Z_0} \quad (2.8)
\]

For the high-pass Π network, $0 < \phi < 90$ (Figure 2.5b):

\[
L = \frac{Z_0 \omega_0 \tan |\phi/2|}{\omega_0 \sin |\phi|} \quad (2.9)
\]

\[
C = \frac{1}{\omega_0 Z_0 \sin |\phi|} \quad (2.10)
\]

For the low-pass T network, $-90 < \phi < 0$ (Figure 2.5c):

\[
L = \frac{Z_0 \tan |\phi/2|}{\omega_0} \quad (2.11)
\]

\[
C = \frac{\sin |\phi|}{\omega_0 Z_0} \quad (2.12)
\]

For the high-pass T network, $0 < \phi < 90$ (Figure 2.5d):

\[
L = \frac{Z_0}{\omega_0 \sin |\phi|} \quad (2.13)
\]

\[
C = \frac{1}{\omega_0 Z_0 \tan |\phi/2|} \quad (2.14)
\]

Two types of phase shifters can be constructed using these networks [16, 18]. The first type switches between one of the networks described above and a bypass line as illustrated in Figures 2.6a – 2.6d. This shifter can produce a relative phase shift $0^\circ < \Delta \phi < 90^\circ$ between its two states. The other type of phase shifter switches between a High-pass and a Low-pass network as illustrated in Figures 2.7a – 2.7b, resulting in a relative phase shift of $0^\circ < \Delta \phi < 180^\circ$.

The high-pass – low-pass phase shifters can result in very compact size when realized in integrated circuit form with spiral inductors and MiM capacitors. Furthermore, the broadband characteristics of the of the T and Π networks allow operation over at least an octave bandwidth [16]. Nevertheless, as mentioned before, the large number of switches utilized requires an advanced CMOS process to minimize the loss at frequencies above 50GHz.
2.3 Digital Phase Shifters

![Network Diagrams](image)

(a) Low-pass Π network.  
(b) High-pass Π network.  
(c) Low-pass T network.  
(d) High-pass T network.

Figure 2.5: Π and T networks.

![Switched Network Diagrams](image)

(a) Switched Low-pass Π – Bypass phase shifter.  
(b) Switched High-pass Π – Bypass phase shifter.  
(c) Switched Low-pass T – Bypass phase shifter.  
(d) Switched High-pass T – Bypass phase shifter.

Figure 2.6: Switched – bypass phase shifters.
2.3.5. Multibit Digital Phase shifters

A simple way to create a multibit digital phase shifter is to cascade a number of single-bit phase shifters. The phase shift that each bit should introduce is decided based on the desired phase shift range and resolution. For example if 360° are required in sixteen, 22.5° steps, the arrangement of Figure 2.8 is possible. In this arrangement, each network switches between 0° and its corresponding phase shift as controlled by bits Bit0 - Bit3. The total phase shift will be given by:

\[ \Delta \phi = 22.5^\circ \times \text{Bit}_0 + 45^\circ \times \text{Bit}_1 + 90^\circ \times \text{Bit}_2 + 180^\circ \times \text{Bit}_3 \]  

(2.15)

The shortcoming of this approach is that the loss of each phase shift bit adds resulting in high loss. For example, in [18] 10dB loss at 30GHz is reported.

A second, distributed approach is depicted in Figure 2.9 and is similar to the one presented in [19]. A transmission line is periodically tapped so that the input signal is delayed by \( \tau_D \) at the input and output of every tap. Only one tap is selected for every state and the corresponding delay for the n\textsuperscript{th} bit is:

\[ \Delta \tau = 2n \tau_D \]  

(2.16)

where \( \tau_D \) is the delay introduced by each transmission line section.

There is a parasitic amplitude modulation resulting from the transmission line loss. The loss when the n\textsuperscript{th} tap is switched is \( 2n \alpha_l \) where \( \alpha_l \) is the loss of each section. Techniques to
2.4 Continuous Phase Shifters

This section discusses and compares different continuous phase shifter architectures. If required, there are several techniques to introduce digital control in these phase shifters. The simplest is to use a multibit DAC at the analog control input.

2.4.1. Analog Reflection Type Phase Shifter

The reflection type phase shifter can be modified by replacing the transmission line load with a reflective, tunable lumped load, as shown in Figure 2.10 [20]. If the load impedance varies from $Z_{L,max}$ to $Z_{L,min}$, the corresponding phase shift can be calculated as:

$$
\Delta \phi = 2 \left[ \tan^{-1} \left( \frac{Z_{L,max}}{Z_0} \right) - \tan^{-1} \left( \frac{Z_{L,min}}{Z_0} \right) \right]
$$

(2.17)

where $Z_0$ is the reference impedance of the hybrid coupler. Since $-90^\circ < \tan^{-1}(x) < 90^\circ$, the maximum attainable phase shift is $180^\circ$. Since the load will always have some series resistance, the phase shifter will exhibit loss, which is predicted by:

$$
|S_{21}| = \alpha^2 \frac{R_L^2 + X_L^2 + Z_0^2 - 2R_LZ_0}{R_L^2 + X_L^2 + Z_0^2 + 2R_LZ_0}
$$

(2.18)

where $\alpha$ is the loss of the hybrid coupler, $R_L$ is the resistive part of $Z_L$ while $X_L$ is the reactance of $Z_L$.

The variable loads are usually realized in integrated circuit form with varactors, L-varactor tanks [20], or $\Pi$ networks [21]. However, because of the low varactor Q factor, the loss of the
analog reflection type phase shifter is usually very high. For example, reference [21] reports 10-12 dB at 24 GHz while [20] reports 5 dB at 6.2 GHz.

2.4.2. Tunable Filter Type Phase Shifter

The Π and T networks presented in figure 2.5 can be made tunable in order to adjust the phase shift that the network introduces. However, both the inductors and the capacitors must change simultaneously in order to preserve the input and output matching of the filter. "Tunable" inductors can be realized by utilizing series capacitors along with a fixed value inductor as illustrated in Figure 2.11 [22] for a Low-pass T network. The variable capacitors can be realized in integrated circuits using varactors.

The reactance of the series $L$ and $C_T$ is:

$$Z_{eq} = j\omega L - \frac{j}{\omega C_T}$$  \hspace{1cm} (2.19)

As a result, at a particular frequency $\omega_0$, $Z_{eq}$ can be represented by an equivalent inductance:

$$L_{eq} = L - \frac{1}{\omega_0^2 C_T}$$  \hspace{1cm} (2.20)

Solving equation (2.11) for $\phi$ yields:

$$|\phi| = 2\tan^{-1}\left(\frac{\omega_0 L_{eq}}{Z_0}\right) = 2\tan^{-1}\left(\frac{\omega_0 L_{eq}}{Z_0} - \frac{1}{\omega_0 C_T Z_0}\right)$$  \hspace{1cm} (2.21)
Assuming that $C_T$ can vary from $C_{T,\text{min}}$ to $C_{T,\text{max}}$, the corresponding phase shift is:

$$|\Delta \phi| = 2 \tan^{-1} \left( \frac{\omega_0 L_{eq}}{Z_0} - \frac{1}{\omega_0 C_{T,\text{max}} Z_0} \right) - 2 \tan^{-1} \left( \frac{\omega_0 L_{eq}}{Z_0} - \frac{1}{\omega_0 C_{T,\text{min}} Z_0} \right)$$

(2.22)

In order to preserve the matching to $Z_0$, $C$ must also vary as:

$$C_{\text{max}} = \frac{\sin |\phi_{\text{max}}|}{\omega_0 Z_0}$$

(2.23)

$$C_{\text{min}} = \frac{\sin |\phi_{\text{min}}|}{\omega_0 Z_0}$$

(2.24)

where,

$$|\phi_{\text{max}}| = 2 \tan^{-1} \left( \frac{\omega_0 L_{eq}}{Z_0} - \frac{1}{\omega_0 C_{T,\text{max}} Z_0} \right)$$

(2.25)

$$|\phi_{\text{min}}| = 2 \tan^{-1} \left( \frac{\omega_0 L_{eq}}{Z_0} - \frac{1}{\omega_0 C_{T,\text{min}} Z_0} \right)$$

(2.26)

The tunable filter phase shifter is very attractive for integrated circuit implementation because of its highly compact size. Nevertheless, the assumption (2.20) is valid only for a 10 - 20 % bandwidth [22]. Furthermore, the attainable phase shift is limited by the varactor capacitance ratio. The loss of the phase shifter is also dominated by the varactor resistance, resulting in high loss as the frequency increases.

### 2.4.3. Periodically Loaded Transmission Line Phase Shifter

The periodically loaded line phase shifter is depicted in figure 2.12 [23] and is composed of a transmission line that is periodically tapped with varactors. By varying the capacitance of the varactors, the characteristics of the resulting synthetic transmission line can also be varied.

The transmission line unit cell is assumed to have characteristic impedance $Z_i$, phase ve-
locity \( v_i \) and length \( l \). The equivalent inductance and capacitance of each section is:

\[
L_t = \frac{I Z_i}{v_i} \tag{2.27}
\]

\[
C_t = \frac{1}{Z_i v_i} \tag{2.28}
\]

The resulting synthetic transmission line’s cut-off frequency is:

\[
f_T = \frac{1}{\pi \sqrt{L_t(C_t + C_V)}} \tag{2.29}
\]

For frequencies below the cut-off frequency, the synthetic transmission line parameters are:

\[
Z_L = \sqrt{\frac{L_t}{C_t + C_V}} \tag{2.30}
\]

\[
v_\phi = \sqrt{\frac{l}{L_t(C_t + C_V)}} \tag{2.31}
\]

The loading factor of the transmission line is defined as

\[
x = \frac{C_{V,\text{max}}}{C_t} \tag{2.32}
\]

whereas the ratio of the minimum to maximum varactor capacitance is also defined as:

\[
y = \frac{C_{V,\text{min}}}{C_{V,\text{max}}} \tag{2.33}
\]

Assuming that the characteristic impedance of the synthetic line is required to be 50Ω when \( C_V = C_{V,\text{max}} \), the phase shift per each section is [23]:

\[
\Delta \phi = 2\pi f \frac{l}{v_i} \left( \sqrt{1 + x} - \sqrt{1 + xy} \right) \tag{2.34}
\]

The above formula is valid under the assumption that \( f < < f_T \). Since \( \tau_D = -\frac{d\phi}{d\omega} \), the periodically loaded line phase shifter in fact creates time delay as long as \( f < < f_T \):

\[
\Delta \tau = \frac{l}{v_i} \left( \sqrt{1 + x} - \sqrt{1 + xy} \right) \tag{2.35}
\]

If the sections of length \( l \) are assumed to be lossless, the insertion loss due to the varactors
2.4 Continuous Phase Shifters

is [23]:

\[ \text{IL} = n_{\text{section}} \pi \frac{f}{f_s} Z_L \]  \hspace{1cm} (2.36)

where \( n_{\text{section}} \) is the number of sections and \( f_s \) is the varactor cut-off frequency:

\[ f_s = \frac{1}{2 \pi r_i C_{V,\text{max}}} \]  \hspace{1cm} (2.37)

where \( r_i \) is the varactor series resistance.

The periodically loaded line phase shifter can achieve 360° of phase shift with a moderate number of sections. Moreover, if designed properly [23], the transmission line loss could be minimized. Nevertheless, as with many other phase shifter topologies suggested up to now, the low quality factors of the varactors at mm-wave frequencies overwhelms the loss and renders the phase shifter impractical for this frequency range.

2.4.4. Dual Gate FET Type Phase Shifter

The dual gate FET type phase shifter originates from dual gate MESFETs which can be fabricated as a separate device in GaAs processes, essentially by sharing a common junction between two FETs. Although this is also possible in CMOS, a more suitable version of the phase shifter is illustrated in Figure 2.13 [24], where the dual gate device is replaced by a cascode configuration. The impedance \( Z \) located at the gate of the common source transistor causes a parallel resonance with the gate source capacitance and thus maximizing the available gain and phase shift. The phase shift is controlled through the gate biasing of the common source transistor.

The dual gate phase shifter is simple compact and can have gain. However, it can only create small phase shifts, less than 90°. Furthermore, the gain and phase shift are interrelated, resulting in severe gain variation as the phase shift varies. Reference [24] reports more than 6
2.4.5. Phase Interpolation Phase Shifter

The phase interpolation phase shifter was originally introduced in [25] and its block level diagram is shown in Figure 2.14a. The input signal is first split into two equal amplitude in-phase and quadrature components. In the next stage, the two components are independently amplified by two variable gain amplifiers (VGAs) and then summed, forming the output signal. Depending on the gain of the two VGAs, any phase between $0^\circ$ and $360^\circ$ can be synthesized. The weighted summation of the I and Q components is sometimes called phase rotation and is graphically shown in Figure 2.14b.

In order to analyze the phase interpolation phase shifter, we utilize phasor representations for the signals and we assume that all the blocks are conjugately matched at their input and output (i.e. there are no reflections). Furthermore, each VGA is assumed to be able to vary its gain in the $[-A,A]$ range. In the following analysis the signals will be represented using the phasor notation.

The input signal is:

$$V_{in} = v_{in} \angle 0^\circ$$  \hspace{1cm} (2.38)

Assuming that the I-Q splitting network is passive, the I and Q outputs are:

$$V_I = \frac{v_{in}}{\sqrt{2}} \angle 0^\circ$$  \hspace{1cm} (2.39)

$$V_Q = \frac{v_{in}}{\sqrt{2}} \angle -90^\circ$$  \hspace{1cm} (2.40)

If the gain of the I and Q VGAs is $A_I$ and $A_Q$ respectively, the signal at the output of the phase
rotator is:

\[ \mathbf{V}_{\text{out}} = A_I \mathbf{V}_I + A_Q \mathbf{V}_Q = \frac{A_I v_{\text{in}}}{\sqrt{2}} \angle (0^\circ - w_I 180^\circ) + \frac{A_Q v_{\text{in}}}{\sqrt{2}} \angle (-90^\circ - w_Q 180^\circ) \]  \hspace{1cm} (2.41)

where

\[ w_I = \begin{cases} 
0 & \text{if } A_I \geq 0 \\
1 & \text{if } A_I < 0 
\end{cases} \]  \hspace{1cm} (2.42)

\[ w_Q = \begin{cases} 
0 & \text{if } A_Q \geq 0 \\
1 & \text{if } A_Q < 0 
\end{cases} \]  \hspace{1cm} (2.43)

Performing the vector addition at the right hand side of (2.41) yields the output phasor:

\[ |\mathbf{V}_{\text{out}}| = \frac{v_{\text{in}}}{\sqrt{2}} \left[ \left( |A_I| \cos (0^\circ - w_I 180^\circ) + |A_Q| \cos (-90^\circ - w_Q 180^\circ) \right)^2 + \left( |A_I| \sin (0^\circ - w_I 180^\circ) + |A_Q| \sin (-90^\circ - w_Q 180^\circ) \right)^2 \right]^{\frac{1}{2}} = \]  \hspace{1cm} (2.44)

\[ = \frac{v_{\text{in}}}{\sqrt{2}} \sqrt{\left( |A_I| \cos (0^\circ - w_I 180^\circ) \right)^2 + \left( |A_Q| \sin (-90^\circ - w_Q 180^\circ) \right)^2} \]

and

\[ \phi = \angle \mathbf{V}_{\text{out}} = 180^\circ k + \tan^{-1} \left[ \frac{|A_Q| \sin (-90^\circ - w_Q 180^\circ)}{|A_I| \cos (0^\circ - w_I 180^\circ)} \right] = \]  \hspace{1cm} (2.45)

where \( k = 0, \pm 1, \pm 2, \ldots \) represents the infinite solutions of the transcendental equation.

Equation (2.45) can be simplified by expanding it according to the various values of \( w_I \) and \( w_Q \):

\[ \phi = \begin{cases} 
\tan^{-1} \left( \frac{|A_Q|}{|A_I|} \right) & \text{if } A_I \geq 0, \ A_Q \geq 0 \\
180^\circ - \tan^{-1} \left( \frac{|A_Q|}{|A_I|} \right) & \text{if } A_I < 0, \ A_Q \geq 0 \\
180^\circ + \tan^{-1} \left( \frac{|A_Q|}{|A_I|} \right) & \text{if } A_I < 0, \ A_Q < 0 \\
-\tan^{-1} \left( \frac{|A_Q|}{|A_I|} \right) & \text{if } A_I \geq 0, \ A_Q < 0 
\end{cases} \]  \hspace{1cm} (2.46)
As a result, the sign of the gain $A_I$ and $A_Q$ determines the quadrant at which the output vector is going to lie into, as illustrated in Figure 2.15.

From equation (2.44), the gain is maximum when $A_I = A_Q = A_{max}$

$$|V_{out}| = v_{in}A_{max}$$ (2.47)

where $A_{max}$ is the maximum gain of each VGA. Under this condition, the resulting phase can be $45^\circ$, $135^\circ$, $225^\circ$ or $315^\circ$. However, if the $90^\circ$ phase is synthesized, then $A_Q = A_{max}$ and $A_I = 0$ and the resulting gain is:

$$|V_{out}| = \frac{v_{in}A}{\sqrt{2}}$$ (2.48)

It is obvious that when both the $45^\circ$ and $90^\circ$ phase need to be synthesized with equal amplitudes, the resulting gain of the $45^\circ$ phase must be decreased by $1/\sqrt{2}$.

It can be proven from equations (2.44) and (2.45) that apart from the simple case where only the $45^\circ$, $135^\circ$, $225^\circ$ or $315^\circ$ phases need to be synthesized, the phase interpolation phase shifter has $1/\sqrt{2} = 3$ dB less gain than the maximum possible gain.

The phase interpolation phase shifter has several advantages. First, it can create any desired phase shift between $0^\circ$ and $360^\circ$. Second, the VGAs and the I-Q splitting circuit can be realized using transistors and lumped components, resulting in very compact size. Third, depending on the gain of the VGAs, the phase shifter itself can have gain. However, the required amplifiers in the signal path give rise to non-linearities which can be limiting for certain radar applications. Furthermore, the finite bandwidth of the I-Q splitter and the tuned VGAs will limit the overall bandwidth of the circuit.
2.5. Phase Shifter Architecture Summary

The table below summarizes the basic properties of the phase shifters presented thus far. The phase shift range of every phase shifter is also provided in the table. Nevertheless, as with digital shifters, the phase shift range of analog phase shifters can be extended by cascading several of them. The penalty of this extension is again the increased loss of the resulting system.

<table>
<thead>
<tr>
<th>Type</th>
<th>Type</th>
<th>Phase Shift Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switched Line</td>
<td>Digital</td>
<td>True Time Delay</td>
</tr>
<tr>
<td>Reflection</td>
<td>Digital</td>
<td>True Time Delay</td>
</tr>
<tr>
<td>Loaded Line</td>
<td>Digital</td>
<td>Constant Phase</td>
</tr>
<tr>
<td>High Pass - Low Pass</td>
<td>Digital</td>
<td>Constant Phase</td>
</tr>
<tr>
<td>Distributed Switch</td>
<td>Digital</td>
<td>True Time Delay</td>
</tr>
<tr>
<td>Analog Reflection</td>
<td>Analog</td>
<td>Constant Phase</td>
</tr>
<tr>
<td>Tunable Filter</td>
<td>Analog</td>
<td>Constant Phase</td>
</tr>
<tr>
<td>Periodically Loaded T-line</td>
<td>Analog</td>
<td>True Time Delay</td>
</tr>
<tr>
<td>Dual Gate</td>
<td>Analog</td>
<td>Constant Phase</td>
</tr>
<tr>
<td>Phase Interpolation</td>
<td>Analog</td>
<td>Constant Phase</td>
</tr>
</tbody>
</table>

2.6. Other Applications of Phase Shifters

Perhaps the most important and widely used application of phase shifters is that of phased arrays, as discussed in section 1.1. In this section, two other well established applications are analyzed.

2.6.1. I-Q Calibration

A generic Hartley quadrature wireless receiver front-end is depicted in Figure 2.16a. This receiver architecture or its heterodyne equivalent is present in almost every modern wireless system. It is a well documented [26, 27] fact that phase imbalance in the I-Q splitter degrades the performance of the receiver. In the case of a heterodyne receiver, it degrades the image rejection ratio (IRR) whereas in a direct conversion receiver, the imbalance causes cross-talk between the data modulated in the I and Q paths.

A possible solution to the I-Q imbalance problem is illustrated in figure 2.16b. In this case, two high-resolution phase shifters with small phase shift range are placed in the I and Q paths, after the I-Q splitting. When an appropriate, known test vector is applied at the input
of the receiver, any possible I-Q imbalance could be detected by the baseband Digital Signal Processor which in turn, can set the appropriate phase shift in the phase shifters to correct the I-Q imbalance.

Although I-Q imbalance could be fully corrected by the baseband DSP [28], the scheme of figure 2.16b is more appropriate for multi-gigabit mm-wave radios since it reduces the already severe computational burden of the DSP.

### 2.6.2. Frequency Translators - Modulators

Consider the system of Figure 2.17 where an analog 0° − 360° phase shifter has its phase control input modulated with a continuous ramp with slope of $r$ degrees/sec. A constant frequency sinusoid of frequency $f_{\text{ref}}$ is applied at the high frequency input of the phase shifter. The output of the phase shifter is:

$$RF_{\text{out}} = \cos(f_{\text{ref}}t + \Delta\phi) = \cos(f_{\text{ref}}t + rt) = \cos(f_{\text{ref}} + r)t$$

Therefore, the frequency of the input signal can be shifted in frequency by $r$ or $-r$ depending on the slope of the ramp. This circuit is known as frequency translator and dates back to the days of microwave ferrite phase shifters which could be used to adjust the frequency of a known reference.
Equation (2.49) can be seen from another point of view. The input carrier is modulated by another sinusoid in one of its two sidebands. As a result, a phase shifter can be utilized as a frequency or phase modulator.

2.7. Conclusion

This chapter presented the various phase shifter architectures encountered in the literature and can be realized in standard integrated circuit form. Mathematical analysis was provided for the various topologies and their main advantages and disadvantages were discussed.
3.1. Choice of Phase Shifter Topology

The main goal of this work is the development of a transmitter (TX) and a receiver (RX) with phase shifting. The transmitter and receiver need to be capable of being integrated in a phased array system, which could be assembled by using only multiple copies of them and an in-phase power combiner or divider. The target frequencies for the arrays are 77GHz and 94GHz.

As discussed in section 1.1, a phased array can either use true time delay phase shifters or constant-phase phase shifters. All time delay elements need transmission lines in order to realize time delays. Assuming that the effective dielectric constant of a transmission line in silicon is $\varepsilon_{\text{eff}} = 3.8$, the resulting length of a $\lambda/4$ transmission line which would be needed to create a $90^\circ$ phase shift is $500\mu m$ at 77GHz and $410\mu m$ at 94GHz. Even if the loss of these lines is small in the case of a thick metallization process, their size is prohibitively large since several of these lines would be required in a phase shifter. As a result, the use of a constant-phase phase shifter was decided.

Most of the passive constant-phase phase shifters require varactors to realize tunable elements. However, the varactor Q factor is ranging from 6-8 at 94GHz in 65-nm CMOS [29] and 5-10 for 130-nm SiGe BiCMOS at 77GHz [30]. These low Q factors would result in very high loss which would be very difficult and power intensive to be compensated using amplifiers. For example, reference [31] presents a loaded line phase shifter with 9.4dB loss at 60GHz, while reference [21] reports 10 – 12dB at 24GHz for a reflection type phase shifter. A different choice would be the High-Pass Low-Pass phase shifter as in section 2.3.4. However, in order to attain, for example, a $0^\circ – 360^\circ$ phase shift range in 22.5$^\circ$ steps, four such phase shifters need to be cascaded, resulting in high loss. Examples of High-Pass Low-Pass phase shifter can be found in [18] and [32] where the losses are 10dB at 30GHz (4 bits) and 20dB at 12GHz (5 bits) respectively. It should be also noted that these losses are going be further exacerbated
at the target frequencies of 77 GHz and 94 GHz and would most likely result in a non-practical phase shifter.

Driven by these facts, the phase interpolation phase shifter was selected. The topology was preferred because of its potential to have low loss, its ability to easily obtain $0^\circ - 360^\circ$ phase shift range and its very compact size. It’s major disadvantage is its potentially poor linearity which can be a major issue in certain radar applications. However, this issue could be partially corrected in the circuit design of the variable gain amplifiers.

3.2. System Analysis of the Phase Interpolation Phase Shifter

The basic theory behind the interpolation phase shifter was presented in section 2.4.5. In order to be able to synthesize phases in all four quadrants, the variable gain amplifiers need to have both positive and negative gain. To accomplish this, the VGAs have to be differential so that their two outputs could be flipped and cause a sign inversion. A more detailed version of the phase shifter, utilizing differential signals, is illustrated in Figure 3.1 where the differential splitting and combining is done using transformers. The input signal is first split into two parts of equal amplitude. The normalized phase of the two signals can be considered to be $0^\circ$ and $180^\circ$ respectively. Similarly, the normalized phases at the output of the first I-Q splitter are $0^\circ$ and $90^\circ$ whereas, at the output of the second splitter, the phases are $180^\circ$ and $270^\circ$. Rearranging the signals, the phases at the input of the first VGA are $0^\circ$ and $180^\circ$ while the phases at the input of the second VGA are $90^\circ$ and $270^\circ$. The outputs of the VGAs are summed in current, as will be shown in the phase rotator section, and the output is converted to single ended using a second transformer.

The mathematical analysis is essentially the same as presented in section 2.4.5. The ratio of the gains of the two VGAs can be calculated, based on the desired phase shift, using equation (2.45):

$$R_{I/Q} = \frac{A_Q}{A_I} = \tan \phi$$

(3.1)
3.3 Error Model for the Interpolation Phase Shifter

If a phase shift in the range of $0^\circ - 360^\circ$ is required in $N$ steps, there are two possible arrangements. First, the $N$ phases could be arranged as $0, 360^\circ / N, 2 \times 360^\circ / N, \ldots, (N-1) \times 360^\circ / N$. A second arrangement is possible if a constant phase offset of $360^\circ / 2N$ is added to every phase shift state, resulting in: $360^\circ / 2N, 3 \times 360^\circ / 2N, 5 \times 360^\circ / 2N, \ldots, (2N-1) \times 360^\circ / 2N$. Table 3.1 shows the ratio $R_{I/Q}$ of the VGA gains when $N = 16$ for the two phase arrangements. The arrangement without phase offset results in a VGA that needs infinite gain adjustment range whereas the arrangement with $11.25^\circ$ offset requires a VGA with only 14 dB of gain adjustment range.

When $R_{I/Q}$ is known based on the phase requirements, the individual gains of the VGAs can be calculated based on the requirement that all phase states have equal amplitudes. If the maximum VGA gain is normalized to 1 (0 dB), solving equation (2.44) yields:

$$A_I = \frac{1}{\sqrt{1 + R_{I/Q}^2}} \quad (3.2)$$
$$A_Q = \frac{R_{I/Q}}{\sqrt{1 + R_{I/Q}^2}} \quad (3.3)$$

The normalized gain of each phase is $-3$ dB, i.e., 3 dB lower than the gain of the individual VGA. Table 3.2 illustrates $A_I$ and $A_Q$, along with their signs, for case of $N = 16$. The phase arrangement with $11.25^\circ$ offset will be utilized in the design of the interpolation phase shifter in this work because of its reduced dynamic range requirement.

### 3.3. Error Model for the Interpolation Phase Shifter

The analysis up to now assumed that all the components used in the system are ideal. Nevertheless, there are various sources of imperfections that can result in both amplitude and phase error in the interpolation phase shifter. The most important of these include:

- **Transformer balun amplitude and phase imbalance.** Due to modeling imperfections and process variations, the transformers used in at the input and output in figure 3.1 will not split the signal exactly in two equal parts and these parts will not be precisely $180^\circ$ out of phase.

- **Quadrature splitter amplitude and phase imbalance.** As with the transformers, the outputs of the quadrature splitters will not be exactly equal, or $90^\circ$ out of phase.

- **Variable gain amplifier phase stability.** Up to now we have assumed that the phase shift introduce by the VGAs is constant as their gain varies. In all practical VGAs though, the phase can vary significantly as the amplitude changes.
### Phase Shifts and Phase Arrangements

<table>
<thead>
<tr>
<th>Phase Shift</th>
<th>$A_Q/A_I$</th>
<th>$A_Q/A_I$ (11.25° offset)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0°</td>
<td>0</td>
<td>0.2</td>
</tr>
<tr>
<td>22.5°</td>
<td>0.414</td>
<td>0.668</td>
</tr>
<tr>
<td>45°</td>
<td>1</td>
<td>1.497</td>
</tr>
<tr>
<td>67.5°</td>
<td>2.414</td>
<td>5.027</td>
</tr>
<tr>
<td>90°</td>
<td>$\infty$</td>
<td>-5.027</td>
</tr>
<tr>
<td>112.5°</td>
<td>-2.414</td>
<td>-1.497</td>
</tr>
<tr>
<td>135°</td>
<td>-1</td>
<td>-0.668</td>
</tr>
<tr>
<td>157.5°</td>
<td>-0.414</td>
<td>-0.2</td>
</tr>
<tr>
<td>180°</td>
<td>0</td>
<td>0.2</td>
</tr>
<tr>
<td>202.5°</td>
<td>0.414</td>
<td>0.668</td>
</tr>
<tr>
<td>225°</td>
<td>1</td>
<td>1.497</td>
</tr>
<tr>
<td>247.5°</td>
<td>2.414</td>
<td>5.027</td>
</tr>
<tr>
<td>270°</td>
<td>$\infty$</td>
<td>-5.027</td>
</tr>
<tr>
<td>292.5°</td>
<td>-2.414</td>
<td>-1.497</td>
</tr>
<tr>
<td>315°</td>
<td>-1</td>
<td>-0.668</td>
</tr>
<tr>
<td>337.5°</td>
<td>-0.414</td>
<td>-0.2</td>
</tr>
</tbody>
</table>

**Gain Range**

| $\infty$ | 14 dB |

Table 3.1: $R_{I/Q}$ for different phase shifts and phase arrangements.

### Phase Shifts and Gain Range

<table>
<thead>
<tr>
<th>Phase Shift</th>
<th>Sign</th>
<th>$A_I$ (dB)</th>
<th>Sign</th>
<th>$A_Q$ (dB)</th>
<th>Sign</th>
<th>$A_I$ (db) 11.25° offset</th>
<th>Sign</th>
<th>$A_Q$ (dB) 11.25° offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>0°</td>
<td>+</td>
<td>0</td>
<td>$\phi$</td>
<td>$-\infty$</td>
<td>+</td>
<td>0</td>
<td>+</td>
<td>-14</td>
</tr>
<tr>
<td>22.5°</td>
<td>+</td>
<td>-0.69</td>
<td>+</td>
<td>-8.34</td>
<td>+</td>
<td>-1.43</td>
<td>+</td>
<td>-4.94</td>
</tr>
<tr>
<td>45°</td>
<td>+</td>
<td>-3</td>
<td>+</td>
<td>-3</td>
<td>+</td>
<td>-4.94</td>
<td>+</td>
<td>-1.43</td>
</tr>
<tr>
<td>67.5°</td>
<td>+</td>
<td>-8.34</td>
<td>+</td>
<td>-0.69</td>
<td>+</td>
<td>-14</td>
<td>+</td>
<td>0</td>
</tr>
<tr>
<td>90°</td>
<td>$\phi$</td>
<td>$-\infty$</td>
<td>+</td>
<td>0</td>
<td>-14</td>
<td>+</td>
<td>0</td>
<td>-14</td>
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<td>-1.43</td>
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</tr>
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<td>+</td>
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<td>8.34</td>
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<td>+</td>
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<td>-</td>
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<td>-8.34</td>
<td>0</td>
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<td>-14</td>
<td></td>
</tr>
</tbody>
</table>

Table 3.2: $A_I$ and $A_Q$ for different phase shifts and arrangements.
The amplitude and phase imbalance of the transformer balun and IQ splitter can be modeled based on the passivity relation of their scattering parameter matrix [33]. Since the transformer is passive its two outputs, including possible errors will be:

\[ V_0^\circ = \alpha_d e^{j0^\circ} \]  
\[ V_{180^\circ} = \sqrt{1 - \alpha_d^2} e^{j(180^\circ + \phi_{e,180^\circ})} \]

where \( 0 \leq \alpha_d \leq 1 \) and \(-90^\circ \leq \phi_{e,180^\circ} \leq 90^\circ\). \( \alpha_d = 1/\sqrt{2} \) and \( \phi_{e,180^\circ} = 0^\circ \) when no errors are present. The transformer amplitude imbalance is defined as

\[ A_{e,180^\circ} = 20\log\left(\frac{\alpha_d}{\sqrt{1 - \alpha_d^2}}\right) \]  

Similarly, the passivity relations of the IQ splitter yield:

\[ V_0^\circ = \alpha_{IQ} e^{j0^\circ} \]  
\[ V_{90^\circ} = \sqrt{1 - \alpha_{IQ}^2} e^{j(90^\circ + \phi_{e,90^\circ})} \]

where \( 0 \leq \alpha_{IQ} \leq 1 \) and \(-45^\circ \leq \phi_{e,90^\circ} \leq 45^\circ\). \( \alpha_{IQ} = 1/\sqrt{2} \), \( \phi_{e,90^\circ} = 0^\circ \) when errors are not considered. The amplitude imbalance is also defined by:

\[ A_{e,90^\circ} = 20\log\left(\frac{\alpha_{IQ}}{\sqrt{1 - \alpha_{IQ}^2}}\right) \]  

In the VGA case, the assumption of linear phase variation is made. At a certain frequency, the transmission phase of the VGA is assumed to vary linearly as the gain varies:

\[ \phi(S_{21}) = \phi_r(^\circ / dB) \cdot |S_{21}|(dB) \]

Simulation and measurement results that will presented later in the thesis will confirm the validity of this linear model. The phase shift is assumed to be independent of the gain sign.

In order to analyze the impact of each non-ideality in the phase shifter, each source of error is considered separately. The result is analyzed using two methods: first, the polar diagram of the transfer \( (S_{21}) \) parameter of the phase shifter for all different phase states is generated. Second, the maximum possible phase error between two consecutive states and the peak-to-peak gain deviation between all states are computed.
(a) Distortion when $A_{e,90^\circ} = 1.5\text{dB}$.

(b) Distortion when $\phi_{e,90^\circ} = 10^\circ$.

(c) Distortion when $A_{e,180^\circ} = 1.5\text{dB}$.

(d) Distortion when $\phi_{e,180^\circ} = 10^\circ$.

(e) Distortion when $\phi_r = 3^\circ/\text{dB}$.

Figure 3.2: Phase shifter signal constellation under various errors.
3.3 Error Model for the Interpolation Phase Shifter

<table>
<thead>
<tr>
<th>Error Condition</th>
<th>Maximum Amplitude Error</th>
<th>Maximum Phase Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_e,90^\circ = 1.5$ dB</td>
<td>1.4 dB</td>
<td>9.5°</td>
</tr>
<tr>
<td>$\phi_e,90^\circ = 10^\circ$</td>
<td>1.4 dB</td>
<td>6.5°</td>
</tr>
<tr>
<td>$A_e,180^\circ = 1.5$ dB</td>
<td>0.1 dB</td>
<td>0.4°</td>
</tr>
<tr>
<td>$\phi_e,180^\circ = 10^\circ$</td>
<td>0.1 dB</td>
<td>0.4°</td>
</tr>
<tr>
<td>$\phi_r = 3^\circ$</td>
<td>2.3 dB</td>
<td>5.4°</td>
</tr>
<tr>
<td>Monte Carlo</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\sigma(A_e,90^\circ) = \sigma(A_e,180^\circ) = 0.2$ dB</td>
<td>5.6 dB</td>
<td>18°</td>
</tr>
<tr>
<td>$\sigma(\phi_e,90^\circ) = \sigma(\phi_e,180^\circ) = 2^\circ$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\sigma(\phi_r) = 0.5^\circ$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3.3: Phase and amplitude errors of the phase shifter.

Figures 3.2a and 3.2b show the distortion of the polar diagram when the amplitude imbalance and phase error of the quadrature splitter are $A_e,90^\circ = 1.5$ dB and $\phi_e,90^\circ = 10^\circ$ respectively. In both cases, the diagram is distorted and gets an elliptic shape. Moreover, amplitude imbalance in the I-Q splitter results in both amplitude and phase error in the phase shifter. The same case holds for the phase imbalance in the splitter.

Figures 3.2c and 3.2d illustrate the distortion when the amplitude imbalance and phase error of the transformer balun are $A_e,180^\circ = 1.5$ dB and $\phi_e,180^\circ = 10^\circ$. The amplitude imbalance case causes a negligible distortion in the third quadrant of the diagram (where both $A_I$ and $A_Q$ are negative). The phase error case adds a constant phase offset without adding a phase error to the final points.

Figure 3.2e depicts the distortion in the polar diagram when the phase shift introduced by the VGA is $\phi_r = 3^\circ/\text{dB}$. The diagram is severely distorted, with both phase and amplitude error. The resulting shape is rectangular with "curled" sides.

Table 3.3 summarizes the peak-to-peak amplitude and phase error of each of the cases discussed above. It can be seen that the most severe error source is the phase variation with gain in the VGAs. A significant error source can also be the phase and amplitude imbalance in the I-Q splitter.

In order to study the overall effect when all error sources are present, a Monte Carlo simulation is utilized. The error sources are assumed to follow uncorrelated normal distributions. The average values of the distributions are set as: $\mu(A_e,90^\circ) = \mu(A_e,180^\circ) = 0$ dB, $\mu(\phi_e,90^\circ) = \mu(\phi_e,180^\circ) = 0^\circ$, $\mu(\phi_r) = 1^\circ$. The deviations are set as: $\sigma(A_e,90^\circ) = \sigma(A_e,180^\circ) = 0.2$ dB, $\sigma(\phi_e,90^\circ) = \sigma(\phi_e,180^\circ) = 2^\circ$, $\sigma(\phi_r) = 0.5^\circ$. The resulting I-Q diagram is shown in Figure 3.3 and the maximum phase shifter errors are summarized in Table 3.3. It is clear that when all the sources of error are present, large errors are possible in the phase shifter. This fact is
true even with the very moderate deviations that were used in the Monte Carlo analysis.

The previous error analysis reveals that, in case the gains $A_I$ and $A_Q$ are set without accounting for non-idealities, the accuracy of the phase shifter can easily be degraded. Nevertheless, equations (2.44) and (2.44) are still valid in the presence of errors. Neglecting the error in the transformer balun (which was shown to be insignificant), the vector addition in the presence of errors can be expressed as:

$$V_{out} = \alpha_{IQ} A_I e^{j\phi_r} 20\log|A_I| + \sqrt{1 - \alpha_{IQ}^2 A_Q e^{j\phi_r} 20\log|A_Q| e^{j(90^\circ + \phi_e 90^\circ)}}$$

Unfortunately it is impossible to find an explicit solution to this equation for $A_I$ and $A_Q$. However, by conducting experiments using a numerical algorithm, it was found that the equation has solutions for $A_I$ and $A_Q$ in the real number domain. For example, in the case where $A_{e, 90^\circ} = 1$ dB, $\phi_{e, 90^\circ} = 10^\circ$ and $\phi_r = 3^\circ$, the equation indeed has a solution; However, the required gain adjustment range of the VGAs is now 26.5 dB, almost twice as high as in the ideal case, and the maximum normalized gain of the phase shifter is $-4$ dB, 1 dB higher loss than the ideal case. These experiments confirm, that even in the presence of non-idealities in the components that comprise the phase shifter, a new set of values for the VGA gains $A_I$ and $A_Q$ can be found that will generate the required phase shift states.
3.4 I-Q Splitting

An essential component of the interpolation phase shifter is the splitting of the signal into in-phase and quadrature complements. There are several methods proposed in the bibliography to achieve this I-Q splitting which include: High-Pass – Low-Pass filters [34], Polyphase Filters [35, 36] and Quadrature Hybrids [33].

In this work, the different approaches to I-Q splitting were studied and compared based on their feasibility for mm-wave frequency operation. The main problem for high frequency operation of most I-Q splitters remains their potentially high loss or the resulting very small component values, which could lead to process variation problems. Two different ways of splitting were finally implemented: an All-Pass Polyphase filter [36] and a lumped quadrature hybrid [37].

3.4.1. All-Pass Polyphase filter

The All-Pass polyphase filter was recently proposed in [36] and is shown in figure 3.4. It consists of four RLC All-Pass filters, arranged to introduce ±45° phase shifts. This principle of operation is similar to the RC polyphase filter where the ±45° phase shifts are created by RC-CR filters.

The values of the resistors in figure 3.4 determine the bandwidth of operation of the filter, its input and output characteristic impedances as well as the tolerance of the filter to variations of its load. Although larger resistance results in increased bandwidth, the loss of the filter also increases leading to bandwidth – loss trade-off. Once the value of the filter quality factor (and bandwidth) $Q$ is selected, the values of $R$, $L$ and $C$ are selected based on the desired frequency of operation:

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

$$Q = \frac{\sqrt{L/C}}{R}$$
where $\omega_0$ is the frequency of operation.

In order to obtain large bandwidth and make the filter insensitive to poorly predictable load variations that are common in mm-wave frequencies, a quality factor value $Q = 0.25$ was selected and $\omega_0 = 90\,\text{GHz}$. Under these conditions, equations 3.12 yield $C = 105\,\text{fF}$, $L = 33\,\text{pH}$ and $R = 75\,\Omega$. This design procedure also sets the input and output impedances of the filter to $75\,\Omega$.

The simulated response of the filter is shown in figure 3.5, where it can be seen that the filter exhibits slightly more than $\pm 1^\circ$ of phase imbalance and less than $1\,\text{dB}$ of amplitude imbalance in the $80\,\text{GHz} - 100\,\text{GHz}$ range. However, the price paid for this broadband behavior is the fact that the filter has $3\,\text{dB}$ additional loss from the input to each of the I and Q outputs. This additional loss is still much lower than the corresponding loss that would be generated by a classical polyphase filter of similar performance.

### 3.4.2. Lumped Quadrature Hybrid

Quadrature hybrids have been commonly used for I-Q splitting in microwave circuits. A quadrature hybrid can be realized utilizing different methods including: branch line couplers, ring hybrids and coupled-line couplers. Of these methods, the coupled line couplers have been extensively utilized because of their high bandwidth of operation. Unfortunately, the length of the coupled lines must be $\lambda/4$ which renders their size relatively large even for mm-wave frequencies. There have been several attempts to reduce the size of coupled line couplers, the most important being the one described in [37, 38]. In this approach, the coupled lines are approximated at a particular frequency $\omega_0$ with lumped elements as depicted in figure 3.6a.
Each individual line is approximated with a $\Pi$ network, whereas the magnetic coupling is realized by introducing coupling between the two inductors and the capacitive coupling is realized using lumped capacitors. The design equations are straightforward:

\[
L = L_{\text{norm}} \frac{Z_0}{\omega_0} \tag{3.13}
\]
\[
C_G = C_{G\text{norm}} \frac{Z_0}{\omega_0} \tag{3.14}
\]
\[
C_M = C_{M\text{norm}} \frac{Z_0}{\omega_0} \tag{3.15}
\]
\[
k = 0.707 \tag{3.16}
\]

where $L_{\text{norm}} = 1.414$, $C_{G\text{norm}} = 0.414$, $C_{M\text{norm}} = 1$.

In mm-wave frequencies, application of equations (3.13 - 3.16) results in components with impractically small values. For example, when $f_0 = 77$ GHz and $Z_0 = 50 \Omega$, then $L = 140\, \text{pH}$, $C_M = 41\, \text{fF}$, $C_G = 17\, \text{fF}$. Clearly the capacitors $C_G$ are very small to be reliably realized with high Q MiM capacitors. In order to alleviate this problem, our design methodology proceeds as follows. First, a transformer with component values as close as possible with the ones predicted by equations (3.13) and (3.16) is designed and the $2 - \Pi$ model [12] for this transformer is extracted. The small capacitors are omitted and the resulting structure is optimized in order to obtain a response as close as possible with the ideal one. Following this methodology, a design centered at 85GHz is shown in figure 3.6b ($L = 96\, \text{pH}$, $C_{M1} = 27\, \text{fF}$, $C_{M1} = 40\, \text{fF}$ and $R = 40\, \Omega$) and its simulated response in figure 3.7. It can be seen that the lumped hybrid coupler also exhibits slightly more than $\pm 1^\circ$ of phase imbalance and less than $1\, \text{dB}$ of amplitude imbalance in the 70GHz – 90GHz range. Moreover, the loss from the input to each of the two outputs remains lower than $1\, \text{dB}$. 
3.5. Variable Gain Amplifiers

The variable gain amplifier is an essential component in the interpolation phase shifter. First, it must have an adequate gain adjustment range in order for the phase shifter to generate $0^\circ - 360^\circ$ phase shift. Most importantly, as numerical experiments in section 3.2 showed, a large gain adjustment range is required in order for the non-idealities of the phase shifter to be corrected. Second, the transmission phase variation with gain control must be as low as possible since it can severely alter the resulting constellation diagram of the phase shifter. Last but not least, the overall linearity of the phase shifter will be determined by the variable gain amplifiers because they are the only active components utilized.

There have been numerous variable gain amplifiers proposed in the literature, since a VGA is needed in every high dynamic range receiver. There are topologies that exhibit both analog [39] and digital [40] gain control. In this work, two different mm-wave VGAs have been implemented: a 65-nm CMOS current steering VGA for the 94-GHz phase shifter and a SiGe BiCMOS Gilbert-cell VGA for the 77-GHz phase shifter. The two VGAs utilize similar circuit topologies. Their main difference is the way the gain control is applied.

3.5.1. 65-nm CMOS, 94 GHz Variable Gain Amplifier

The CMOS current steering VGA is shown in figure 3.8. The VGA is very similar to a Gilbert multiplier where the cascode transistors M4-M7 are used only to control the sign of the output signal with respect to the input. When the sign bit switches from 0 to 1.2V, the positive and negative outputs are flipped and as a result, the phase of the output changes by $180^\circ$. The
3.5 Variable Gain Amplifiers

In M1 GainCtrl LC

M2 M3

M4 M5 M6 M7

LMLM

sign

sign

sign

sign

Out

Cdec

Parameter | Value
---|---
$W_{M1}$ | $2 \mu m$
$W_{M2}, W_{M3}$ | $16 \mu m$
$W_{M4} - W_{M7}$ | $24 \mu m$
$L_C$ | $140 \text{pF}$
$L_M$ | $140 \text{pF}$
$C_{dec}$ | $500 \text{fF}$

Figure 3.8: 65-nm CMOS, 94 GHz CMOS variable gain amplifier.

differential input signal is applied to the gates of transistors M2 and M3 and is amplified by the cascode formed by M2-M4 (M5 when sign = 0) and M3-M6 (M7). At DC, M1 forms a current mirror with M2 and M3 and thus, it is able to control the bias currents of M2 and M3. As the voltage GainCtrl is decreased from its nominal value, the current flowing through the cascodes M2-M4 and M3-M6 is decreased. The decreasing current results in reduced effective $f_T$ in the cascodes and consequently reduced gain.

The inductor $L_C$ helps improve the common mode rejection properties of the amplifier whereas, inductors $L_M$ create a series resonance with the drain capacitances of M2-M3 and the source capacitances of M4-M7, improving the overall gain of the VGA [11]. In order to ensure high frequency stability of the amplifier, decoupling capacitors $C_{dec} = 500 \text{fF}$ are placed in the gates of the common-gate transistors M4-M7.

The transistors M2 and M3 are biased at 0.3 mA/$\mu m$ when their gain is maximum. This corresponds to the peak $f_T$ current density for this process and biasing at this level provides the maximum possible gain. The resulting power consumption is 11.5 mW (9.5 mA from 1.2 V).

A critical aspect with this VGA topology stems from the bias current variation itself. As the bias point varies, the parasitic capacitances of the transistors will also change. As a result, the transmission phase of the VGA will depend on the gain state. Another side effect associated with the bias current variation is the fact that the input impedance of the VGA also changes,
resulting in non-constant loading of its preceding and succeeding stages.

There are two limiting factors in the linearity of the VGA, as expressed by its input compression point. First, if the input signal amplitude is very large, the gate source voltage of transistors M2 and M3 swings below their threshold voltage and causes them to turn off. This mode of operation is identical to class AB amplifiers and results in gain reduction at large signal amplitudes. The second limiting mechanism is the fact that the output signal swing cannot be larger than $V_{DD} - 2V_{SAT}$, where $V_{SAT}$ is the drain-source saturation voltage of the MOSFETs. If the input signal is large enough to cause the output swing to exceed this value, the output voltage will clip and also result in gain reduction.

When the gain of the VGA is reduced by decreasing the bias current flowing through transistors M2 and M3, the DC gate-source voltage $V_{GS}$ of the transistors is also reduced, resulting in degradation of the input linearity of the amplifier. However, since the output voltage is:

$$v_{OUT} = V_{DD} - g_m v_{in} |Z_{out}|$$

and $g_m$ decreases with bias current (when the current density $J_{DS}$ is less than 0.15 mA/μm), the output non-linear behavior of the amplifier improves as the gain is reduced.

Based on the above analysis, the input compression point of the VGA is initially expected to improve as the gain reduces. However, there will be a gain setting where the input non-linearity of the M2 and M3 will dominate the linearity of the VGA. Beyond this point, there will not be any further improvement of the compression level.

### 3.5.2. 130-nm SiGe BiCMOS, 77 GHz Variable Gain Amplifier

The Gilbert-cell type SiGe BiCMOS variable gain amplifier is illustrated in figure 3.9. A BiCMOS topology with MOS transconductors was selected in order to facilitate low supply voltage operation and high linearity. Moreover, because the pole at the drain of the MOSFET and the emitter of the HBT is pushed beyond the HBT $f_T/2$, the MOS-HBT cascode has higher stability phase margin than an HBT-HBT cascode while providing over 10dB of power gain from a lower supply [41].

The differential input signal is applied at the gates of the MOS transconductors. The gain control is achieved by steering the current between transistors Q1-Q2 and Q3-Q4 through a differential DC control signal applied at their bases. When maximum positive gain is required, all the bias current is steered through transistors Q1 and Q3, while Q2 and Q4 remain off. In order to reduce the gain, a portion of the current is steered through Q2 and Q4, resulting in addition of the opposite phases of the input signal at the output. The sign of the gain of the VGA can be flipped by steering the current through Q2 and Q4 instead of Q1 and Q3.
This gain adjustment procedure has the advantage that the bias current at the transconductors M1 and M2 remains constant as the gain is varied. As a result, the input impedance of the VGA will remain constant to a first order approximation. For the same reason, the transmission phase versus gain is also expected to remain roughly constant. Furthermore, the gate-source voltage of the MOS transconductors is held constant and as a result, based on similar arguments as with the CMOS VGA, the linearity is expected to improve as the gain is reduced, until it is completely dominated by the input non-linearity of the MOS transconductors. However, the gain where the input non-linearity will dominate the linearity of the VGA is going to be much lower than the corresponding one in the CMOS VGA because of the constant $V_{GS}$ in M1 and M2.

Inductors $L_{in}$ and $L_E$ facilitate conjugate matching with the previous stage. In addition, the inductors $L_E$ provide series feedback in the MOS transconductors, improving their linearity, with a penalty in the gain of the VGA. As with the 65-nm VGA, capacitors $C_{dec}$ assure the high frequency stability of the amplifier and make it immune to possible base interconnect inductances. Similarly, inductor $L_C$ improves the common mode rejection properties of the amplifier.

The sizing ratio between the MOS and HBT transistors is such that all transistors are biased at the peak $f_T$ current density when the quad transistors are fully switched. The bias current per side is 5.2 mA and the power supply voltage, which is applied through the center tap of a transformer as will be shown in the next section, is 2.5 V, resulting in a total power consumption

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_{M1}, W_{M2}$</td>
<td>$16 \times 1.125 \mu m$</td>
</tr>
<tr>
<td>$l_{Q1-Q4}$</td>
<td>$2.8 \mu m$</td>
</tr>
<tr>
<td>$L_C$</td>
<td>$100 \text{pH}$</td>
</tr>
<tr>
<td>$L_E$</td>
<td>$35 \text{pH}$</td>
</tr>
<tr>
<td>$C_{dec}$</td>
<td>$500 \text{fF}$</td>
</tr>
</tbody>
</table>

Figure 3.9: 130-nm SiGe BiCMOS, 77 GHz variable gain amplifier.
of 25mW.

In order to examine how the input and output impedance of the quad formed by transistors Q1-Q4 will vary with gain, the model of figure 3.10 is employed. In this model, we assume that the transistor input and output admittances $Y_{in}$ and $Y_{out}$ are arbitrarily dependent on the transistor base voltage, while the collector and emitter voltages are held constant. The input admittance $Y_1$ can be expressed as:

$$Y_1 = Y_{in}(V_{B1}) + Y_{in}(V_{B2}) \quad (3.18)$$

The admittances $Y_{in}(V_{B1})$ and $Y_{in}(V_{B2})$ and can be expanded in a Taylor series around the voltage $(V_{B1} + V_{B2})/2$:

$$Y_{in}(V_{B1}) = Y_{in}\left(\frac{V_{B1} + V_{B2}}{2}\right) + \frac{dY_{in}}{dV_B}\bigg|_{V_B = \frac{V_{B1} + V_{B2}}{2}} \cdot \left(V_{B1} - \frac{V_{B1} + V_{B2}}{2}\right) =$$

$$= Y_{in}\left(\frac{V_{B1} + V_{B2}}{2}\right) + \frac{dY_{in}}{dV_B}\bigg|_{V_B = \frac{V_{B1} + V_{B2}}{2}} \cdot \left(V_{B1} - \frac{V_{B1} + V_{B2}}{2}\right) \quad (3.19)$$

$$Y_{in}(V_{B2}) = Y_{in}\left(\frac{V_{B1} + V_{B2}}{2}\right) + \frac{dY_{in}}{dV_B}\bigg|_{V_B = \frac{V_{B1} + V_{B2}}{2}} \cdot \left(V_{B2} - \frac{V_{B1} + V_{B2}}{2}\right) =$$

$$= Y_{in}\left(\frac{V_{B1} + V_{B2}}{2}\right) + \frac{dY_{in}}{dV_B}\bigg|_{V_B = \frac{V_{B1} + V_{B2}}{2}} \cdot \left(-V_{B1} + V_{B2}\right) \quad (3.20)$$

As a result the input admittance $Y_1$ becomes:

$$Y_1 = 2Y_{in}\left(\frac{V_{B1} + V_{B2}}{2}\right) \quad (3.21)$$
3.6 Phase Rotators

Following the same reasoning, the remaining input and output admittances are:

\[ Y_2 = 2Y_{in}\left(\frac{V_{B1} + V_{B2}}{2}\right) \]  
\[ Y_3 = 2Y_{out}\left(\frac{V_{B1} + V_{B2}}{2}\right) \]  
\[ Y_4 = 2Y_{out}\left(\frac{V_{B1} + V_{B2}}{2}\right) \]  

(3.22)  
(3.23)  
(3.24)

It is clear from the above equations that the voltages \( V_{B1} \) and \( V_{B2} \) may vary independently, but as long as their sum \( V_{B1} + V_{B2} \) is constant, the input and output admittances of the quad will remain constant to a first order approximation. As a matter of fact, expansion with more Taylor series terms in equations (3.19) and (3.20) reveals that all the odd terms cancel while the even terms remain and add up. Assuming that all the series terms above the third order are negligible, any impedance variation will come from:

\[ \frac{d^2Y_{in}}{dV_B^2}\bigg|_{V_B=V_{B1}+V_{B2}} \cdot \left(\frac{V_{B1} - V_{B2}}{2}\right)^2 \]  

(3.25)

The above analysis reveals how the DC control voltage of the quads should be applied, i.e. \( V_{B1} + V_{B2} \) should be held constant in order to minimize variations in \( Y_1-Y_4 \) with gain.

3.6. Phase Rotators

3.6.1. 65-nm CMOS, 94 GHz Phase Rotator

The 65-nm CMOS phase rotator is illustrated in figure 3.11. It is composed of two VGAs, as presented in section 3.5.1. The outputs of the two VGAs are summed in current at the output transformer. The transformer, apart from providing the tuned load to the circuit, it AC-couples the output and provides differential to single ended conversion.

The sign of the gain of each VGA is selected by the two bits signI and signQ at the the top CMOS switches of the two VGAs. This sign selection essentially also selects the quadrant of the applied phase shift. Inside the selected quadrant, the phase is controlled in analog fashion by changing gain through the bias currents of the common source MOSFETs in the I and Q VGAs. A multi-bit DAC could replace the analog control in an all-digital control version.

In order to assess the performance of each VGA in the rotator, the Q input is terminated to 100 \( \Omega \) differentially and S-parameter simulation ports are connected to the I input of the other VGA and the output. Figure 3.12a shows the simulated magnitude of \( S_{21} \) at 94 GHz versus the control current flowing through the mirror transistor M1 and the control input GainI. It can be
seen that the power gain peaks when the current density of M2 and M3 is set to approximately 0.35 mA/μm while it reduces in a linear-in-dB fashion as the current is decreased.

Figure 3.12b reproduces the phase of $S_{21}$ at 94 GHz versus the current flowing through M1. The phase varies significantly, by almost 60 degrees, over the gain control range. The variation of the parasitic capacitances of transistors M2 and M3 as their current density varies, causes the transmission delay through the transistors as well as the input and output matching characteristics to shift, resulting in significant phase shift variation.

Figure 3.13a illustrates the transmission phase of the VGA at 94 GHz versus the small signal gain ($S_{21}$) of the amplifier. The phase shift characteristics are similar to those of Figure 3.12b, where the phase varies by approximately 60$^\circ$ as the gain is reduced by 2 dB to −40 dB. This approximate linear phase shift versus gain variation confirms the linear model utilized in section 3.3, especially at lower gains.

Figure 3.13b highlights the input 1-dB compression point of the VGA versus small signal gain. The input compression point improves linearly as the gain is reduced which was expected due to the output swing reduction. When the gain is lower than −2 dB, the slope of the gain curve changes and the input compression point appears to improve almost exponentially. This slope change beyond that point occurs because the amplifier gain is expanding as the input...
3.6 Phase Rotators

The signal amplitude is increased, instead of compressing.

3.6.2. 130-nm SiGe BiCMOS, 77 GHz Phase Rotator

The SiGe BiCMOS phase rotator is illustrated in figure 3.14. It is also composed of two Gilbert cell VGAs, identical to those presented in section 3.5.2. The outputs of the two VGAs are added in current at the output 3:1 transformer. The 3:1 transformer features a primary inductance $L_p = 140 \, \text{pH}$, a secondary inductance $L_s = 50 \, \text{pH}$ and a coupling factor $k = 0.7$.

Figure 3.15a shows the simulated $S_{21}$ and $S_{11}$ of the VGA versus $\Delta V_{\text{ctrl}}$ at 77GHz. It can be seen that the maximum gain is 10dB with more than 50dB of gain control. When $\Delta V_{\text{ctrl}} = 0$, the quad transistors are balanced (equal current flows through all of them) and as a result, the gain is theoretically zero, although in practice this is going to be limited by phase imbalance of the differential inputs and mismatch between the transistors. The input matching varies by about 7dB across the whole gain control range. However, it remains reasonably well matched with $S_{11} = -8.5 \, \text{dB}$ at the worst case.

Figure 3.15b illustrates the simulated phase of $S_{21}$ versus $\Delta V_{\text{ctrl}}$. The phase is relatively constant in the [-100 mV,0] and (0,100 mV] regions; around $\Delta V_{\text{ctrl}} = 0$, the phase rapidly switches by $180^\circ$ since the mixing quads also switch and the output phases are flipped (i.e. the transmission phase changes by $180^\circ$). This switching also highlights the fact that the VGA can attain both positive and negative gain.

Figure 3.16a details the simulated transmission phase variation as a function of the small signal gain ($|S_{21}|$) at 77GHz. The phase varies by a total of less $8^\circ$ when the gain of the VGA is reduced by 40dB. This simulation result validates the mathematical analysis of section 3.5.2 where the phase was shown to remain constant to a first order as the gain is varied.

Figure 3.12: Transfer characteristics versus gain control for the SiGe variable gain amplifier.
(a) Transmission phase versus small signal gain.

(b) $I_{P_{1dB}}$ versus small signal gain.

Figure 3.13: $S_{21}$ and $I_{P_{1dB}}$ variations as a function of small signal gain for the CMOS variable gain amplifier.

Figure 3.14: 130-nm SiGe BiCMOS, 77 GHz phase rotator.
3.6 Phase Rotators

Figure 3.15: Transfer Characteristics versus gain control for the SiGe Variable Gain Amplifier.

Figure 3.16: $S_{21}$ and $IP_{1dB}$ variations as a function of small signal gain for the SiGe variable gain amplifier.
Figure 3.17 depicts the input referred 1 dB compression point ($IP_{1dB}$) as a function of the small signal gain of the variable gain amplifier at 77 GHz. At the high gain states, the linearity of the VGA is limited by the output non-linearity; i.e., the output swing of the amplifier is large enough to drive the HBTs in saturation and the MOSFETs into triode. As the gain is reduced, the output swing is also smaller and as a result, the input compression point improves since the VGA can handle more input power. Eventually, at low gain states, the linearity is limited by the MOS transconductor’s input non-linear behavior; i.e. the input signal swing is large enough to drive the MOSFETs in the cut-off region. No further improvement in linearity can occur beyond this point.

3.7. 130-nm SiGe BiCMOS, 77 GHz Receiver with Phase Shifting

The block diagram of the 77 GHz Receiver with phase shifting is illustrated in Figure 3.17. The input signal is first amplified by a three stage Low Noise Amplifier (LNA), which accommodates 50 Ω input matching at its first stage, and single ended to differential conversion in its third stage. The differential signal from the output of the LNA drives two identical quadrature hybrids which were presented in section 3.4.2. The configuration of the two hybrids is also shown in figure 3.17 and is able to create two differential IQ signals at its output. The differential IQ signals are processed by the phase rotator (presented in section section 3.6.2) which performs the phase interpolation.

The schematic of the LNA is depicted in figure 3.18 and is similar with the one presented in [8]. The first two stages are biased for optimum noise figure whereas the last, cascode stage is biased for maximum gain. The last stage is loaded with a transformer which facilitates the single-ended to differential conversion. The two capacitors at the output are selected such that the single ended-impedance $Z_{out}$ looking at each one of the output ports $Out_p$ and $Out_n$ is
3.7 130-nm SiGe BiCMOS, 77 GHz Receiver with Phase Shifting

Figure 3.18: SiGe BiCMOS 77 GHz low noise amplifier.

approximately 50Ω which is the input impedance of the quadrature hybrids. The single-ended input impedance of the phase rotator is also matched to 50Ω which is approximately the output impedance of each of the I and Q ports of the hybrid.

In order to find the values of the phase rotator VGA control voltages that correspond to 16 phase states of 22.5° step, the following procedure is utilized. First, the control voltages of both VGAs are swept over their entire control range. From these data, the points that correspond to the 16 phase values and have equal amplitudes are extracted and their S-parameters are plotted over frequency. This procedure essentially corresponds to an approximate solution of equation (3.11), including any possible errors coming from the non-idealities of the I-Q splitter and phase rotator.

Figures 3.19a and 3.19b illustrate the simulated phase of $S_{21}$ over frequency for the different phase steps and the corresponding phase error respectively. The phase error of each phase state is less than $\pm 22.5° / 2 = \pm 11.25°$ in the 60 – 90GHz range.

Figure 3.19c reproduces the simulated $S_{21}$ over frequency for the different phase steps. During the design phase of the circuit, no layout parasitic extraction tool was available. In order to compensate for these un-modeled parasitic capacitances, the design was intentionally centered at 80GHz, slightly higher than the target 77GHz goal. The simulated peak-to-peak amplitude imbalance of the phase shifter is less than 2dB at 80GHz and has a worst-case value of 3dB at 60GHz. The 3dB bandwidth extends from 72 to 88GHz.

Figure 3.19d shows the simulated $S_{11}$ and $S_{22}$ of the the receiver versus frequency for the 16 phase states. $S_{11}$ remains varies slightly as the phase changes, a result which was expected
(a) Simulated phase vs. frequency characteristics of the 77-GHz receiver.

(b) Receiver phase error vs. frequency.

(c) Receiver $S_{21}$ vs. frequency.

(d) Receiver $S_{11}$ and $S_{22}$ vs. frequency.

(e) Simulated noise figure versus frequency of the SiGe 77-GHz receiver.

Figure 3.19: SiGe 77-GHz receiver simulations.
due to the high reverse isolation of the LNA. Nevertheless, its value is $-12\,\text{dB}$ at 80GHz which is relatively poor for the case of low noise receivers. The reason for this design inconsistency was the fact that the value of the input pad capacitance was overestimated and the inductor at the input of the LNA was larger than it should have been. The output reflection coefficient $S_{22}$ varies from $-12\,\text{dB}$ to $-18\,\text{dB}$ at 80GHz. However, the bandwidth over which $S_{22}$ is better than $-10\,\text{dB}$ is relatively narrow.

Figure 3.19e illustrates the simulated noise figure of the receiver versus frequency of the receiver. Although this simulation is generally unreliable because of the lack of modeling of noise correlation in the transistor model [42], it provides an estimate of the noise figure, typically a few dB higher than the expected measured one.

### 3.8. 65-nm CMOS, 94 GHz Transmitter with Phase Shifting

The block diagram of the 65-nm CMOS, 94 GHz transmitter is illustrated in figure 3.20. The input signal under phase shift is first amplified by a two stage cascode buffer shown in figure 3.21a. The buffer, apart from amplifying the input signal, provides input matching to 50Ω and output matching to 75Ω which is the input resistance of the following all-pass polyphase filter (presented in section 3.4.1).

The input buffer utilizes the topology discussed in [43] and features input shunt-series transformer feedback matching to 50Ω. The output transformer, apart from matching to 75Ω, it facilitates single-ended-to-differential conversion. It consumes a total of 16mA from 1.2V power supply.

In order to assure constant 75Ω loading of the all-pass polyphase filter, differential buffers were inserted between its output and the input of the phase rotator. The schematic of the differential buffers is shown in figure 3.21a, where a cascode topology was preferred due to its increased reversed isolation. This isolation is highly desirable since it shields the filter from any input impedance variation that might occur in the phase rotator. The 75Ω input matching network is formed by employing series-series inductive feedback, formed by the two 85pH and 90pH inductors. 130pH series peaking inductors are inserted between the common source and
common base transistors in order to increase the gain. The output matching network is formed by the 72\,\text{pH} shunt inductors and 44\,\text{fF} series capacitors. Each differential buffer consumes 10 mA from 1.2 V power supply.

After the buffered polyphase filter, the phase rotator, which was presented in section 3.6.1, completes the phase interpolation and generates the desired phase shift. The phase shifted signal is then fed to a 4-stage medium-power power amplifier shown in figure 3.22. The power amplifier was presented in [44] and features two input cascode stages followed by an AC-coupled cascode stage that maximizes the signal swing at the output node. To ensure reliable operation, the final common-gate stage is implemented with a low-power (LP) transistor, which has a thicker gate oxide than the general purpose (GP) MOSFETs used elsewhere, making it more immune to degradation due to large voltage swings. The power amplifier draws 65 mA from 1.2 V power supply. It was measured as a separate breakout and exhibits small signal gain of 7\,\text{dB} at 90 GHz and a saturated output power of +3 dBm.

A similar simulation methodology as in the 77 GHz receiver was followed for the 94 GHz CMOS transmitter. Figures 3.23a and 3.23b illustrate the simulated phase of $S_{21}$ over frequency for the different phase steps and the corresponding phase error respectively. The phase error of each state remains below $\pm 11.25^\circ$ in the 86 – 97 GHz range.

Figure 3.23c reproduces the simulated $S_{21}$ over frequency for the different phase steps. The design was purposefully centered at 90 GHz instead of 94 GHz since the layout parasitic extractor provided with the technology tends to overestimate the parasitic capacitances in MOSFETs.
This usually results in a design being centered slightly higher than simulated. The measurement capabilities with the available VNA extend up to 94GHz and had the design ended up higher than 94GHz, measurements at peak gain would have been impossible. The peak-to-peak amplitude imbalance is 3dB at 90GHz while the peak gain is 16dB.

Finally, figure 3.23d shows the simulated reflection coefficients $S_{11}$ and $S_{22}$ over frequency for the different phases. Due to the reverse isolation provided by the input buffer and power amplifier, any variation of the phase rotator impedance does not affect the reflection coefficients. Both simulated $S_{11}$ and $S_{22}$ remain below $-10$dB between 90 and 100GHz.
(a) Simulated phase vs. frequency characteristics of the 94-GHz transmitter.

(b) Transmitter phase error vs. frequency.

(c) Transmitter $S_{21}$ vs. frequency.

(d) Transmitter $S_{11}$ and $S_{22}$ vs. frequency.

(e) Simulated input-output power characteristics of the transmitter at 94 GHz.

Figure 3.23: CMOS 94-GHz transmitter simulations.
4 Characterization

4.1. 77 GHz Receiver with Phase Shifting

The 77GHz receiver was fabricated in STMicroelectronics’ BiCMOS9MW process. The die photo is illustrated in figure 4.1. The circuit occupies $660 \times 690 \mu m^2$ including the pads and $150 \times 500 \mu m^2$ without pads. The layout configuration was purposefully arranged so that the circuit has a narrow and long shape. This configuration would be necessary in order to vertically stack several of these receivers and add their outputs to form a phased-array. The total measured power consumption is 128 mW from 1.5 V and 2.5 V power supplies.

First, On-wafer S-parameter measurements were carried out in the 55−94GHz range using a Wiltron 360B Vector Network Analyzer (VNA) and 110-GHz Cascade Infinity probes. The LRRM (Line-Reflect-Reflect-Match) calibration method was used in order to correct the non-idealities of the VNA and the 110GHz setup required to connect and probe the circuit. The analog control voltages of the phase shifters were provided by an Agilent 4155 semiconductor parameter analyzer, as shown in figure 4.2a.

The S-parameter measurement methodology was similar with the simulation methodology. The control voltages of the variable gain amplifiers were swept over their entire range and S-parameter measurements were conducted at each point. Then, the required phase states were extracted. Figures 4.3a and 4.3b illustrate the measured phase and phase errors over frequency when the phase is varied from $0^\circ$ to $360^\circ$ in sixteen $22.5^\circ$ steps. Good agreement is observed with the corresponding simulation results of figures 3.19a and 3.19b. The phase error remains below $6^\circ$ in the 72−76GHz range and below $8^\circ$ in the 70−77GHz range which is the 3-dB bandwidth of the entire receiver. Figure 4.3c shows the measured amplitude of $S_{21}$ for the corresponding phase states. The maximum gain is 17 dB with less than 2 dB of peak-to-peak gain imbalance. A shift of 6 GHz in the center frequency of the receiver is observed compared with simulation (figure 3.19c) as well as narrower 3 dB bandwidth. Although the receiver was originally centered at higher frequency to account for possible shifts, the frequency shifted by 4 GHz.
more than was originally anticipated. Furthermore, the narrower 3-dB receiver bandwidth is a result of higher inductor Q factor than simulated.

After the S-parameter characterization, the receiver input compression point was measured using the setup of figure 4.2b. A 74GHz signal is generated using a lower frequency source and a frequency multiplier. In order to control the amplitude of the signal at the input, a W-band variable attenuator is used. Figure 4.3d illustrates the measured output versus input power of the receiver at 74GHz. The input 1dB compression point is $-22$ dBm. Although no linearity simulations of the receiver were possible due to convergence problems, based on the VGA linearity simulations of figure 3.16b, it can be concluded the input 1 dB compression point is
Figure 4.2: 77 GHz receiver measurement setups.
Figure 4.3: 77GHz receiver measurement results.

Figure 4.4: 77GHz receiver measured noise figure.
limited by the LNA linearity. In case a better compression point is required, which is likely the case for radar receivers, gain control could be implemented in the LNA.

Finally, the noise figure of the receiver was measured using the setup of figure 4.2c. An ELVA W-band noise source was used to provide the input to the receiver while an external downconverter and noise figure analyzer where connected to the output. Noise figure measurements in the 75 – 87.5 GHz are possible with this setup. Figure 4.4 illustrates the measured noise figure of the receiver in this range. Its minimum value is 7 dB which is in good agreement with simulation.

Table 4.1 below summarizes the measured performance of the 77 GHz receiver.

<table>
<thead>
<tr>
<th></th>
<th>Measured</th>
<th>Simulated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>17 dB</td>
<td>17 dB</td>
</tr>
<tr>
<td>3 dB Bandwidth</td>
<td>7 GHz (70 – 77 GHz)</td>
<td>16 GHz (72 – 88 GHz)</td>
</tr>
<tr>
<td>Phase Shift</td>
<td>0° – 360° (22.5° steps)</td>
<td>0° – 360° (22.5° steps)</td>
</tr>
<tr>
<td>RMS phase error @ 3dB BW</td>
<td>&lt; 4°</td>
<td>&lt; 3.5°</td>
</tr>
<tr>
<td>p-p phase error @ 3dB BW</td>
<td>&lt; 8°</td>
<td>&lt; 10°</td>
</tr>
<tr>
<td>p-p phase error @ maximum gain</td>
<td>5°</td>
<td>6°</td>
</tr>
<tr>
<td>p-p gain error @ maximum gain</td>
<td>2 dB</td>
<td>2 dB</td>
</tr>
<tr>
<td>IP1dB</td>
<td>-22 dBm</td>
<td>did not converge</td>
</tr>
<tr>
<td>NF</td>
<td>7 dB</td>
<td>7 dB</td>
</tr>
</tbody>
</table>

Table 4.1: Measured versus simulated performance of the 77 GHz receiver.

4.2. 94 GHz Transmitter with Phase Shifting

The 94 GHz transmitter was fabricated in STMicroelectronics’ 65 nm CMOS process. The transmitter was part of a larger chip as shown in figure 4.5 where the output of the power amplifier is connected to a pad through a \( \lambda / 4 \) SPTD switch [45]. The complete transmit chain consumes 142 mW from 1.2 V supply while occupying 800 × 150 \( \mu m^2 \).

In order to conduct S-parameter measurements, the input and output are connected to the Wiltron VNA while the analog controls to the Agilent 4155 semiconductor parameter analyzer. The controls of the SPDT switch and the digital controls of the phase shifter are loaded to an on-chip shift register through a pattern generator. Figure 4.6a illustrates the measured phase versus frequency while figure 4.6b shows the phase error over frequency of the transmitter for the 16 different phase states. The phase error reaches a minimum of 4° at 90 GHz, at the center of the PA bandwidth. Good agreement with the corresponding simulations of figures 3.23a and 3.23b is observed.

Figure 4.6c illustrates the amplitudes of \( S_{21}, S_{11} \) and \( S_{22} \) over frequency for the different phases. A maximum small-signal gain of 3.8 dB is demonstrated, with a maximum peak-to-
peak gain variation among all states of less than 4 dB, at 90 GHz. Compared with the simulated $S_{21}$ of figure 3.23c, the center frequency of $S_{21}$ is at exactly the same frequency. However, the gain is approximately 10 dB lower and the amplitude imbalance slightly higher. This relatively large inconsistency between measurement and simulated $S_{21}$ has been a subject of extensive investigation by the author. Different simulation models were tested along with different extraction methods for parasitics with limited success in reproducing the measured gain reduction. Furthermore, several different measurement techniques were attempted under various conditions. What was observed is that the measured gain increased significantly when the power supply was raised to values higher than 1.2 V. Although this is case with every CMOS circuit that utilizes cascodes from 1.2 V, it may also be an indication of a layout inconsistency that causes an IR drop in the on-chip power supply distribution. This is especially true since the transmitter is a part of a more complicated chip in which designing a supply distribution has been extraordinarily difficult.
4.2 94 GHz Transmitter with Phase Shifting

(a) Transmitter measured phase vs. frequency.

(b) Transmitter measured phase error vs. frequency.

(c) Transmitter measured $S_{21}$ vs. frequency.

Figure 4.6: 94GHz transmitter measurement results.
Table 4.2: Measured versus simulated performance of the 94GHz transmitter.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Gain</th>
<th>Phase Arrangement</th>
<th>Phase Error</th>
<th>Gain Error</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>34GHz</td>
<td>11 dB</td>
<td>0° – 360°, 16 steps</td>
<td>7° RMS</td>
<td>3 dB</td>
<td>[18]</td>
</tr>
<tr>
<td>24GHz</td>
<td>−11.3 dB</td>
<td>0° – 360°</td>
<td>-</td>
<td>2.4 dB</td>
<td>[21]</td>
</tr>
<tr>
<td>12GHz</td>
<td>3.5 dB</td>
<td>0° – 360°, 16 steps</td>
<td>5.5° RMS</td>
<td>1 dB</td>
<td>[19]</td>
</tr>
<tr>
<td>20GHz</td>
<td>−4.6 dB</td>
<td>0° – 360°, 16 steps</td>
<td>6.5° RMS</td>
<td>1.1 dB RMS</td>
<td>[36]</td>
</tr>
<tr>
<td>60GHz</td>
<td>−5.5 dB</td>
<td>0° – 180°</td>
<td>-</td>
<td>3.3 dB</td>
<td>[46]</td>
</tr>
<tr>
<td>60GHz</td>
<td>−2 dB</td>
<td>0° – 360°</td>
<td>3° RMS</td>
<td>-</td>
<td>[46]</td>
</tr>
<tr>
<td>60GHz</td>
<td>−9.4 dB</td>
<td>0° – 180°, 8 steps</td>
<td>9.2° RMS</td>
<td>6.2</td>
<td>[47]</td>
</tr>
<tr>
<td>77GHz</td>
<td>−19.2 dB</td>
<td>0° – 360°, 16 steps</td>
<td>11° RMS</td>
<td>7.4 dB</td>
<td>[48]</td>
</tr>
<tr>
<td>74GHz</td>
<td>17 dB</td>
<td>0° – 360°, 16 steps</td>
<td>4° RMS</td>
<td>2 dB</td>
<td>This work</td>
</tr>
<tr>
<td>90GHz</td>
<td>3.8 dB</td>
<td>0° – 360°, 16 steps</td>
<td>5° RMS</td>
<td>4 dB</td>
<td>This work</td>
</tr>
</tbody>
</table>

Table 4.3: Comparison of different phase shifters.

The output power of the transmitter was measured with a similar setup as the one described in figure 4.3d. However, due to the unavailability of a signal source with high output power at 90GHz, it was impossible to drive the transmitter into compression and determine the $OP_{1dB}$ and $P_{SAT}$.

Table 4.2 below summarizes the measured performance of the 94GHz transmitter.

### 4.3. Comparison with Relevant Work

Table 4.3 provides a comparison of different phase shifters. Although this comparison is not absolute since the phase shifters are at different frequencies and target different applications, it provides a summary of the phase and amplitude errors achieved by different phase shifters found in the literature. Furthermore, it illustrates that the results presented in this work are of equal performance or even better than lower frequency phase shifters.
In this thesis, different phase shifter architectures were investigated and their potential for realization in IC form and operation in mm-wave frequencies was assessed. Although many phase shifter topologies have been proposed during the last 60 years, only a handful of them are capable to satisfy both requirements. The phase interpolation phase shifter was found to be the best candidate due to its compact size, its ability to have gain and generate phase shifts in the $0^\circ - 360^\circ$ range.

Two circuits are required to realize the phase interpolation phase shifters: An I-Q splitter and a variable gain amplifier. Extensive bibliographic studies were also conducted in order to pick the proper topologies for both building blocks. Furthermore, two different I-Q splitters and variable gain amplifiers were implemented in two different IC processes. The theoretical analysis of the interpolation phase shifter revealed that the variable gain amplifiers need to have as constant phase shift as possible when their gain varies. Variable gain amplifiers that satisfy this requirement have not been extensively studied in the literature.

5.1. Contributions

The first CMOS phase shifter operating above 60GHz has been presented in this thesis. A transmitter with phase shifting capabilities was also developed by utilizing the phase shifter. The transmitter was able to generate phase shifts of $0^\circ - 360^\circ$ in 22.5° steps. Although this transmitter was developed in October 2007, to the best of the author’s knowledge, no other CMOS or SiGe BiCMOS phase shifter in the same frequency range has been reported up to this date.

A 77GHz SiGe BiCMOS receiver has also been developed. There have been other 77GHz phase shifters published prior to this receiver, the proposed receiver was the first to utilize phase shifting in the RF front-end and as a result, the first to show calibrated VNA $0^\circ - 360^\circ$ phase shift in this frequency range.

In the circuit design level, two novel phase rotator topologies have been proposed. First,
a 65nm CMOS rotator that facilitates both coarse digital phase control with respect to the selected quadrant and analog fine control within the quadrant. Second, a SiGe BiCMOS rotator based on MOS-HBT cascode variable gain amplifiers and exhibits improved phase stability and linearity due to the constant current through the MOS transconductors. Moreover, the feasibility of a compact, low-loss 3dB quadrature hybrid at W-band frequencies was proven. The hybrid offers significantly reduced size than its transmission line counterparts while exhibiting very broadband characteristics.

5.2. Future Work

The phase shifters presented in this thesis operate in an analog (or semi-analog) fashion and require extraction of the phase shift states during measurements because of possible component variations. Moreover, in a practical phased array system, there are several other sources of error, as illustrated in figure 5.1 [49]. Most of the error sources, such as antenna coupling, are out of the control of the circuit designer. As a result, calibration of the array is required [49]. This calibration procedure would also require an external mm-wave source in case the coupling between the antennas, line lengths and air interface are considered, which can be a costly and time consuming procedure.

Figure 5.1: Errors in phased array systems.

Future research could focus on the development of a calibration procedure that would avoid the use of an external source. A two step procedure, utilizing on-chip loopback through couplers or SPDT switches, and off-chip loopback through a reflector could be developed.
5.3. Publication

The results of this thesis were published in the IEEE RFIC 2009 Symposium [50].
Bibliography


