NetTM: Faster and Easier Synchronization for Soft Multicores via Transactional Memory

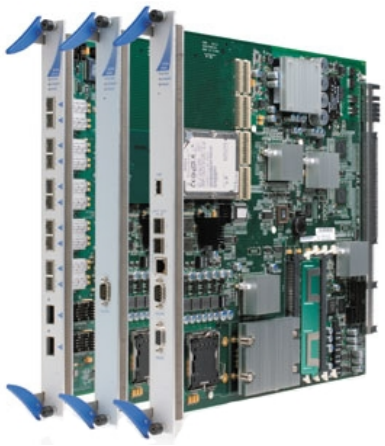
Martin Labrecque

Prof. Greg Steffan

University of Toronto

FPGA, February 27th 2011

Processors in FPGAs



FPGAs in Telecommunications:

- Present in most high-end routers
- More than 40% of FPGA market

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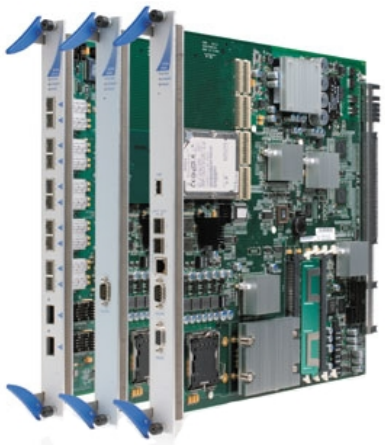

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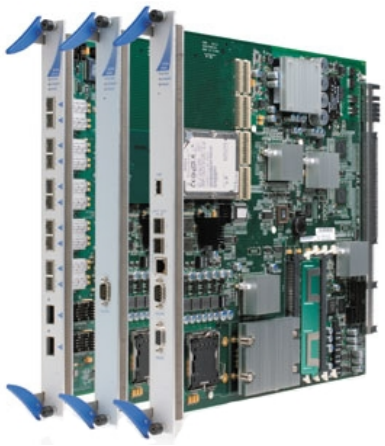

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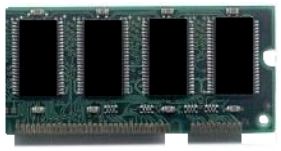
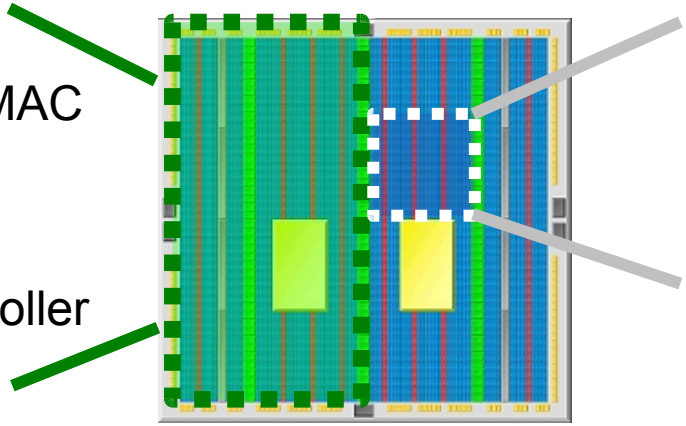
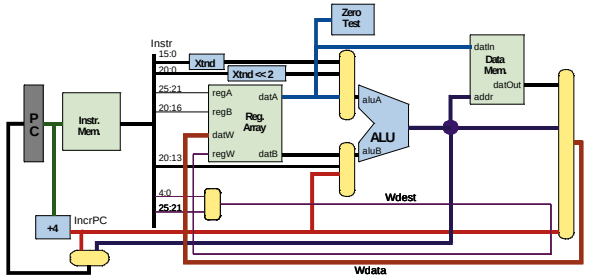
Ethernet MAC



DDR controller





Processor(s)

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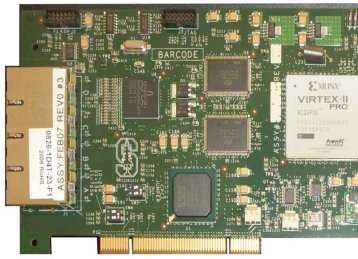
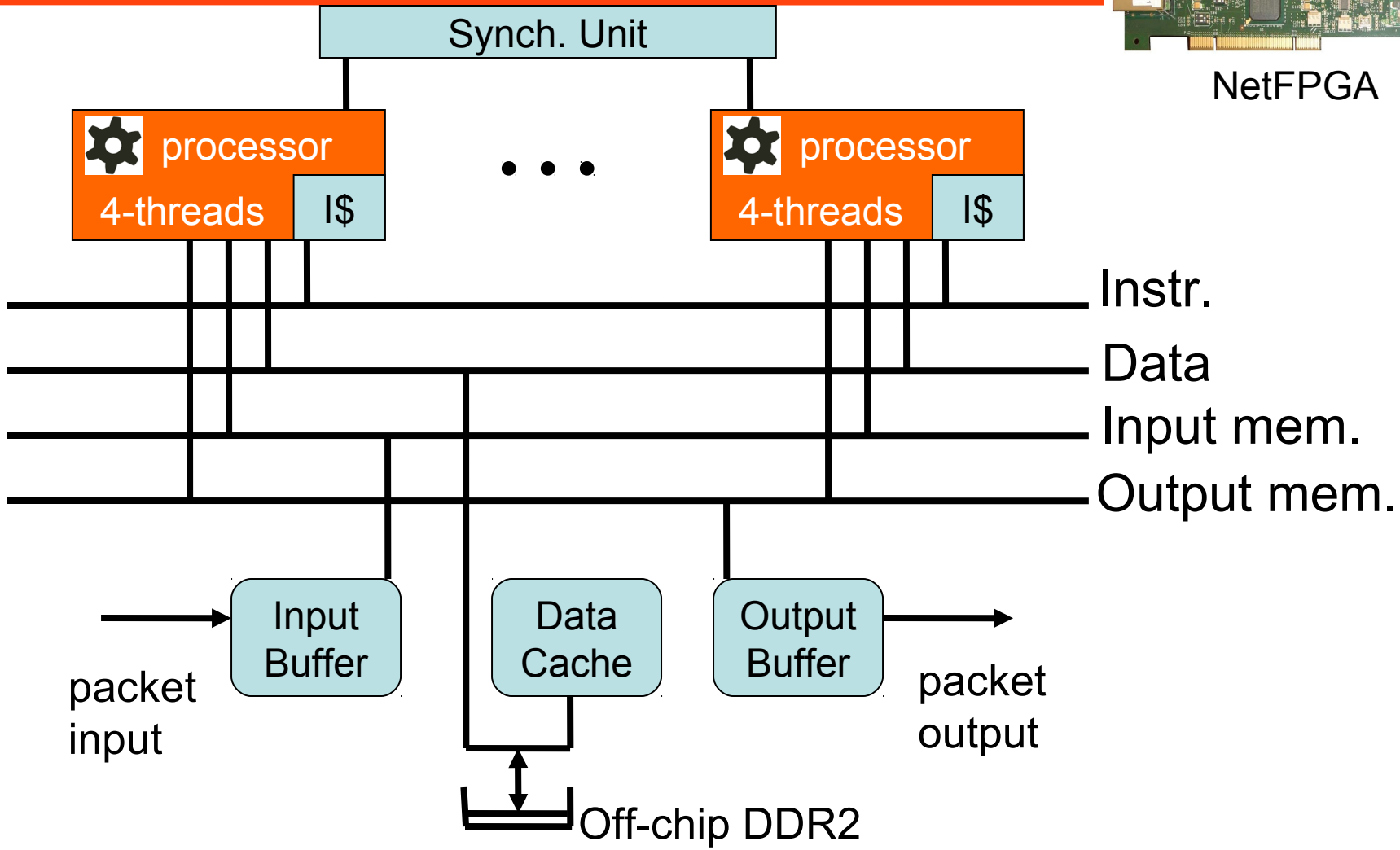
NetThreads: Our Base System



NetFPGA



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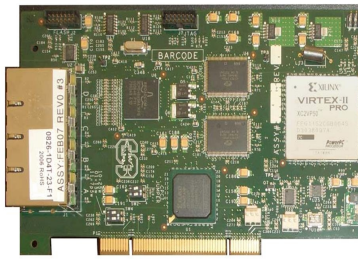

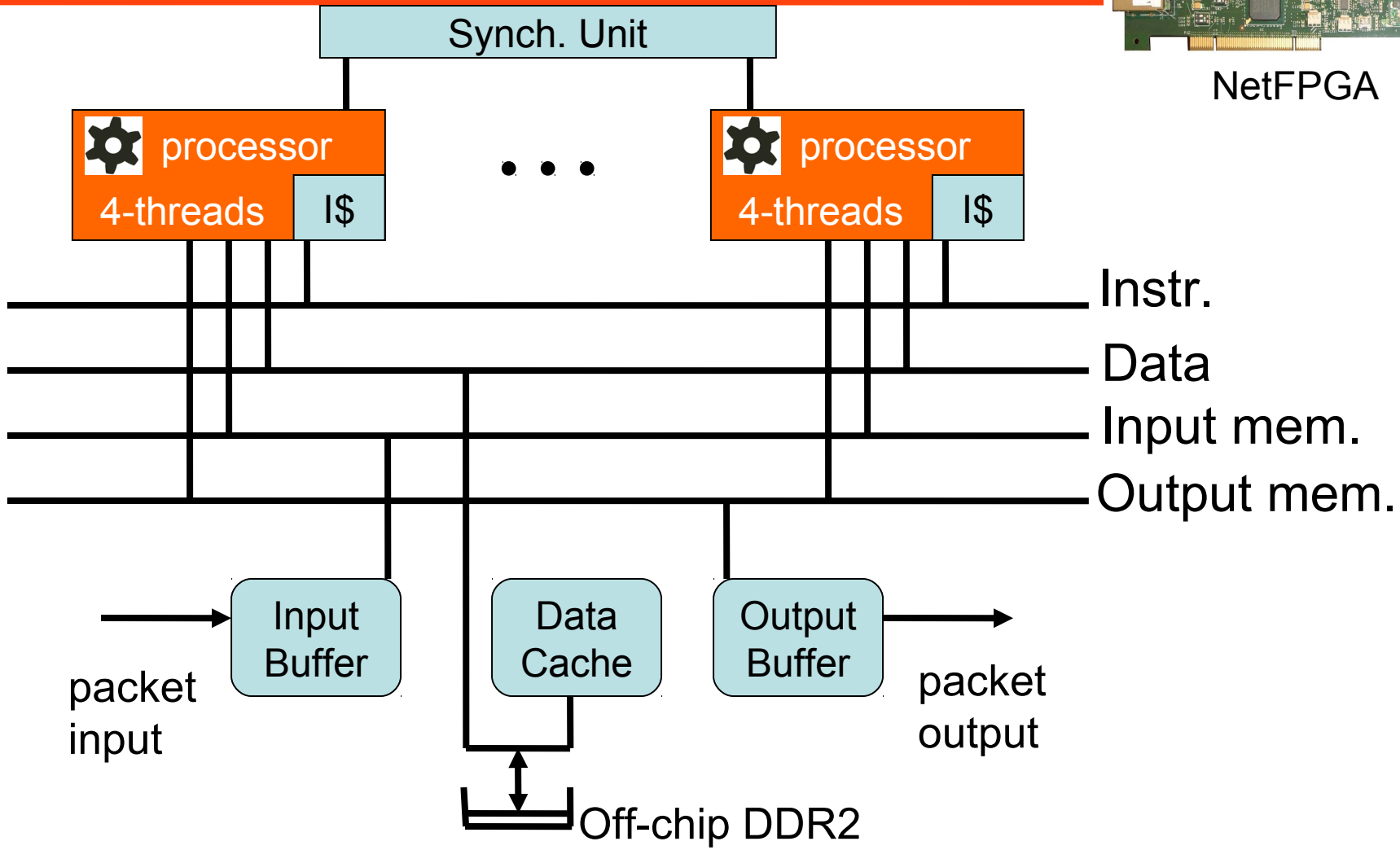

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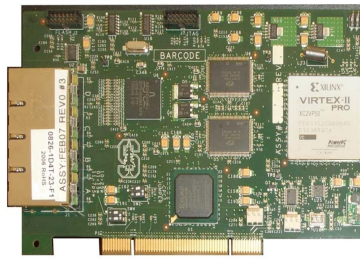

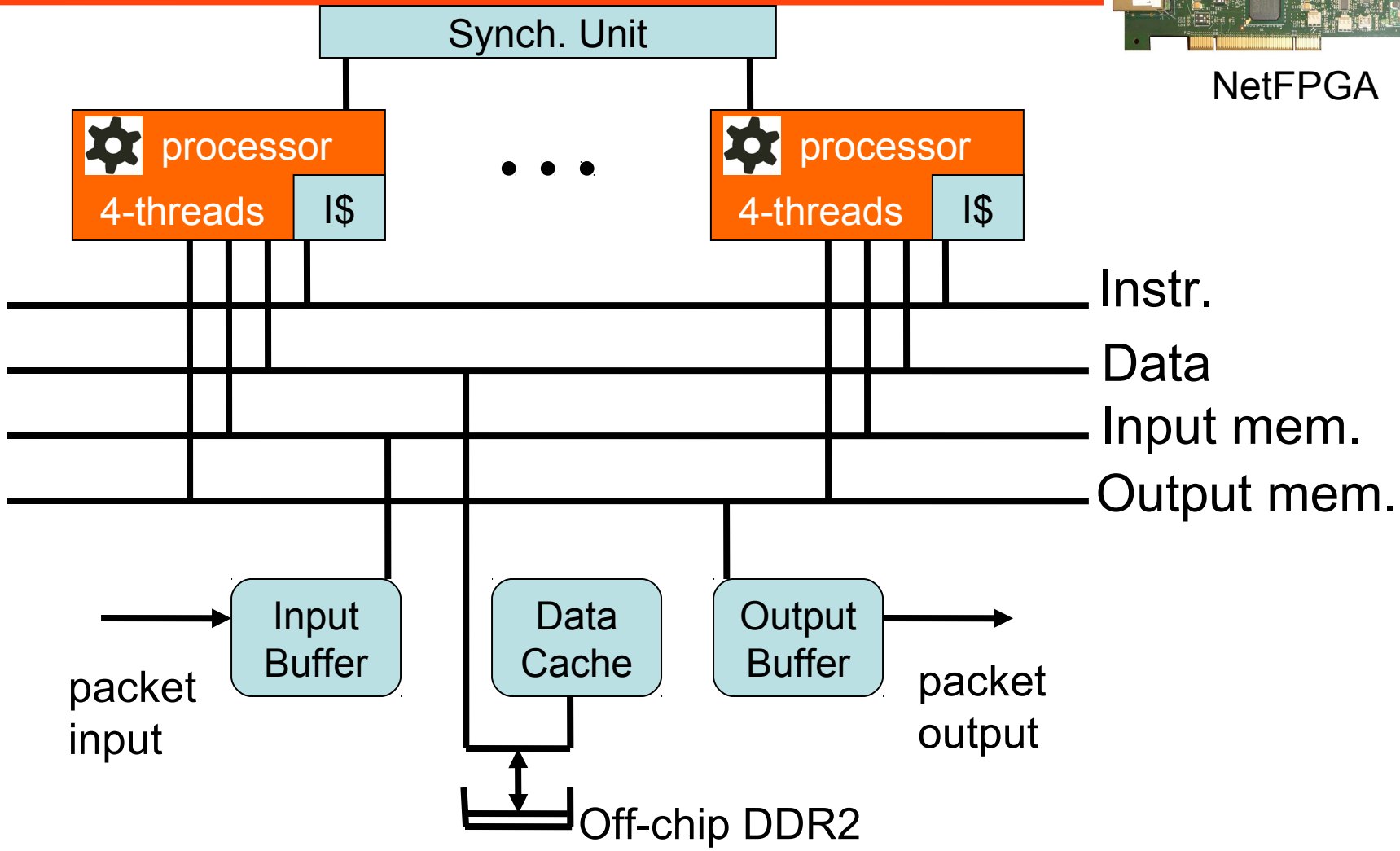

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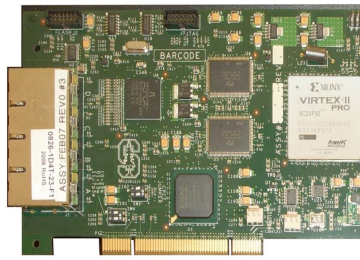

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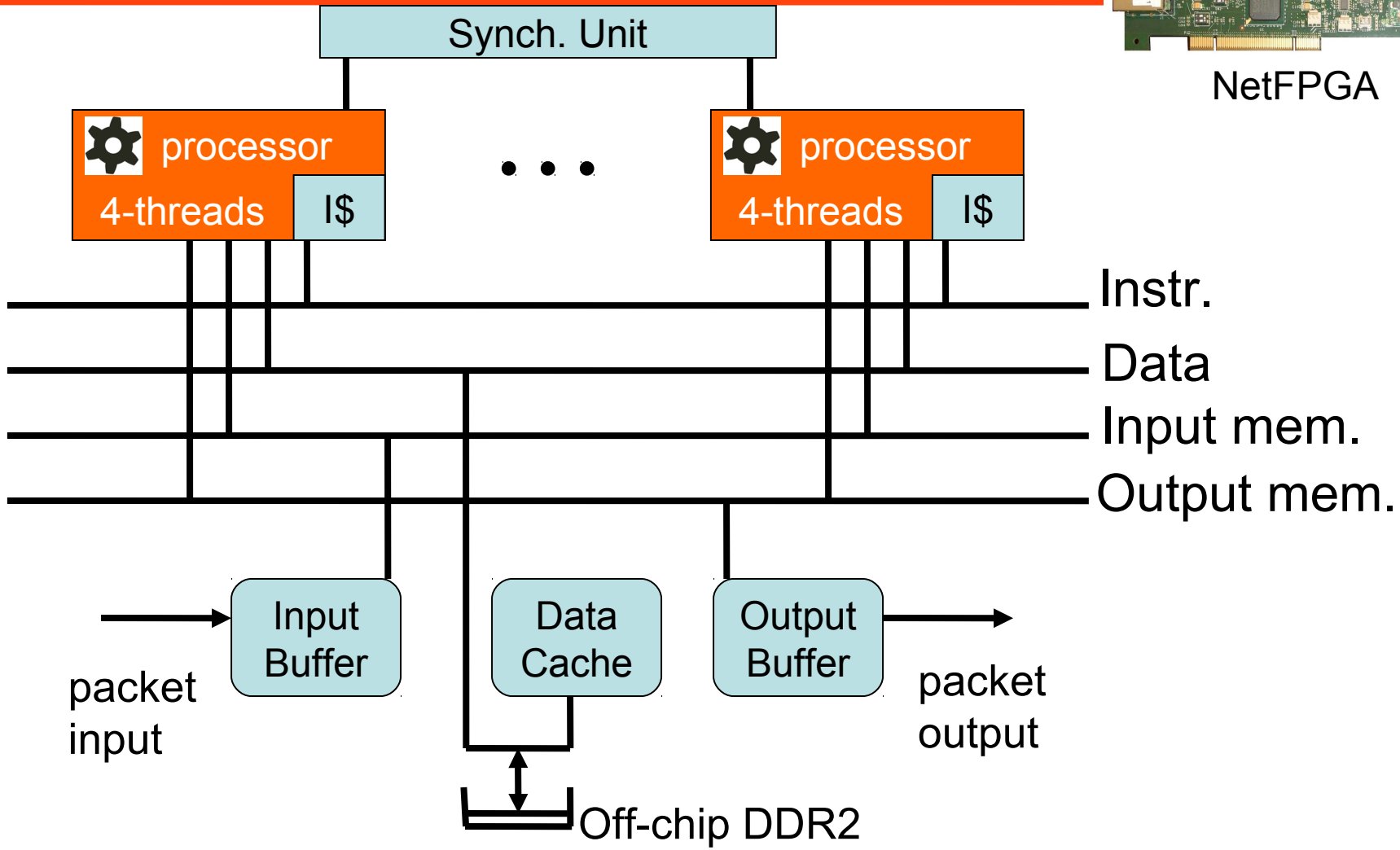

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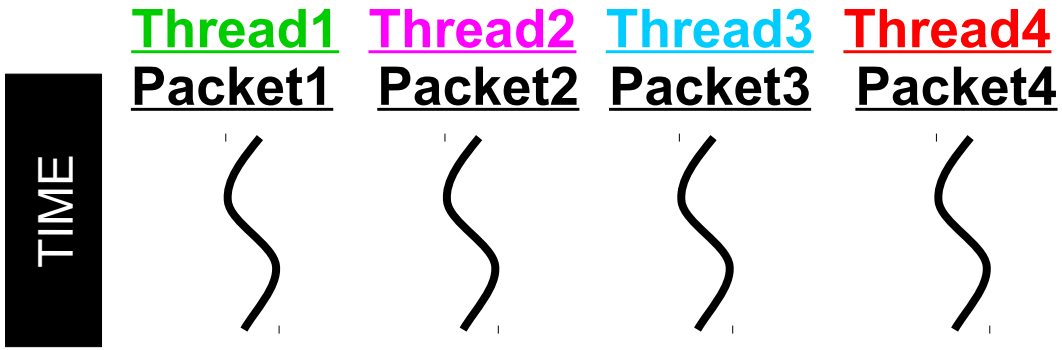
Released online: Google netfpga+netthreads

Parallelizing Stateful Applications

Ideal scenario:

Packets are data-independent and are processed in parallel



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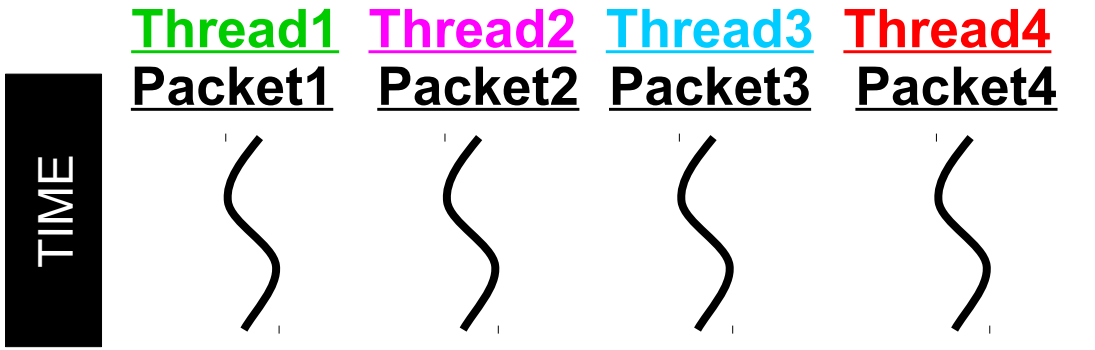

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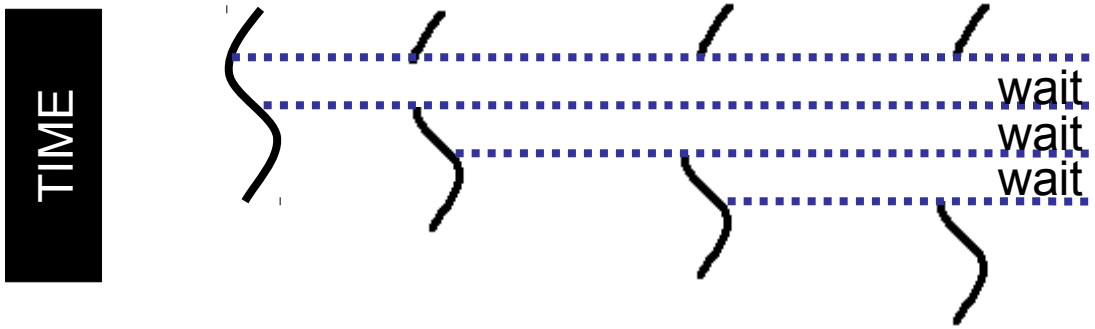
Programmers need to insert locks **in case** there is a dependence



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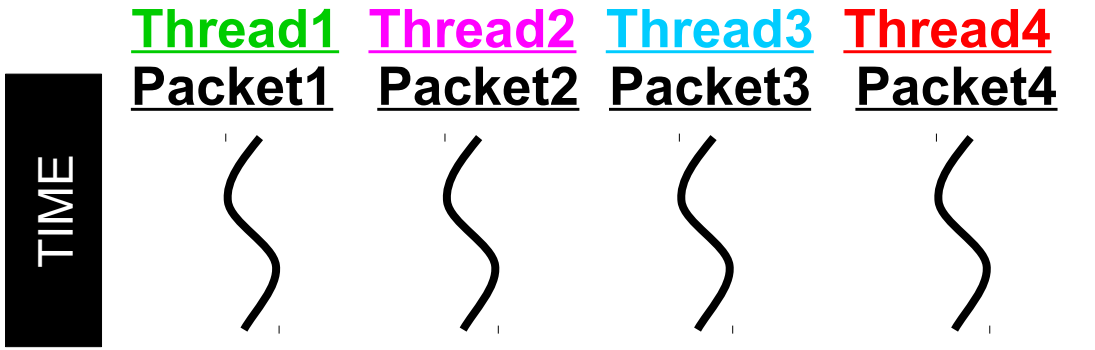

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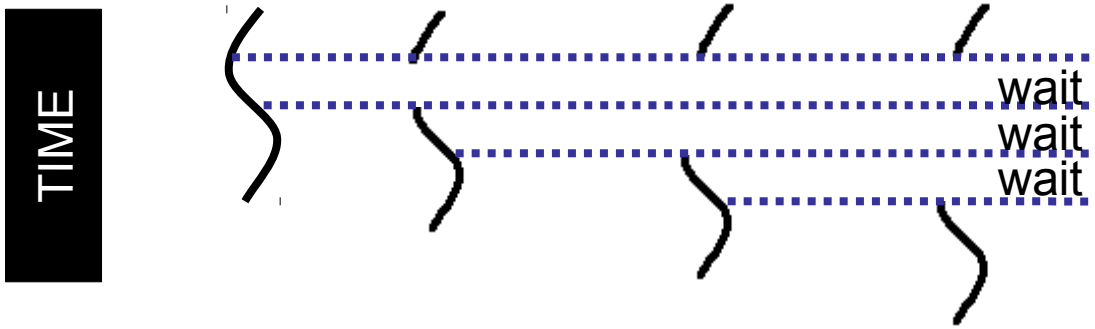

Experimental result: Synchronizing packet processing threads with fine/medium-grained global locks is overly-conservative 80-90% of the time [ANCS'10]

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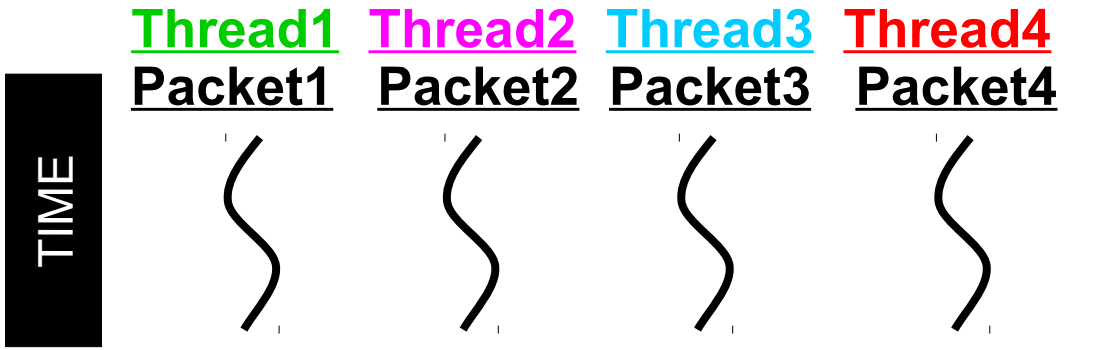

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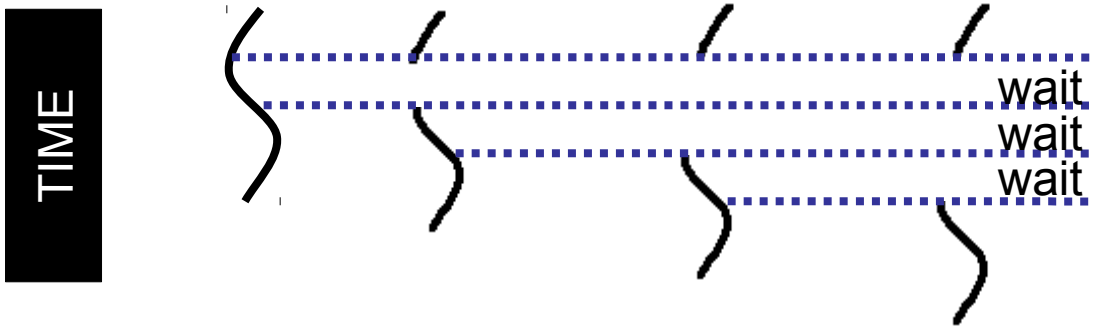
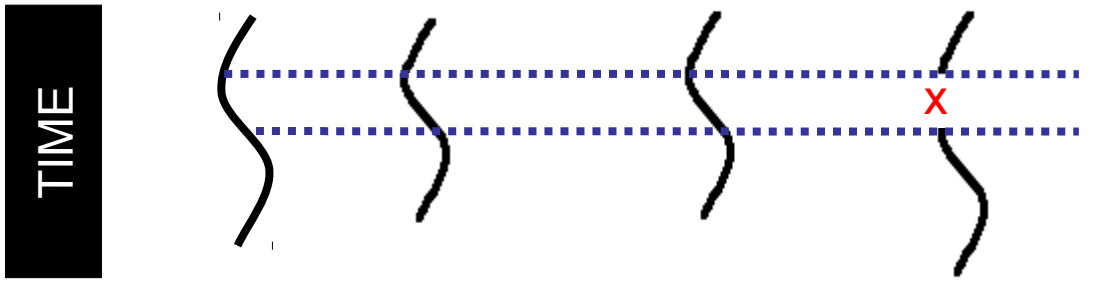
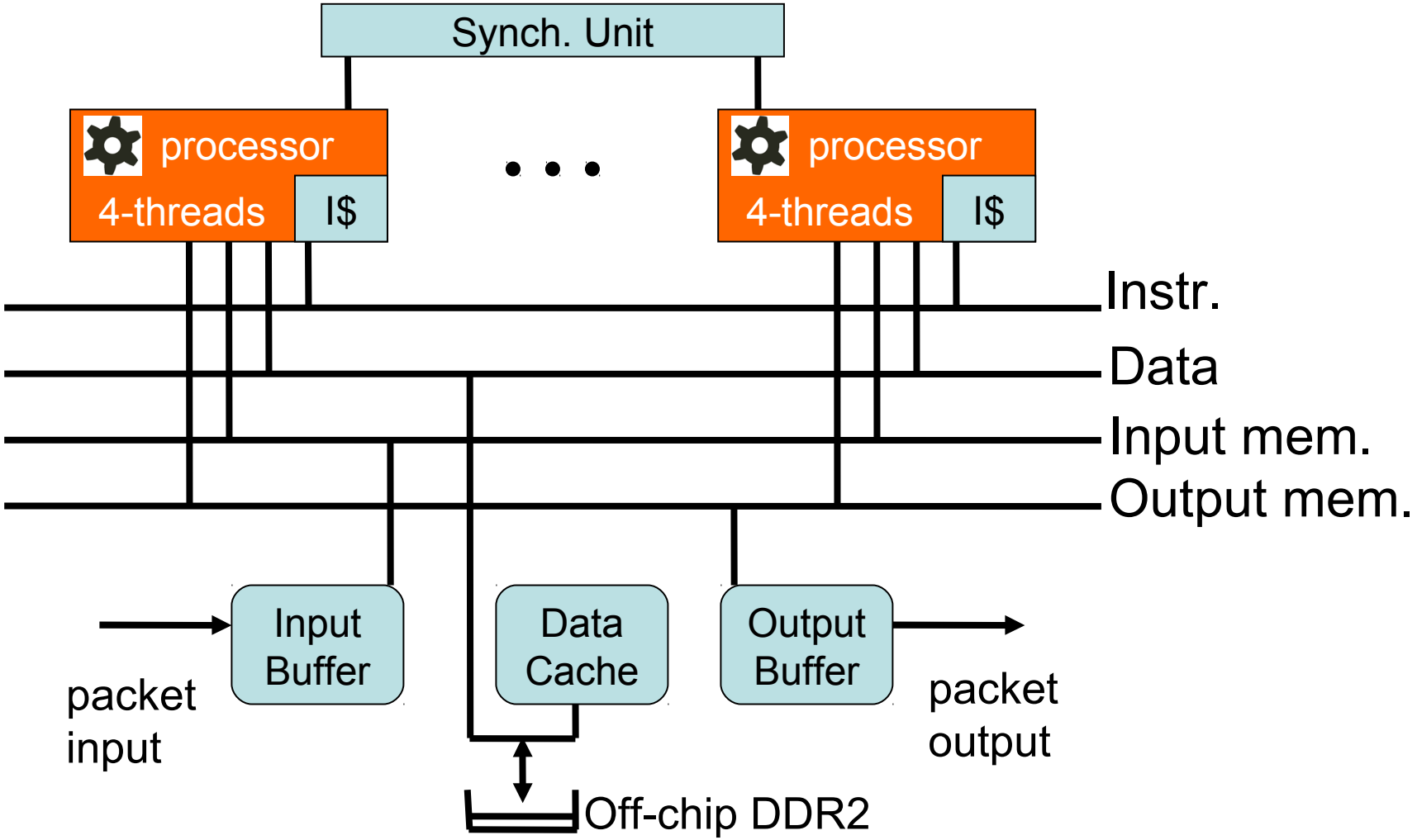


Transactional memory
Data-independent packets are processed in parallel



NetTM: extending NetThreads for TM



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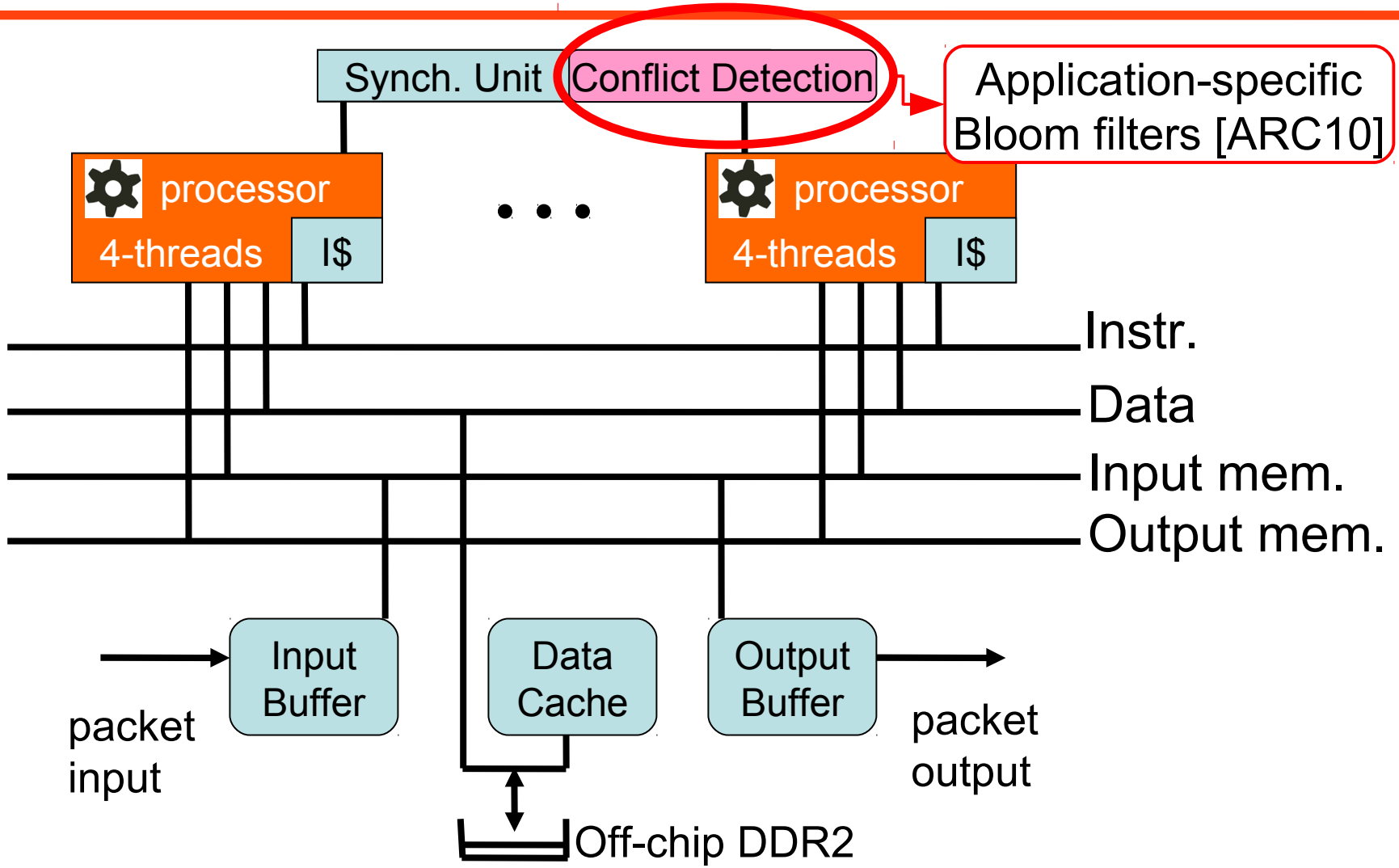

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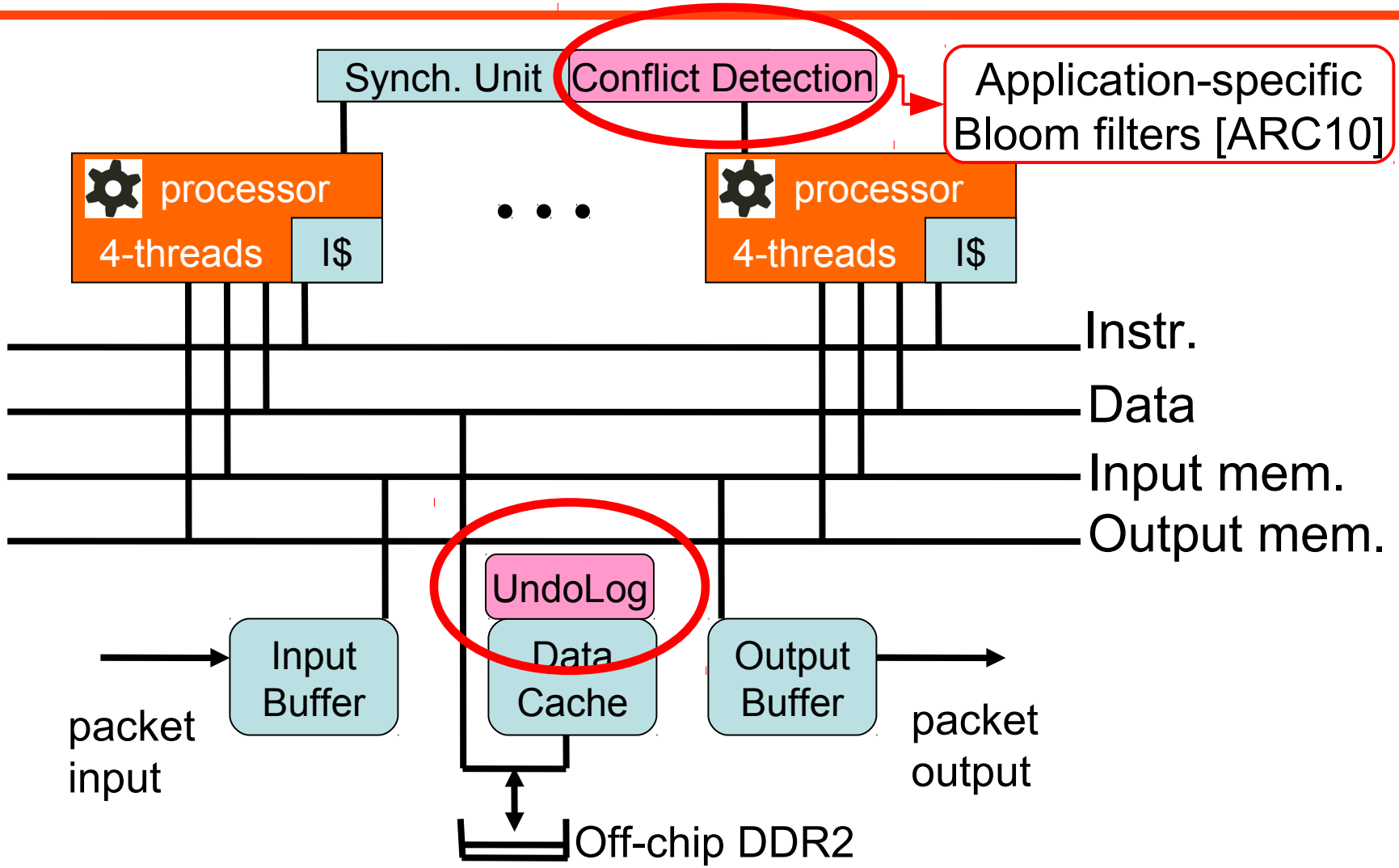

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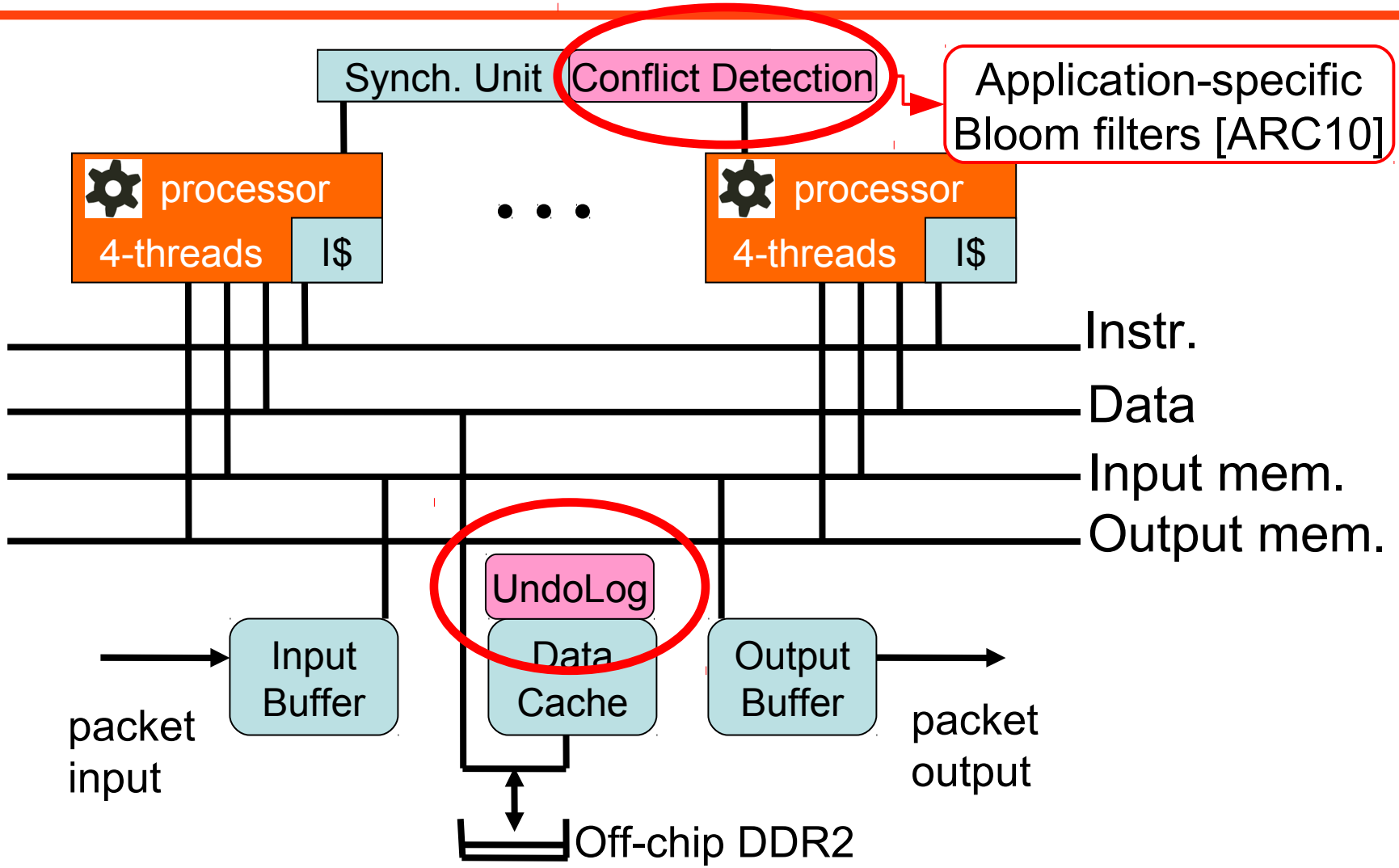

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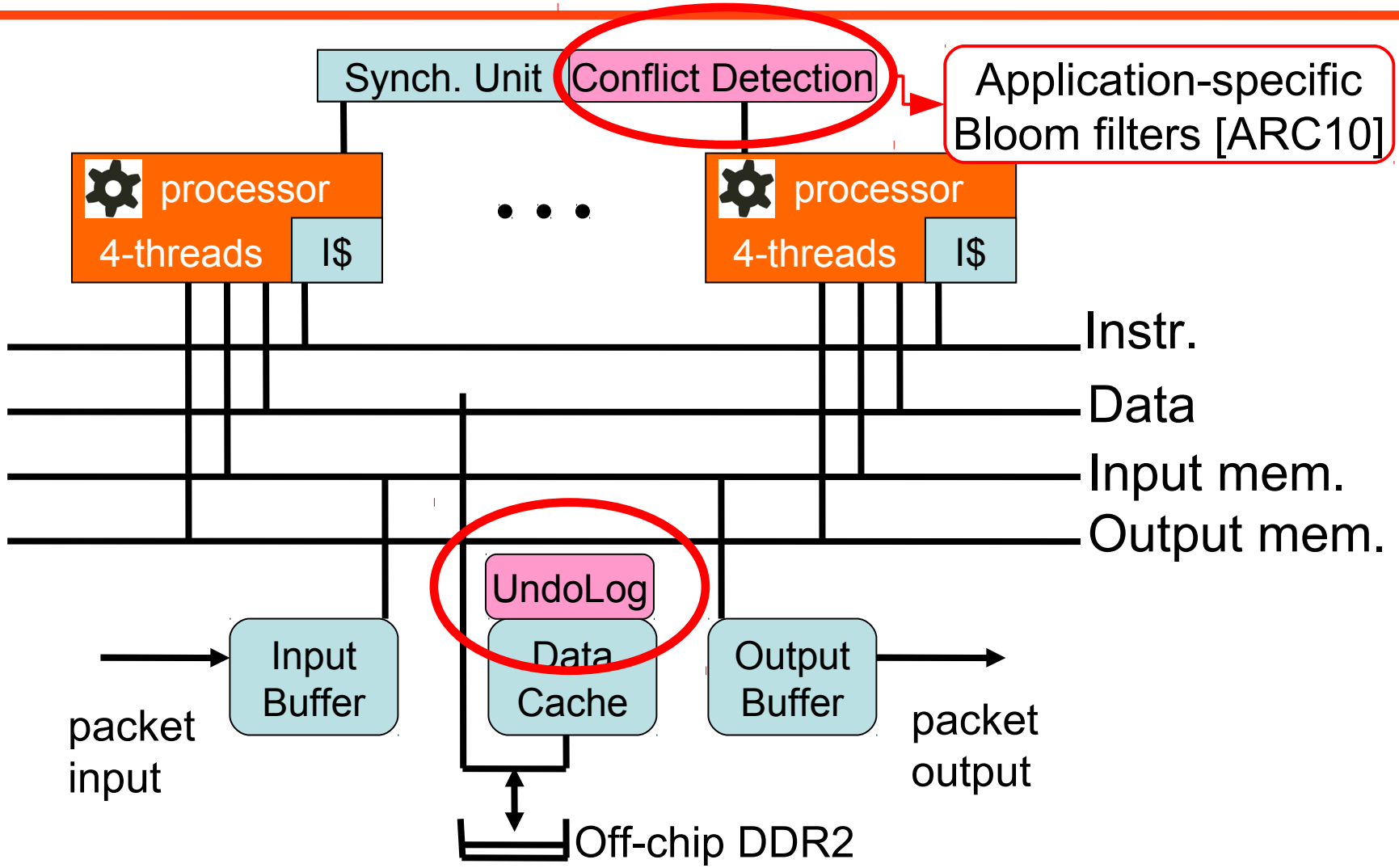

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- 4-LUT: +21% 16K BRAMs: +25% Preserved 125 MHz

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NetTM and NetThreads available online

Google : netfpga+netthreads

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