

A Sub-mW Spectrum Sensing Architecture for Portable IEEE 802.22 Cognitive Radio Applications

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Abstract—A low power integrating mixer successive approximation register (SAR) prototype chip for spectrum sensing is fabricated for portable transceivers targeting IEEE 802.22 cognitive radio applications. The integrating mixer SAR combines mixing, current-domain windowing, and integration to implement the short-time Fourier transform. Integration with programmable time constant is incorporated within the mixer by utilizing binary-weighted capacitive loads, which double as the sampling capacitors of a SAR ADC. The design operates over a frequency range of 0.05-1.25GHz, consumes 0.88mW from 1.1/1.2V supplies and obtains an average dynamic range (DR) of 25.7-27.9dB.

I. INTRODUCTION

Cognitive radios (CR) are reactive devices that identify unused spectrum segments and dynamically adjust their transmission characteristics into these segments while avoiding interference with licensed/primary users. Spectrum sensing is the enabling technology behind CR, which allows efficient spectrum utilization. The IEEE 802.22 standard specifies the air interface and cognitive medium access control for fixed and portable devices in the 54-862MHz DTV bands. Portable devices require spectrum sensing every 2s with an accuracy of -114dBm . One potential application is public safety networks, which require power efficient operation for mobile devices in order for emergency personnel to broadcast voice, data, and location services. The spectrum sensing component of recent mixed-signal implementations that target the DTV bands consume 17.5% to 24% of the total receiver power dissipation [1]–[3]. Low power spectrum sensing can result in a substantial overall power savings for CR transceivers.

In this work, we estimate the spectrum directly utilizing the short-time Fourier transform (STFT) in the analog-domain and incorporate a SAR ADC to provide a digital estimate. The STFT applies time-domain windowing to the Fourier transform that shapes its frequency response and restricts its integral to a finite time segment. The power spectrum can be calculated directly from the STFT while the detection bandwidth (DBW) is set by the applied window function. This work expands upon [6] from the same authors by utilizing an array of mixer cells to remove current-domain restrictions on the window function thereby reducing its side-lobe oscillations while binary-weighted load capacitors enable charge redistribution to be incorporated for a SAR ADC. The architecture results in power consumption an order-of-magnitude lower than previously reported methods based on energy detection [1]–[5] while obtaining spectral estimates over the full bandwidth (BW) within a few milliseconds.

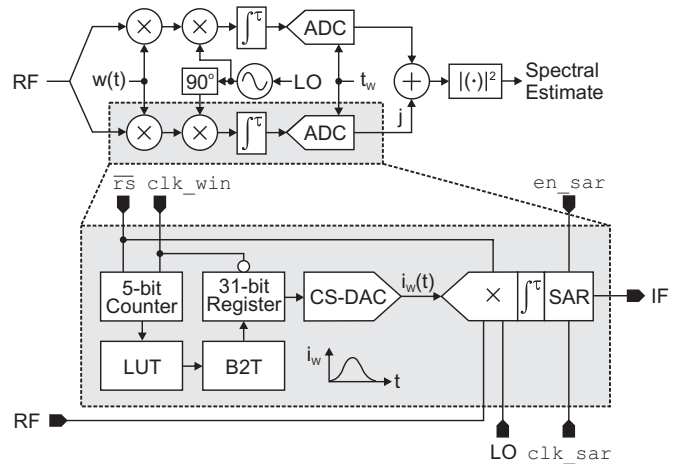


Fig. 1. Block diagram of the integrating mixer SAR illustrated for a single path of an STFT-based spectral estimate (chip implements both paths).

II. CONCEPT

The integrating mixer SAR implements the STFT in the analog-domain and digitizes its amplitude at the end of the integration period. The window function is implemented in the current-domain while integration is incorporated within the mixer by utilizing capacitive loads, which double as the sampling capacitors of a SAR ADC. There are three modes of operation: a *reset mode* where both terminals of the capacitors are connected to V_{DD} , resetting the accumulated signal and discharging the capacitors; an *integration/sample mode* where the capacitive loads provide bias current while integrating the AC signal; and a *conversion mode* where charge redistribution is applied to the sampled STFT signal across the binary-weighted capacitors of the SAR ADC.

The system block diagram is illustrated in Fig. 1, where $\overline{rs} = '0'$ and $\overline{rs} = '1'$ correspond to reset and integration/sample modes, respectively. The window function is generated by a 5-bit counter that cycles through the binary coefficients stored in a lookup table (LUT) each integration period at a frequency set by clk_win . A binary to thermometer encoder (B2T) with registered output drives a distributed 5-bit current-switching digital-to-analog converter (CS-DAC) that implements the window function in the current-domain and is mirrored to the integrating mixer. The en_sar signal triggers a SAR conversion at a frequency set by clk_sar and cannot switch modes until the conversion is complete.

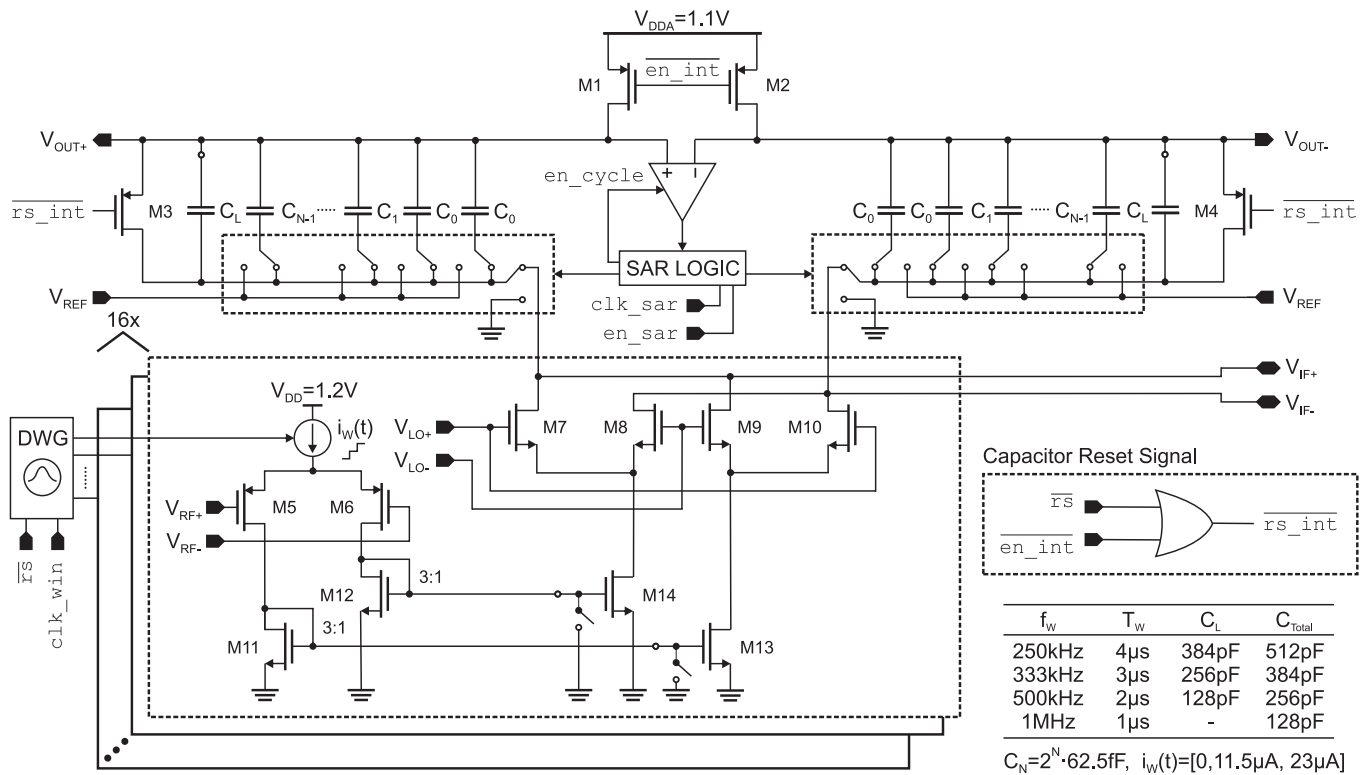


Fig. 2. Integrating mixer SAR schematic with switches in the integration/sample mode.

III. CIRCUIT DESIGN

A schematic of the proposed integrating mixer SAR is illustrated in Fig. 2. An array of 16 folded mixers with 3-level CS-DAC are driven by a digital window generator (DWG), which turns on/off individual cells to implement the window function in the current-domain. This removes current restrictions on the window function. The Hann function is selected for the window function and results in a DBW of $1.44 \cdot f_w$, where f_w is the window frequency. During a conversion, V_{DDA} is disconnected from the circuit while $\overline{rs_int}$ prevents the capacitors from being reset when $\overline{rs} = '0'$. The mixer array is connected to binary-weighted load capacitors that form the sampling capacitors of an 11-bit SAR ADC. Additional load capacitors, C_L , are used to increase the integration period from $1\mu\text{s}$ to $4\mu\text{s}$. Signals $V_{OUT+/-}$ are connected to the input of the comparator, which is implemented using a double-tail voltage sense amplifier [7]. The input voltage fluctuates during a SAR conversion with a maximum $V_{OUT+/-} = V_{DDA} - V_{IF+/-} + 3/4V_{REF}$. As the integrating mixer is designed to operate above a minimum of $V_{IF+/-} \geq 600\text{mV}$, a maximum of $V_{OUT+/-} = 1.325\text{V}$ occurs when $V_{DDA} = 1.1\text{V}$. This eliminates the need for bootstrapping since $V_{DS} \leq 1.6\text{V}$ in the target technology.

A folded mixer cell is utilized to maximize g_m in the first stage while minimizing the current in the second stage. In the first stage, the tail current of the input differential pair is provided by a 3-level CS-DAC while the windowing operation is implemented by g_{m5} and g_{m6} . The differential pair operates

linearly over a 600mV differential swing with $V_{CM} = 475\text{mV}$. The output currents are mirrored to the second stage with a gain of $\sim 1/3$. The second stage consists of a mixing quad that connects to the load capacitors through switching arrays that toggle between $V_{IF+/-}$, V_{REF} and 0V based on the mode.

In the reset mode, transistors M1:M4 are in deep triode while the load capacitors are switched to $V_{IF+/-}$. This causes the capacitors to discharge and resets the accumulated AC signal since V_{DDA} is applied to $V_{OUT+/-}$ and $V_{IF+/-}$. Furthermore, switches disable the current mirrors between the mixer stages (M13:M14 are in cutoff), which reduces the time to discharge the capacitors. In the integration/sample mode, M3:M4 are in cutoff, which disconnects $V_{OUT+/-}$ from $V_{IF+/-}$, M1:M2 are in deep triode such that $V_{OUT+/-} = V_{DDA}$ and the capacitors are switched to $V_{IF+/-}$. Finally, in the conversion mode, M1:M4 are in cutoff disconnecting the binary-weighted capacitors from the remainder of the circuit, allowing a SAR conversion to take place.

IV. IMPLEMENTATION RESULTS

A full quadrature prototype of the integrating mixer SAR was implemented in IBM's CMRF8SF 0.13 μm CMOS process with 1.33mm^2 using low- V_t devices for analog components and metal-insulator-metal capacitors (MIMCAPs). A die microphotograph is shown in Fig. 3. The DWG and SAR logic are isolated from the analog circuitry in guard rings and located directly under the MIMCAPs. The binary-weighted SAR capacitor arrays are surrounded by 64pF load capacitors.

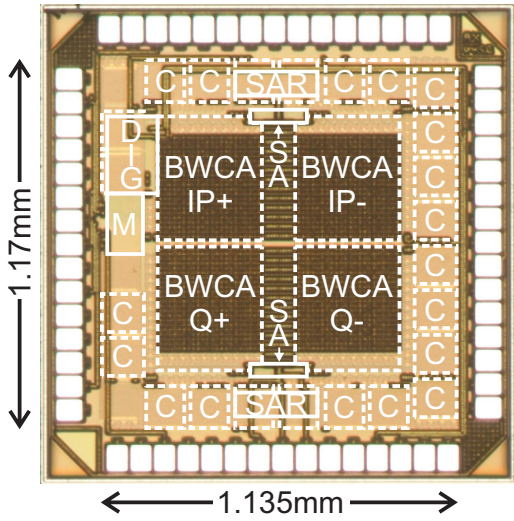


Fig. 3. Die microphotograph (BWCA: binary-weighted capacitor array, DIG: digital window, IP: in-phase, M: mixer, Q: quadrature, SA: switch array).

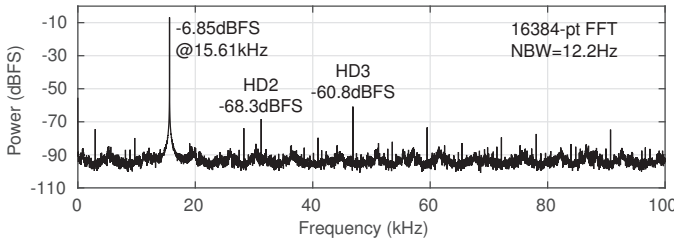


Fig. 4. Measured SAR ADC output power spectrum for $f_s = 200\text{kHz}$.

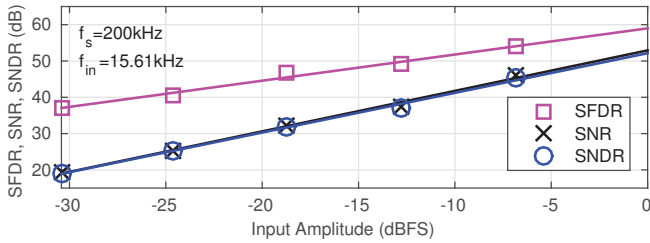


Fig. 5. Measured SAR ADC SFDR, SNR, and SNDR vs. input amplitude.

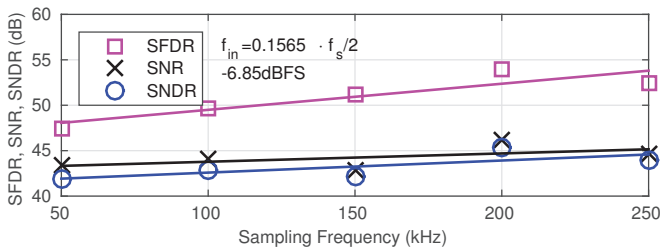


Fig. 6. Measured SAR ADC SFDR, SNR, and SNDR vs. sampling frequency.

A. SAR ADC

In order to characterize the integrated 11-bit SAR ADC, the converter is isolated from the integrating mixer by applying the input signal directly to $V_{IF+/-}$ and setting $V_{CM} = 0\text{V}$ for the mixer LO, thereby cutting off the LO switching pairs and tail

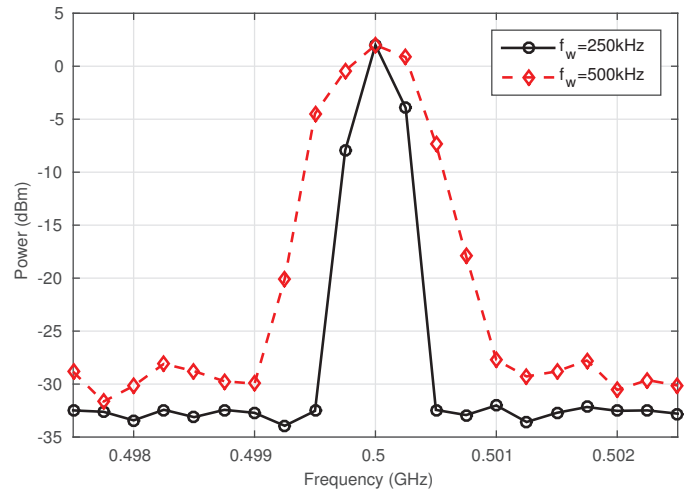


Fig. 7. Spectrum estimates for a tone at 0.5GHz with +2dBm of power and $f_w = 250\text{kHz}$ and $f_w = 500\text{kHz}$.

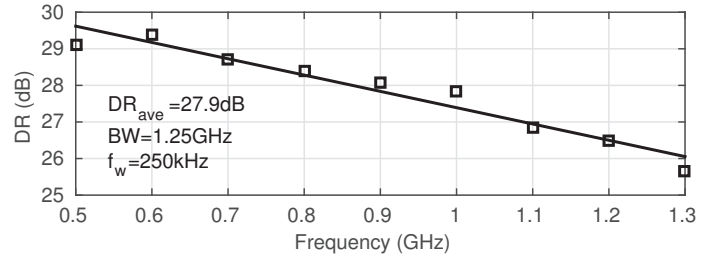


Fig. 8. DR over 0.5GHz to 1.3GHz with line of best fit for $f_w = 250\text{kHz}$.

currents in the mixer. The SAR ADC is designed to operate for a single-ended input voltage between $0.6\text{V} \leq V_{IF+/-} \leq 1.1\text{V}$ for a 1V differential voltage, which restricts the maximum input to -6.85dBFS and the converter resolution to 9.86-bit.

The peak SNDR of 45.4dB at -6.85dBFS 15.6128kHz input is observed with $f_s = 200\text{kHz}$, which results in 7.25-ENOB while consuming a total of $134\mu\text{W}$ from 1.1V/1.2V supplies. Fig. 4 illustrates the measured spectrum at peak SNDR. The third order harmonic is -54dBc , which indicates the converter is limited by thermal noise rather than linearity.

The SNDR, SNR, and SFDR performance is measured versus input amplitude and sampling frequency. In Fig. 5, the input signal amplitude is increased from -30.42dBFS to -6.80dBFS . The SNDR increases linearly with input signal amplitude and the extrapolated SNDR value at 0dBFS is 52.14dB. In Fig. 6, the sampling frequency is increased from 50kHz to 250kHz while maintaining the same $f_{in} : f_s$ ratio. The SNDR increases with sampling frequency at a rate of $+1.33\text{dB}/100\text{kHz}$ with peak SNDR at 200kHz. The performance results are summarized in Table I.

B. Spectrum Estimation and Comparisons

The measured power spectrum of a tone at 0.5GHz with an input power of +2dBm is illustrated in Fig. 7 for $f_w = 250\text{kHz}$ and $f_w = 500\text{kHz}$. The LO frequency is swept over 250kHz intervals, which shows spreading of the input

TABLE III

COMPARISON OF MIXED-SIGNAL SPECTRUM SENSING IMPLEMENTATIONS BASED ON ENERGY DETECTION COVERING THE DTV BAND.

	[1]	[2]	[3]	[4]	[5]	[6]	Proposed
Technology	0.18 μ m	0.18 μ m	90nm	0.18 μ m	0.13 μ m	0.13 μ m	0.13 μ m
Supply (V)	1.8	1.8	1.2	1.8	1.5/1.3	1.2	1.2/1.1
P (mW)	43.2 ^a	23.8 ^a	13.9 ^a	17.8 ^a	19.5–28.5	2.5	0.9
DR (dB)	32	24	29–48	34	n/a	21–24	25.7–27.9
Range (GHz)	0.4–0.9	0.4–0.9	0.03–2.4	0.4–0.8	0.25–3.25	0.05–3	0.05–1.25
Window	$\cos^4 x$	$\cos^4 x$	n/a	n/a	n/a	Hann ($\alpha = 0.85$)	Hann ($\alpha = 0.5$)
f_w (MHz)	0.025–1	0.025–1	n/a	n/a	n/a	1–4	0.25–1
DBW (MHz)	0.05–2	0.05–2	0.2–30	0.4	40	1–4	0.36–1.44

^a Power for [1], [2]: analog correlator and DWG, [3]: mixer, BB filter and RSSI circuitry, and [4]: mixer and LPF.TABLE I
INTEGRATING MIXER SAR MEASUREMENT SUMMARY.

Integrating mixer SAR	
Technology	0.13 μ m
Supply	1.1V and 1.2V
Bandwidth	1.25GHz
DR _{ave} (f_w : 250kHz, 500kHz)	27.9dB, 25.7dB
Int. Gain (f_w : 250kHz, 500kHz)	–13.9dB, –13.5dB
1dB Compression	+0.2dBm
OIP3	+13.4dBm
Integrated 11-bit SAR ADC	
Max Input, Full Scale	1V, 2.2V
Bandwidth	250kHz
SNDR (Peak, $0.5 \cdot f_s$)	45.4dB, 43.8dB
SNR (Peak, $0.5 \cdot f_s$)	46.2dB, 44.5dB
SFDR (Peak, $0.5 \cdot f_s$)	54.0dB, 52.7dB
DNL, INL	+1.7/ – 1 LSB, +2.3/ – 3.4 LSB
Power	164.0 μ W

TABLE II
INTEGRATING MIXER SAR POWER SUMMARY.

Circuit	Measured	Simulated
Input pair, SA Latch, CS-DAC (positive half)	329 μ W	380 μ W
CS-DAC (negative half)	408 μ W	380 μ W
Second stage of mixer	48 μ W	46 μ W
SAR & window generation logic	93 μ W	135 μ W
	878 μ W	941 μ W

signal. The side-lobe oscillations are nearly completely suppressed, which is expected as the Hann window function achieves > 30 dB side-lobe reduction. As shown in Table I and illustrated in Fig. 8 for $f_w = 250$ kHz, the measured BW is 1.25GHz while the average DR is 27.9dB for $f_w = 250$ kHz and 25.7dB for $f_w = 500$ kHz. There is a constant integration gain associated with each window frequency, which is proportional to the voltage drop across the capacitive loads.

Two-tone testing was performed for input tones at 0.8GHz and 1GHz with a power of +2dBm, which result in an output third-order intercept (OIP3) of +13.4dBm. The 1dB compression point is +0.2dBm while the THD for a tone at 0.5GHz with a power of –0.5dBm is 0.79%. The overall performance is summarized in Table I while a breakdown of the power dissipation is listed in Table II. The total power dissipation is 878 μ W, which is within 8% of that simulated.

In Table III, the proposed integrating mixer SAR is compared to recent spectrum sensing implementations based on energy detection [1]–[6]. The proposed design achieves the

lowest power dissipation while improving the DR and DBW over the integrating mixer implementation in [6]. In order to match the minimum sensitivity of –83dBm, the proposed design would require an analog front end with a LNA and gain stages that provide a gain of 58dB, which is 9dB less than [3]. The DBW of the proposed design is limited by the integrating capacitor size but maintains a respectable minimum of 360kHz. The proposed design is well suited as the first in a dual-stage sensing process to quickly identify potential vacant spectrum for detailed sensing with a method such as feature detection.

V. CONCLUSION

A full quadrature prototype chip for spectrum sensing was fabricated in IBM’s CMRF8SF 0.13 μ m CMOS process that consists of an array of folded mixers combining mixing, current-domain windowing, integration and SAR A/D conversion to obtain a digital estimate of the STFT. The design operates over a frequency range of 0.05–1.25GHz, consumes 0.88mW and obtains an average DR of 25.7–27.9dB. The architecture results in the lowest reported power consumption for mixed-signal spectrum sensing and includes mixing, baseband filtering and A/D conversion, which further reduces the overall receiver power dissipation. Spectral estimates can be obtained in as little as 6.7ms over the DTV bands. The architecture is well suited for incorporation within CR transceivers that target portable IEEE 802.22 applications.

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