DIRECT GMSK GENERATION USING SIGMA-DELTA MODULATION

by

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April 2003

Supervisor: Anthony Chan Carusone

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Abstract

A constant-envelope, continuous phase modulation architecture is presented in which a sigma-delta modulator is combined with a direct modulator. The main advantages of this architecture are that linearity of the oscillator's tuning device is ensured and implementation is simplified due to the use of discrete frequency switching in the oscillator. The main disadvantage is that the quantization noise introduced by the Σ–Δ modulator must be filtered out or spread out to ensure wireless noise specifications are met. The architecture is simulated in an open-loop configuration implementing GMSK modulation for use in a GSM transceiver. A prototype, low-frequency implementation of the modulation architecture is constructed and experimental results are found to match simulations. By increasing the Σ–Δ modulation frequency, the quantization noise is filtered out by the VCO and disappears beneath the measurement noise floor.

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List of Abbreviations

A/D	Analog to Digital
D/A	Digital to Analog
DAC	Digital to Analog Converter
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
MSK	Minimum Shift Keying
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
VCO	Voltage Controlled Oscillator
S-D	Sigma-Delta

Chapter 1

Introduction

1.1: Motivation

As the world continues to adopt wireless electronic devices, there exists a demand for engineers to develop faster, cheaper, and more reliable circuits to power these devices. Despite the dot.com meltdown at the start of the millennium, growth in the wireless market shows no signs of slowing. GSM, a second generation wireless technology used in cellular phones, currently has 800 million subscribers worldwide and there are expected to be 1.3 billion GSM subscribers by 2006 [1].

At the heart of every wireless device is a phase-locked loop (PLL), an analog circuit used for frequency synthesis and clock recovery. The design of the phase-locked loop is critical – it significantly affects the power consumption, cost, and transmission quality of the device. Since most wireless devices are mobile and are powered by a battery, decreased power consumption and hence increased battery life is an important consideration to consumers. The cost of the device is also important to consumers. The transmission quality of the device is usually more of a concern to companies than consumers. For example, a company must ensure that its GSM cellular phones transmit wireless signals that adhere to international standards. Otherwise, the phone will not work reliably or will disrupt the operation of other cellular phones.

This thesis will discuss a new frequency synthesizer architecture that can be used in wireless devices to modulate a digital signal. Section 1.2 will provide an outline of existing modulation architectures and Section 1.3 will explain a few key concepts that are used in the proposed modulation architecture.

1.2: Applications and the State of the Art

There are three popular methods to perform phase/frequency modulation of a digital signal: quadrature modulation, open-loop modulation, and modulated synthesis. Fig. 1 shows block diagrams for each of these methods.

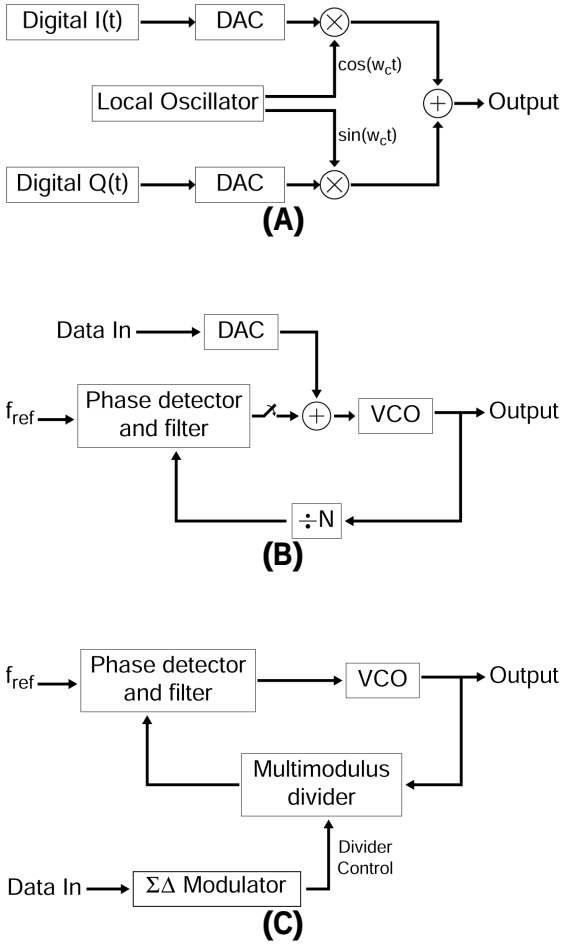


Figure 1. Three popular methods to modulate a signal
A) Quadrature modulation
B) Open-loop modulation
C) Modulated synthesis

Quadrature Modulation

Of these three methods, quadrature modulation is the most commonly used approach for digital phase/frequency modulation. This method allows for a high-quality signal to be generated because the oscillator is disassociated from the baseband signals [2]. The architecture is also very flexible. However,

these advantages come at the cost of increased circuit complexity. There is the need for two DACs and two analog multipliers to accommodate the in phase and quadrature signals.

Open-loop Modulation

An architecture that eliminates the need for quadrature baseband DACs and a separate local oscillator is the open-loop modulator. Although the open-loop modulator still requires a single DAC, the architecture is simple to implement and is an attractive option for a low-cost, low-power modulator. Unfortunately, there are several problems inherent in the open-loop modulator architecture. While transmitting data, the open-loop modulator must periodically halt transmission to stabilize the center frequency of the VCO. In addition, the VCO must have a linear tuning curve to ensure that the output is not distorted. Even if the VCO has a linear tuning curve, the slope of the curve determines the bandwidth of the output signal and thus must be calibrated to control the output bandwidth.

Modulated Synthesis

In the modulated synthesizer, the data is modulated by switching the value of a frequency divider in the feedback path of the PLL. The data is first passed through a sigma-delta modulator to quantize the data and move the quantization noise to a high frequency. Like the open-loop modulator, the modulated synthesizer does not require as much analog circuitry as the quadrature modulator. As well, the modulated synthesizer does not suffer from the open-loop modulator's requirements of a linear VCO tuning curve and periodic frequency stabilization [3]. However, the modulated synthesizer requires a multimodulus divider and precompensation or two-point-modulation of the input signal to compensate for bandpass filtering caused by the PLL [4].

1.3: Background

1.3.1: Sigma-Delta Modulation

Sigma-delta modulation is most often used in oversampling D/A and A/D converters. It allows for shaping of the quantization noise to improve the signal to noise ratio in the bandwidth of interest. As with traditional oversampling converters without noise shaping, sigma-delta modulators use oversampling to spread the quantization noise over a larger frequency range. When the oversampled signal is passed through a low-pass filter, there exists a greater signal to noise ratio than if the signal had been sampled at its Nyquist rate with the same quantizer. The noise-shaping transfer function used in a sigma-delta modulator can have arbitrary order. Higher-order noise shaping results in less quantization noise power in the bandwidth of interest, but more quantization noise power overall. Figure 2 shows a discrete-time block diagram for a second-order sigma-delta modulator [5].

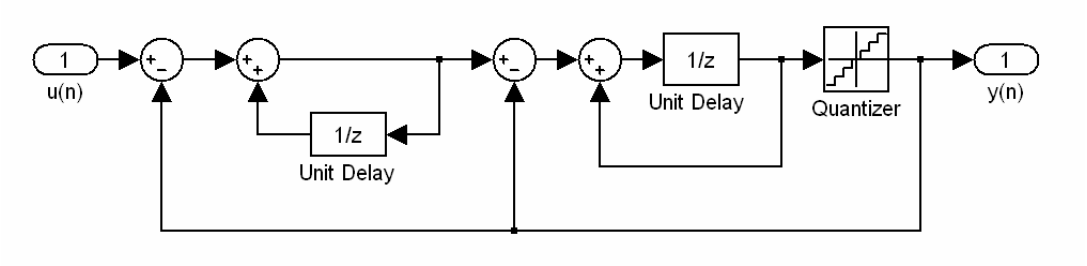


Figure 2. A Second-Order Sigma-Delta Modulator

The frequency spectrum of a sigma-delta modulated signal can be seen in Figure 3. At low frequencies, the quantization noise is not significant and the sinusoid's frequency component is clearly visible. At higher frequencies, the quantization noise increases, reaching a maximum at half the sampling frequency.

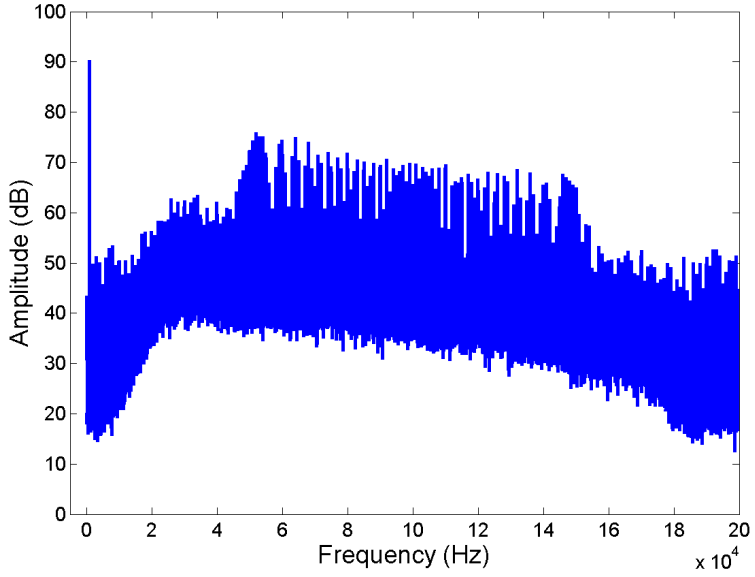


Figure 3. Frequency Spectrum of a Second-Order Sigma-Delta Modulator (Input sinusoid of 1 KHz, Oversampling ratio of 200)

1.3.2: Minimum Shift Keying (MSK)

Minimum Shift Keying is a spectrally efficient, continuous phase, continuous envelope modulation scheme [6]. In MSK, the frequency of oscillation switches between two frequencies with continuous phase. The two frequencies are spaced such that the phase of the signal increases or decreases by $p/2$ in a baud rate period depending on whether a 1 or -1 is being transmitted. The two frequencies that represent -1 and 1 are equal to:

$$f_L = f_C - \frac{1}{4T}, \qquad f_H = f_C + \frac{1}{4T}$$

T represents the baud rate and f_C represents the carrier frequency.

An MSK waveform can thus be represented by the following equation:

$$y(t) = A\cos\left(2pf_c t + q_0 + \frac{p}{2T}\int_{-\infty}^{t} f(t)dt\right)$$

In the above equation, $\phi(\tau)$ is either -1 or 1, representing the bit that is being transmitted. Fig. 4 shows four baud rate periods of an arbitrary MSK waveform.

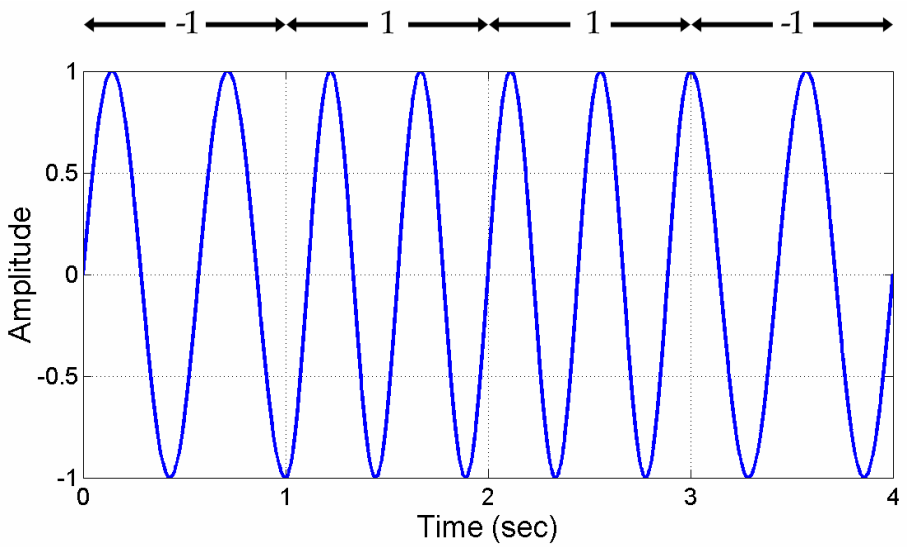


Figure 4: A MSK Encoded Signal

(T = 1 sec, F_C = 2 Hz)

Gaussian Minimum Shift Keying (GMSK) is a modulation scheme based on MSK that is used in GSM cellular phones. In GMSK, the binary data is passed through a Gaussian filter before being modulated. This filter introduces a small amount of intersymbol interference into the modulated signal but also increases the overall spectral efficiency.

1.3.3: GSM (Global System for Mobile Communications)

GSM is the dominant mobile communications technology used in cellular phones. At the end of 2002, there were 787 million GSM subscribers worldwide [1]. GSM is available in a variety of technologies as shown in Table 1.

GSM Technology	Availability	Operating Frequency	Channel Baud Rate
GSM 900	Europe, Asia, Australia	900 MHz	270 kb/sec
GSM 1800 / DCS 1800	Europe, Asia, Australia	1800 MHz	270 kb/sec
GSM 1900 / PCS 1900	US, Canada, Latin-America	1900 MHz	270 kb/sec

Table 1: Current GSM technologies

1.4: Outline

Chapter 2 will outline the proposed modulation architecture and examine it from a systems perspective. The modulation architecture's advantages and disadvantages will be discussed and system-level frequency spectrum plots will be shown. A circuit implementation of the proposed architecture will be presented in Chapter 3. HSPICE circuit simulations results will be compared to the results in Chapter 2. Finally, Chapter 4 will describe a discrete implementation of the proposed modulation architecture and the experimental results of this implementation will be presented and compared with both system and circuit level simulations.

Chapter 2

Proposed Modulation Architecture

2.1: Overview of Architecture

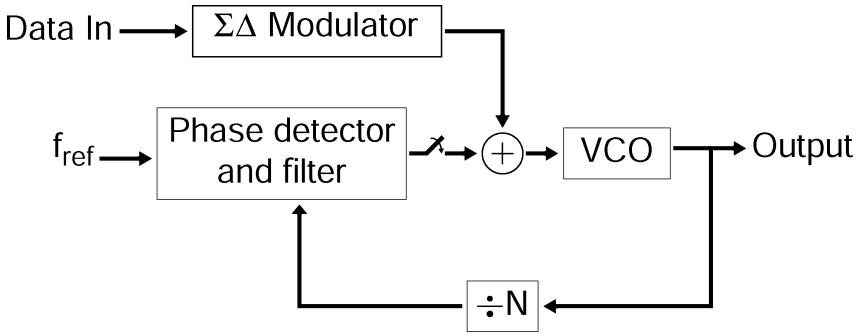


Figure 5: A Sigma-Delta Based Open-Loop Frequency Modulator

The proposed architecture, seen in Figure 5, is a sigma-delta based open-loop modulator. Like the modulated synthesizer, this approach uses a Σ–Δ modulator to avoid using a DAC and thus decreases the analog circuit requirements. In a Σ–Δ based open-loop modulator, the output frequency switches between a discrete set of frequencies as the output of the Σ–Δ modulator switches between discrete levels. As with the traditional open-loop modulator, the loop must periodically close to stabilize the center frequency.

A drawback with using a Σ–Δ modulator is that its quantization noise must be filtered out before transmitting the output signal. Modulated synthesizers filter out the quantization noise by using the bandpass filtering built into the PLL. However the PLL bandwidth cannot be easily controlled as it is primarily determined by other system requirements such as frequency tracking and jitter specifications.

Similar quantization noise issues arise with the Σ–Δ based open-loop modulator, except that the VCO bandwidth needs to be considered instead of the PLL bandwidth. The VCO bandwidth represents the extent to which the signals outside the frequency bandwidth of interest are attenuated. This attenuation is primarily determined by how quickly the VCO can switch between frequencies. At low Σ–Δ frequencies, the VCO frequency switching can be considered to be instantaneous, and thus all of the quantization noise is passed to the output of the PLL. However, when the Σ–Δ modulator frequency becomes sufficiently high, the VCO frequency switching time becomes significant and the VCO can ideally act as a bandpass filter, filtering out the quantization noise.

2.2: Advantages

2.2.1: VCO Linearity

When a one-bit Σ–Δ modulator is used, the VCO only switches between two frequencies and the tuning curve of the VCO is assured to be linear, regardless of the linearity of the tuning device. In traditional open-loop modulators, high quality varactors are needed to achieve a linear tuning curve. Even though a one-bit Σ–Δ modulator can ensure a linear VCO tuning curve, it is still necessary to control the slope of the tuning curve, which defines the output bandwidth.

2.2.2: Adder Simplification

The Σ–Δ based frequency modulator can be thought of essentially the same as the open-loop modulator in Figure 1.B) except that the low-pass filter in the DAC has been removed. Even though this low-pass filter is relatively trivial to implement, by removing it there are significant repercussions throughout the rest of the PLL. One such repercussion is that the adder design can be simplified. Instead of adding two analog signals together, the adder needs to only add an analog with a digital signal. This simplification is shown in Figure

6. Due to the negative feedback of the PLL when the loop is closed, it is not necessary for the adder to be perfectly linear. However, the adder would need to be linear if a multi-bit Σ–Δ modulator was used.

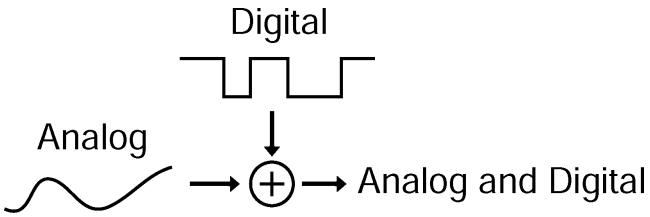


Figure 6: Adder Simplification due to the Σ–Δ modulator

2.3: Disadvantages

As stated in 2.1, a drawback with using a Σ–Δ modulator is that its quantization noise must be filtered out before transmitting the output signal. By examining the power spectrum of a GSM signal, one can determine what Σ–Δ modulator frequency is necessary to ensure a sufficiently large signal-to-noise ratio in the bandwidth of interest. Figure 7 shows the power spectrum of random data and Gaussian filtered random data.

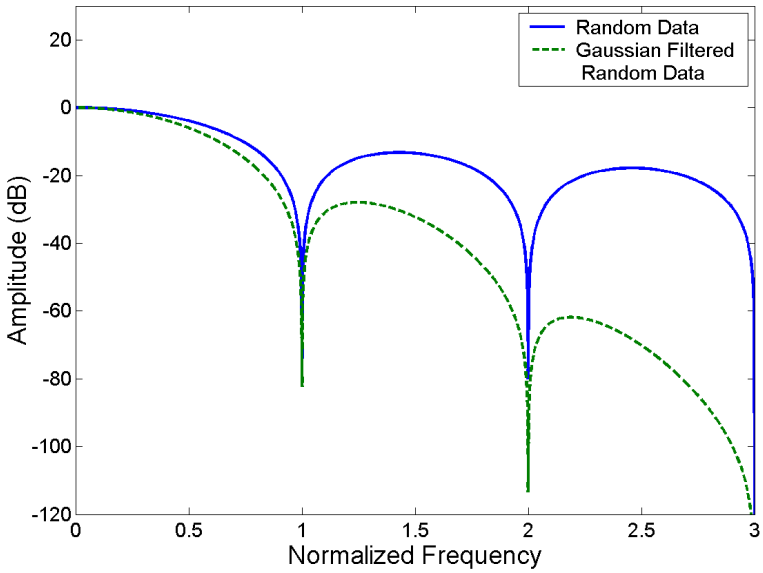


Figure 7: Power spectrum of random data and Gaussian filtered random data (Frequency axis normalized to half the data rate)

The Gaussian filters used in Figure 7 and in GMSK have a -3 dB frequency of $0.3F_{data}$. Because the Gaussian filtered power spectrum is significantly attenuated at frequencies greater than $0.5F_{data}$, the oversampling ratio, M, can be considered to equal $\frac{F_s}{0.5F_{data}}$. By increasing the Σ–Δ modulator frequency, the quantization noise is moved farther away from the carrier frequency and the PLL is able to filter out more of this noise. However, power consumption in digital circuits is proportional to the square of frequency and circuit complexity increases as the Σ–Δ modulator frequency increases. Thus, the Σ–Δ modulator should operate at the lowest frequency at which the wireless standards are met. For example, the GSM standard requires that spurious emissions are less than -83 dBc/Hz for frequencies 0.2 to 0.4 MHz away from the carrier frequency [7].

2.4: Frequency Analysis

The frequency power spectrums of a GMSK signal and a second-order, single-bit Σ–Δ modulated GMSK signal are shown in Figure 8 and Figure 9. The oversampling ratio for the Σ–Δ modulated GMSK signal is approximately 740 (100 MHz clock frequency, 270/2 = 135 kHz signal bandwidth). Nearby the carrier frequency, the quantization noise floor is 90 dB below the main peak. The quantization noise reaches its maximum value 50 MHz from the carrier frequency (corresponding to half the clock frequency), 60 dB below the main peak.

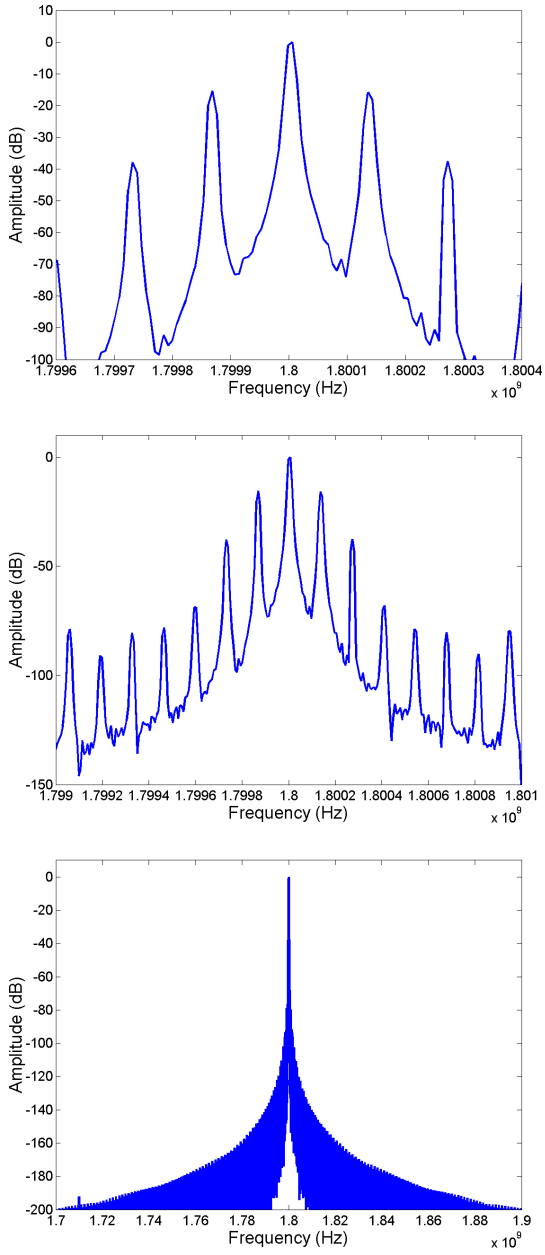


Figure 8: Frequency Power Spectrum of a GMSK Signal

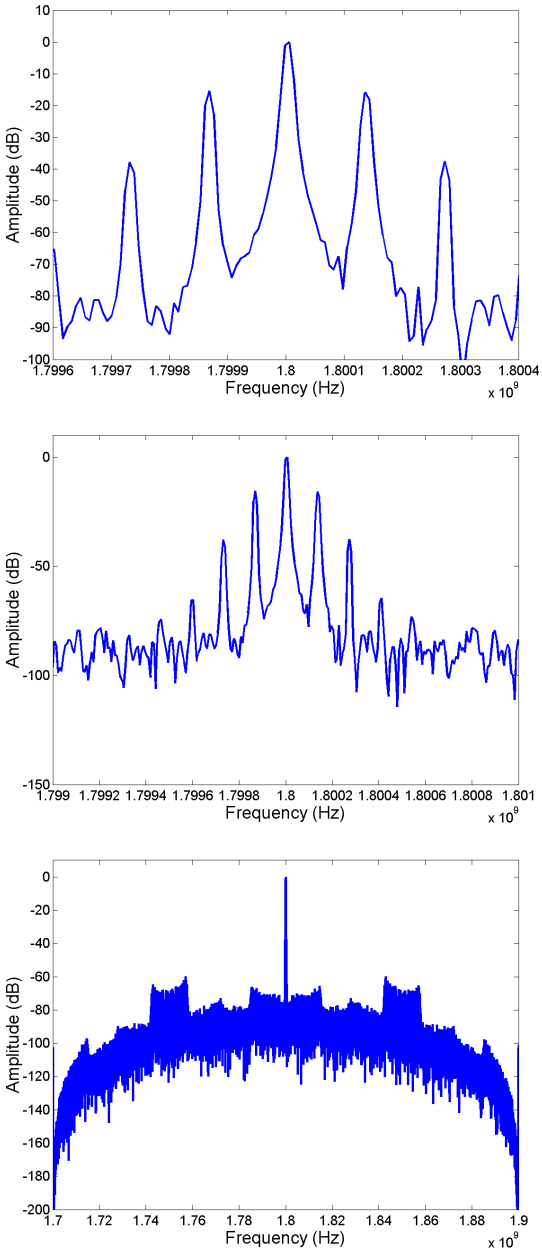


Figure 9: Frequency Power Spectrum of a Sigma-Delta Modulated GMSK Signal
(Σ–Δ Frequency of 100 MHz)

2.5: System Analysis of PLL

One important design consideration in the design of a PLL for a sigma-delta based frequency synthesizer is the bandwidth of the VCO. In direct modulation, where the data enters directly into the VCO, the bandwidth of the VCO can significantly affect the quantization noise of the input signal. Figure 10 shows the linearized system diagram of a PLL.

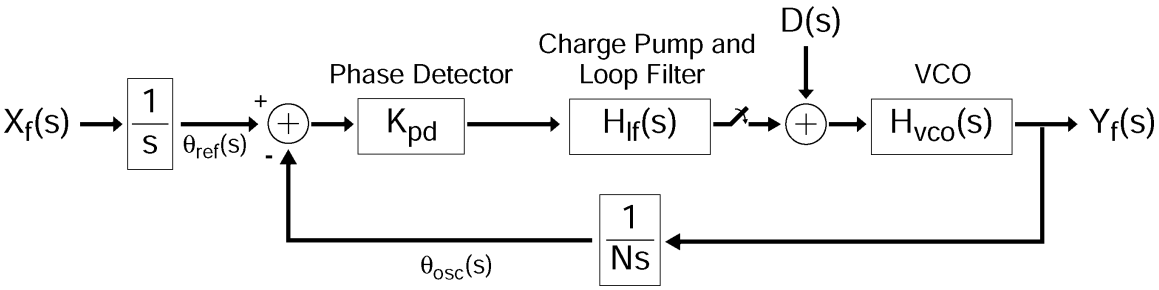


Figure 10: Linearized system diagram of a PLL

Traditionally, analysis of the PLL is conducted by examining the phases of the input and output signals. However, when analyzing open-loop effects in a PLL, it can be useful to examine frequencies instead. Thus, $X_f(s)$ and $Y_f(s)$ represent the frequencies of the reference signal and oscillator, respectively.

The phase/frequency detector is modelled as a gain block, K_{pd}, that amplifies or attenuates the difference in phase between the output $Y_f(s)$ and the reference $X_f(s)$. θ_{ref} and θ_{osc} represent the phases. N is the feedback frequency divider value.

The charge pump and loop filter are represented by the transfer function $H_{lf}(s)$. $H_{lf}(s)$ typically has two poles and one zero. The lower frequency pole, w_{p1}, determines the bandwidth of the PLL and the zero, w_z, improves the stability and tracking of the loop. The high frequency pole, w_{p2}, removes some non-ideal effects and can be neglected in this analysis.

$$H_{lf}(s) = \frac{1+\frac{s}{w_z}}{\left(1+\frac{s}{w_{p1}}\right)\left(1+\frac{s}{w_{p2}}\right)} \approx \frac{1+\frac{s}{w_z}}{1+\frac{s}{w_{p1}}}$$

In some applications the low frequency pole, w_{p1}, is moved to dc:

$$H_{lf}(s) = \frac{1+\frac{s}{w_z}}{s\left(1+\frac{s}{w_{p2}}\right)} \approx \frac{1+\frac{s}{w_z}}{s}$$

The VCO block in Figure 10 converts a voltage to a frequency. Typically the VCO is represented by a gain block, K_{VCO}. This is because in a closed-loop PLL configuration, the only input into the VCO block comes from the loop filter, and this input typically does not have any high frequency components. Because the input is over a narrow frequency range, the frequency response of the VCO can be assumed to be uniform. However, when D(s) is a sigma-delta modulated input, the control voltage into the VCO now has high frequency components. Thus, high-frequency characteristics of the VCO must be considered. Various second and third-order models exist for the VCO that affect its frequency switching response [8]. In one of its simplest forms, the VCO can be modelled as a low-pass filter, with a -3dB frequency that is significantly greater than the -3dB frequency of the charge pump and loop filter.

$$H_{VCO}(s) = \frac{K_{VCO}}{1+\frac{s}{w_{vco}}}$$

Direct modulation can be implemented in both an open and closed-loop configuration. In an open-loop configuration, the loop alternates between transmitting data and locking the carrier frequency. In a closed-loop configuration, locking of the carrier frequency occurs at the same time as transmitting data.

Open-Loop Configuration

Section 1.2 provided an introduction to open-loop modulation and its advantages and disadvantages. The system analysis of open-loop direct modulation is relatively straightforward. When data is being transmitted, the transfer function from D(s) to $Y_f(s)$ is $H_{VCO}(s)$. The only design consideration is to ensure that the sigma-delta modulation quantization noise is sufficiently attenuated by $H_{VCO}(s)$ and spread over a wide enough bandwidth so that the transmission quality meets specifications. If this can not be achieved, an additional bandpass filter may be required prior to transmission.[1] The rest of the PLL is designed in a traditional manner for good locking characteristics.

Closed-Loop Configuration

The analysis and design of the PLL in a closed-loop configuration is more complicated than in an open-loop configuration because the loop must be able to stay in lock at the same time as it is transmitting data. The benefit of this approach is that there is no longer the need to periodically halt transmission and close the loop to lock the carrier frequency.

In a closed-loop configuration, the transfer function from D(s) to $Y_f(s)$ is:

$$\frac{Y_f(s)}{D(s)} = \frac{H_{VCO}(s)}{1+(Ns)^{-1}H_{VCO}(s)K_{PD}H_{lf}(s)} = \frac{sNH_{VCO}(s)}{sN+H_{VCO}(s)K_{PD}H_{lf}(s)}$$

At low frequencies ($s \approx 0$), it can be seen that $\frac{Y_f(s)}{D(s)} \approx 0$.

At high frequencies ($s \to j\infty$), it can be seen that $\frac{Y_f(s)}{D(s)} \approx H_{VCO}(s)$.

Assuming that $H_{VCO}(s)$ has a low pass response, the transfer function from the data input to the frequency output is bandpass with a lower -3dB cutoff frequency of w_L. If we only consider the low frequency pole and zero of the loop filter, we can obtain an expression for w_L (See Appendix A):

[1] In some systems, this may already be present.

$$w_L = \sqrt{-0.5b + 0.5\sqrt{b^2 + 4N^{-2}K_{VCO}{}^2K_{PD}{}^2w_{p1}{}^2}}$$

where $b = 2w_{p1}{}^2 + 2K_{VCO}K_{PD}N^{-1}w_{p1} - \left(w_{p1} + \frac{K_{VCO}K_{PD}w_{p1}}{Nw_Z}\right)^2$

For applications where the low frequency pole is located at dc, we have the following expression for w_L:

$$w_L = \sqrt{-0.5b + 0.5\sqrt{b^2 + 4N^{-2}K_{VCO}{}^2K_{PD}{}^2}}$$

where $b = 2K_{VCO}K_{PD}N^{-1} - \left(\frac{K_{VCO}K_{PD}}{Nw_Z}\right)^2$

For the data D(s) to be transmitted at the output, it is important that its frequency spectrum lie between w_L and w_{VCO}. Otherwise, the signal will be attenuated. The signal will be bandlimited below w_{vco} by the Gaussian filter, and simple coding can be applied to the data stream to ensure it has no dc content.

Analyzing a typical PLL in a closed-loop configuration

An existing 1.4 GHz GMSK modulator has the following PLL specifications:

w_{p1}	Located at dc
w_{p2}	$2\pi \times 148$ kHz
w_Z	$2\pi \times 12.5$ kHz
K_{VCO}	$2\pi \times 200$ MHz/V
K_{PD}	1 V/rad (assumed)
N	87.5

Table 2: PLL specifications from [9]

w_{vco} is assumed to be 100 MHz.

Using these values, w_L is calculated to be $2\pi \times 219$ Hz. This value of w_L agrees with the simulated bode plot for the closed-loop PLL shown in Figure 11. The magnitude peaking near w_L can be prevented by lowering the zero frequency, w_Z. If the data stream is encoded to have no components at frequencies near w_L, this magnitude peaking is not a problem.

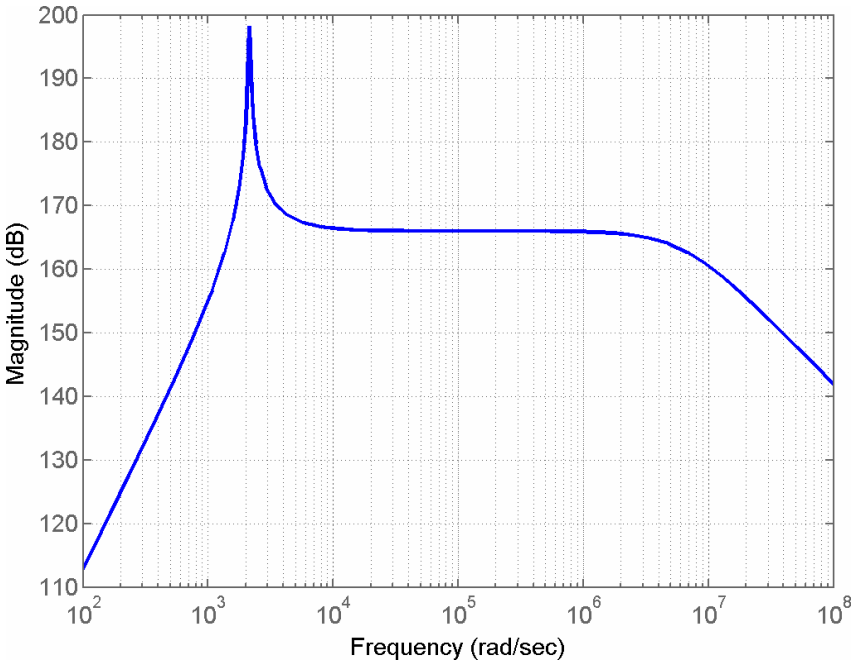


Figure 11: Bode plot of $Y_f(s)/D(s)$ for the PLL in a closed-loop configuration

Chapter 3

Circuit Implementation

3.1: Overview

To verify the feasibility of the proposed modulation architecture, a voltage-controlled oscillator circuit for use in a GSM 1800 transceiver was designed in CMOS 0.35 μm technology. A sigma-delta modulated signal was direct modulated by the oscillator in an open-loop configuration and frequency spectrum plots were found to match the simulated plots in Chapter 2.

3.2: Voltage-Controlled Oscillator

3.2.1: Overall circuit

The voltage-controlled oscillator was an LC oscillator designed in CMOS 0.35 μm technology. An LC oscillator was used instead of a ring oscillator because the GSM specifications require very little phase noise [10]. A differential oscillator was implemented to reduce the effect of DC offsets. The oscillator operated with a power supply voltage of 2.5 V and required 20 mW of power. Tuning of the oscillator was accomplished using PMOS based capacitors. Figure 12 shows the circuit diagram of the differential LC oscillator that was used.

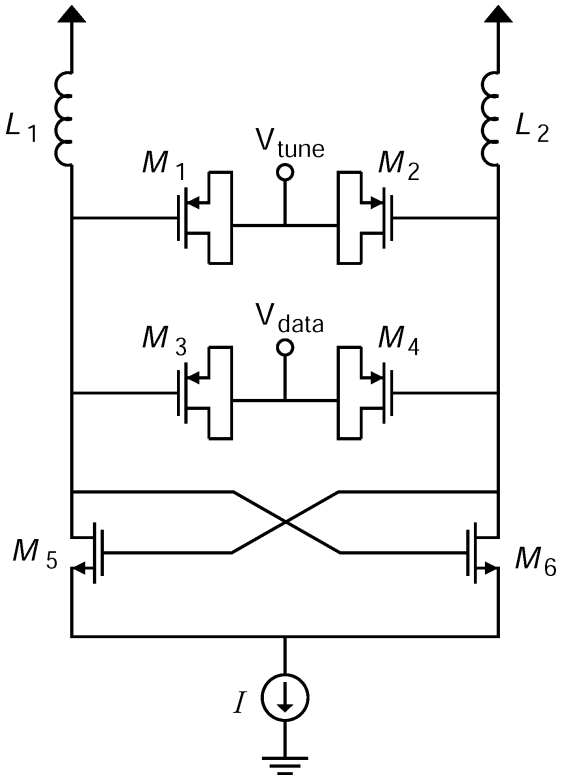


Figure 12: Circuit diagram of differential LC oscillator

L_1, L_2	3 nF
M_1, M_2	L = 1.4 µm W = 10 µm (x 40)
M_3, M_4	L = 0.7 µm W = 1 µm
M_5, M_6	L = 0.35 µm W = 10 µm
I	8 mA

Table 3: Values for Figure 12

3.2.2: On-chip inductor

For accurate simulation results, on-chip inductors were modelled using Asitic, CAD software that can model spiral inductors in integrated circuits [11]. Although it was assumed that the inductors were isolated from one another, the inductors could have been cross-coupled together, thereby increasing the Q

of each inductor and reducing the phase noise of the oscillator [12]. The differential LC oscillator could have also been implemented with a single inductor, as described in [13].

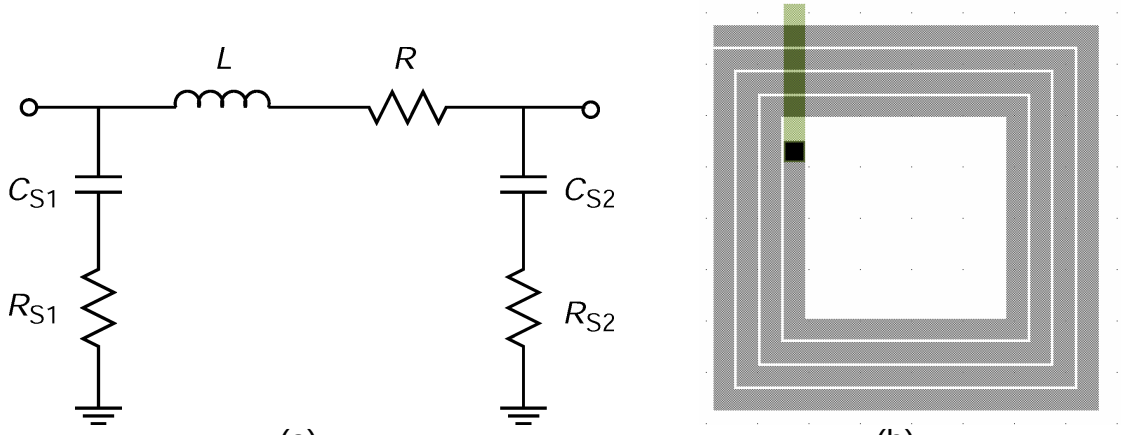


Figure 13: (a) Circuit diagram and (b) layout of the modelled on-chip inductor

L	2.95 nH
R	7.45 Ω
C_{S1}	60.4 fF
C_{S2}	60.5 fF
R_{S1}	1.89 Ω
R_{S2}	0.374 Ω
Q	4.38
$F_{resonant}$	11.91 GHz

Table 4: Values for the on-chip inductor

3.2.3: Tuning characteristics

Frequency tuning of the oscillator was accomplished using PMOS transistors M_1, M_2, M_3 and M_4 in Figure 12. Transistors M_1 and M_2 were responsible for broad tuning of the VCO from 1.7 GHz to 2.2 GHz. Figure 14 shows the broad tuning curve of the VCO for input voltages ranging from 0 V to 2.5 V.

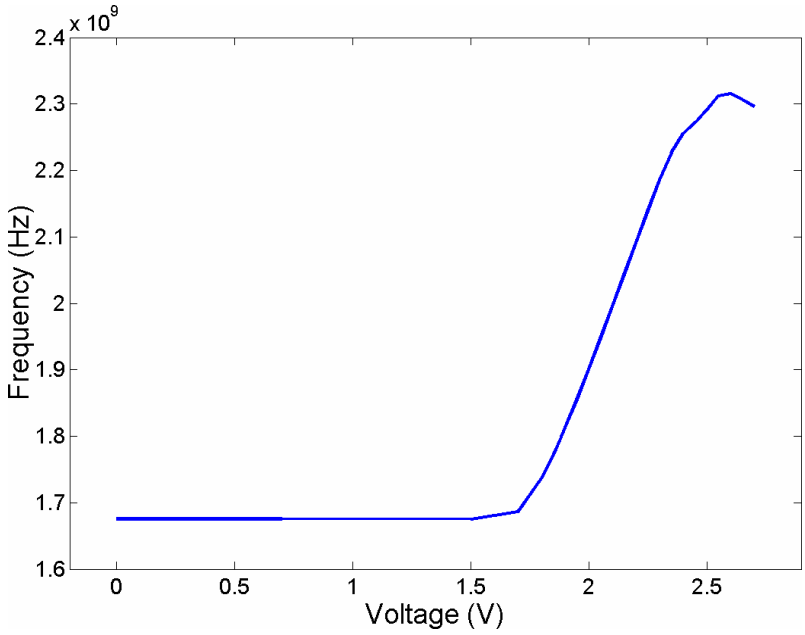


Figure 14: Broad tuning curve of the VCO

Transistors M_3 and M_4 were responsible for the narrow frequency switching due to the Σ–Δ modulator. When using a one-bit Σ–Δ modulator, V_{data} would switch between 0 V and 2.5 V depending on the output of the modulator. The VCO would then switch between two frequencies, f_1 and f_2, as seen in Figure 15. To improve the effective resolution of the Σ–Δ modulator, it is important to keep the difference between frequencies f_1 and f_2 not significantly greater than the bandwidth of the signal being transmitted. In GSM, the channel bandwidth is 200 kHz, and thus frequencies f_1 and f_2 were spaced approximately 1 MHz apart. This was accomplished by choosing sufficiently small transistor sizes of M_3 and M_4 in relation to M_1 and M_2.

In existing implementations of direct modulators, the VCO tuning curve is assumed to be linear over small changes in the input voltage. For an input voltage between 1.7 V and 2.5 V, the tuning curve seen in Figure 15 is relatively linear. However, perfect linearity cannot be achieved without digital precompensation of the input signal and complete characterization of the

tuning curve. A one-bit Σ–Δ modulator results in a linear tuning curve regardless of the linearity of the tuning device that is used.

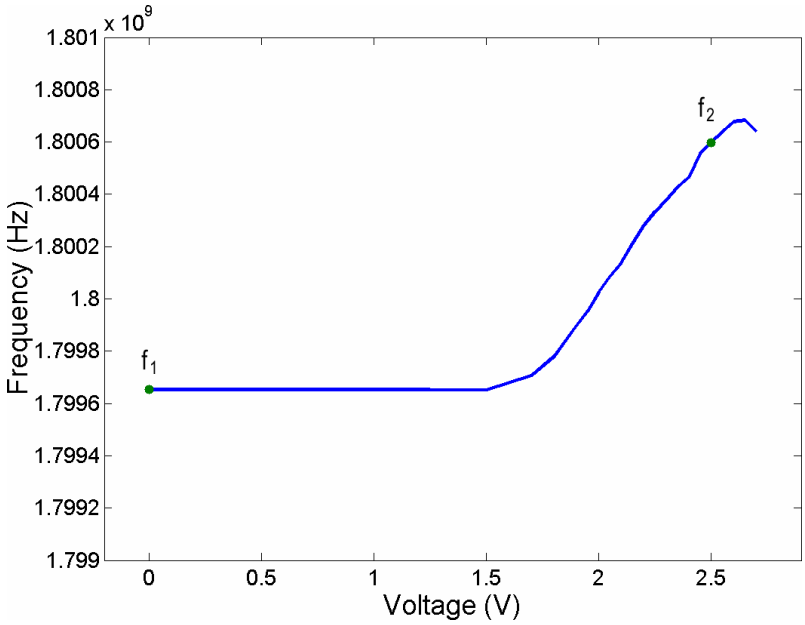


Figure 15: Fine tuning curve of the VCO

3.3: Circuit Simulations

3.3.1: Instantaneous frequency switching of VCO

An important design consideration in the proposed modulation architecture is how the VCO responds to instantaneous changes in frequencies. If the VCO slowly changes between frequencies, then it has a low-pass response and the high frequency components of the input into the VCO are filtered out. If the VCO overshoots when switching between frequencies, then some high-frequency components of the input are amplified. Figure 16 shows the instantaneous frequency response of the differential LCO when driven by a Σ–Δ modulator at 100 MHz. In the figure, it can be seen that the frequency switching characteristic of the VCO varies with time. This is because the frequency switching occurs at different times in the period of the oscillator. At some frequency switches, the oscillator overshoots by 40%. At other times, the oscillator has almost no overshoot. Since the frequency response is clearly not

low-pass, one cannot assume that the VCO will filter out the Σ–Δ modulator quantization noise. Therefore, it is desirable to use a high oversampling ratio in the Σ–Δ modulator to spread out the quantization noise. Other bandpass filtering may be required throughout the transmitter to further attenuate the quantization noise, possibly by implementing a narrowband power amplifier or a narrowband antenna.

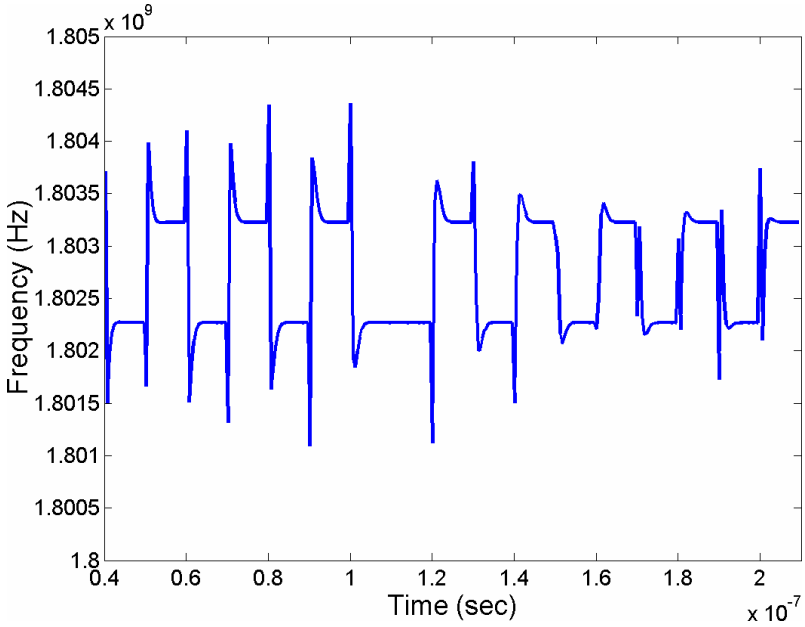


Figure 16: Instantaneous frequency response of the VCO

3.2.2: Frequency spectrum plots

A Σ–Δ modulated input of Gaussian filtered alternating 1's and -1's was inputted into the VCO to generate a GMSK waveform. Frequency spectrum plots of this waveform for Σ–Δ modulator frequencies of 10 MHz and 100 MHz are shown in Figure 17 and Figure 18. The frequency plots shown in Figure 18 closely match the ideal MATLAB simulated frequency plots shown in Figure 9. By increasing the Σ–Δ modulator frequency, the quantization noise is attenuated as expected. With a Σ–Δ frequency of 100 MHz, the quantization noise has a maximum value of -50 dB compared to a maximum value of -25 dB with a Σ–Δ frequency of 10 MHz.

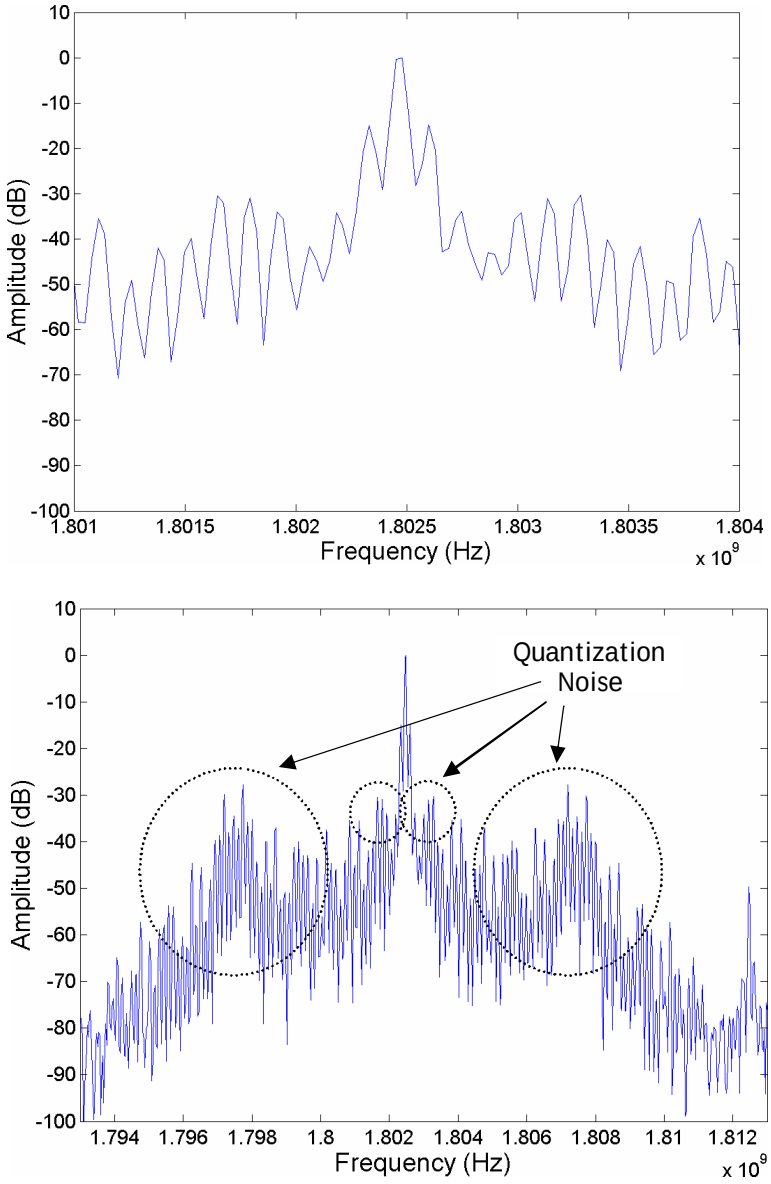


Figure 17: Frequency spectrum plots of GMSK output
(Σ–Δ Frequency of 10 MHz)

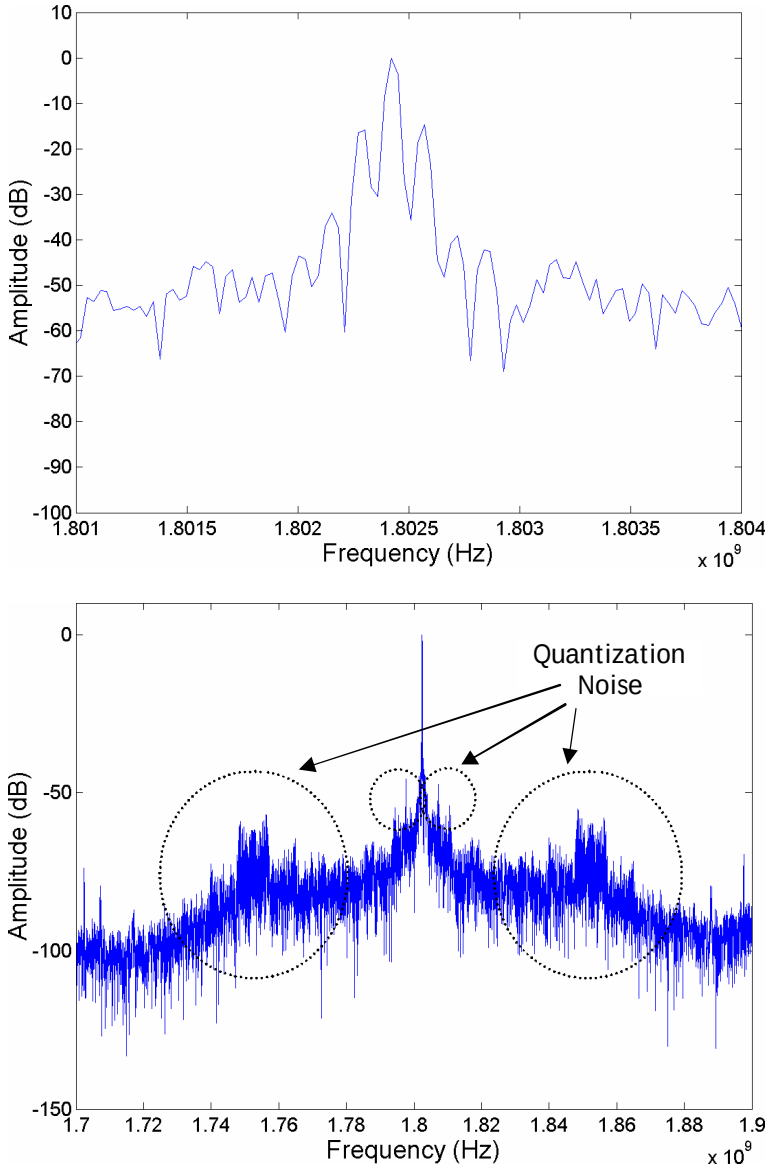


Figure 18: Frequency spectrum plots of GMSK output
(Σ–Δ Frequency of 100 MHz)

Chapter 4

Experimental Results

4.1: Overview

To test the feasibility of the proposed modulation architecture, a voltage-controlled oscillator was prototyped on a two-sided printed circuit board using discrete components. For simplicity, narrowband frequency/phase modulation was implemented at a carrier frequency of 120 MHz. The voltage-controlled oscillator was implemented using a single-ended Colpitts LC oscillator as shown in Figure 19.

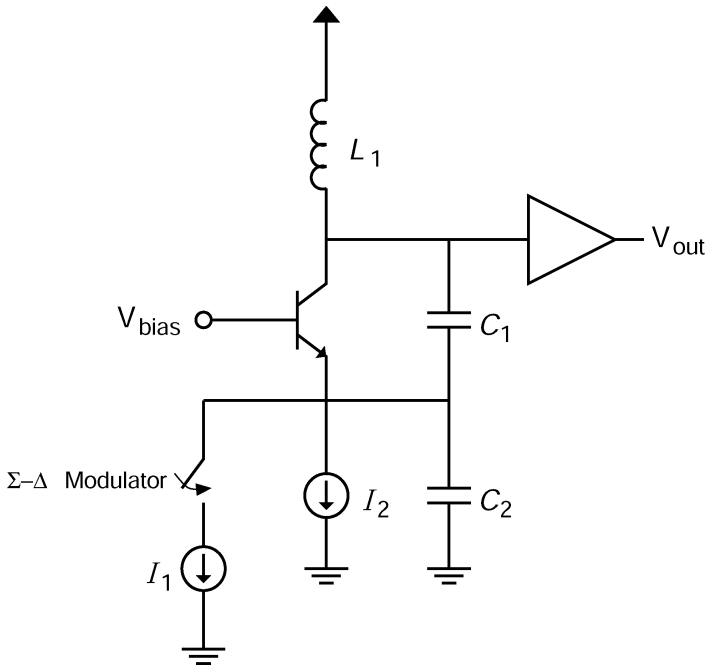


Figure 19: Single-ended Colpitts LC oscillator

L_1	20 nH
C_1	39 pF
C_2	270 pF
I_1	57.2 µA
I_2	3.07 mA
V_{bias}	1.8 V

Table 5: Values for the single-ended LC oscillator

The printed circuit board was constructed using a milling machine and the discrete transistors used were Intersil HFA 3127 ultra-high frequency transistor arrays. Figure 20 shows a picture of the printed circuit board.

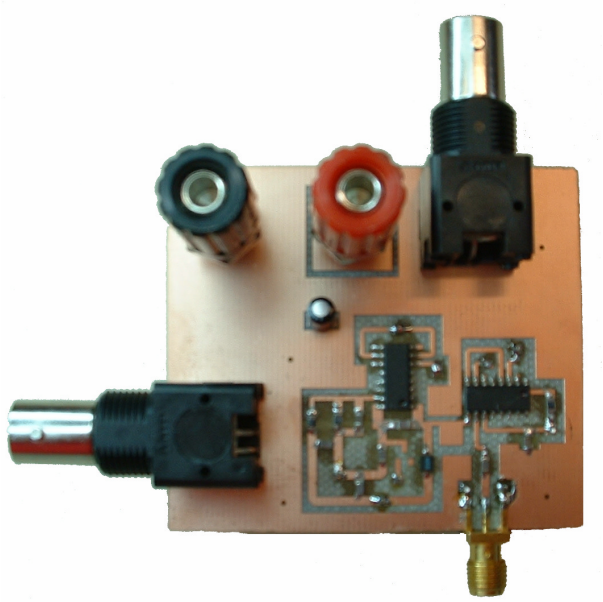


Figure 20: Printed Circuit Board

A 4 kHz sinusoid was passed through a second-order, one-bit Σ–Δ modulator at various oversampling ratios. To reduce the complexity of the PCB, the Σ–Δ modulation was done in MATLAB and then imported into a function generator. The Σ–Δ modulated data from the function generator switched the bias current through the oscillator, thereby switching the oscillation frequency between the two frequencies shown in Figure 21.

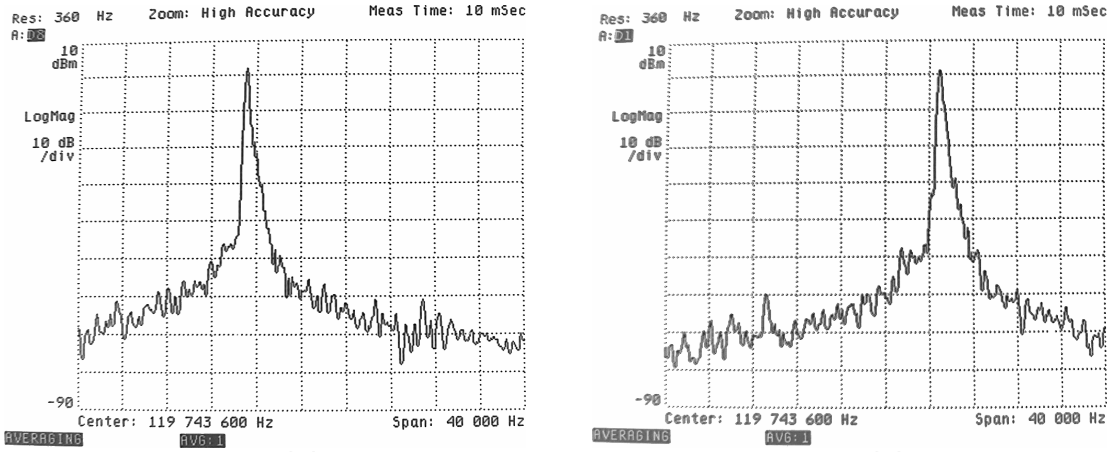
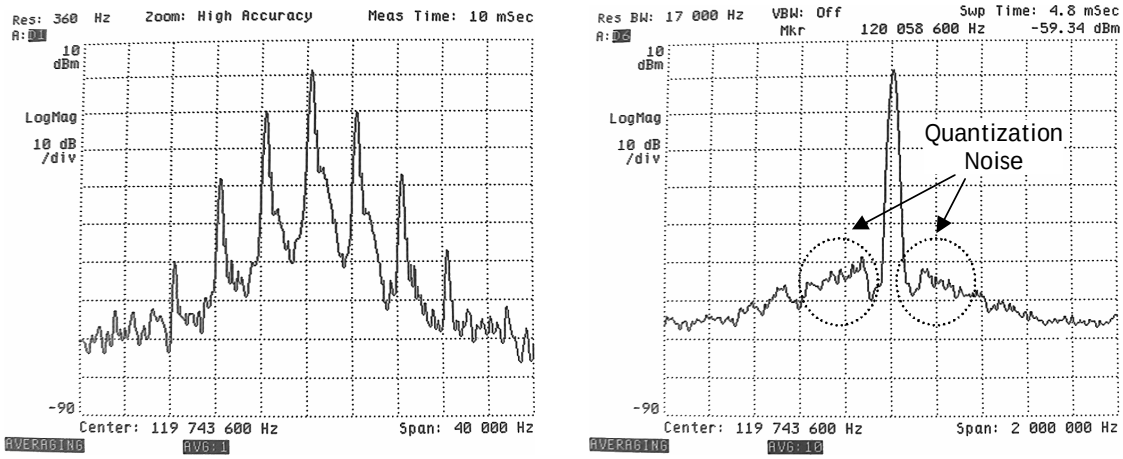


Figure 21: (A) Lower frequency and (B) upper frequency that the oscillator switched between

4.2: Frequency Spectrum Plots

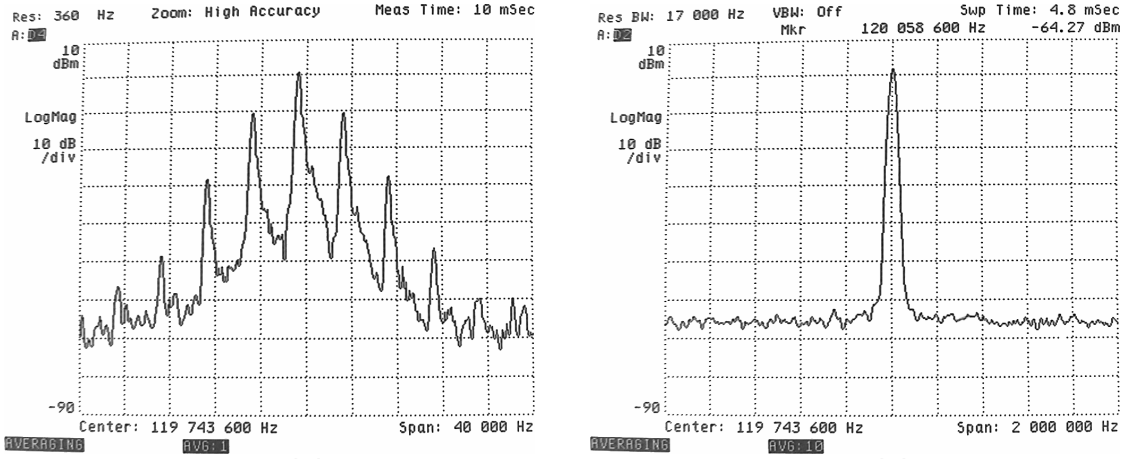
Figure 22 shows the narrow band and wide band output frequency spectrums when the Σ–Δ modulator was clocked at 1 MHz. As expected, the Σ–Δ quantization noise is at a minimum at the carrier frequency and at 1 MHz away from the carrier frequency.

To reduce the quantization noise in the output, the Σ–Δ frequency was increased. Figure 23 shows the narrow band and wide band frequency spectrums when the Σ–Δ modulator was clocked at 10 MHz. Over a narrow bandwidth, the frequency spectrums in Figure 22 and Figure 23 look identical. However, Figure 23.b) has significantly less quantization noise visible than Figure 22.b). This can be explained due to two reasons. A 10 MHz Σ–Δ modulator still generates quantization noise, but at a frequency sufficiently far away from the carrier frequency such that the noise is filtered out by the VCO. As well, with a higher frequency Σ–Δ modulator, the quantization noise is spread over a larger frequency range.



(A) (B)

Figure 22: (A) Narrow band and (B) wide band frequency spectrum of a FM sine wave (Σ–Δ clocked at 1 MHz)



(A) (B)

Figure 23: (A) Narrow band and (B) wide band frequency spectrum of a FM sine wave (Σ–Δ clocked at 10 MHz)

Chapter 5

Conclusion

5.1: Summary

A constant-envelope, continuous phase modulation architecture was presented in which a sigma-delta modulator is combined with a direct modulator. The main advantages of this architecture are that linearity of the oscillator's tuning device is ensured and implementation is simplified due to the use of discrete frequency switching in the oscillator. The main disadvantage is that the quantization noise introduced by the Σ–Δ modulator must be filtered out or spread out to ensure wireless noise specifications are met.

In Chapter 2, the architecture was analyzed from a systems perspective in both open-loop and closed-loop configurations. The instantaneous frequency response of the VCO was found to be an important design consideration. In Chapter 3, the architecture was simulated in an open-loop configuration implementing GMSK modulation for use in a GSM transceiver. A prototype, low-frequency implementation of the modulation architecture was constructed and experimental results were presented in Chapter 4. By increasing the Σ–Δ modulation frequency, the quantization noise was filtered out by the VCO and disappeared beneath the measurement noise floor.

5.2: Future Work

One area of future work is designing an integrated PLL and fully-differential VCO on-chip that is capable of implementing the proposed modulation architecture in both an open-loop and closed-loop configuration. Other areas of research include investigating multi-bit or bandpass Σ–Δ modulators in this

architecture and designing a VCO that has a narrowband instantaneous frequency response to aid in filtering out the quantization noise.

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Appendix A: PLL Closed-Loop Calculations

Assuming that $H_{VCO}(s)$ has a low pass response, the transfer function from the data input to the frequency output is bandpass with a lower -3dB cutoff frequency of w_L. Solving for w_L:

$$\left|H_{VCO}(s)K_{PD}H_{lf}(s)+Ns\right|=\left|\sqrt{2}Ns\right|$$

$$\left|H_{VCO}(jw_L)K_{PD}H_{lf}(jw_L)+jNw_L\right|=\sqrt{2}Nw_L$$

If we only consider the low frequency pole and zero of the loop filter:

$$\left|\frac{K_{VCO}K_{PD}\left(1+\frac{jw_L}{w_Z}\right)}{\left(1+\frac{jw_L}{w_{p1}}\right)}+jNw_L\right|=\sqrt{2}Nw_L$$

$$\left|\frac{\frac{K_{VCO}K_{PD}}{w_L}+j\frac{K_{VCO}K_{PD}}{w_Z}-\frac{Nw_L}{w_{p1}}+Nj}{\left(1+\frac{jw_L}{w_{p1}}\right)}\right|w_L=\sqrt{2}Nw_L$$

$$\left|\frac{\frac{K_{VCO}K_{PD}}{w_L}-\frac{Nw_L}{w_{p1}}+j\left(N+\frac{K_{VCO}K_{PD}}{w_Z}\right)}{\left(1+\frac{jw_L}{w_{p1}}\right)}\right|=\sqrt{2}N$$

$$\frac{\sqrt{\left(\frac{K_{VCO}K_{PD}}{w_L}-\frac{Nw_L}{w_{p1}}\right)^2+\left(N+\frac{K_{VCO}K_{PD}}{w_Z}\right)^2}}{\sqrt{\left(\frac{w_L}{w_{p1}}\right)^2+1}}=\sqrt{2}N$$

This is a quadratic equation in terms of w_L^2. Expanding in terms of w_L^2:

$$\left(\frac{K_{VCO}K_{PD}}{w_L}-\frac{Nw_L}{w_{p1}}\right)^2+\left(N+\frac{K_{VCO}K_{PD}}{w_Z}\right)^2=2N^2\left(\frac{w_L}{w_{p1}}\right)^2+2N^2$$

$$K_{VCO}{}^2K_{PD}{}^2+\frac{N^2}{w_{p1}{}^2}w_L{}^4-\frac{2K_{VCO}K_{PD}N}{w_{p1}}w_L{}^2+\left(N+\frac{K_{VCO}K_{PD}}{w_Z}\right)^2w_L{}^2=\frac{2N^2}{w_{p1}{}^2}w_L{}^4+2N^2w_L{}^2$$

$$\frac{N^2}{{w_{p1}}^2} {w_L}^4 + \left(2N^2 + \frac{2K_{VCO}K_{PD}N}{w_{p1}} - \left(N + \frac{K_{VCO}K_{PD}}{w_Z} \right)^2 \right) {w_L}^2 - {K_{VCO}}^2 {K_{PD}}^2 = 0$$

$${w_L}^4 + \left(2{w_{p1}}^2 + 2K_{VCO}K_{PD}N^{-1}w_{p1} - \left(w_{p1} + \frac{K_{VCO}K_{PD}w_{p1}}{Nw_Z} \right)^2 \right) {w_L}^2 - N^{-2}{K_{VCO}}^2 {K_{PD}}^2 {w_{p1}}^2 = 0$$

Solving the quadratic equation:

$${w_L}^2 = -0.5\left(2{w_{p1}}^2 + 2K_{VCO}K_{PD}N^{-1}w_{p1} - \left(w_{p1} + \frac{K_{VCO}K_{PD}w_{p1}}{Nw_Z} \right)^2 \right)$$

$$\pm 0.5\sqrt{\left(2{w_{p1}}^2 + 2K_{VCO}K_{PD}N^{-1}w_{p1} - \left(w_{p1} + \frac{K_{VCO}K_{PD}w_{p1}}{Nw_Z} \right)^2 \right)^2 + 4N^{-2}{K_{VCO}}^2 {K_{PD}}^2 {w_{p1}}^2}$$

Since w_L must be positive and real:

$$w_L = \sqrt{-0.5b + 0.5\sqrt{b^2 + 4N^{-2}{K_{VCO}}^2 {K_{PD}}^2 {w_{p1}}^2}}$$

where $b = 2{w_{p1}}^2 + 2K_{VCO}K_{PD}N^{-1}w_{p1} - \left(w_{p1} + \frac{K_{VCO}K_{PD}w_{p1}}{Nw_Z} \right)^2$

If we instead assume that the low frequency loop filter pole is placed at dc, we can conduct a similar analysis:

$$H_{lf}(s) = \frac{1 + \frac{s}{w_z}}{s}$$

$$\left| \frac{K_{VCO}K_{PD}\left(1 + \frac{jw_L}{w_Z}\right)}{jw_L} + jNw_L \right| = \sqrt{2}Nw_L$$

$$\left| \frac{\frac{K_{VCO}K_{PD}}{w_L} + j\frac{K_{VCO}K_{PD}}{w_Z} - Nw_L}{jw_L} \right| w_L = \sqrt{2}Nw_L$$

$$\left| \frac{\frac{K_{VCO}K_{PD}}{w_L} - Nw_L + j\frac{K_{VCO}K_{PD}}{w_Z}}{jw_L} \right| = \sqrt{2}N$$

$$\frac{\sqrt{\left(\frac{K_{VCO}K_{PD}}{w_L} - Nw_L\right)^2 + \left(\frac{K_{VCO}K_{PD}}{w_Z}\right)^2}}{w_L} = \sqrt{2}N$$

This is a quadratic equation in terms of w_L^2. Expanding in terms of w_L^2:

$$\left(\frac{K_{VCO}K_{PD}}{w_L} - Nw_L\right)^2 + \left(\frac{K_{VCO}K_{PD}}{w_Z}\right)^2 = 2N^2 w_L^2$$

$$K_{VCO}^2 K_{PD2}^2 + N^2 w_L^4 - 2K_{VCO}K_{PD}Nw_L^2 + \left(\frac{K_{VCO}K_{PD}}{w_Z}\right)^2 w_L^2 = 2N^2 w_L^4$$

$$N^2 w_L^4 + \left(2K_{VCO}K_{PD}N - \left(\frac{K_{VCO}K_{PD}}{w_Z}\right)^2\right) w_L^2 - K_{VCO}^2 K_{PD}^2 = 0$$

$$w_L^4 + \left(2K_{VCO}K_{PD}N^{-1} - \left(\frac{K_{VCO}K_{PD}}{Nw_Z}\right)^2\right) w_L^2 - N^{-2}K_{VCO}^2 K_{PD}^2 = 0$$

Solving the quadratic equation:

$$w_L^2 = -0.5\left(2K_{VCO}K_{PD}N^{-1} - \left(\frac{K_{VCO}K_{PD}}{Nw_Z}\right)^2\right) \pm 0.5\sqrt{\left(2K_{VCO}K_{PD}N^{-1} - \left(\frac{K_{VCO}K_{PD}}{Nw_Z}\right)^2\right)^2 + 4N^{-2}K_{VCO}{}^2K_{PD}{}^2}$$

Since w_L must be positive and real:

$$w_L = \sqrt{-0.5b + 0.5\sqrt{b^2 + 4N^{-2}K_{VCO}{}^2K_{PD}{}^2}}$$

where $b = 2K_{VCO}K_{PD}N^{-1} - \left(\frac{K_{VCO}K_{PD}}{Nw_Z}\right)^2$