A Digital Phase-Locked Loop With Calibrated Coarse and Stochastic Fine TDC

Amer Samarah, *Student Member, IEEE*, and Anthony Chan Carusone, *Senior Member, IEEE*

***Abstract*—A coarse–fine time-to-digital converter (TDC) is presented with a calibrated coarse stage followed by a stochastic fine stage. On power-up, a calibration algorithm based on a code density test is used to minimize nonlinearities in the coarse TDC. By using a balanced mean method, the number of registers required for the calibration algorithm is reduced by 30%. Based upon the coarse TDC output, the appropriate clock signals are multiplexed into the stochastic fine TDC. The TDC is incorporated into a 1.99–2.5-GHz digital phase-locked loop (DPLL) in 0.13-μm CMOS. The DPLL consumes a total of 15.2 mW of which 4.4 mW are consumed in the TDC. Measurements show an in-band phase noise of −107 dBc/Hz which is equivalent to 4-ps TDC resolution, approximately an order of magnitude better than an inverter delay in this process technology. The integrated random jitter is 213 fs rms for a 2-GHz output carrier frequency with 700-kHz loop bandwidth. The calibration reduces worst-case spurs by 16 dB.**

***Index Terms*—Bang bang, code density test, coarse–fine time-to-digital converter (TDC), digital loop filter, digital phase-locked loop (DPLL), digitally controlled oscillator (DCO), nonlinearities, stochastic TDC, TDC calibration.**

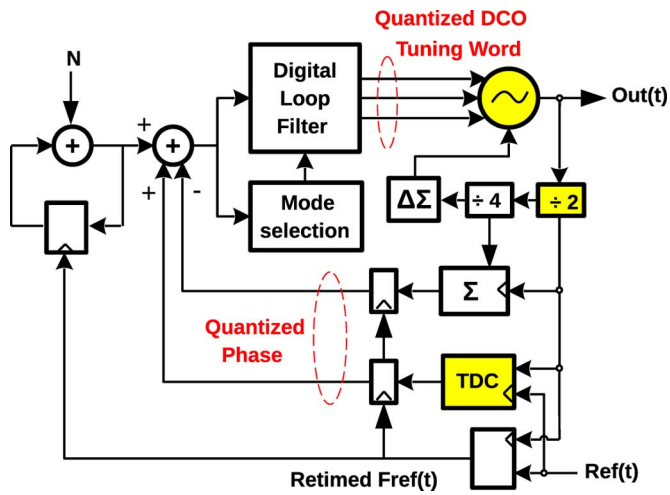

Fig. 1. DPLL architecture for fractional frequency synthesis [21].

I. Introduction

MODERN wireless and wireline communication standards place challenging demands on the phase noise, spurious tones, jitter accumulation, and modulation bandwidth of phase-locked-loops (PLLs) [1]. Research on digital PLLs (DPLLs) has been actively trying to replace or complement traditional analog PLLs by taking advantage of aggressive CMOS scaling and operating under lower supply voltages.

DPLLs offer several advantages over their analog counterparts. Analog PLLs require large on-chip capacitors whose leakage can seriously degrade PLL jitter performance [2]. Furthermore, it becomes harder to design low-noise charge pumps to operate under the low supply voltages of advanced nanoscale CMOS technologies. State-of-the-art analog PLLs employ analog phase-noise-cancellation techniques to enable low fractional spurs and low phase noise at loop bandwidths of 700 kHz to 1 MHz [3]. However, matching a DAC cancellation signal to the phase error is a complicated and difficult analog circuit challenge. On the other hand, DPLLs are less sensitive to external noise and process parameter, voltage, and temperature (PVT) variations since many DPLL building blocks are realized with purely digital logic circuits.

However, DPLLs do impose new design challenges due to the quantization of frequency and phase which introduces noise and, hence, jitter. The DPLL architecture considered in this work is shown in Fig. 1. It comprises an integer counter and a time-to-digital-converter (TDC) which together provide a fractional frequency count. The result is digitally subtracted from a reference value with a simple finite-state-machine (FSM), digitally filtered, and then applied to a digitally controlled oscillator (DCO). TDC quantization noise and reference clock jitter are low-pass filtered by the DPLL's dynamics and are therefore dominant at low frequencies within the DPLL loop bandwidth. On the other hand, DCO noise is high-pass filtered and dominant at high frequencies as shown in Fig. 2.

Combining wide loop bandwidth and excellent in-band phase noise performance remains particularly challenging for DPLLs. The work in [4] demonstrates that a DPLL can meet even the difficult GSM specification. However, its loop bandwidth of 40 kHz remains an order of magnitude lower than that achieved by the analog techniques described above. In applications where only high-frequency phase noise is of interest, a wide loop bandwidth can be accommodated in a DPLL with a simple bang-bang phase detector (no TDC), such is the case in [5], where, for a particular wireline application only phase noise above $f_c/1667$ matters. However, more generally in DPLLs with wide loop bandwidth, it is desirable to have very fine TDC resolution. At the same time, the TDC's input dynamic range should be large enough to cover at least one DCO period in order for the

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The authors are with the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4 Canada (e-mail: samaraha@eecg.utoronto.ca).

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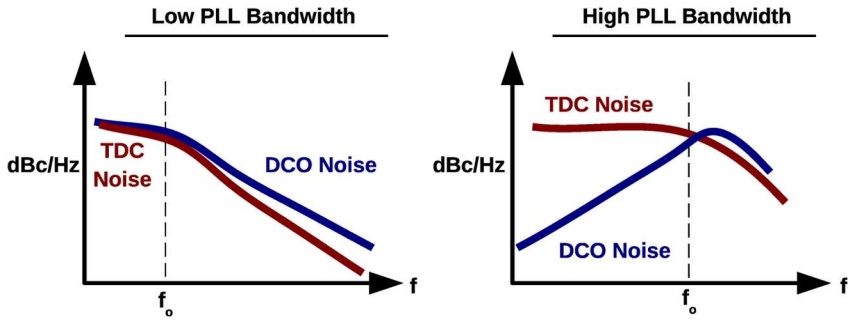

Fig. 2. Phase noise contributions for low- and high-bandwidth DPLLs.

DPLL to estimate the phase error across a complete DCO period. An even larger dynamic range of at least two DCO periods is needed if on-chip jitter measurement is to be performed. Although two recent DPLLs extended loop bandwidths to 142 kHz [6] and 3 MHz [7], the former one cannot achieve low in-band phase noise while the latter work sacrifices its out-of-band noise performance.

Fine TDC resolution also prevents detrimental nonlinear dynamics from arising in DPLLs. If a DPLL is operating as a fractional-N synthesizer, the phase relationship between DCO output and reference input is scrambled over time, and the quantization error introduced by the TDC may be approximated as white noise [8]. However, if the DPLL is locked in an integer-N mode, the phase relationship between TDC inputs is fixed and the TDC may exhibit either bang-bang behavior (associated with unpredictable loop bandwidth) or it may exhibit a dead-zone behavior resulting in chaotic dynamics that are very dependent upon the initial conditions of the loop. This is evident in Fig. 3 which shows several phase-noise simulations of a DPLL having a TDC resolution of 32 ps operating in an integer mode. Each simulation has a different initial phase difference between the REF clock and DCO output clock. The DPLL output phase noise is very inconsistent. This can be mitigated by dithering the phase error as demonstrated in [9] or by improving TDC resolution. This work focuses on improving TDC resolution as doing so improves the noise performance of DPLLs in both integer and fractional synthesis modes.

The simplest implementation of a TDC uses an inverter-delay line [10]. Its time resolution is limited by the inverter delay which is technology-dependent. In 0.13-μm CMOS, the nominal inverter delay is about 30–40 ps while in 28-nm CMOS technology the inverter delay is around 10–12 ps.

Vernier delay lines are a straightforward method to improve TDC resolution, using two delay lines with slightly different stage delays, T_a and T_b, so that the TDC resolution is determined by the delay difference between the two inverters [$T_a - T_b$] [7], [11]. However, Vernier TDCs require considerable additional power consumption and area. For example, the Vernier delay line in [12] uses two delay lines consisting of 80 buffers providing 5-ps resolution but resulting in a relatively high DPLL power consumption of 50 mW in a 90-nm CMOS process. A two-dimensional (2-D) Vernier TDC [13] is proposed to reduces the number of delay stages and the power consumption. However, 2-D Vernier TDC resolves 4.8 ps only in 65-nm CMOS technology. A DPLL employing a 2-D Vernier TDC [14] shows

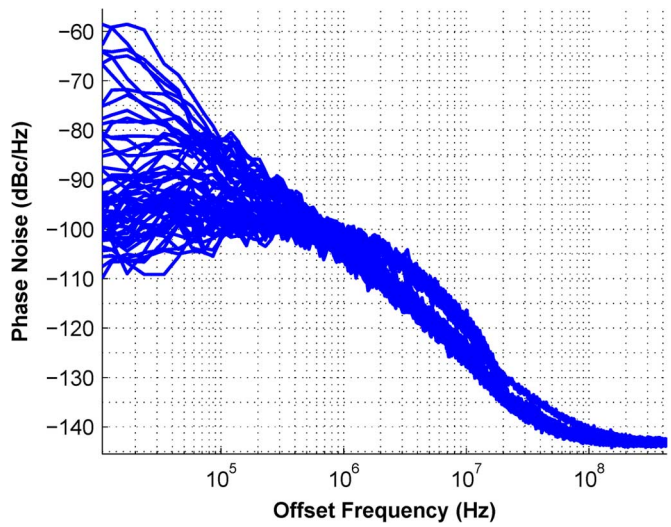

Fig. 3. DPLL exhibiting very inconsistent output phase noise responses when simulated under different initial phase conditions during integer mode operation due to dead-zone nonidealities [9].

a very good noise performance while consumes 41.6 mW in 55-nm process.

Recently, several other TDC architectures have been explored to improve TDC resolution. The gated ring-oscillator (GRO) TDC reported in [8] achieved an effective resolution of 6 ps in a 0.13-μm technology. It measured the phase error between two signals by enabling a ring oscillator only during the measurement window providing first-order quantization noise shaping. The GRO-based TDC employs multi-phase coupled oscillators to average its delay and so it consumed up to 21 mW for large phase errors.

Two-step TDCs combine a coarse stage and a fine stage to provide fine resolution while still covering a wide dynamic range of input phase error. For example, the two-step TDC in [15] uses a delay-line TDC as the coarse TDC followed by a Vernier delay-line fine TDC. In [16], the residual phase error after a coarse TDC is time-amplified and applied to another TDC with relatively coarse resolution. Unfortunately, the time amplifier has high power consumption and a complex analog design which conflicts with the goal of digitizing the PLL circuits.

An interpolation-based TDC is reported in [17]. It employs a differential delay line to obtain coarse delay steps. It then interpolates between neighboring phases with a resistor voltage

divider to achieve a small delay step of 4.7 ps in 90-nm technology. However, that TDC uses two auxiliary TDCs and an extra digital loop filter for correction and calibration making it power-hungry.

In [18], a dual-loop DPLL architecture is presented that employs a frequency detector and a stochastic time-to-digital converter (STDC) during lock state to accurately resolve the phase error between the reference clock and DCO divided clock after frequency acquisition. The STDC improves the noise performance compared with the frequency detector but that architecture does not allow direct wide-bandwidth modulation while keeping low noise performance since the loop will keep going back and forth between frequency acquisition and phase tracking modes due to the narrow phase-detection range of the STDC.

In this paper, we present a fractional DPLL that incorporates a novel low-power two-step coarse–fine TDC to achieve low in-band phase noise operation. We employ a STDC for the fine TDC stage while still achieving wide locking range using a coarse delay-line TDC.

This paper is structured as follows. In Section II, an overview of the proposed coarse-fine TDC is given. In Section III, we discuss TDC nonlinearities and their effect on phase noise along with a low-area calibration algorithm to alleviate these problems. In Section IV, we present the DPLL z-domain model with insights on loop dynamics. Finally, measurement results of the DPLL prototype are shown Section V.

II. Fine–Coarse TDC

A TDC is widely used in many applications such as nuclear experiments for timing single-shot events, laser range finders, and space science instruments [19]. In DPLLs, it has been employed for the measurement of phase difference between a reference and output clock.

TDCs quantize the phase difference which results in a quantization noise determined by the TDC resolution. The phase noise contributed by TDC quantization in, for example, [4], [6], and [20] is unacceptable for many applications that require wide loop bandwidth like LAN, WCDMA, HSPCA, and LTE [1]. However, designing a fine-resolution and low-power TDC is a challenging task.

Assuming the TDC uniformly quantizes the phase difference with a given TDC resolution $\Delta t_{\rm tdc}$, the in-band noise floor of the DPLL with output frequency $f_{\rm out}$ and reference frequency $f_{\rm ref}$ is [10]

$$\ell = \frac{\pi^2}{3}\cdot\left(\frac{\Delta t_{\rm tdc}}{T_{\rm out}}\right)^2\cdot\frac{1}{f_{\rm ref}} = \left(\frac{\pi^2}{3}\cdot\frac{f_{\rm out}^2}{f_{\rm ref}}\right)\Delta t_{\rm tdc}^2. \quad (1)$$

Reducing TDC resolution by factor of 10 reduces in-band phase noise by 20 dB. For example, with a 20-MHz reference clock, 2.5-GHz output clock, and 40-ps TDC resolution, the in-band phase-noise contribution is around -87 dBc/Hz. If the TDC resolution is reduced to 4 ps, the phase noise will drop to -107 dBc/Hz. This work reports on a low-power coarse–fine TDC achieving 4-ps TDC resolution in a 0.13-μm technology [21]. As shown in Figs. 4 and 5, the proposed TDC architecture uses a coarse-resolution TDC to select a delayed version of the reference clock for further comparison with the output clock

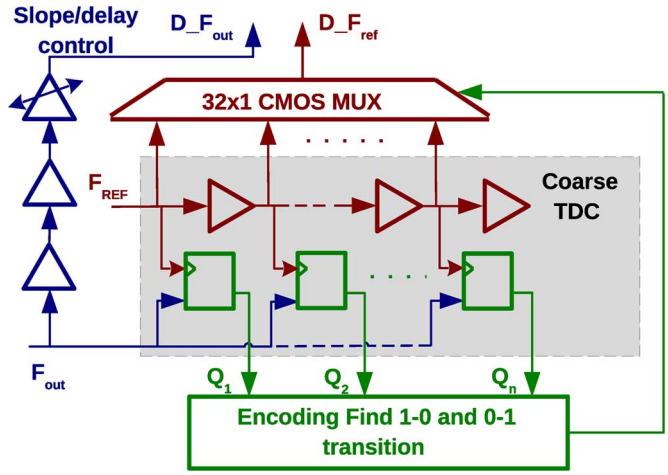

Fig. 4. Coarse TDC architecture of a two-step TDC. The closest delayed version of $F_{\rm ref}$ to $F_{\rm out}$ is muxed to the second TDC stage. Path delays for the selected reference phase $F_{\rm ref}$ to $D\_F_{\rm ref}$ and DCO clock $F_{\rm out}$ to $D\_F_{\rm out}$ are matched.

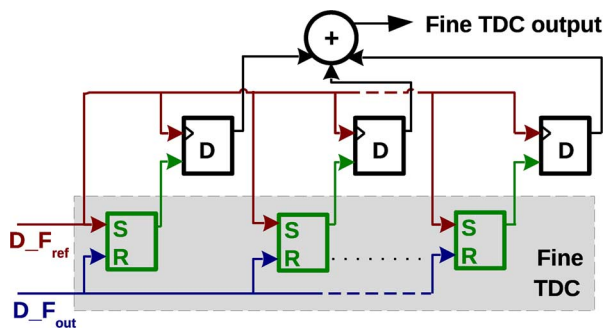

Fig. 5. Fine stochastic TDC (STDC) architecture of the two-step TDC. The STDC outputs are sampled on the rising edge of the delayed reference clock.

in a fine-resolution TDC. The fine-resolution TDC then uses the stochastic variation of latch offsets to provide a resolution much better than the technology's inverter delay.

A. Coarse TDC

The coarse TDC shown in Fig. 4 generates 32 delayed versions of the low-frequency reference clock by passing it through chain of pseudo-differential inverters with adjustable delay. Then, the delayed reference clocks are used for sampling the high-frequency output clock using sense-amplifier flip-flops that have a narrow symmetric metastability window [10]. The coarse TDC must cover at least one DCO period at the slowest operating frequency of the DPLL. Passing the low-frequency reference clock rather than the high frequency output clock through the inverter chain provides two advantages: lower power consumption and lower jitter induced by the power supply during the sharp transitions on both the rising and falling edges of the clock signal through the inverters.

An encoder and 32-to-1 multiplexer is used to to select one of the delayed versions of the reference clock for further comparison with the output clock using the fine TDC. The encoder introduces a delay which makes it impossible to tap the output of the delay buffer where the 1–0 transition occurs, since by then the reference clock edge has propagated further. To solve this problem, the mux selects the output of the second buffer after

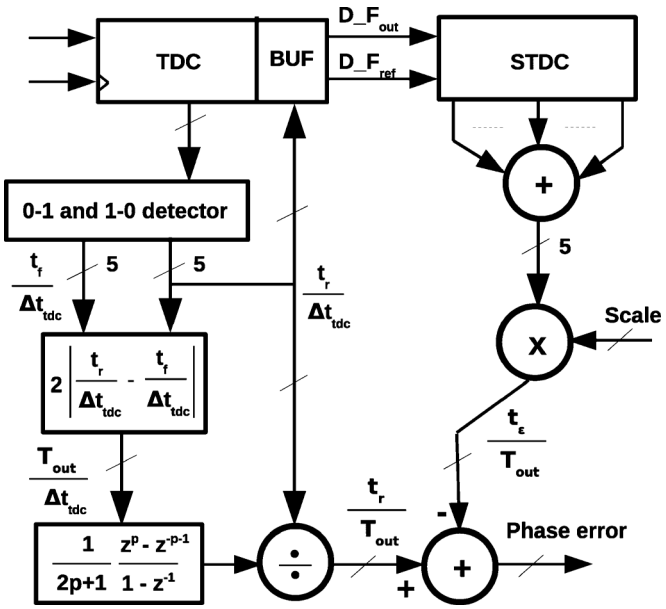

Fig. 6. Phase error computation and normalization with respect to one DCO period, performed digitally. The phase error computed by the coarse TDC is refined by the STDC.

the 1–0 edge transition, passing it into the fine TDC. Moreover, the DCO clock is also delayed to mimic the extra delay experienced by the selected reference clock phase, before comparison by the fine TDC, as shown on the left of Fig. 4.

The raw TDC output data forms a pseudo-thermometer code which is encoded into two binary numbers using a priority encoder, shown in Fig. 6. One number represents the position of the $1 \rightarrow 0$ transition, t_f, while the other number represents the position of the $0 \rightarrow 1$ transition, t_r. The approximate instantaneous DCO period in number of inverter delays, $T_{\rm out}$, is calculated by doubling the absolute difference between t_f and t_r. Note that, using this scheme, duty cycle distortion causes an instantaneous error in the estimate of $T_{\rm out}$. This error is time varying such that, on average, it has no or little effect especially with the use of moving average filter after the estimation block in Fig. 6. This could be eliminated by increasing the length of the delay line to capture two consecutive rising edges of the output clock and taking the difference between them, with a corresponding increase in power consumption. Variations in the DCO period estimate $T_{\rm out}$ are averaged over time using a moving average filter. The resulting averaged $T_{\rm out}$ then normalizes the timing of the DCO clock rising edge t_r at the bottom of Fig. 6. The normalized phase difference is then further refined using the fine TDC output.

B. Fine Stochastic TDC

The stochastic TDC is composed of N identical arbiters evaluating in parallel the phase relationship between two incoming signals [18]. Ideally, each arbiter circuit instantly generates a logical '0' or '1' depending upon which one of the two input signals transitions first.

In reality, the arbiters exhibit several non idealities. The output settling time increases when the time offset between the incoming signals Δt is small. If the time offset is in the vicinity of zero, the arbiter exhibits metastability and can take a very long time to settle. Moreover, due to device mismatch, each arbiter exhibits a random input offset voltage $V_{\rm OS}$ that creates different voltage thresholds for each arbiter, as shown in Fig. 7(a). Over a large number of arbiters, these voltage offsets will be Gaussian-distributed with a standard deviation σ_V.

The voltage offsets translate into input-referred time offsets $T_{\rm OS}$ which will also be Gaussian distributed with standard deviation σ_T. If the input clock signals have a long rise time, even a small voltage offset $V_{\rm OS}$ will translate into a large time offset $T_{\rm OS}$. Accordingly, the time offset of an arbiter can be related to its voltage offset by the slope of the input signals, $T_{\rm OS} = V_{\rm OS}/S$ and $\sigma_T = \sigma_V/S$.

The cumulative distribution function (CDF) of the Gaussian-distributed arbiter random time offsets follows the error function and is given by $\mathrm{CDF}(t_d) = \int_{-\infty}^{t_d} (1)/(\sqrt{2\pi}\sigma_T) e^{-(T_{\rm OS}^2)/(2\sigma_T^2)}\, dt$. The average stochastic TDC output can be estimated using a Taylor series expansion of the error function, $\mathrm{erf}(x) = (2)/(\sqrt{\pi})(x - (x^3)/(3) + (x^5)/(10) - \cdots)$. Hence, assuming that the time offset has 0 mean and σ_T standard deviation, its CDF is$\mathrm{CDF}(t_d; 0, \sigma_T) = (1)/(2)[1 + \mathrm{erf}((t_d)/(\sigma_T\sqrt{2}))]$ whose linear approximation around the mean is $\mathrm{CDF}(t_d; 0, \sigma_T) \approx (1)/(2) + (1)/(\sqrt{2\pi}\sigma_T) t_d$. Hence, the summed output of a population of N arbiters has the following CDF:

$$\mathrm{CDF}(t_d; 0, \sigma_T) \approx \frac{N}{2} + \frac{N}{\sqrt{2\pi}\sigma_T} t_d. \tag{2}$$

The CDF function's approximately linear region is around $t_d \epsilon [-\sigma_T, \sigma_T]$, as shown in Fig. 8. The stochastic TDC resolution can be estimated as the inverse of the slope of the CDF function around the mean

$$\Delta\mathrm{LSB} = \frac{\sqrt{(2\pi)}\sigma_T}{N} = \frac{\sqrt{(2\pi)}\sigma_V}{S \cdot N}. \tag{3}$$

From the above equation, it is obvious that the resolution of the stochastic TDC is determined by the number of arbiters used, the statistical properties of the transistors used to design those particular arbiters, and the slope of the input signals. Large latch mismatch can be achieved by using minimal transistor sizes. However, the slope of the incoming signal has an even greater effect on the stochastic TDC resolution and dynamic range and is therefore controlled using a programmable slope control circuit, implemented by modifying the PMOS load of a CMOS buffer. Although this may increase short-term jitter, its impact upon performance was deemed relatively insignificant for the targeted resolution.

A digital normalizing "Scale" factor is provided on the right-hand side of Fig. 6 to normalize the fine TDC output against uncertainty in the clock signal slope S and time offset statistics σ_T. In our case, the Scale factor can be adjusted with 2 b of resolution. Since the statistical mismatch parameters of the transistors were not accurately known during the design phase, the Scale factor was adjusted during testing. In a commercial product, the Scale factor can be calibrated using a technique similar to the one described in Section III for the coarse TDC. In this work, only calibration of the coarse TDC was implemented on-chip since any inaccuracies there will be dominant.

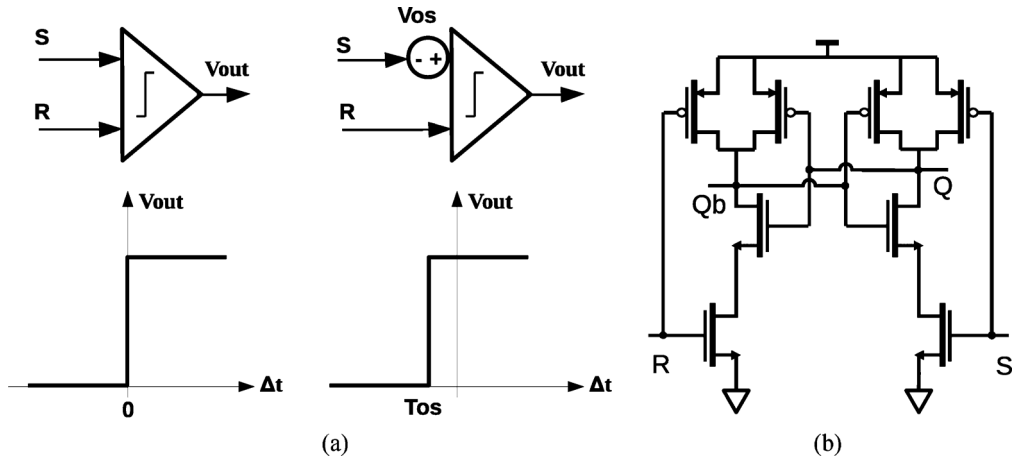

Fig. 7. (a) Stochastic TDC arbiter input–output relationship without and with random mismatch. Input-referred voltage offset due mismatch tranlates into time offset. (b) SR-Latch used in the stochastic TDC as arbiter.

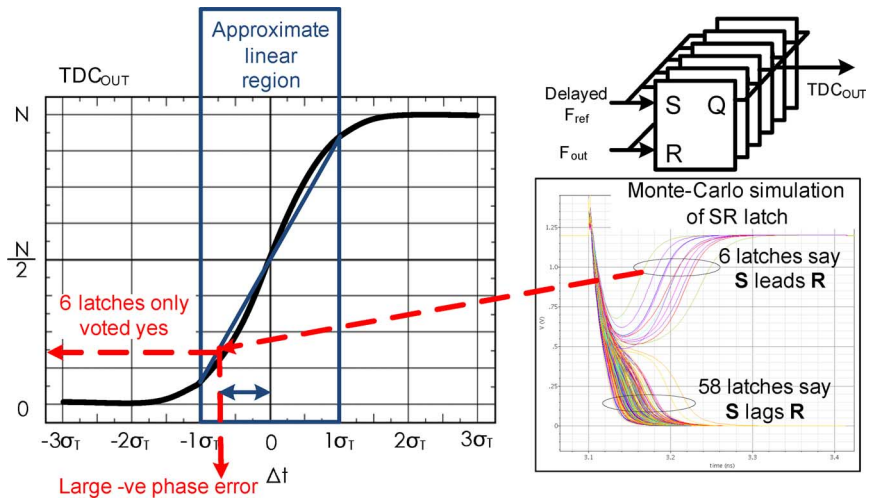

Fig. 8. Monte Carlo simulation of the stochastic TDC for a given negative phase error. The sum of all STDC arbiter outputs translates into a phase error within the linear region of the time-offset's statistical CDF.

The arbiters have been implemented as set-reset latches based on cross-coupled NAND gates, as shown in Fig. 7(b). The output of these arbiters are sampled on the rising edge of the delayed reference clock, as shown in Fig. 5. This is important to ensure that the STDC captures the correct value of the arbiter before it may change its state.

The arbiters within the STDC were estimated to have a voltage offset with a standard deviation of 16 mV, according to Monte Carlo simulations. The reference signal is buffered such that its rise time has a slope of 2 V/ns. Accordingly, the STDC has an offset that exhibits a standard deviation of 32 ps. This enables the fine STDC to have a 64-ps approximately linear region which is around two times the coarse TDC resolution. A wide linear range is desirable since any systematic mismatch (for example as caused by layout mismatch) will shift the CDF to left or right and reduce the useful linear range and the ability of the STDC to accurately resolve time differences [21]. It is possible to extend the linear range of the STDC by using methods similar to those used for stochastic ADCs. For example, the work in [22] demonstrates a stochastic ADC with two groups of arbiters where their PDFs are shifted left and right by applying a symmetric offset. This would create a virtually uniform distribution of the arbiters' offsets and improve the CDF linearity with fewer arbiters.

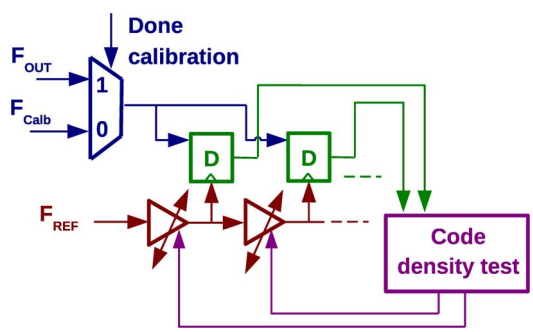

Fig. 9. On-chip low-area calibration algorithm of the coarse TDC based on a code density test. The dedicated calibration clock F_{calb} is sampled by the CTDC during calibration phase, and, once done, the CTDC samples the DCO clock.

To achieve 2-ps average resolution, at least 40 arbiters are required. To ensure the targeted resolution could be robustly achieved in the presence of random variations in the arbiters'

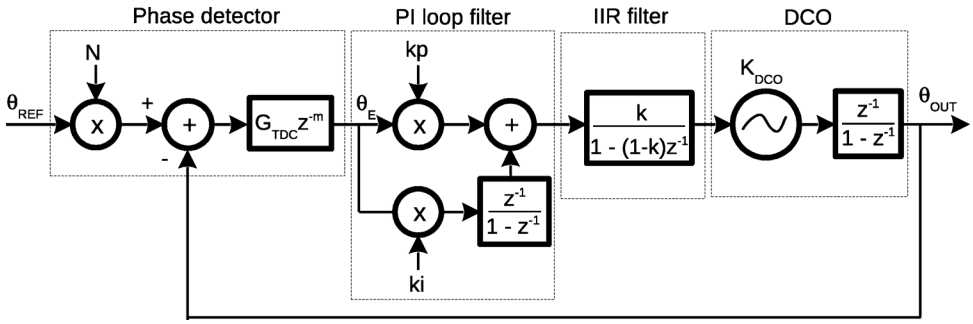

Fig. 10. DPLL model in discrete time. The DCO gain K_{DCO} is normalized to the DCO frequency. The phase detector gain G_{TDC} is unity for fractional mode and is inversely proportional to the input phase error during integer mode.

mismatches, 64 were used in this design. There is a tradeoff between the power consumption and the differential nonlinearity (DNL) of the stochastic TDC. Using a large number of latches improves the STDC resolution as well as the DNL. Recall also that STDC resolution can be adjusted by changing the reference signal slope S.

The power consumption of the proposed coarse–fine TDC is 4.4 mW from a 1.2-V supply voltage. This is quite low compared with other published fine-resolution TDC architectures. For example, the coarse–fine TDC based on a time amplifier in [16] consumes 70 mW and the GRO in [8] consumes 2.2–21 mW depending upon the phase error.

At the design stage, 2-ps fine TDC resolution was targeted, but, according to the measured in-band phase noise, the resolution appears to be 4 ps. This could be due to other noise sources within the DPLL such as reference and power supply noise, which were not modeled during design. Moreover, although nonlinearities in the coarse TDC are calibrated on-chip, the fine stochastic TDC may have nonlinearities resulting in 4-ps effective resolution.

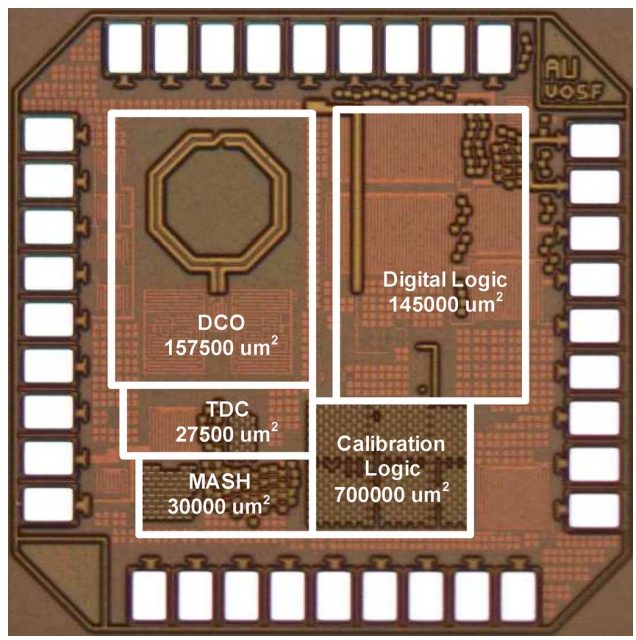

Fig. 11. Die photograph of the DPLL (active area is 0.43 mm^2).

III. TDC Calibration

To reap the full performance benefits of a fine-resolution TDC, it must have good linearity. In [23], the reference clock signal is recycled through a single delay cell to avoid the nonlinearity that arises from mismatch along a row of delay cells, and an auxiliary loop fixes the delay against PVT variations. More typically, however, calibration is used to avoid nonlinearity in a TDC.

In a two-step TDC, linearity of the coarse TDC is of prime importance since nonlinearities there will introduce more jitter than in the fine-resolution TDC. In this work, the delay of each stage in the coarse TDC varied from 28 to 38 ps over 200 Monte Carlo simulations of process and mismatch variations with a Gaussian-like distribution at an average of 33 ps and 1.89 ps standard deviation. Hence, calibration is needed to prevent the coarse TDC mismatch from limiting overall performance. Furthermore, calibration of the coarse TDC is crucial to ensure that the residual quantization error applied to the fine stochastic TDC is within its acceptable range.

To permit calibration, the coarse TDC comprises independently programmable delay stages. Each differential delay stage is comprised of CMOS inverters whose outputs are cross-coupled by two more inverters and loaded by a 4-b binary-weighted capacitor bank. The capacitor bank is implemented with differential MOS capacitors and provides a programmable delay that can be varied 15 ps, which is sufficient to cover delay variations due to process variations and mismatch.

In this work, a statistical calibration method is used to measure the coarse TDC nonlinearity. The time-varying difference between the DCO and reference clock phases is relied upon to perform a code-density test [24], as shown in Fig. 9. A similar statistical (there called "stochastic") method for measuring DNL is applied to a Vernier TDC in [12]. Unlike that work, however, here, each cell delay is individually adjusted according to the test results until uniform code density is observed.

Code-density testing generally needs a large number of clock cycles to achieve accuracy. Accordingly, a wide register would be needed to store the number of hits observed in each delay bin during calibration. In this work, a balanced mean rather than an absolute mean is used to store the accumulated number of hits in each delay bin during calibration [25]. Using a balanced mean, the size of the storage registers can be significantly reduced.

Assume a TDC consists of N delay elements and a register is used to store the number of hits for each delay element (bin).

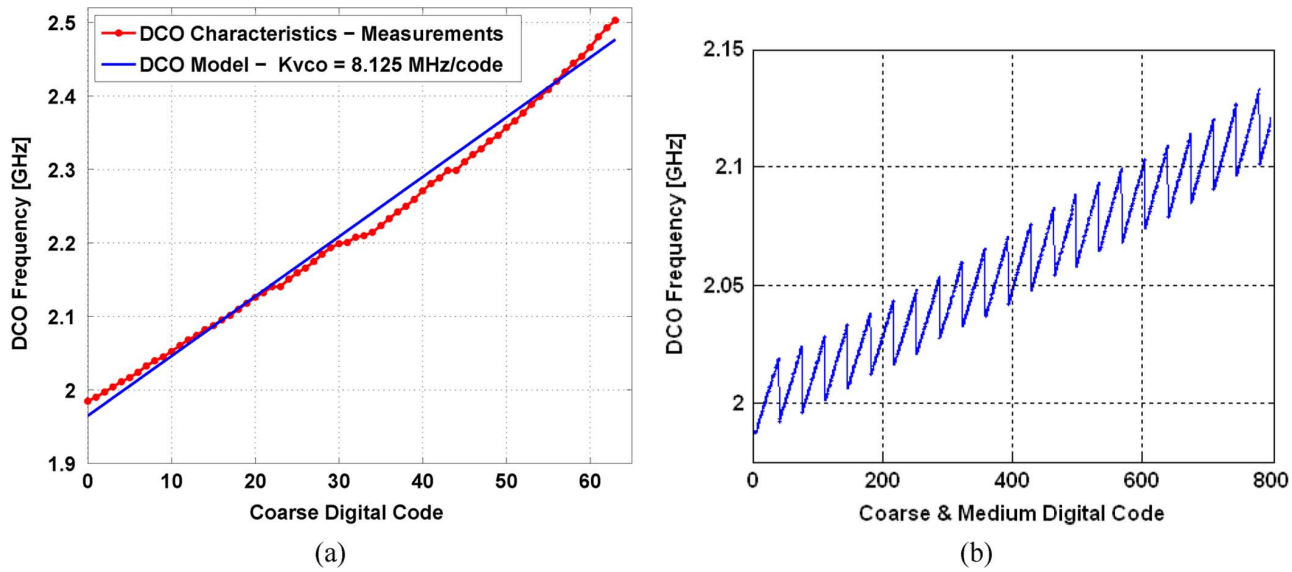

Fig. 12. DCO gain measurements (a) Coarse DCO gain = 8125 kHz/code (sweeping only the coarse DCO control word). (b) Medium DCO gain = 726 kHz/code (sweeping both the coarse and medium DCO control word).

Using a balanced mean, whenever a hit occurs for the ith bin, the controller increments the ith register by $(N-1)$ and decrements the other $(N-1)$ registers by one. Note that the mean value stored in all registers remains zero because [no. of hits $\times (N-1)$] + [no. of missing hits $\times (-1)$] $= 0$.

At the end of balanced mean calibration, registers store the DNL of each TDC bin. To achieve a DNL of 2% with 99% confidence, a 16-bit register is used for each coarse TDC bin rather than a 23-bit register which would be required without the use of the balanced mean method, saving 224 registers in total.

To ensure proper operation, a TDC with mismatched delay elements is modeled in VerilogAMS and the calibration algorithm is coded in Veriolg HDL. The simulation shows the effectiveness of the algorithm whenever the DNL is in the range -7 ps to $+8$ ps. Any nonlinearities outside this range will saturate the correction at the appropriate limits.

IV. Implementation of the DPLL

The DPLL has been realized using synthesized Verilog code for the loop filter, normalization algorithm, TDC calibration algorithm, a $\Delta\Sigma$ modulator (DSM), high-speed counter, and synchronization logic between the reference clock, output clock, and DSM. Other blocks such as a CML divide by two, the DCO, and TDC were custom designed.

A. Digital Loop Filter (DLF)

After calibration and digital normalization of the TDC output, the digital phase and frequency error is passed to the DLF. The DLF consists of a proportional path with gain k_p and a delaying integral path with gain k_i. Both k_p and k_i are programmable via a serial bus. The DLF is followed by an optional infinite impulse response (IIR) filter with a programmable gain k. The digital output of the DLF is applied directly to an array of varactors in the DCO to control the output frequency.

B. DCO

The DCO is an *LC*-oscillator with digitally controlled capacitors. The *LC* tank includes three capacitor banks: coarse, medium and fine. The coarse bank uses binary-weighted MIM capacitors in a common centroid layout. It has 6 b of resolution to cover the frequency range 1.99–2.5 GHz resulting in a resolution of approximately 8 MHz. The medium and fine capacitor banks are realized with MOS accumulation-mode varactors that digitally switch between low and high capacitance values. The medium capacitor bank is designed to have enough range to provide at least 50% overlap between adjacent coarse bank settings and ensure all frequencies are covered. Similarly, the fine capacitor banks provide more than enough range to cover adjacent medium capacitor bank settings, and are thermometer-coded to ensure monotonicity. Unit-sized accumulation-mode varactors provide a frequency resolution of 11 kHz. To achieve finer frequency resolution, the remaining capacitors in the fine bank are dithered.

The DCO introduces another source of quantization because it only changes its output frequency in discrete steps which introduces spurious tones at offset frequencies beyond the loop bandwidth. A DSM is used to shape the quantization noise of the DCO to high offset frequencies and achieve fine frequency control. The DSM is implemented with a MASH-1-1-1 architecture, with each succeeding stage having shrinking accuracy and area. The first stage of the DSM is the most important one, so 16-bit registers are used there. The second stage uses only 11-bit registers while the last stage uses only 6-bit registers. The DSM operates from the output clock divided by 8, hence in the range of 250–312 MHz.

The output clock of the DCO is divided by two using a CML static divider. The CML output is ac coupled before passing it through a pseudo-differential CMOS buffer. After that CML to CMOS stage, the half-rate clock is fed to a CMOS divider and a counter. Aside from the CML divide-by-2, all circuits are

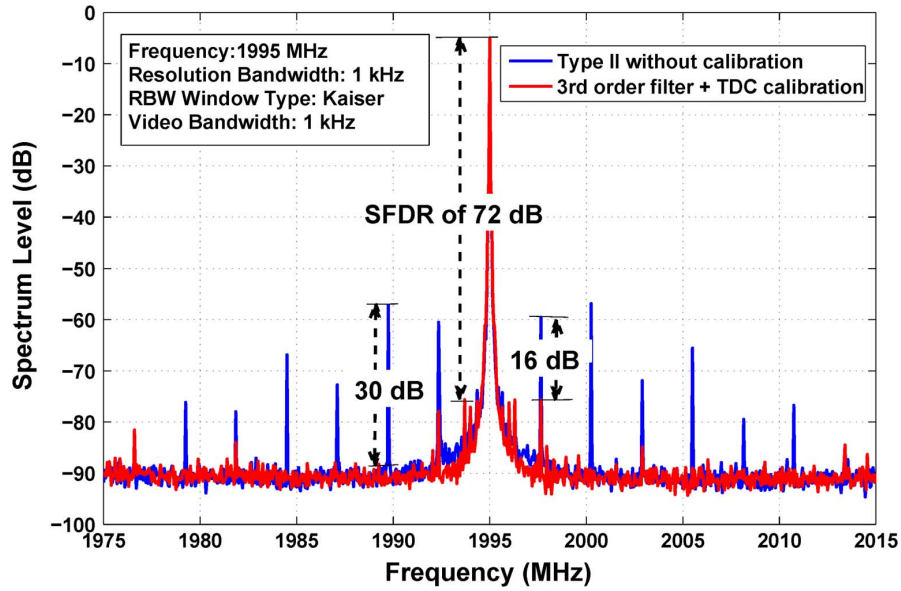

Fig. 13. Reduction of the spurs after TDC calibration with third-order loop filter (measured using Tektronix RSA 6114A real-time spectrum analyzer).

made from a standard cell library using standard digital synthesis tools.

C. DPLL Model

The DPLL can be represented by a discrete time model as shown in Fig. 10. Based on that model, the open loop transfer function is given by

$$H_{\rm ol}(z^{-1}) = \left(G_{\rm TDC}\cdot z^{-m}\right)\left(k_p + k_i\frac{z^{-1}}{1-z^{-1}}\right) \times \left(\frac{k}{1-(1-k)z^{-1}}\right)\left(K_{\rm DCO}\frac{z^{-1}}{1-z^{-1}}\right) \quad (4)$$

where T is the sampling reference period, and k_p, k_i, and k are the DLF coefficients. The gain of the TDC, $G_{\rm TDC}$, is equal to 1 during fractional mode but can be very big during integer-mode operation when the DPLL exhibits "bang-bang" behavior. The term z^{-m} represents extra delay within the DPLL and depends upon the details of the implementation of the particular TDC. It is worth noting that the DCO gain $K_{\rm DCO}$ is normalized to one DCO period. Hence, defining the average resolution of the DCO as Δf, $K_{\rm DCO} = \Delta f \cdot T_{\rm DCO} = (\Delta f)/(f_{\rm DCO})$.

Using a forward-rectangular discrete- to continuous-time conversion, the equivalent continuous-time model has an open-loop response

$$H_{\rm ol}(s) = G_{\rm TDC}(1-mTs)\left(k_p+\frac{k_i}{sT}\right)\left(\frac{1+sT}{1+sT/k}\right)\left(\frac{K_{\rm DCO}}{sT}\right). \quad (5)$$

If $k \approx 1$, then the IIR terms are approximately unity and can be omitted form the open-loop response equation (5). Also, assuming the TDC does not introduce significant extra delay within the loop, i.e., $m \approx 0$ resulting in

$$H_{\rm ol}(s) \approx G_{\rm TDC}\left(k_p+\frac{k_i}{sT}\right)\left(\frac{K_{\rm DCO}}{sT}\right). \quad (6)$$

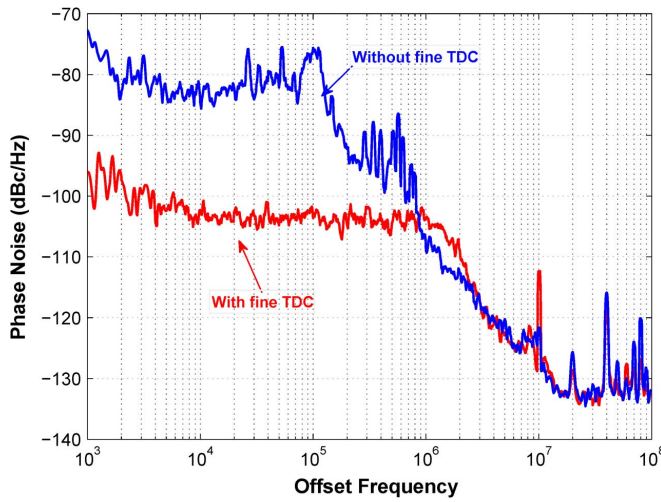

Fig. 14. Phase-noise measurement of 2 GHz clock using an HP8565C analyzer with and without a fine TDC. The reference clock is a 20-MHz temperature-controlled oscillator.

A second-order model can then be adopted for the closed-loop response

$$\begin{aligned} G(s) &= N\frac{H_{\rm ol}}{1+H_{\rm ol}} \\ &\approx N\frac{(k_pK_{\rm DCO}G_{\rm TDC}/T)s + (k_iK_{\rm DCO}G_{\rm TDC}/T^2)}{s^2+(k_pK_{\rm DCO}G_{\rm TDC}/T)s+(k_iK_{\rm DCO}G_{\rm TDC}/T^2)} \\ &= N\frac{2\zeta\omega_n s+\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} \end{aligned} \quad (7)$$

where

$$\omega_n = \frac{\sqrt{k_iK_{\rm DCO}G_{\rm TDC}}}{T} = \sqrt{\frac{k_iG_{\rm TDC}\Delta f}{T}} \quad (8)$$

$$\zeta = \frac{k_p}{2}\sqrt{\frac{K_{\rm DCO}G_{\rm TDC}}{k_i}} = \frac{k_p}{k_i}\frac{\omega_nT}{2}. \quad (9)$$

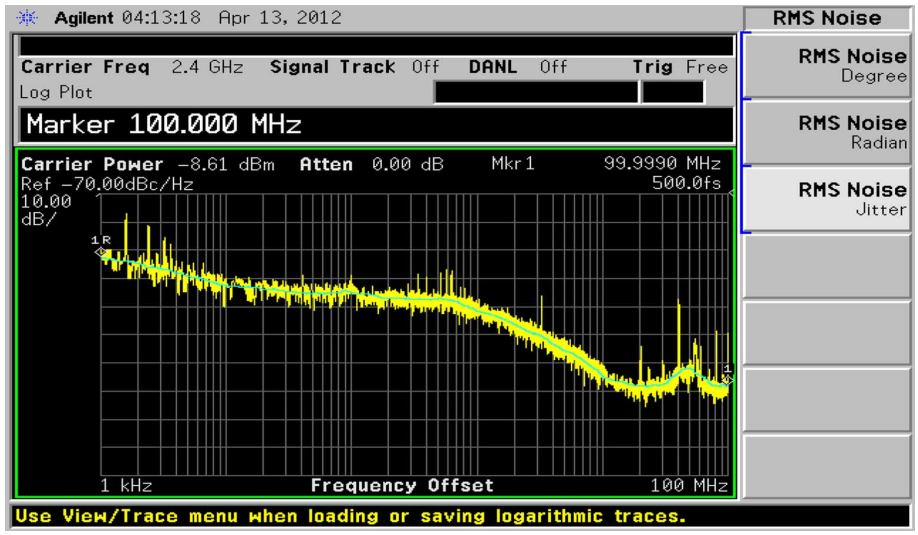

Fig. 15. DPLL output phase-noise spectrum at 2.4 GHz captured by an Agilent E4448A spectrum analyzer. The in-band noise is −107 dBc/Hz while the integrated jitter is 500 fs rms (0.43 degree) from 1 kHz to 100 MHz for a loop bandwidth of 1.42 MHz.

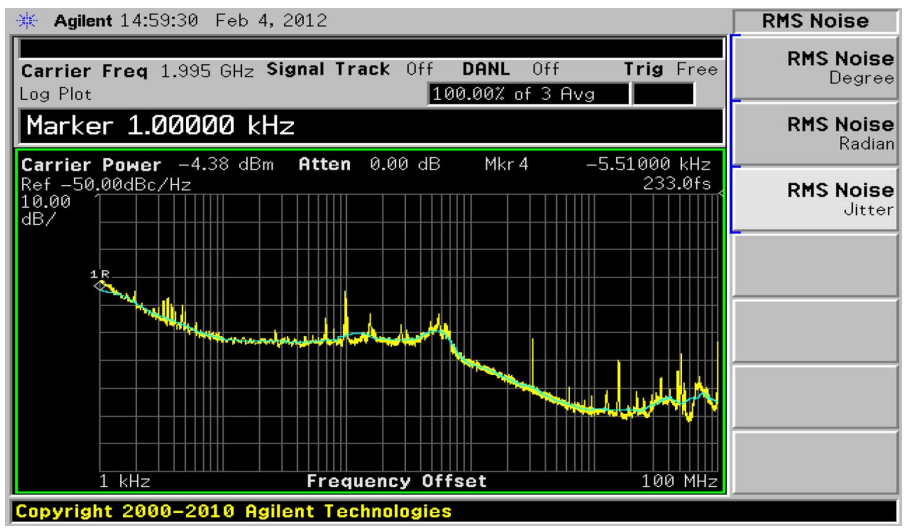

Fig. 16. DPLL output phase-noise spectrum at 1.995 GHz captured by an Agilent E4448A spectrum analyzer. The in-band noise is −104 dBc/Hz while the integrated jitter is 233 fs rms from 1 kHz to 100 MHz for a loop bandwidth of 700 kHz. A third-order loop filter was used.

Any DCO intrinsic phase noise will be high-pass filtered by $[1-G(s)]$ while any frequency noise due to the quantization and dithering process will be band-pass filtered by $[(2\pi)/(s)][1-G(s)]$. Furthermore, the DPLL behavior is mainly defined by the loop filter, DCO resolution, and reference frequency. The division ratio N does not affect the loop bandwidth.

Behavioral simulations were done in MATLAB to show the jitter contributed by various sources in the DPLL for a 2.4-GHz output frequency with 20-MHz reference. In all cases, dithering of the DCO LSB inputs contributed negligibly to the rms jitter. With a loop bandwidth of 700 kHz, DCO intrinsic noise contributes 179-fs rms jitter; improving TDC resolution from 40 to 4 ps reduces the TDC's jitter contribution from 3324 fs rms down to 232 fs, effecting a reduction in total output rms jitter from 3329 fs down to 295 fs. With a loop bandwidth of 1400 kHz, DCO intrinsic noise contributes 155 fs rms jitter while the jitter contributed by TDC quantization can be reduced from 5645 fs down to 394 fs rms by improving TDC resolution from 40 down to 4 ps resulting in a reduction in overall rms jitter from 5647 fs down to 424 fs rms. These results are consistent with those observed in measurement. Hence, the fine resolution offered by the STDC in this case plays a key role in achieving low DPLL output jitter.

V. Measurement Results

A prototype was fabricated in 0.13 μm CMOS technology from IBM and mounted on a FR-4 printed circuit board (PCB). The PCB has an Altera Cyclone IV FPGA to control the digital filter coefficients and division ratio via serial shift registers. A temperature-controlled 20 MHz reference clock with a phase noise of approximately −143 dBc/Hz from 10 kHz to 100 MHz was used.

The active area of the proposed DPLL is 0.43 mm^2, of which 0.07 mm^2 is the calibration algorithms. Also, the inductor coil occupies 20% of the active area. A die photograph of the fabricated prototype is shown in Fig. 11.

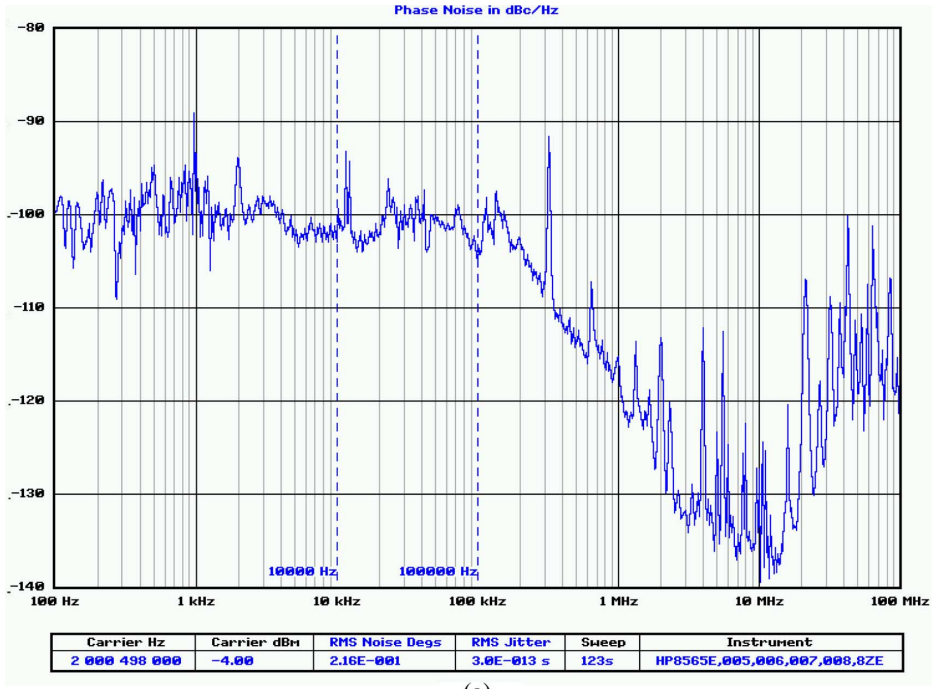

Fig. 17. Fractional synthesis measurements using HP8565C analyzer with (a) a 21-MHz input reference at channel $95+67/256$ and (b) a 20-MHz input reference at channel $109+64/256$ exhibiting less than 1-ppm frequency error.

Fig. 12 shows the open-loop test measurements using serially shifted DCO control words from the on-board FPGA. The coarse DCO bank gain $K_{\rm vco}$ is 8.125 MHz/code on average, the medium DCO bank gain is around 726 kHz/code on average, and the fine DCO bank gain is 11 kHz/code on average. The DPLL can lock to any frequency between 1.99–2.5 GHz from a nominal reference of 20 MHz.

The DCO output clock is buffered through a four-stage differential CML buffer that consumes 34 mW and captured by a Tektronix RSA 6114A real-time spectrum analyzer revealing a 370-mV peak-to-peak amplitude.

Fig. 13 shows spectrum measurements where spurs have been reduced from -54 to -70 dB at 2.65-MHz offset from the 1.995-GHz carrier by the calibration. Spurs at larger offsets were reduced by 30 dB thanks to the use of the third-order digital IIR loop filter.

Fig. 14 shows phase-noise measurements at a 2-GHz DPLL output frequency and 20-MHz reference clock, using

TABLE I
STATE-OF-THE-ART FINE-RESOLUTION TDC

Reference	Interpolative Line [17]	Cyclic Vernier [11]	Periodic Vernier [7]	Time Amp [16]	GRO [8]	2D Vernier [13]	This work
Number of bits	7	12	6	9	11	7	10
Effective resolution [ps]	4.7	8	12	1.25	6	4.8	4
INL [LSB]	2.4	N.A.	1.15	2	N.A.	3.3	N/A
DNL [LSB]	1.2	N.A.	1	0.8	N.A.	< 1	N/A
Bandwidth [MHz]	180	15	40	10	1	50	20
Area [mm^2]	0.02	0.26	0.04	0.06	0.04	0.08	0.028
Supply Voltage [V]	1.2	1.5	1.2	1	1.5	1.2	1.2
Power [mW]	3.6	7.5	2.5	70	2.2 - 21	1.7	4.4
Technology [nm]	90	130	120	90	130	65	130

TABLE II
COMPARISON AMONG PUBLISHED DIGITAL SYNTHESIZERS

Reference	[12]	[7]	[27]	[28]	[29]	[30]	[31]	[2]	[14]	This work
Technology [nm]	90	130	65	130	130	90	90	65	55	130
Reference frequency [MHz]	40(2x)	40	25	50	26	40	N/A	35	26	20
Carrier [GHz]	5-6	2	3	3.67	3.6	2.5	3.96	3.5	1.8	1.99-2.5
Bandwidth [MHz]	0.5	3	1.2	0.5	0.15	0.5	0.3	3	1	0.7-1.42
In-band Phase noise [dBc/Hz]	-94	-102	-100	-106	-95	-105	-96	-101	-108	-104 to -107
Normalized phase noise [dBc/Hz]	-211	-212	-216	-220	-212	-217	N/A	-216	-219	-217 to -222
In-band spurs [dBc]	-60	-42	-45	-42	-75	-75	-68	-58	-50	-72
Power [mW]	50	25	9.5	46.7	60	9.7	9.6	9	41.6	15.2
Active area [mm^2]	1.2	0.8	0.4	0.95	0.85	0.37	0.34	0.44	0.7	0.43

a HP8565C spectrum analyzer and KE5FX tool, with and without the fine TDC activated. The in-band noise is not less than -83 dBc/Hz when the fine STDC is disabled which is equivalent to approximately 40-ps TDC resolution, as expected. Once the fine TDC is enabled, the in-band phase noise drops to -104 dBc/Hz, which is equivalent to 4-ps resolution with only 3 mW of additional power consumption due to the fine STDC. The loop bandwidth is approximately 1.42 MHz while the integrated random jitter is 697 fs (0.502 degree). Also note that the results were consistent, even when operating in integer-synthesis modes, indicating that the achieved TDC resolution was sufficiently fine to avoid the undesirable nonlinear loop dynamics that can be associated with integer-synthesis.

A phase-noise measurement, using an Agilent E4448A spectrum analyzer, with the coarse TDC calibrated and fine TDC activated is shown in Fig. 15 for a 2.4-GHz output frequency. The in-band phase noise is -107 dBc/Hz while the jitter is 500 fs rms (0.432 degree) integrated from 1 kHz to 100 MHz for a loop bandwidth of 1.42 MHz. Furthermore, the phase noise is -116 dBc/Hz at 2-MHz offset and -137 dBc/Hz at 19-MHz offset. The random jitter reported by a 25-GS/s real-time oscilloscope was approximately 50% higher than from the phase noise analyzer, perhaps because some small fractional spurs are interpreted by the oscilloscope as random jitter.

For 2-GHz carrier, the jitter is 213 fs rms (0.153 degree) integrated from 1 kHz to 100 MHz for a loop bandwidth of 700 kHz. Once the loop bandwidth is extended to 1.42 MHz, the jitter becomes 697 fs rms (0.502 degree) integrated from 1 kHz to 100 MHz.

A phase-noise measurement with the coarse TDC calibrated, fine TDC activated, and third-order loop filter is shown in Fig. 16 for a 1.995-GHz output frequency. The in-band phase noise is -104 dBc/Hz while the jitter is 233 fs rms (0.167 degree) integrated from 1 kHz to 100 MHz.

Fractional operation was also confirmed at several other frequencies. For example, with a reference frequency $f_{\rm ref} = 21$ MHz at synthesized channel of $(95 + 67/256)f_{\rm ref} = 95.26171875 f_{\rm ref} = 2.000496094$ GHz, as shown in Fig. 17(a). Another example, with a reference frequency $f_{\rm ref} = 20$ MHz at synthesized channel of $(109 + 64/256)f_{\rm ref} = 109.25 f_{\rm ref} = 2.185$ GHz, as shown in Fig. 17(b). The results reveal less than 1 ppm frequency error. Moreover, with a reference frequency of 20 MHz and a loop bandwidth of 1.4 MHz, jitter was measured at 4 fractional channels between 120 and 121, all exhibiting random jitter within 20% of that observed at an integer channel of 120.

Table I summarizes state-of-the-art TDC architectures and performances, while Table II shows a comparison among

state-of-the-art published digital frequency synthesizers. For fair comparison of DPLLs with different reference and carrier frequencies, all phase noises are normalized using Banerjee's figure of merit (BFM) [26]. It is defined as $\mathrm{BFM} = \mathrm{PN} - 20 * \log(f_{\mathrm{carrier}}) + 10 * \log(f_R)$ where BFM is the normalized phase noise, PN is the measured phase noise, f_{carrier} is the output carrier frequency and f_R is the reference frequency. Note that the BFM does not take into account the dissipated power or the loop bandwidth. The presented coarse-fine DPLL consumes 15.2 mW at 2.4 GHz. The DCO and CML divide-by-two consume 7.8 mW, the coarse TDC consumes 1.4 mW, the fine TDC consumes 3 mW, and the remaining standard-cell digital logic consumes 3 mW.

VI. Conclusion

In summary, the performance of DPLLs is still in need of improvement, particularly with respect to spurs and phase-noise performance in wide-bandwidth applications. Specifically, TDC quantization noise and nonlinearity are major contributors to in-band phase noise and spurs, respectively. Improving TDC resolution (quantization step) from 40 to 4 ps can, ideally, improve in-band phase noise by 20 dB. However, achieving 4-ps resolution is not an easy task. Also, improving the linearity of the TDC reduces the folding of high-frequency phase noise to low-offset frequencies and reduces the spurious tone levels. Accordingly, efficient on-chip calibration algorithms are essential.

A DPLL with a novel calibrated coarse–fine TDC was presented that is suitable for modern wireless and wireline standards. The proposed DPLL achieves -104 to -107 dBc/Hz in-band phase noise, which is equivalent to 4-ps TDC resolution. The DPLL can lock to any frequency from 1.99 to 2.5 GHZ using a 20-MHz reference while the loop bandwidth is around 700 kHz to 1.42 MHz. The entire DPLL consumes 15.2 mW from a 1.2-V supply in IBM's 0.13-μm bulk CMOS technology. The integrated random jitter from 1 kHz to 100 MHz is 0.167 degree for a 1.995-GHz carrier with 700-kHz bandwidth, 0.153 degree for a 2-GHz carrier with 700-kHz bandwidth, 0.502 degree for a 2-GHz carrier with 1.42-MHz bandwidth, and 0.432 degree for a 2.4-GHz carrier with 1.42-MHz bandwidth.

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Amer Samarah (S'07) received the B.Sc. degree from An-Najah National University, Palestine, in 2002, and the M.A.Sc. degree from Concordia University, Montreal, QC, Canada, in 2006. He is currently working toward the Ph.D. degree in electrical engineering at the University of Toronto, Toronto, ON, Canada.

His research interests include digital phase-locked loops, clock recovery techniques, and analog design automation. From May 2010 to September 2010, he was with Broadcom Corporation as a Graduate Intern. Since August 2012, he has been an independent consultant to industry in the area of high-speed communication circuits.

Anthony Chan Carusone (S'96–M'02–SM'08) received the Ph.D. degree from the University of Toronto, Toronto, ON, Canada, in 2002.

Since 2001, he has been with the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada, where he is currently a Professor and the Associate Chair, Research. In 2008, he was a Visiting Researcher with the University of Pavia, Pavia, Italy, and later with the Circuits Research Laboratory, Intel Corporation, Hillsboro, OR, USA. He is a coauthor, with David Johns and Ken Martin, of the textbook *Analog Integrated Circuit Design* (Wiley, 2011, 2nd ed.). He is also an occasional consultant to industry in the areas of integrated circuit design, clocking, and digital communication.

Prof. Chan Carusone was a coauthor of the Best Student Papers at the 2007, 2008, and 2011 Custom Integrated Circuits Conferences, the Best Invited Paper at the 2010 Custom Integrated Circuits Conference, and the Best Paper at the 2005 Compound Semiconductor Integrated Circuits Symposium. He is an appointed member of the Administrative Committee of the IEEE Solid-State Circuits Society and the Circuits and Systems Society's Board of Governors. He has served on the technical program committee for the Custom Integrated Circuits Conference and International Solid-State Circuits Conference and is currently a member of the technical program committee for the VLSI Circuits Symposium. He has been a guest editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS and was on the editorial board of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS from 2006 until 2009 when he was Editor-in-Chief. He is currently an associate editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.