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Chip-level Power Integrity Methodology for High-Speed Serial Links

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Abstract:

A methodology for chip level power integrity analysis is presented. The approach accurately estimates the jitter induced on a victim block due to the current of an aggressor block through the power distribution network and linear voltage regulators. The analysis relies on simple stand-alone simulations of different blocks while the system-level analysis is completed by combining the results analytically. This procedure allows different designers to perform fewer and quicker simulations and as a result, there can be many iterations of the power integrity analysis to find the optimal solution. For example, the analysis can drive decisions regarding die capacitance partitioning and/or requirements for regulation on various circuit blocks.

Author Biographies:

Shayan Shahramian received his Ph.D. from the Department of Electrical and Computer Engineering at the University of Toronto, Canada, in 2016. His focus is on high-speed chip-to-chip communication for wireline applications. He is the recipient of the NSERC Industrial Postgraduate scholarship in collaboration with Semtech Corporation (Gennum Products). He is the recipient of the best young scientist paper award at ESSCIRC 2014 and received the Analog Devices outstanding designer award for 2014. He joined Huawei Canada in January 2016 and is currently working in system/circuit level design of high-efficiency transceivers for short reach applications.

Behzad Dehlaghi received the B.Sc. degree from University of Tehran, Tehran, Iran, in 2009, and the M.Sc. degree from University of Calgary, AB, Canada, in 2012, both in electrical engineering. He completed the Ph.D. degree in electronics at the University of Toronto, Toronto, ON, Canada in 2017. During his Ph.D. he worked on parallel ultra-short reach die-to-die links. Since January 2016 he has been working at Huawei Canada where he was involved in the system/circuit level design of energy-efficient high-speed transceivers. His research interests include on-chip measurement circuits and high-speed chip-to-chip communication.

Yue Yin received the B.AS. degree from Engineering Science in 2011, and the M.Sc. degree from Electrical Engineering in 2017 respectively, both from University of Toronto, Ontario, Canada. During her M.Sc. studies, she worked on power integrity analysis and LDO designs for single-ended transmitters and clocking circuits for high speed memory interface applications. Since 2017, she has been working as an IC design and verification engineer on high speed ADC products in Analog Devices Inc, Toronto, Ontario, Canada.

Rudy Beerkens received the B.Sc. degree in EE from the University of Waterloo in 1986. He has extensive experience in semiconductor technology, including silicon process development, reliability, circuit design and signal/power integrity. Since 2014 he has been working with Huawei Canada on high-speed SerDes development.

David Cassan received the M.A.Sc degree in Electrical Engineering from the University of Toronto in 2001. He is currently working at Huawei Canada where he is a Technical Director of the High-Speed Interfaces Research Team in Toronto, Canada. He has extensive experience in the area of wireline transceivers including analog design, system design, and SI/PI analysis.

Davide Tonietto received his Laurea Degree in 1995 from University of Pavia, Italy. Currently he is the Director of SerDes Development at Huawei Canada Research Center, Ottawa. He has more than 15 years of experience in signal integrity and high speed serial interface design and development. Previously he was Senior Manager of Signal Integrity IC development at Gennum Corporation, Manager of SerDes IP development at STMicroelectronics and lead designer of high speed serial interfaces, at Broadcom and other companies.

Anthony Chan Carusone received the Ph.D. from the University of Toronto in 2002 and has since been with the Department of Electrical and Computer Engineering at the University of Toronto where he is currently a Professor. He is also an occasional consultant to industry in the areas of integrated circuit design, clocking, and digital communication. Prof. Chan Carusone has co-authored over 90 conference and journal papers on integrated circuit design, including the Best Student Papers at the 2007, 2008 and 2011 Custom Integrated Circuits Conferences, the Best Invited Paper at the 2010 Custom Integrated Circuits Conference, the Best Paper at the 2005 Compound Semiconductor Integrated Circuits Symposium, and the Best Young Scientist Paper at the 2014 European Solid-State Circuits Conference. He authored, along with David Johns and Ken Martin, the 2nd edition of the classic textbook Analog Integrated Circuit Design. He was Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS in 2009, and has served on the technical program committee for the Custom Integrated Circuits Conference and the VLSI Circuits Symposium. He currently serves on the editorial board of the IEEE JOURNAL OF SOLIDSTATE CIRCUITS, as a member of the Technical Program Committee of the International Solid-State Circuits Conference, and as a Distinguished Lecturer for the IEEE Solid-State Circuits Society.

I. Introduction:

Power integrity and distribution are an essential part of any successful IC development. Power integrity analysis investigates the effect of the supply current consumption of different circuits along the power distribution network (PDN) on the system performance. In high-speed link design, the severity of power supply induced jitter needs to be analyzed for sensitive circuits to determine the overall link margin. Ideally, a transient simulation of the entire chip along with the PDN network is performed to give the most accurate results on the overall system performance compared to measurement results, however, the simulation time makes this prohibitive. Therefore, the problem needs to be simplified into smaller, and more manageable simulations. The problem is complicated by the fact that sensitive circuits in modern transceivers are often isolated from the global PDN by voltage regulators.

A methodology for chip level power integrity analysis is presented in section III. The approach accurately estimates the jitter induced on a victim block due to the current of an aggressor block through the power distribution network and linear voltage regulators. The analysis relies on simple stand-alone simulations of the various circuit blocks while the system-level analysis is completed by combining the results analytically. This procedure allows different designers to perform fewer and quicker simulations and as a result, there can be many iterations of the power integrity analysis to find the optimal solution. For example, the analysis can drive decisions regarding die decoupling capacitance partitioning and/or requirements for regulation on various circuit blocks. A list of required simulations and sample results are provided in section III.A.

The proposed method consists of steps to find the jitter induced on a victim block due to supply noise. The supply noise on the victim block can be broken down into two segments: the supply noise induced by an aggressor block, and the self-induced supply noise. Section III.B will cover the analytical procedure to calculate the total PSIJ at the output of a victim block.

Section IV.A includes a set of simulations results showing the accuracy of the proposed methodology vs. transistor level simulation of the regulators and the PDN with currents mimicking the aggressor and victim blocks. Section IV.B demonstrates the power integrity design methodology applied to clock distribution (victims) and transmitters (aggressors).

II. Background:

Methods for PSIJ analysis and simulation may be broadly categorized as either time domain or frequency domain.

A. Time Domain Methods

A straightforward approach to estimating power supply induced jitter (PSIJ) is to employ transient simulations. For example, transceiver netlists can be simulated with

(pseudo)random patterns of data capturing both the transient noisy supply voltage waveforms and the resulting impact upon clock and data jitter. Various circuit blocks can be selectively (de)activated to identify the predominant underlying sources of noise. Such approaches may result in lengthy simulations and may not afford the same insights as frequency-domain methods. Time-domain simulations are used in [1] to determine the supply voltage noise induced on a given PDN (although frequency-domain approaches are then used to find the resulting PSIJ). With a pseudo random bit sequence (PRBS) feeding all transmitter pins at 4.8Gbps, a peak to peak supply noise of 81mV is reported. When the PRBS input pattern is replaced with a clock pattern at the PDN resonance frequency (60MHz), 116mV peak to peak supply noise is reported.

Analytical models of PSIJ have been developed based upon transient analysis of small-signal models [2], [3] resulting in faster simulation time than full transient simulation. They are used to provide statistical information, such as the rms jitter of clocking circuits based upon knowledge of the power supply noise variance. However, those analyses are not readily generalized to the wide variety of circuits in a complex modern transceiver, and may not consider the spectrum of the power supply noise and hence of the resulting jitter.

B. Frequency Domain Methods

A frequency domain approach to predict and measure PSIJ for high speed I/O interfaces is introduced in [4], then extended and applied in [5], [6], [7]. Supply voltage noise spectra are obtained and multiplied by the frequency-dependent supply sensitivity of signal-path circuits to find PSIJ spectra. Two methods for simulating the jitter sensitivity are presented. The conventional way is by transient simulation: noise is introduced at a specific frequency by superimposing a small-amplitude sinusoid onto the supply voltage and the resulting jitter at that frequency is obtained. Sweeping the frequency in this manner provides the circuit's jitter sensitivity as a function of frequency. Another method is to use period-steady-state (PSS) and periodic AC (PAC) simulation, where PSS computes the periodic steady-state response of a circuit and PAC linearizes the circuit over its PSS response.

The impact of a voltage regulator was considered briefly in [8]. However modern systems employ multiple supply domains isolated from each other by independent voltage regulators that share a common global power supply. In such situations, the crosstalk between supply domains and the circuits operating under them is of great interest. A modeling methodology that allows for the rapid estimation of supply-induced jitter in this environment allows for optimal supply partitioning, decoupling capacitor allocation, and voltage regulator specification in the early stages of a design. Therefore, we here present methodologies that extend prior frequency-domain approaches to allow for rapid modeling and simulation of power-supply noise on high-speed signal integrity in environments where multiple voltage regulators are used to isolate transmitter, receiver, and clocking circuits.

III. Simulation Methodology:

The overall block diagram of the scenario being analyzed is shown in Figure 1. The goal is to find the PSIJ on the output of the victim block. This PSIJ has two separate sources which can be analyzed separately. Part of the jitter is caused by the aggressor block and includes the current that is drawn from the PDN by regulator 1 and transferred to the victim block through regulator 2 as shown in Figure 1a. The second portion of the jitter on the victim block is caused by the current drawn by the victim block from regulator 2 (the self-induced jitter) as shown in Figure 1b. This methodology can be used both to characterize the system performance as well as help guide the design of the regulators and the PDN. Decisions such as how to distribute a fixed amount of decoupling capacitance between different regulators can be made using this system level PI analysis as discussed in section IV.

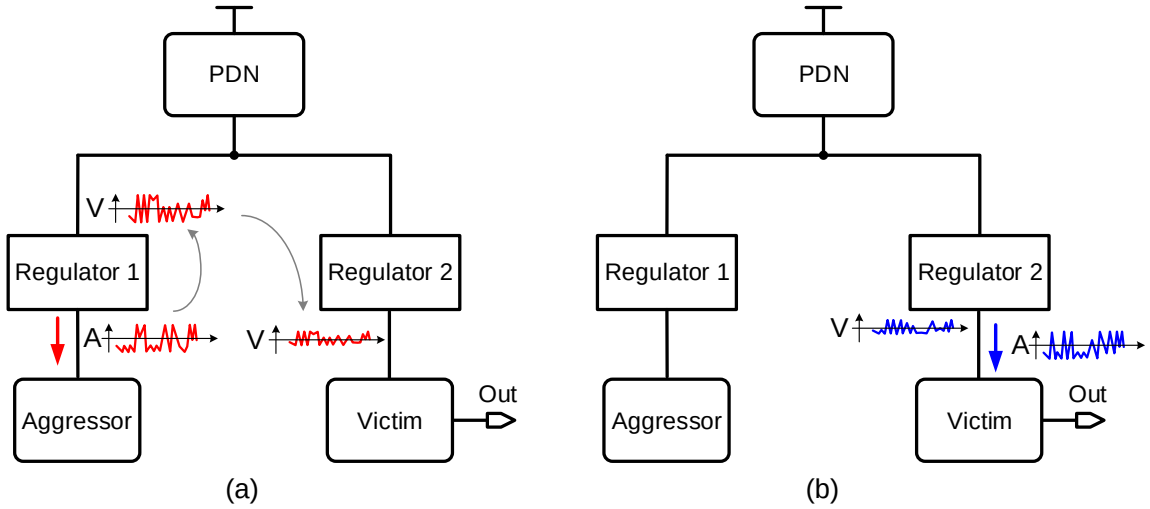

Figure 1: (a) Noise from aggressor shows up at the PDN and subsequently at the victim block supply. (b) The current consumption of the victim causes some self-induced PSIJ.

The power integrity simulation methodology consists of two main steps. Firstly, individual simulations are performed on the different blocks. These simulations include gathering current profiles, regulator parameters, PDN models, and jitter sensitivities which are outlined in section IIIA. Secondly, the simulation results are combined analytically in the frequency domain to obtain the jitter impact on the victim blocks. The self-induced jitter from the victim block is considered as well as the jitter induced from the aggressor blocks. The calculations are described in section IIIB.

A. Individual Block Simulations:

One of the main benefits of this simulation methodology is that it requires only independent simulations of the different blocks shown in Figure 1. Ideally, it is best to limit the number of long transient simulations that are required to perform the power integrity analysis. Reducing the number of components and simulating each block individually helps perform the power integrity analysis quickly. Furthermore, this creates a modular analysis

environment, where different blocks can easily be switched in and out to compare multiple scenarios.

Step 1 involves simulating the aggressor and victim block current with an ideal supply as shown in Figure 2a. This is a simulation that would be done by the circuit designer and would simulate the current under typical operating conditions. A sample current waveform is shown in Figure 2b.

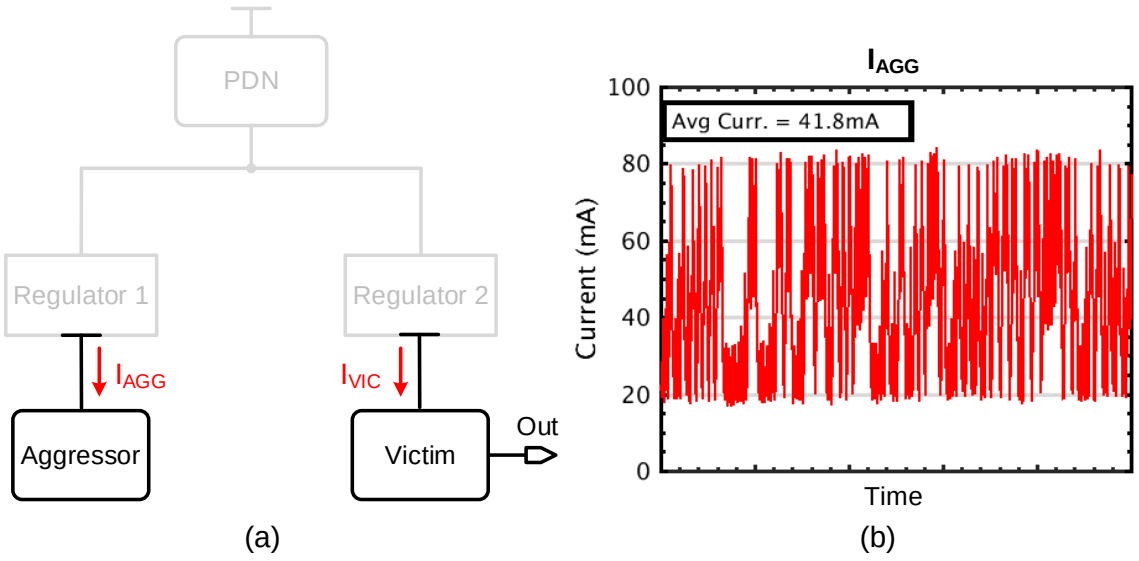

Figure 2: Step 1 - Simulate Aggressor & Victim Block Current

Step 2 requires simulating the regulator current isolation transfer function $H_{REG1}(s)$ as shown in Figure 3a. The regulator is biased using the average value of the aggressor current I_{AGG}. An AC current source, I_T, is placed under the regulator to simulate the current isolation:

$$\boldsymbol{H_{REG1}(s) = \frac{I_{REG1}(s)}{I_T(s)}} \qquad \textbf{(1)}$$

This transfer function will capture how much of the current of the aggressor block is drawn from the PDN vs the amount that is provided by the decoupling cap C_{DEC}. The goal of the current isolation is to determine how much of the aggressor block current shows up at the PDN and causes noise on other circuits. For blocks that are problematic noise sources, the regulator can be specifically designed for enhanced current isolation. An exemplar current isolation response is shown in Figure 3b for different amounts of C_{DEC} under the regulator.

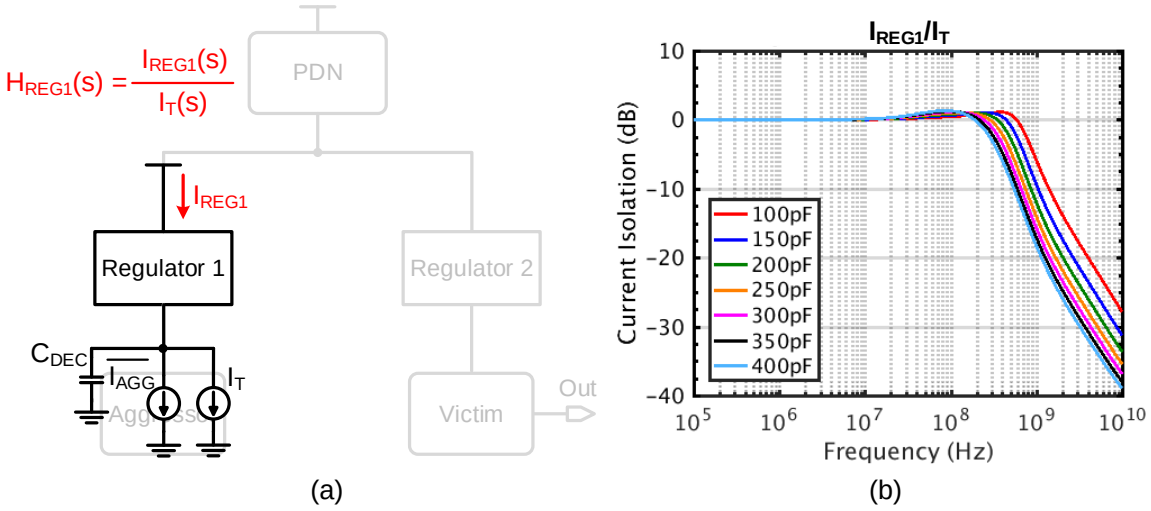

Figure 3: (a) Step 2 - Simulate Regulator 1 Current Isolation. (b) Example results for various values of C_{DEC}.

Step 3 involves simulating the regulator impedance seen from the power supply as shown in Figure 4a. This impedance will then be placed in parallel with the PDN impedance and leads to more accurate results. The impedances need to be simulated for all the regulators that are connected to the same PDN network. In Figure 4a, there are two regulators connected and they both need to be simulated to obtain Z_{VCC1} & Z_{VCC2}. Figure 4b shows a sampled Z_{VCC} for different values of C_{DEC} on the regulator.

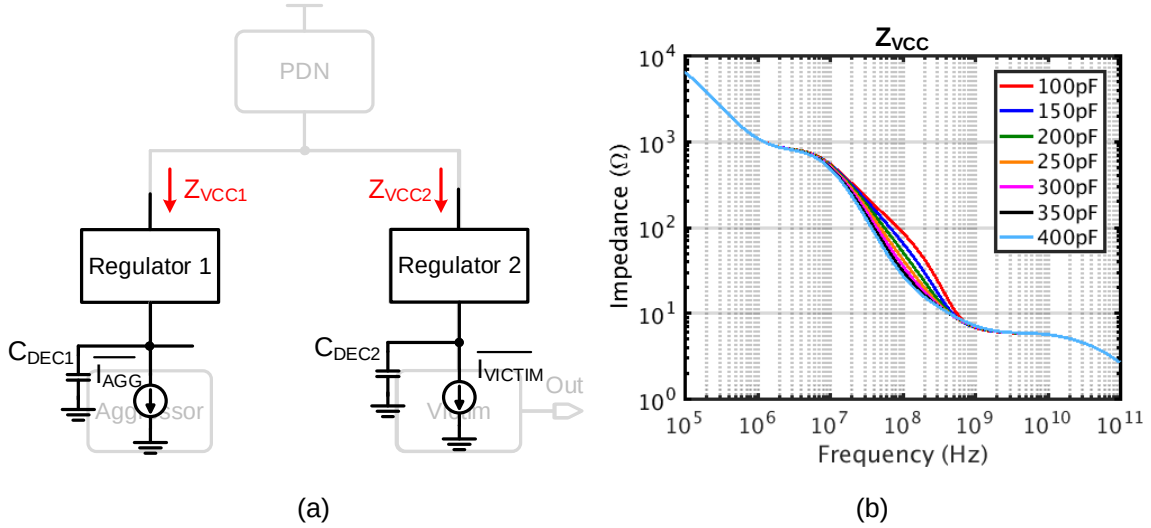

Figure 4: (a) Step 3 - Simulate the regulator impedance seen from the supply. (b) $Z_{VCC1,2}$ for various values of C_{DEC1}=C_{DEC2}.

Step 4 requires simulating the PDN impedance seen by the regulators as shown in Figure 5a. The PDN can be modeled by a lumped element model consisting of the on-chip decoupling capacitance as well as the package model including any on-package decoupling

capacitance and via/bump/ball inductance/capacitance. It is well-established that PDNs are typically subject to resonance at several 100's MHz (e.g. [9]). Any current around the PDN peak frequency needs to be carefully considered since it can be a large contributor to the overall PSIJ. A sample PDN impedance vs frequency is shown in Figure 5b.

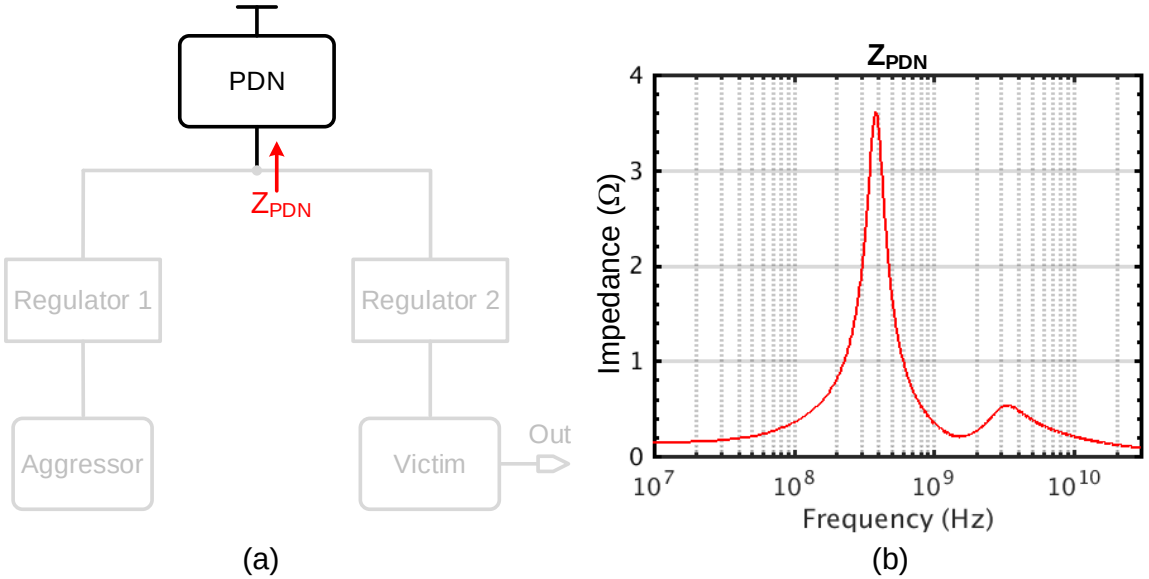

Figure 5: (a) Step 4 - Simulate the PDN impedance at the point where the regulators are connected. (b) Example PDN network Impedance

Step 5 involves simulating the impedance of the victim regulator as seen by the victim block, Z_{LOAD2}, as shown in Figure 6a. The impedance is simulated with an ideal supply for the regulator and does not include the PDN. The peak frequency of Z_{LOAD} is also important as it determines which frequencies of the current from the victim block cause the largest self-induced PSIJ. A few different regulator load impedances are shown in Figure 6b for different decoupling capacitors C_{DEC2} under the regulator.

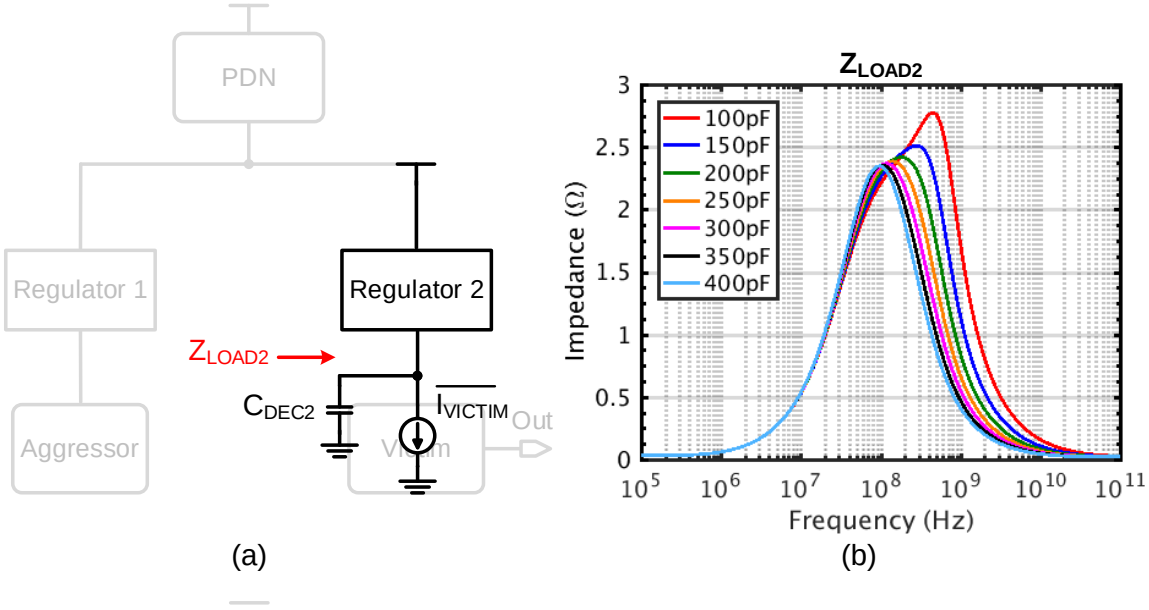

Figure 6: (a) Step 5 - Simulate the victim regulator impedance seen by the load. (b) Z_{LOAD2} for various values of C_{DEC2}.

Step 6 requires a simulation for the victim block regulator, the power supply rejection ratio (PSRR) shown in Figure 7a. The PSRR is used to determine how much of the supply noise present on the PDN shows up at the supply of the victim block. Depending on the sensitivity of the block, the PSRR can be optimized to isolate at frequencies where there is more noise on the PDN. Figure 7b shows the PSRR of a regulator with different amounts of decoupling capacitance.

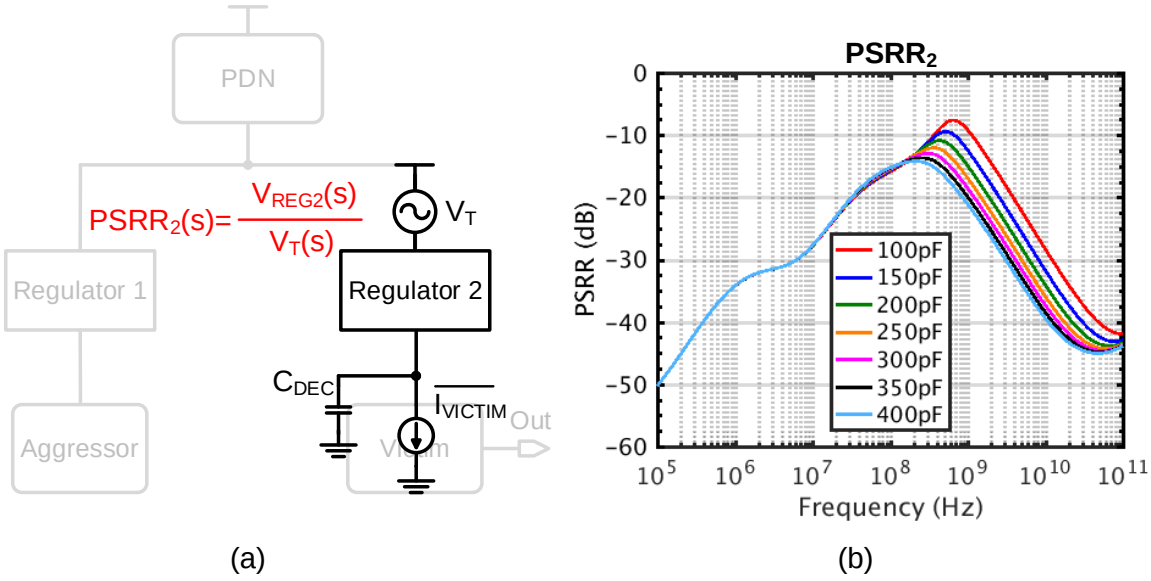

Figure 7: (a) Step 6 – Simulating the regulator PSRR. (b) Example PSRR results shown for various values of C_{DEC}.

The final step in gathering the required data for the PI analysis is the jitter sensitivity of the victim block, JS(s). To obtain the jitter sensitivity, several transient simulations are performed on the victim block. A sinusoidal noise is applied with a fixed amplitude at the supply of the block and the jitter at the output is measured. The output jitter is divided by the supply noise amplitude to obtain the jitter sensitivity at each frequency in fs/mV. The frequency of the supply noise is varied to obtain a plot similar to Figure 8b.

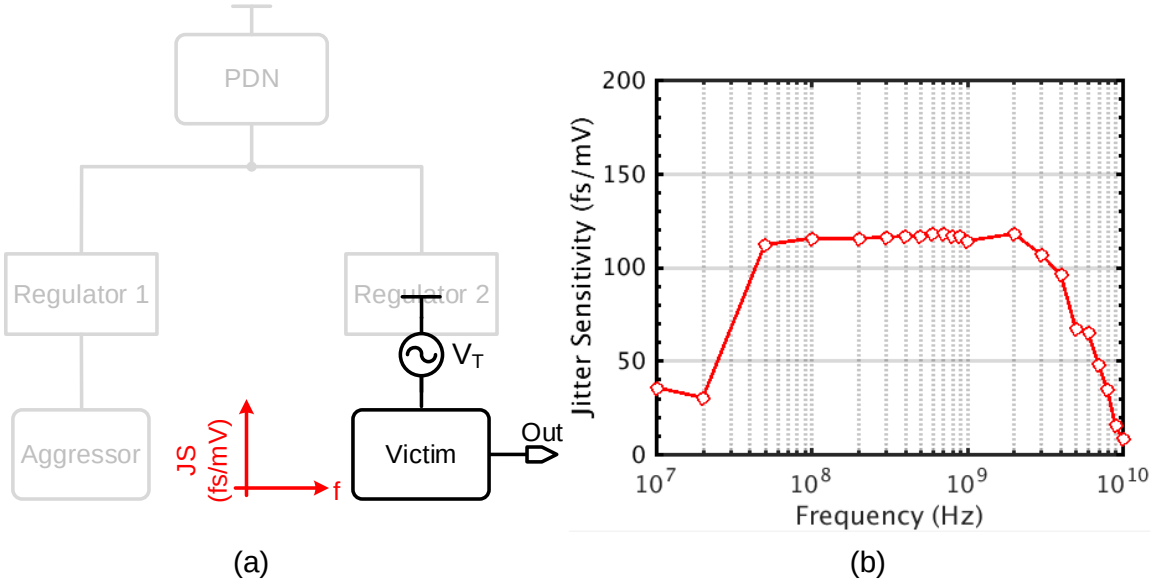

Figure 8: (a) Step 7 - Simulating the jitter sensitivity of the victim block. (b) Example jitter sensitivity simulation result

B. Analytical Power Integrity Analysis:

After gathering all the results obtained in section IIIA, they can now be combined to determine the PSIJ at the output of the victim block. The PSIJ is divided into two components as described in section III and can be written as:

$$\boldsymbol{Jitter_{OUT}(s) = Jitter_{AGG}(s) + Jitter_{SELF}(s)} \qquad \textbf{(2)}$$

To calculate the jitter due to the aggressor, the current drawn by the aggressor from the PDN needs to be calculated by multiplying the aggressor current by the regulator current isolation:

$$\boldsymbol{I_{PDN,AGG}(s) = I_{AGG}(s) \times H_{REG1}(s)} \qquad \textbf{(3)}$$

The impedance at the PDN needs to be calculated to find the voltage noise at the PDN caused by all the blocks. The impedances at this node is the impedance looking into the PDN, $Z_{PDN}(s)$, and the two regulator impedances looking in from the supply, Z_{VCC1} & Z_{VCC2}. The impedances are placed in parallel to obtain the total impedance at the point where the regulators connect to the PDN:

$$\boldsymbol{Z_{VCC,TOT}(s) = Z_{PDN}(s) \parallel Z_{VCC1}(s) \parallel Z_{VCC2}(s)} \qquad \textbf{(4)}$$

The voltage noise at the PDN can now be calculated by multiplying equation (3) by (4).

$$\boldsymbol{V_{PDN}(s) = I_{PDN,AGG}(s) \times Z_{VCC,TOT}(s)} \quad \textbf{(5)}$$

The supply noise at the victim block supply due to the noise on the PDN can now be calculated by multiplying (5) by $PSRR_2(s)$:

$$\boldsymbol{PSN_{AGG}(s) = V_{PDN}(s) \times PSRR_2(s)} \quad \textbf{(6)}$$

The jitter on the victim caused by the aggressor can then be written as the product of the supply noise at the victim caused by the aggressor, $PSN_{AGG}(s)$, and the jitter sensitivity of the victim block.

$$\boldsymbol{Jitter_{AGG}(s) = VCC_{AGG}(s) \times JS_{VIC}(s)} \quad \textbf{(7)}$$

The self-induced supply noise on the victim can be calculated by multiplying the current of the victim block by the regulator impedance:

$$\boldsymbol{PSN_{SELF}(s) = I_{VIC}(s) \times Z_{LOAD2}(s)} \quad \textbf{(8)}$$

The self-induced PSIJ of the victim block can be calculated by multiplying the supply noise by the jitter sensitivity:

$$\boldsymbol{Jitter_{SELF}(s) = PSN_{SELF}(s) \times JS_{VIC}(s)} \quad \textbf{(9)}$$

Finally, the complete jitter at the output of the victim block can be calculated by adding the outputs of equation (7) & (9) as shown in equation (2). In this paper the phase relationship between the victim and aggressor blocks is assumed to be random, for more accurate results, the phase relationship can be determined using SPICE simulations.

IV. Simulations Results: Case Study

Section IV.A will show the accuracy of the model compared with SPICE simulations when connecting two regulators to the PDN with different currents to mimic victims and aggressors. Section IV.B will show a case study and will show how the complete model can be used to predict the jitter at the output of various blocks and to help guide regulator design decisions.

A. SPICE vs. Model Correlation

Figure 9 shows the scenario being used to illustrate the accuracy of the power integrity model. Two different current sources are used to mimic the aggressor and the victim blocks. The aggressor has a time varying current with large and sudden changes arising from a PRBS pattern. The victim block draws only DC current and therefore does not cause any noise on other blocks. These currents are shown in Figure 9.

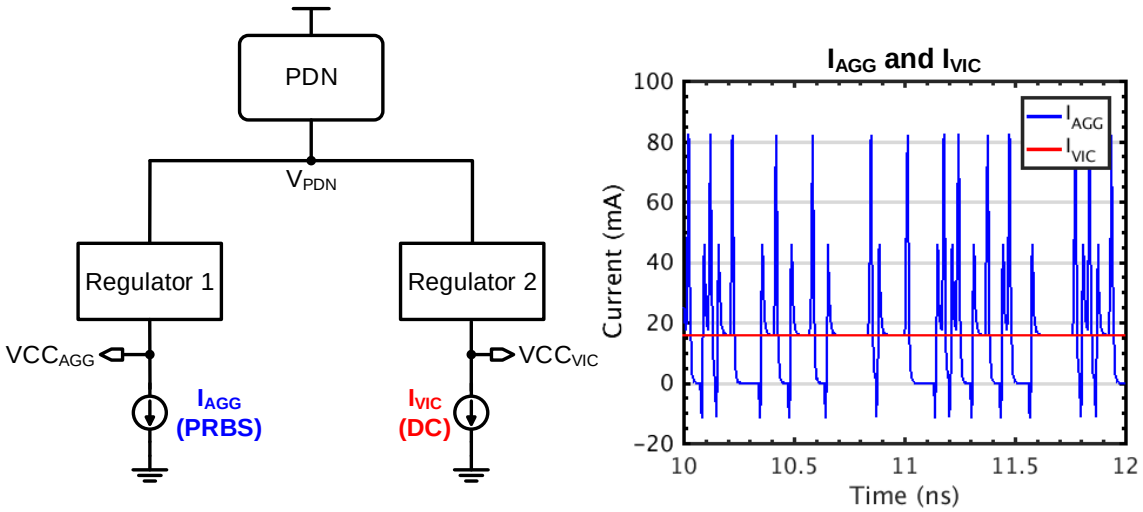

Figure 9: Simulation setup with currents mimicking aggressor and victim circuits

Figure 10 shows the current being drawn from V_{PDN} from regulator 1. In the model, I_{REG1} is calculated by multiplying the I_{AGG} current by the regulator current isolation transfer function as described in equation (1). I_{REG1} is plotted vs time by taking the inverse Fourier transform of the calculated signal:

$$\boldsymbol{I_{REG1}(t) = \mathcal{F}^{-1}\{I_{AGG}(j\omega) \times H_{REG1}(j\omega)\}} \qquad \textbf{(10)}$$

It is evident that the current isolation transfer function can be used to accurately calculate the IREG1 and have a very good correlation with SPICE level simulations as shown in Figure 10.

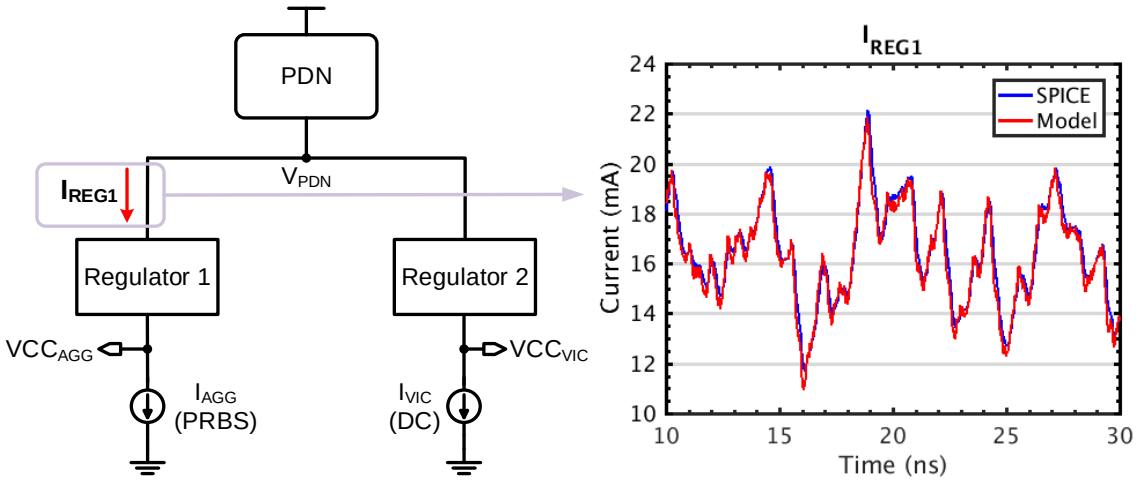

Figure 10: Comparison of SPICE vs. Model for I_{REG1}

The next step is to ensure the voltage on the PDN (V_{PDN}) can accurately be calculated using the model. Figure 11 shows the impedances required to calculate the equivalent resistance

seen at the V_{PDN} node. Using the impedances and the I_{REG1} calculated in the previous step, the voltage at the PDN can be determined:

$$\boldsymbol{V_{PDN}(t) = \mathcal{F}^{-1}\{I_{REG1}(j\omega) \times (Z_{PDN}(j\omega) \parallel Z_{VCC1}(j\omega) \parallel Z_{VCC2}(j\omega))\}} \quad \textbf{(11)}$$

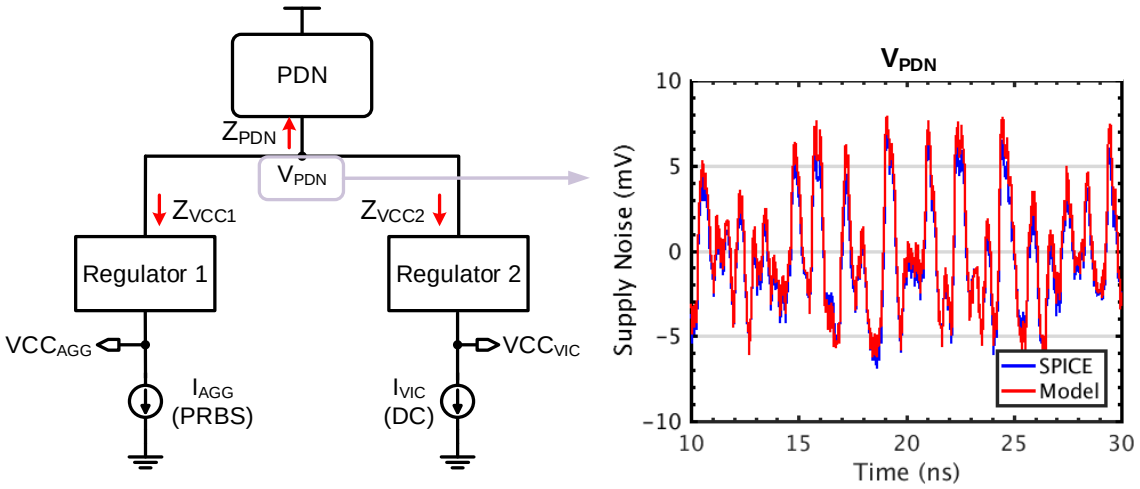

Figure 11: SPICE vs. Model comparison for voltage at PDN, V_{PDN}

The next step is to see if VCC_{VIC} at the victim block can be accurately captured using the model as shown in Figure 12. By using the value determined in equation (11), the victim supply VCC_{VIC} is calculated by multiplying the V_{PDN} by the PSRR of the 2nd regulator.

$$\boldsymbol{VCC_{VIC}(t) = \mathcal{F}^{-1}\{V_{PDN}(j\omega) \times PSRR_2(j\omega)\}} \quad \textbf{(12)}$$

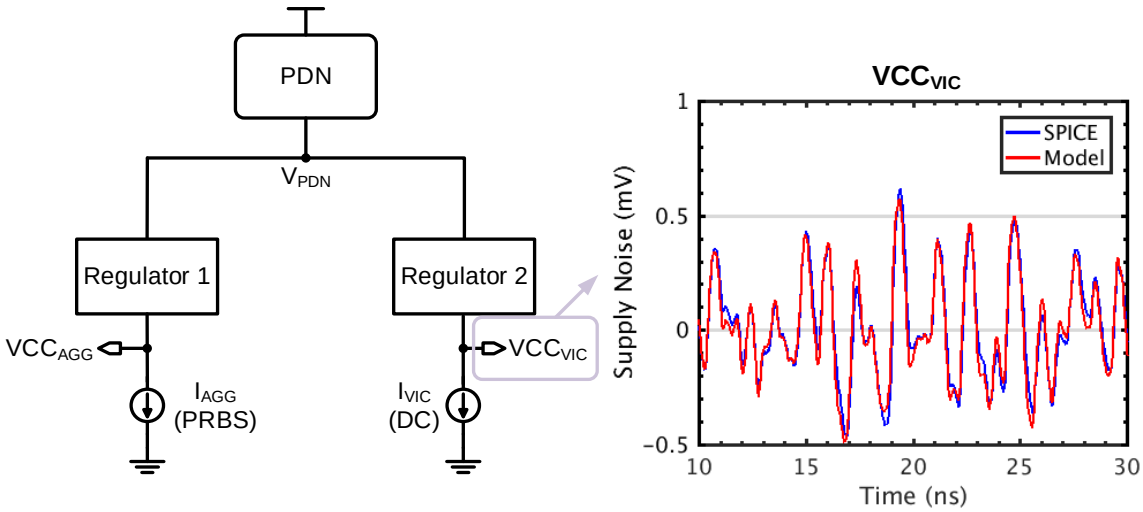

Figure 12: Spice vs. Model comparison for calculating supply noise at victim block

Finally, the VCC of the aggressor block due to the self-induced noise is calculated. Figure 13 shows the self-included noise on the aggressor (VCC_{AGG}). The self-induced supply noise is calculated by multiplying the regulator load impedance by the aggressor current:

$$\boldsymbol{VCC_{AGG}(t) = \mathcal{F}^{-1}\{I_{AGG}(j\omega) \times Z_{LOAD1}(j\omega)\}} \qquad \textbf{(13)}$$

It is important to note that if other blocks were present that could contribute to the supply voltage noise, their effect would also need to be added using superposition.

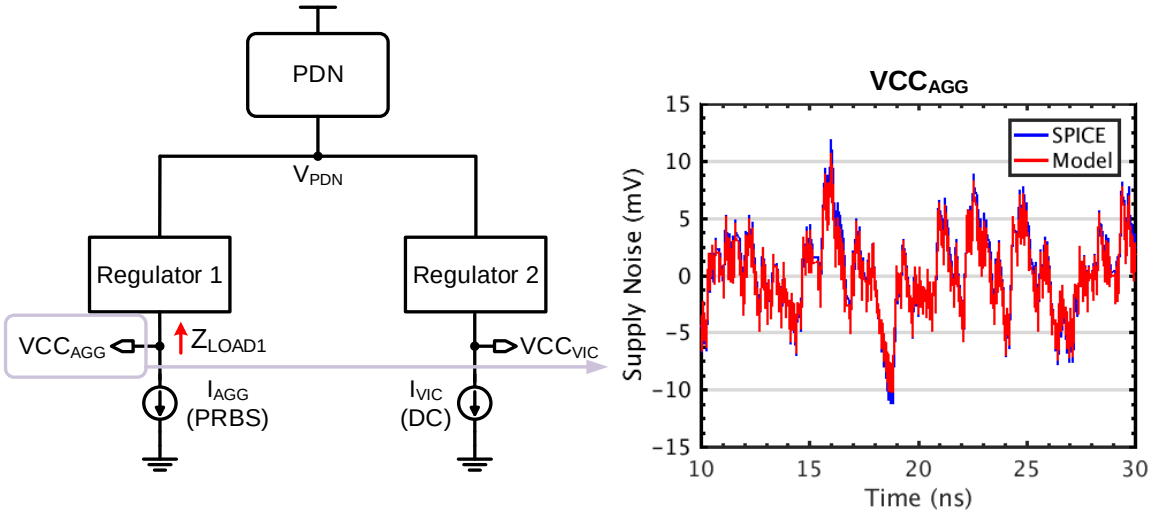

Figure 13: SPICE vs. Model comparison for calculating the self-induced noise at the aggressor block

Overall, there is a good correlation between the SPICE simulations and the model analytical results. This demonstrates that the current isolation and the PSRR can be used to capture transient currents and voltages at different points of the regulators.

B. Case Study – Transmitter and Clocking

In this section, the PSIJ of two common types of circuits will be analyzed. Figure 14a shows a block diagram of the case study: clock distribution circuitry is placed under a regulator while a transmitter (TX) is placed under a second regulator. The analysis outlined in the previous sections is applied to determine the jitter at the output of these blocks. The jitter will be broken down into self-induced jitter and the jitter caused by the other block. Finally, the power integrity analysis methodology is used to determine how best to distribute a fixed amount of decoupling capacitance between the two regulators. Figure 14b shows the current consumption of the TX and clock distribution; from the waveforms it is evident that the transmitter will be the dominant source of PSIJ due to both the larger average current value and rapid variations in the amount of current drawn from the supply.

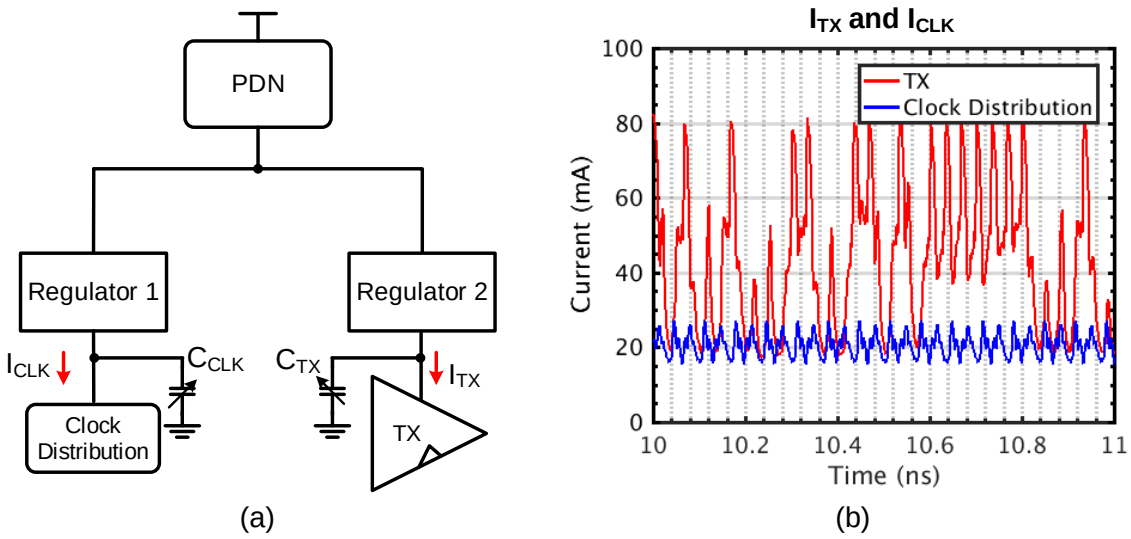

Figure 14: (a) Block diagram of the scenario being considered to find the impact of clock distribution and transmitter on each other (b) Current consumption of the transmitter and clock distribution

Figure 15 shows the PSIJ on the transmitter and the clock distribution circuits under different operating conditions. The results are based on the fact that there is area for 500pF of total decoupling capacitance and that has been equally shared by the clock distribution circuits and the transmitter circuits, C_{CLK}=C_{TX}=250pF. Looking at the TX jitter, it is evident that regardless of whether the clocking circuitry is ON/OFF, the same amount of jitter is present at the output of the transmitter. This arises from the fact that the TX jitter is mainly self-induced and the clocking circuitry does not cause a lot of jitter on the transmitter. Another observation is that there is a large difference in the jitter at the output of the clock distribution depending on whether the transmitter is ON/OFF. This again lines up with our assumption that the transmitter is a major source of jitter for other blocks.

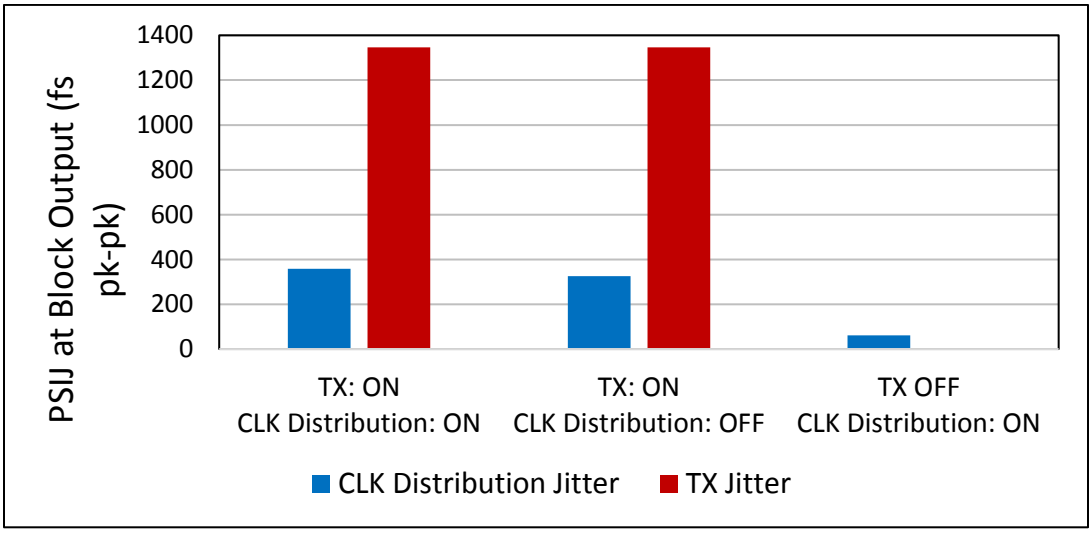

Figure 15: PSIJ on TX & Clock Distribution with different circuits powered ON/OFF

In Figure 15 the PSIJ is reported for the case where the total decoupling capacitance of 500pF was split equally between the clock distribution and the transmitter. The proposed power integrity analysis can also be used to determine how best to allocate the decoupling capacitance in a fast and efficient way. Figure 16 shows the PSIJ as a function of the regulator capacitance of C_{TX} and C_{CLK}. The main requirement is that $C_{TX}+C_{CLK}=500pF$, while keeping both $C_{TX}\geq100pF$ & $C_{CLK}\geq100pF$ to maintain a minimum level of regulator performance. In the analysis, there are also two operating conditions considered for the transmitter. In the first scenario, the transmitter is operating with a PRBS input pattern and there are no consecutive identical digits (CIDs) present. In the second scenario, the transmitter has a PRBS input pattern with intermittent CID patterns of 100 zeros. The CID patterns create low frequency content in the current spectrum close to the where the PSRR and Z_{Load} of the regulators peak. As a result, the CID patterns will stress the power distribution and cause additional jitter on the blocks. This is evident in Figure 16 whenever the transmitter has CID patterns, it leads to higher jitter for both the clock distribution and the transmitter. Based on the analysis, we can see that for the clock distribution, the optimal capacitance value would be $C_{CLK}=C_{TX}=250pF$ which leads to the lowest jitter, however, this is not the case for the transmitter. When looking at the transmitter, it is apparent that the larger the capacitor C_{TX}, the better the jitter performance. Depending on which block is more critical in overall link margin, the decision can be made regarding the decoupling capacitance allocation. Assuming both blocks are equally important, the optimal solution would be to use the maximum decoupling capacitance in the TX ($C_{TX}=400pF$) and to put $C_{CLK}=100pF$. This leads to a small increase on the clock distribution jitter relative to the optimal point but a large decrease in the jitter on the transmitter and hence the overall jitter would be lower.

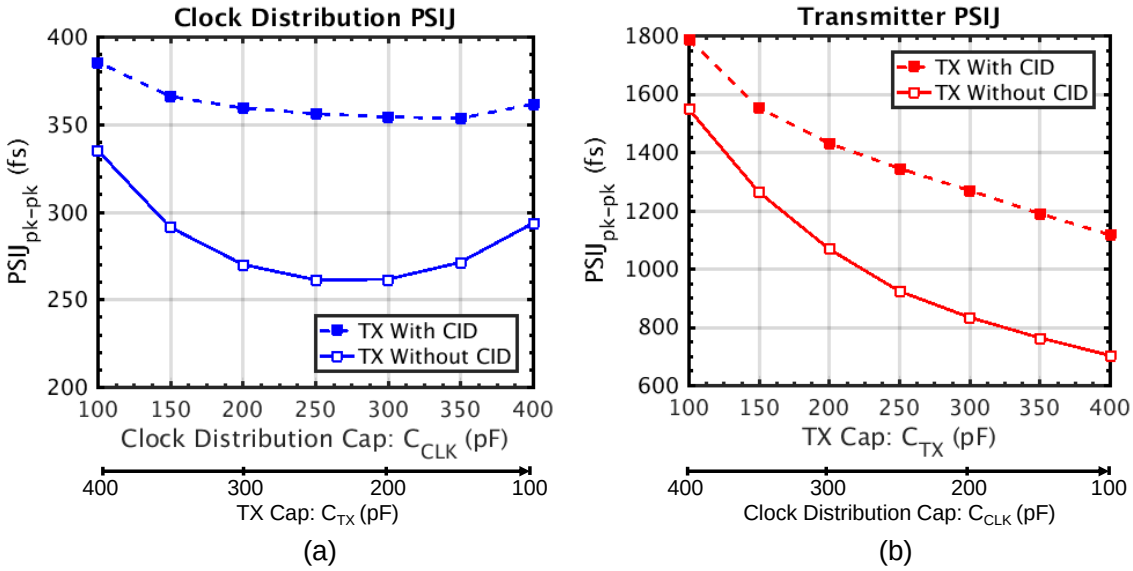

Figure 16: PSIJ with various decoupling capacitor values on (a) the clock distribution and (b) the transmitter.

V. Conclusion

A methodology for chip level power integrity was presented. The approach allows the output PSIJ of a block to be accurately calculated. The PSIJ is broken down into two components, a self-induced component caused by the current consumption of the block under study and a jitter caused by the current consumption of nearby circuits. The approach captures the interaction of the blocks through the regulators and the PDN. The different steps required to perform the analysis were outlined. The simulations required are kept as independent as possible to allow for quick iterations and comparisons. Finally, a sample case study was presented for PI analysis of clocking and transmitter circuits.

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