A 40-Gbps 0.5-pJ/bit VCSEL Driver in 28nm CMOS with Complex Zero Equalizer

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***Abstract*—This paper presents a tunable equalizer to compensate for the under-damped response of VCSELs. The equalizer transfer function has a pair of tunable complex zeros to cancel the complex conjugate poles in the VCSEL's electrical-optical transfer function enabling faster operation at lower VCSEL bias. A prototype was fabricated in 28nm CMOS technology. Utilizing the equalizer the prototype achieved 40Gbps operation with 0.5pJ/b power efficiency and 1.3dBm OMA.**

I. Introduction

In the past decade there has been a trend toward increasing use of optical links within data centers and high performance computing. The majority of these links are less than 300-m long where vertical cavity surface emitting lasers (VCSELs) are widely used due to their low cost. However, to reach the 30+ Gbps speed requirement of emerging and future protocols it is necessary to electrically equalize for VCSEL intrinsic bandwidth limitations.

Although non-linear, if linearized about a bias point, a VCSELs electro-optical response can be modeled by a second-order transfer function with natural frequency of ω_v and damping factor of ξ_v given by,

$$H_v(s) = \frac{K\omega_v^2}{s^2 + 2\xi_v\omega_v s + \omega_v^2} \quad (1)$$

with ξ_v proportional to the VCSELs bias current minus its threshold current and ω_v^2 proportional to the square of the bias current minus the threshold current [1]. A low damping factor in the transfer function causes ringing in the pulse response and severely degrades the eye opening at high bit-rates. This is shown in Fig. 1 where a PRBS7 pattern is applied to the transfer function (1) with $\xi_v = 0.45$. It can be seen that the ringing causes excessive overshoot and eye-closure especially for $f_{bit} > 2 \cdot \omega_v/(2\pi)$, where f_{bit} is the data rate.

Hence, the VCSEL response varies significantly with bias current. At high bias current, a critically or over-damped response is obtained. Hence, many works operate at relatively high bias currents to obviate the need for equalization up to about 20Gb/s in modern VCSELs. However, this approach results in higher power consumption. Moreover, since maximum optical output power is limited by eye safety and/or VCSEL thermal constraints, higher bias current also leads to lower extinction ratio (ER) and optical modulation amplitude (OMA). In [3], [4], and [5] the VCSEL bias is increased for a critically or over damped transfer function. Then a conventional FFE is used to extend the speed of the link. Though 25G, 40G, and 71Gbps operations were demonstrated, at 4pJ/b, 13.2pJ/b, and 13.4pJ/b, the power efficiencies remain poor due to the power hungry delay cells and the high bias current of the VCSEL.

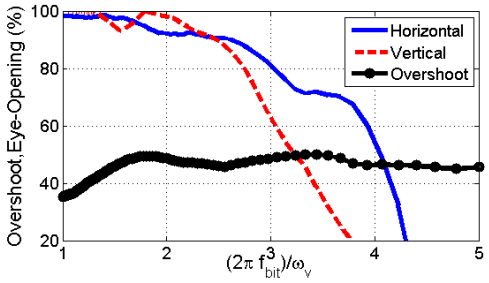

Fig. 1: Eye closure penalty and overshoot due to ringing in VCSEL's electro-optical transfer function response at high bit rates

Several other works employ pre-emphasis tailored to compensate for ringing in the VCSEL response. In [2] an asymmetrical feedforward equalizer (FFE) is utilized to apply different pre-emphasis for high current and low current for a symmetric output and to compensate for ringing due to low damping factor of the VCSEL. This approach achieved a good power efficiency of 0.77-pJ/b however the speed remains limited to 20Gbps by the low VCSEL bandwidth at low bias. In [7] a double-pulse asymmetric equalizer is proposed. The equalizer injects two pulses in each signal transition. The first one equalizes for the bandwidth limitation due to parasitics. The second pulse reduces the ringing due to the VCSEL electro-optical response. The amplitude of the pulses can be adjusted independently for the rising/ falling edges to account for the VCSEL's bias-dependent transfer function. Fabricated in 90nm CMOS the prototype reached 17Gbps operation with a 9GHz bandwidth VCSEL with 8.8pJ/b power efficiency. In [8] a 2-tap capacitively coupled pre-emphasis is used to compensate for VCSEL ringing at high extinction ratio. The transmitter reaches 2.3dBm OMA at 9dB extinction ratio with 2pJ/b power efficiency at 15Gbps.

Operation up to 40-Gbps has also been demonstrated [6] using an interesting group-delay compensation however the power efficiency remains at 7.8-pJ/b due to the large number of BiCMOS amplifier stages.

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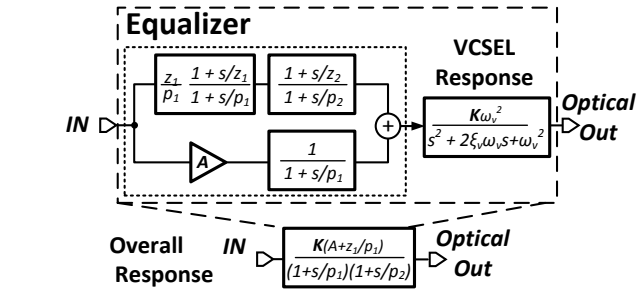
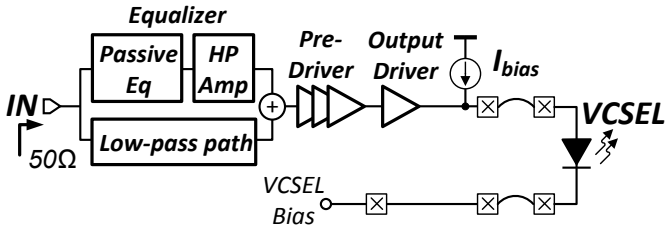


(a)



(b)

Fig. 2: (a) Proposed equalization technique (b) Block diagram of the transmitter

This work proposes an equalizer with tunable complex zeros to cancel out the effect of the complex conjugate poles in VCSEL response and to thereby reach 40-Gbps operation. The lower required bias current of the VCSEL in combination with the low-power transmitter circuit allows for a record low power consumption of 0.5-pJ/bit at 40Gbps.

II. Equalizer

To compensate for the ringing of the complex conjugate poles in (1) an equalizer with a transfer function consisting of a pair of complex conjugate zeros is used. As shown in Fig. 2 the equalizer transfer function is synthesized by adding a high-pass transfer function with two real poles (p_1 and p_2) and two real zeros (z_1 and z_2) to a low-pass transfer function with low frequency gain of A and a pole at p_1. The overall transfer function of this equalizer is given by,

$$H_e(s) = \frac{A + z_1/p_1}{(1 + s/p_1)(1 + s/p_2)} \cdot \frac{s^2 + 2\xi\omega_n s + \omega_n^2}{\omega_n^2} \quad (2)$$

$$\omega_n^2 = z_1 z_2 + A p_1 z_2 \quad (3)$$

$$2\xi\omega_n = z_1 + z_2 + A z_2 p_1/p_2 \quad (4)$$

To compensate for the VCSEL transfer function in (1) the parameters in (2) need to be chosen such that $\xi = \xi_v$ and $\omega_n = \omega_v$. In this case the overall transfer function becomes,

$$H(s) = H_v(s)H_e(s) = \frac{K(A + z_1/p_1)}{(1 + s/p_1)(1 + s/p_2)} \quad (5)$$

After cancellation of the VCSEL's complex conjugate poles with the equalizer's complex conjugate zeros, the overall transfer function will have two real poles at p_1 and p_2. To equalize different VCSELs at different bias currents both the natural frequency of the equalizer (ω_n) and its damping factor (ξ) have to be tunable. As shown in Fig. 3, ω_n can be set by changing z_2. Once ω_n is set, ξ can be adjusted by changing the gain of the low-pass path (A).

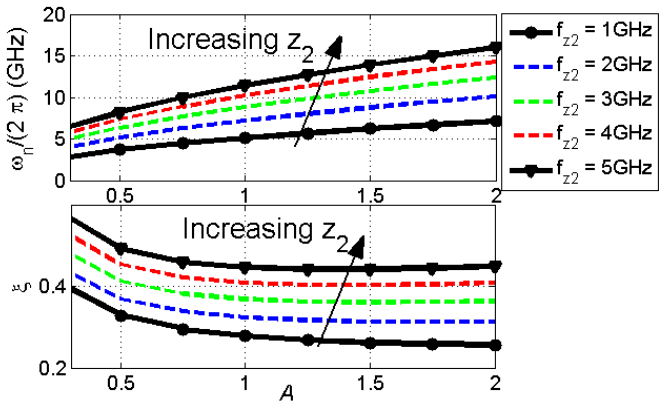


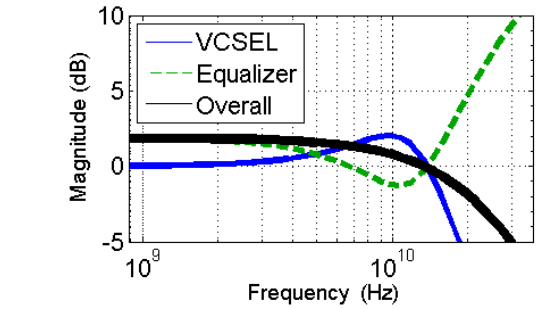
Fig. 3: Tuning ω_n and ξ of the equalizer by changing z_2 and A. ($f_{z2} = z_2/(2\pi)$.)

The effect of the equalizer on the transient eye can be seen in Fig. 4. The model used in these simulations is based on [9] and fit to a commercial 20Gbps VCSEL. The model uses rate equations and includes the self heating of the VCSEL.

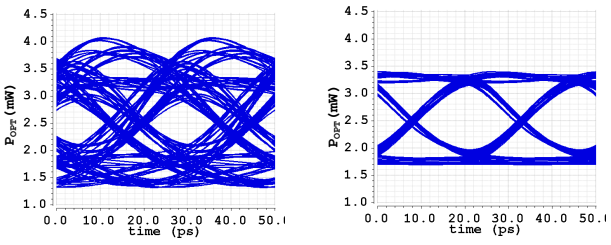
In Fig. 4a shows that the VCSEL has an underdamped frequency response. Applying the equalizer to this response results in a flat frequency response. The transient effect of the equalizer can be seen where a 40Gbps PRBS7 pattern is applied to the VCSEL. Fig. 4b shows the eye-diagram without the equalizer. It can be seen that the VCSEL's ringing causes excessive jitter and reduces the vertical eye-opening. In Fig. 4c the equalizer is added to remove the ringing and opening the eye-diagram.

III. Circuit Implementation

The circuit implementation of the equalizer is shown in Figure 5. The high-pass branch is realized by a cascade of a tunable passive equalizer and a source degenerated continuous-time linear equalizer. It can be shown that p_1 and p_2 are the high frequency poles of the passive equalizer and the source degenerated equalizer (HP Amp). The low-pass branch consists of two differential pairs. Both differential pairs have resistive source degeneration to improve the linearity of the low-pass branch. A pair of digitally tunable capacitors is used to fine tune the pole of the low-pass branch to the same frequency as pole of the passive equalizer (p_1). The outputs of the high-pass and low-pass branches are added in a current summer node with inductive peaking. To provide 3-mA of modulation current the output of the equalizer goes through a pre-driver consisting of three differential pairs with inductive peaking and the output stage, shown in Figure 6. The VCSEL is connected in a common-cathode configuration with a negative anode bias voltage. To reduce the supply noise due to the single-ended load of the driver, an on-chip capacitor



(a)



(b) (c)

Fig. 4: (a)Equalizing a VCSEL with ω_v=2π12GHz and ξ_v= 0.45 with the complex zero equalizer (p_1=2π·25GHz, p_2=2π·30GHz, z_1=2π·1GHz, z_2=2π·3GHz, A = 2). Simulated 40Gbps optical eye using a 20Gbps VCSEL model. I_0=5mA, I_1=9mA, (b) without equalizer (c) with equalizer and ξ=0.45, ω_n=2π.12GHz.

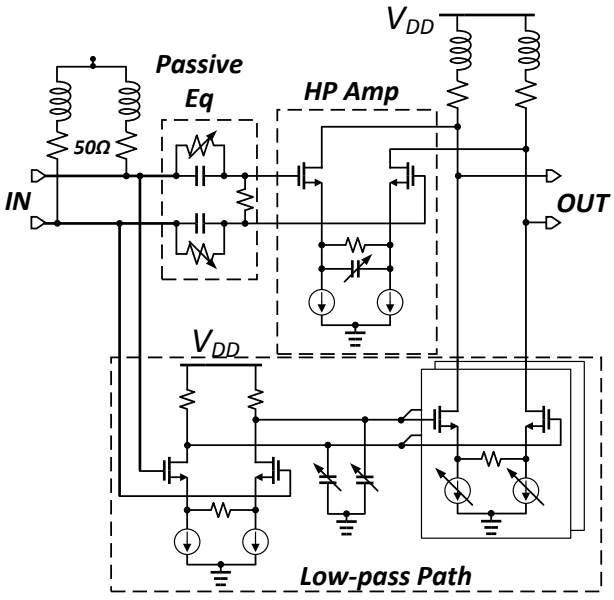


Fig. 5: Circuit implementation of the equalizer

decouples the VCSELs negative bias voltage to the supply of the output stage.

The fully CMOS implementation of the driver with 1V supply voltages facilitates integration with networking ASICs. Note that the negative voltage is only connected to the VCSEL

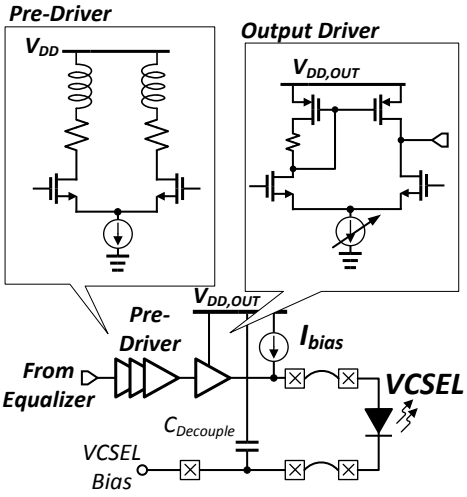


Fig. 6: Output stage and VCSEL connection

and does not cause reliability concerns for the transistors. Also the anode-driving structure of the driver makes it compatible with most commercially available VCSEL arrays where the shared substrate is the n-type cathodes.

IV. Measurement Results

A prototype was fabricated in TSMC 28nm CMOS technology. The equalizer and the pre-driver/output stage occupy 120μm×75μm and 120μm×200μm respectively. The CMOS chip and the VCSEL array were then placed in a QFN package and wirebonded together. The die photo of the assembly is shown in Fig.7. The VCSEL has a 1060nm wavelength with forward bias voltage of 1.6V and f_{3dB}=19GHz at 3.5mA bias. The high speed input was applied to the transmitter using electrical probes, and the VCSEL optical output was collected using a lensed fiber. The O/E oscilloscope module used to capture the light has a 35GHz bandwidth. In the following measurements mild averaging is used in the oscilloscope to reduce the high frequency noise of the O/E module and better highlight the effect of the equalizer on the VCSEL transient response. All circuits are connected to 1V supply and the negative supply (-1.1V for VCSEL bias of 3.5mA and -0.9V for VCSEL bias of 1.7mA) is only used to bias the VCSEL's common-cathode.

The effect of the equalizer can be seen in Fig. 8 where the VCSEL has been biased at very low bias current of 1.7mA and driven with an extinction ratio of 4.5dBm. A 30Gbps PRBS7 pattern is applied to the transmitter. Under these conditions the VCSEL response shows significant ringing which results in excessive jitter and overshoot and closes the eye diagram. The equalizer can open the eye by reducing the ringing.

Fig. 9a shows the optical output of the driver with the high-pass branch disabled. In this case the path through the equalizer only consists of real poles and no complex zeros (f_{3dB} >30GHz). In Fig. 9b the equalizeer is enabled by enabling the high-pass path. It can be seen that the peak-to-peak jitter reduces by a factor of two from 23ps to 11.3ps.

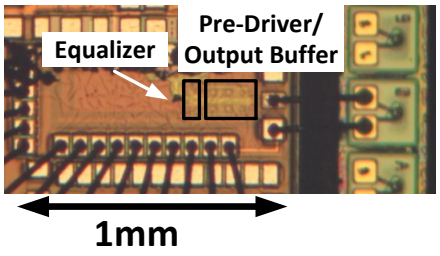
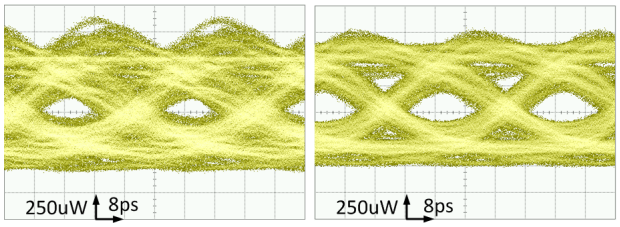
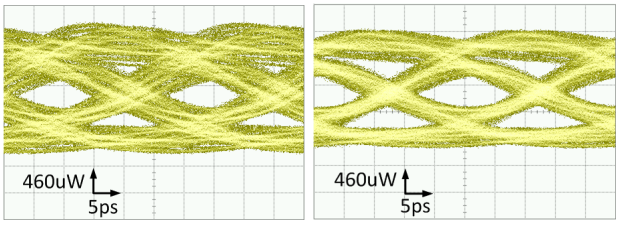


Fig. 7: CMOS chip and VCSEL array assembly



(a) (b)

Fig. 8: (a) 30Gbps optical eye-diagram ER = 4.5dBm and VCSEL bias of 1.7mA(a) Without equalizer (b) with equalizer .



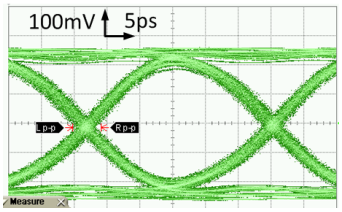
(a) (b)

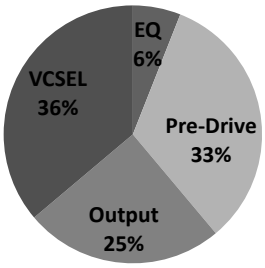
Fig. 9: (a) 40Gbps optical eye-diagram OMA = 1.3dBm and VCSEL bias of 3.5mA(a) Without equalizer J_{p-p}=23ps (b) with equalizer J_{p-p}=11.3ps.

In this condition the equalizer, pre-driver, output stage, and VCSEL biasing (the VCSEL and the biasing current source) consume,1.2m, 7m, 5.8m,and 7.1mW respectively translating to the power efficiency of 510pJ/b. Table I compares this work to other state-of-the-art VCSEL drivers with equalizers in CMOS and BiCMOS.

V. Conclusion

An equalizer with tunable complex zeroes has been proposed. The equalizer cancels out the ringing in the VCSEL's transient response to reduce the jitter and extend the usable speed of the VCSEL. The fabricated prototype achieves a record low power efficiency of 0.5pJ/s and the fastest CMOS VCSEL driver operation of 40Gbps.





(a) (b)

Fig. 10: (a) Single-ended electrical input eye-diagram ($450mV_{pp}$)(b) Power breakdown at 40Gbps, the total power is 20.05mW.

	[3]	[2]	[5]	[6]	This work
Equalization	FFE 1-tap	Asym FFE 1-tap	FFE 2-tap	GD comp	Complex zero eq
Technology	CMOS 65nm	CMOS SOI 32nm	SiGe 0.13μm	SiGe 0.13μm	CMOS 28nm
Data Rate (Gbps)	25	20	71	40	40
Supply(V)	1.2/3.6	1/2.5	4.0	2.5/3.3	1/-1.1
Power (pJ/b)	4	0.77	13.4	7.8	0.5
VCSEL Bias(mA)	6	N/A	8.2	7	3.5
VCSEL Bandwidth(GHz)	22.5	N/A	26	16	19
OMA (dBm)	0.8	0.9	3.6	2.3	1.3
Driver Type	Cathode Drive	Cathode Drive	Cathode Drive	Anode Drive	Anode Drive

TABLE I: Table of Comparison.

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