

All-Digital Calibration of Timing Mismatch Error in Time-Interleaved Analog-to-Digital Converters

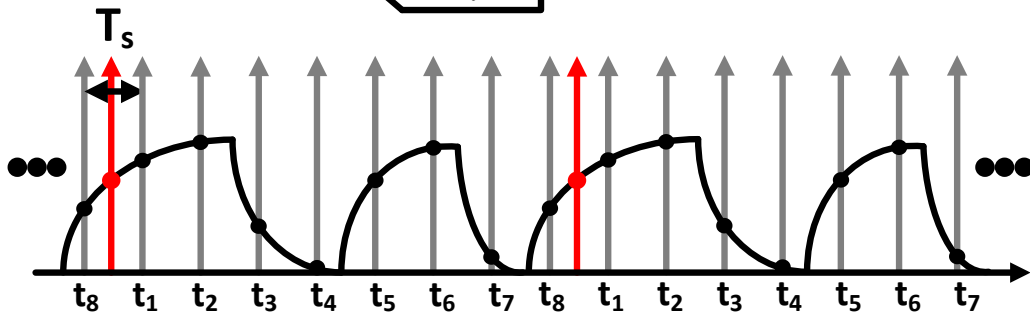
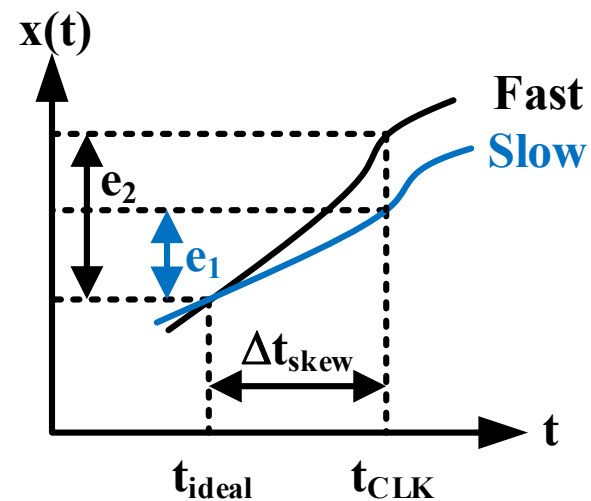
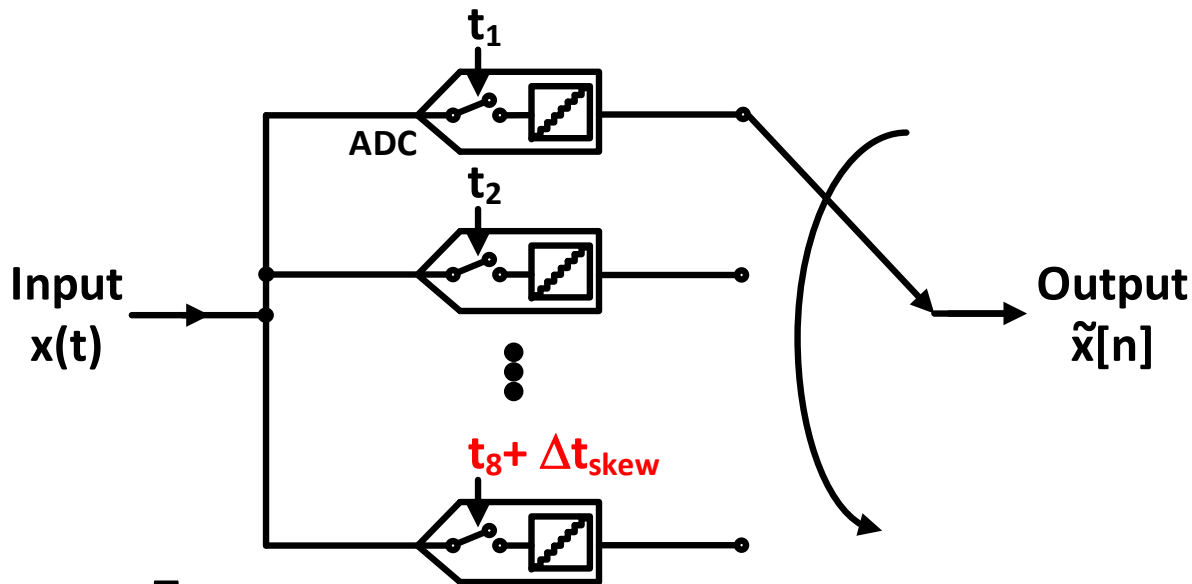
Shuai Chen, Luke Wang, Hong Zhang, Rosanah Murugesu, Dustin Dunwell, Anthony Chan Carusone

Outline

- Motivation
- Derivative-Based Digital Correction
- Difference-Based Skew Estimation
- Proposed All-Digital Timing Calibration
- Simulation & Measurement Results
- Conclusion

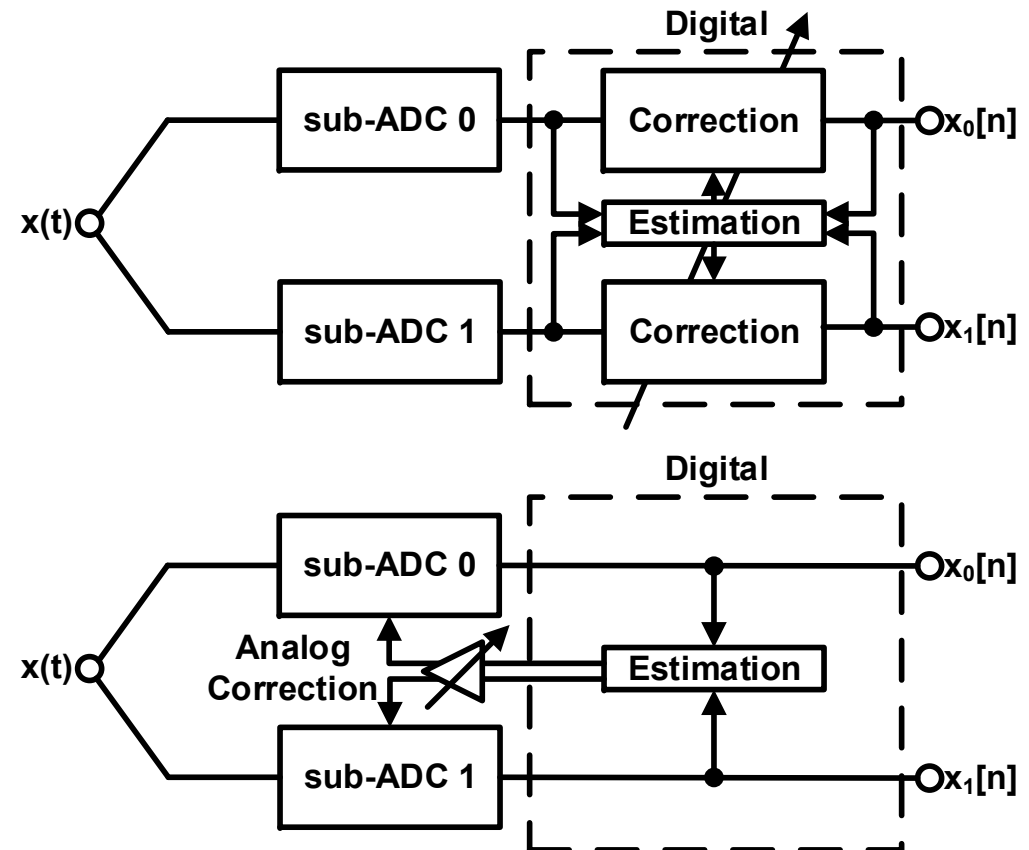
Motivation

- For a time-interleaved ADC, timing skew mismatch degrades SNDR significantly at high frequencies



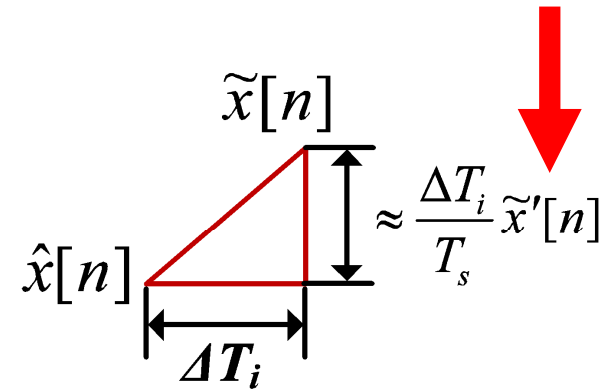
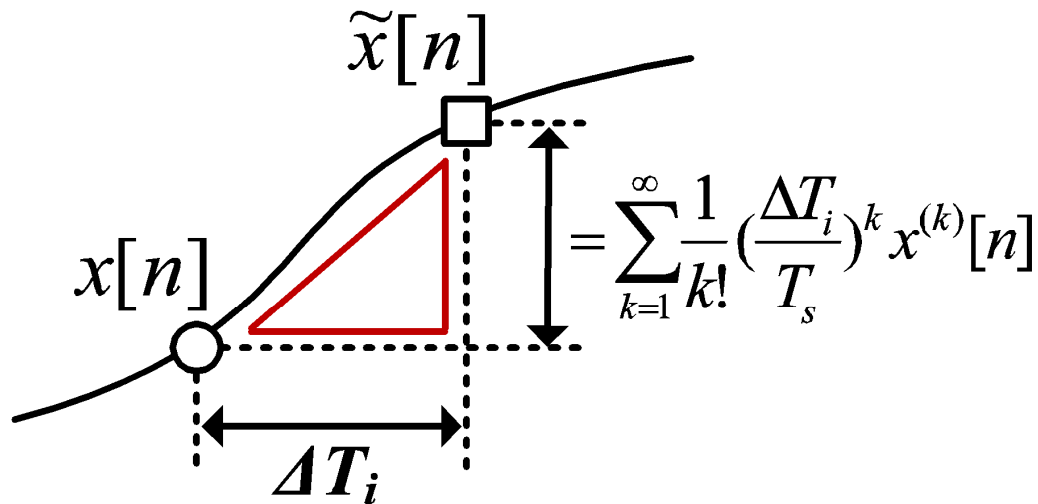
Motivation

- Estimation & correction using mixed-signal approaches or purely digital approaches
- Digital Cal. is immune to PVT variations and doesn't introduce additional jitter: analog variable delay line (VDL) is not required
- DSP cost (power, area) also decreases as technology scaling continues



Derivative-based Correction

- The amplitude error due to skew in i^{th} subADC (ΔT_i) can be expressed as a Taylor series expansion around the ideal sampling point
- 1st term suggests correction can be done using a derivative estimate



Sampling in the i^{th} Sub-ADC

Derivative-based Correction

- Consider a **4**-way TI-ADC, take sub-ADC1 as the reference channel and normalize timing mismatches to $r_{2\sim4} = (\Delta T_{2\sim4} - \Delta T_1) / T_s$
- The SNDR with timing mismatches can be shown to be

$$SNDR = \frac{1}{\frac{1}{6} \left(\frac{2}{2^B} \right)^2 + \frac{1}{4} \pi^2 [(r_2 - r_3 + r_4)^2 + 2(r_2 - r_4)^2 + 2r_3^2]} \left(\frac{f_{in}}{f_s} \right)^2 \quad (9)$$

- If skew is bounded by $[\Delta T_{\min}, \Delta T_{\max}]$, the worst SNDR in (9) arises when $r_2 = r_4 = \pm r_{\max}$ and $r_3 = 0$, where $r_{\max} = (\Delta T_{\max} - \Delta T_{\min}) / T_s$.

$$SNDR_{worst} = \frac{1}{\frac{1}{6} \left(\frac{2}{2^B} \right)^2 + \pi^2 r_{\max}^2} \left(\frac{f_{in}}{f_s} \right)^2 \quad (10)$$

Derivative-based Correction

- With derivative-based skew correction, we can derive a similar expression

$$SNDR_{cal} = \begin{cases} \frac{1}{\frac{1}{6} \left(\frac{2}{2^B} \right)^2 + |A_1|^2 + |A_2|^2 + |A_3|^2}, & f_{in} < \frac{f_s}{4} \\ \frac{1}{\frac{1}{6} \left(\frac{2}{2^B} \right)^2 + |B_1|^2 + |B_2|^2 + |B_3|^2}, & f_{in} > \frac{f_s}{4} \end{cases} \quad (13)$$

$$\begin{cases} A_1 = \frac{\pi^2 f_{in}}{4 f_s} \left[\left(\frac{f_{in}}{f_s} - \frac{1}{2} \right) (r_2^2 + r_4^2 - r_3^2) - r_2 r_4 + j r_3 (r_2 - r_4) \right] \\ A_2 = \frac{\pi^2 f_{in}}{4 f_s} \left(\frac{f_{in}}{f_s} - \frac{1}{2} \right) (r_4^2 - r_2^2 + j r_3^2) \\ A_3 = \frac{\pi^2 f_{in}}{4 f_s} \left[\left(\frac{f_{in}}{f_s} - \frac{1}{2} \right) (r_4^2 - r_2^2 + j r_3^2) + (1 + j) (j r_2 r_3 + r_3 r_4) \right] \end{cases} \quad (14)$$

$$\begin{cases} B_1 = \frac{\pi^2 f_{in}}{4 f_s} \left[\left(\frac{f_{in}}{f_s} - \frac{3}{2} \right) (r_2^2 + r_4^2 - r_3^2) + r_2 r_4 - j r_3 (r_2 - r_4) \right] \\ B_2 = \frac{\pi^2 f_{in}}{4 f_s} \left(\frac{f_{in}}{f_s} - \frac{3}{2} \right) (r_4^2 - r_2^2 - j r_3^2) \\ B_3 = \frac{\pi^2 f_{in}}{4 f_s} \left[\left(\frac{f_{in}}{f_s} - \frac{3}{2} \right) (r_4^2 - r_2^2 - j r_3^2) - (1 + j) (r_2 r_3 + j r_3 r_4) \right] \end{cases} \quad (15)$$

- Worst case SNDR can be shown to be

$$SNDR_{cal, worst} = \frac{1}{\frac{1}{6} \left(\frac{2}{2^B} \right)^2 + \frac{11}{16} \pi^4 r_{\max}^4 \left(\frac{f_{in}}{f_s} \right)^4} \quad (16)$$

Derivative-based Correction

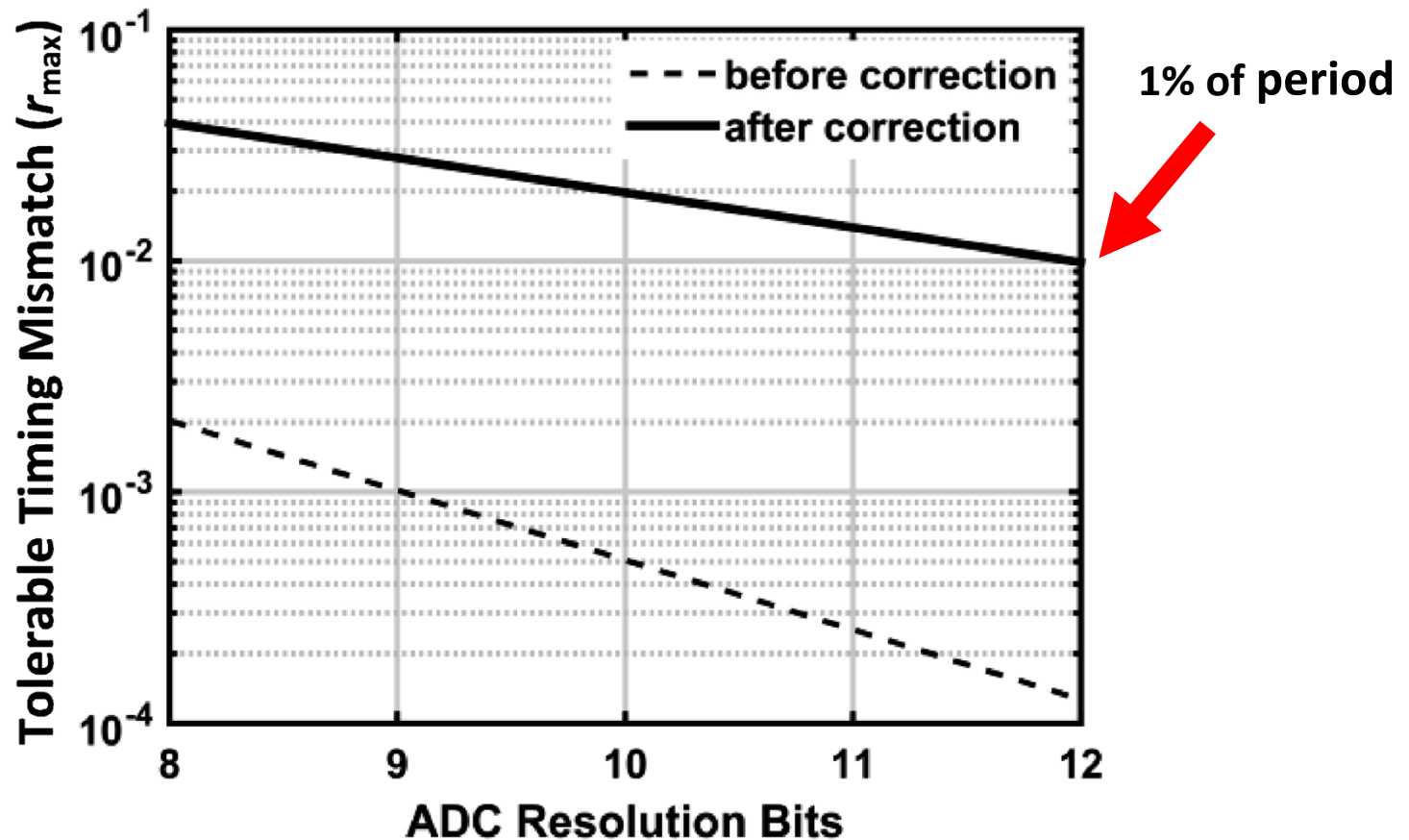
- Comparison of worst-case expressions

$$SNDR_{worst} = \frac{1}{\frac{1}{6} \left(\frac{2}{2^B} \right)^2 + \pi^2 r_{\max}^2 \left(\frac{f_{in}}{f_s} \right)^2} \quad (10)$$

$$SNDR_{cal,worst} = \frac{1}{\frac{1}{6} \left(\frac{2}{2^B} \right)^2 + \frac{11}{16} \pi^4 r_{\max}^4 \left(\frac{f_{in}}{f_s} \right)^4} \quad (16)$$

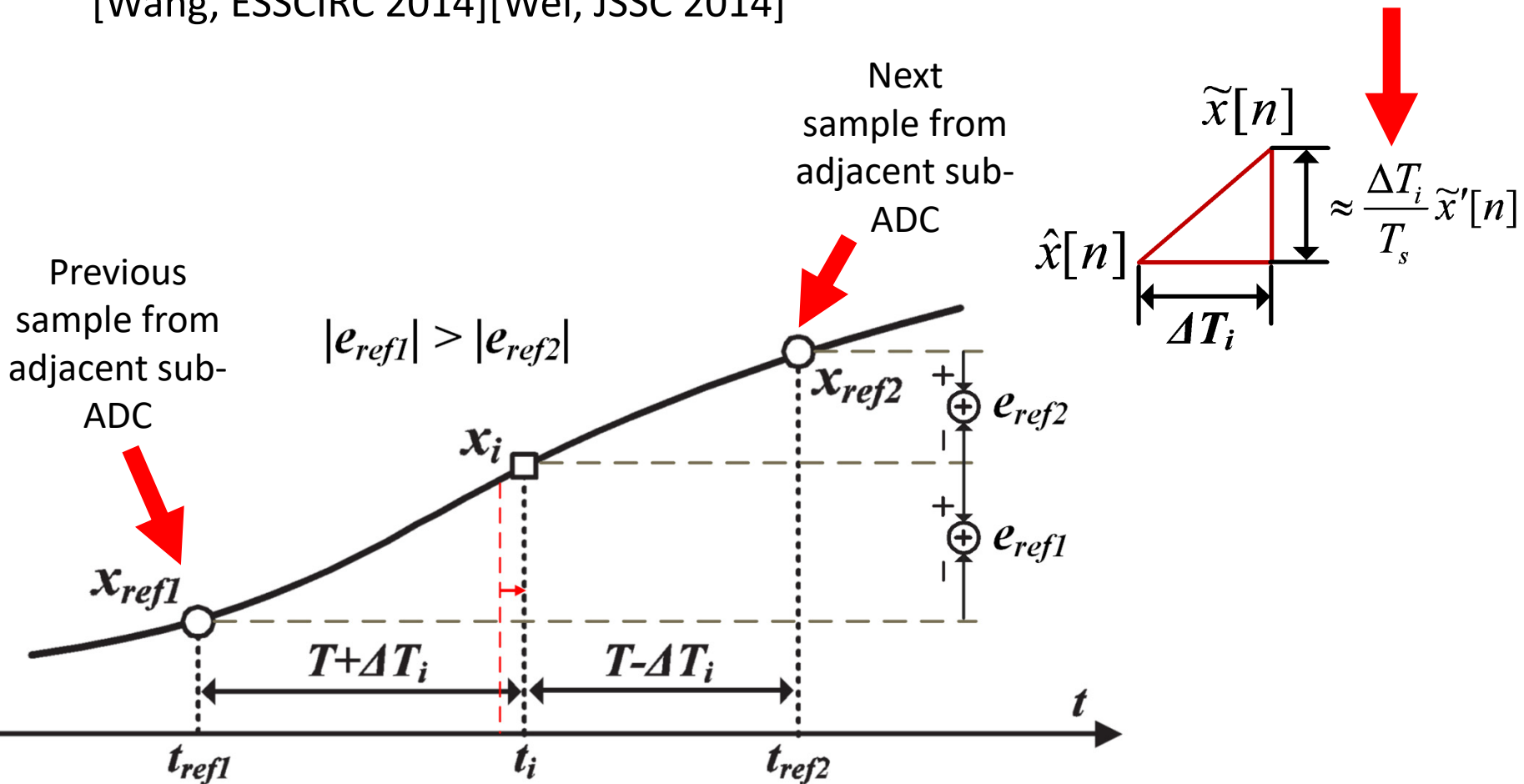
Derivative-based Correction

- If we budget 3dB degradation in SNDR at Nyquist frequency, the timing skew tolerance improves **~76x** for a 12-bit 4-way TI-ADC after correction



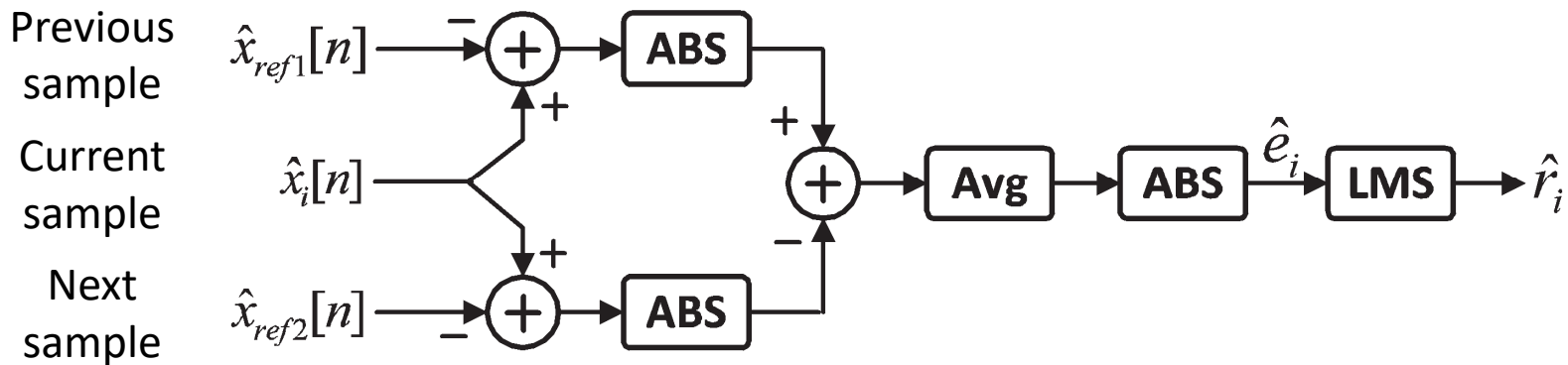
Difference-based Skew Estimation

- In order to estimate the skew ΔT_i , difference-based approach is used [Wang, ESSCIRC 2014][Wei, JSSC 2014]



Difference-based Skew Estimation

- This **Timing Mismatch Estimator** is shown here in block diagram form, where the estimate can be updated via LMS

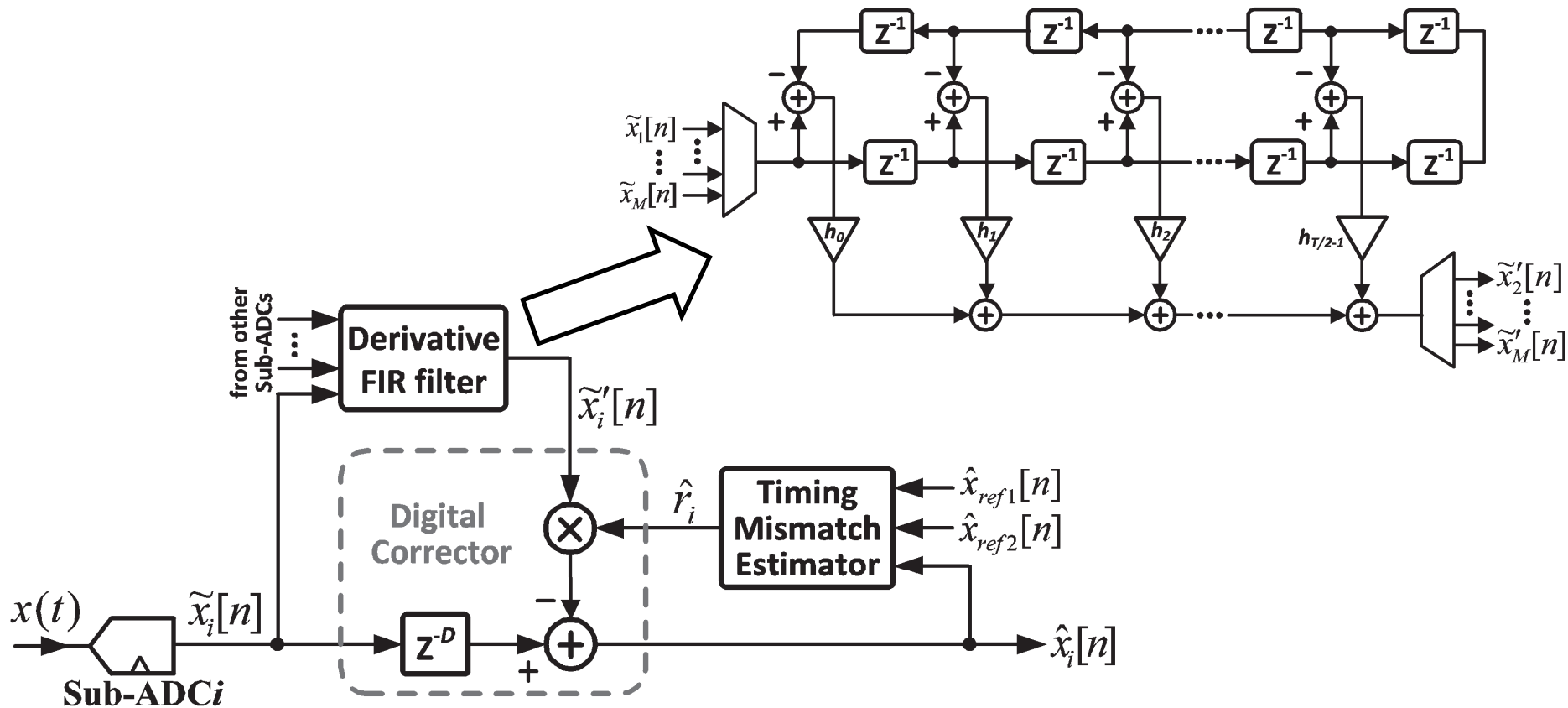


$$\hat{e}_i = \left| \frac{1}{N} \sum_{k=1}^N (|\hat{x}_i[k] - \hat{x}_{ref1}[k]| - |\hat{x}_i[k] - \hat{x}_{ref2}[k]|) \right| \quad (17)$$

$$\hat{r}_i(n+1) = \hat{r}_i(n) - \mu \cdot \hat{e}_i[n] \cdot \frac{\text{sign}(\hat{e}_i[n] - \hat{e}_i[n-1])}{\text{sign}(\hat{r}_i[n] - \hat{r}_i[n-1])} \quad (24)$$

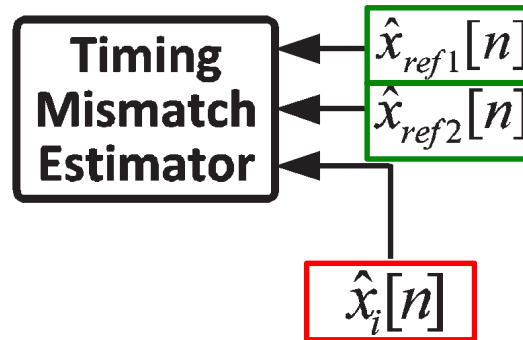
Proposed All-Digital Calibration

- Estimation and correction can thus be done both in the digital domain
- Filter is full-rate type III 33 tap FIR with cut-off frequency of $0.42f_s$



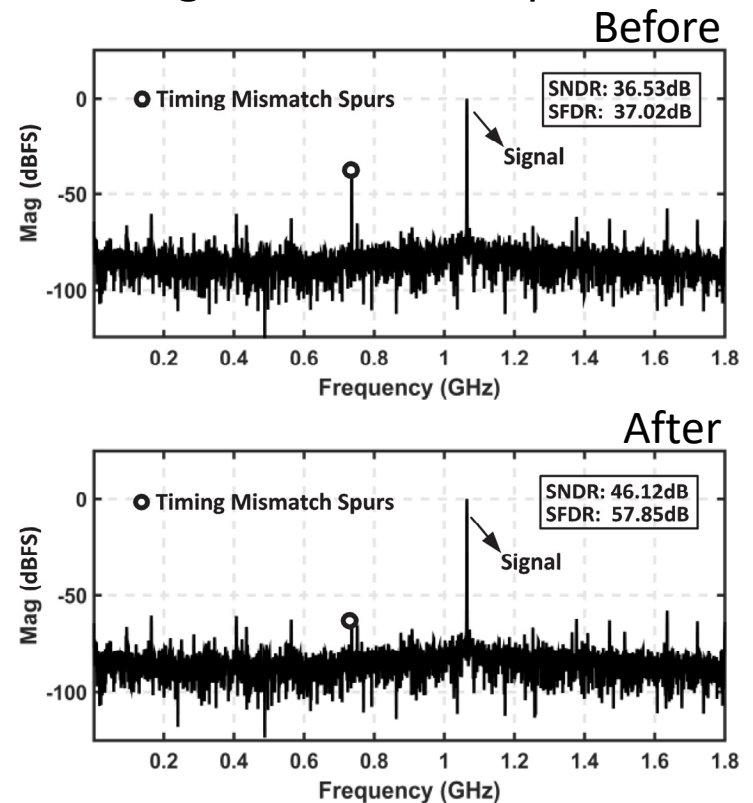
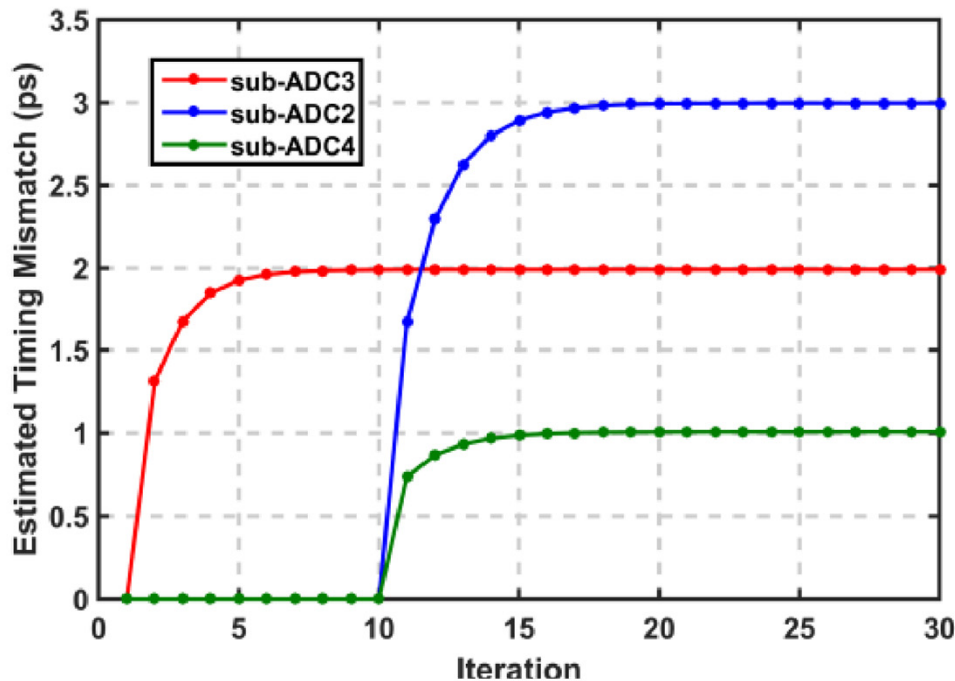
Proposed All-Digital Calibration

- Estimation strategy can also be extended to **4** channels by changing the channel in calibration & “reference channels” x_{ref1} and x_{ref2} iteratively



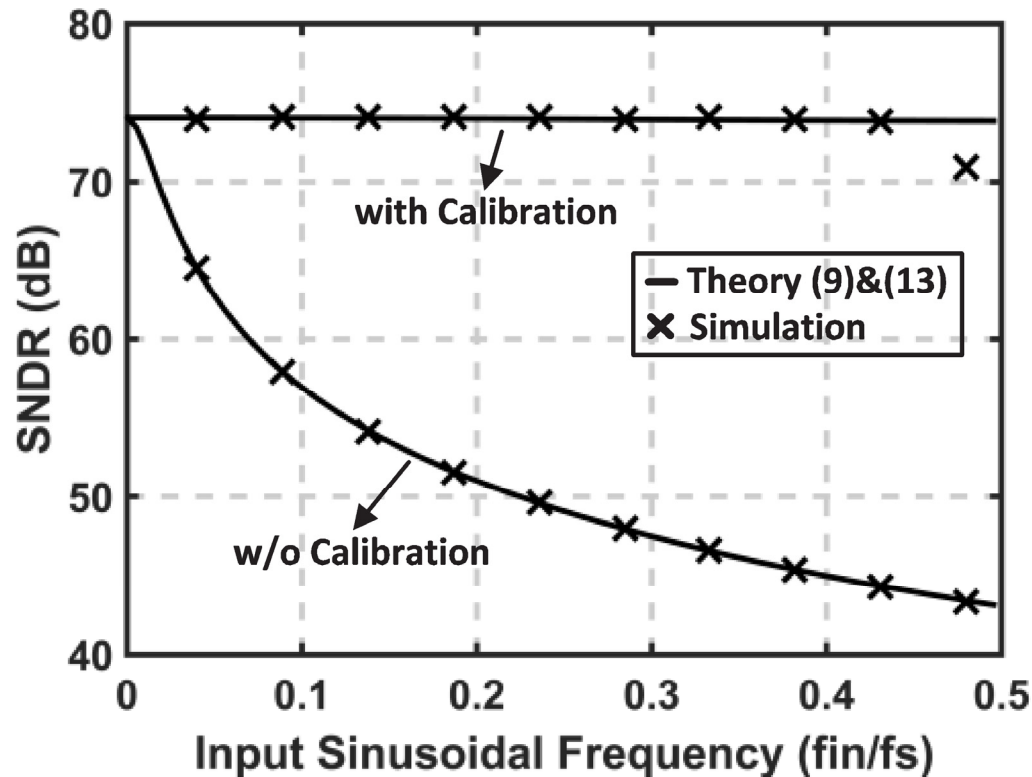
Simulation Results

- Simulation for 4xTI 12b 2GS/s ADC, $\Delta T_{1\sim 4} = [1ps, 4ps, 3ps, 2ps]$, $f_{in} = 0.41f_s$
- The estimator can accurately converge to $\Delta T_{2\sim 4} - \Delta T_1$ with $< 0.1\%$ error
- Every iteration collects 4000 points and the timing estimation loop converges in about 20 iterations



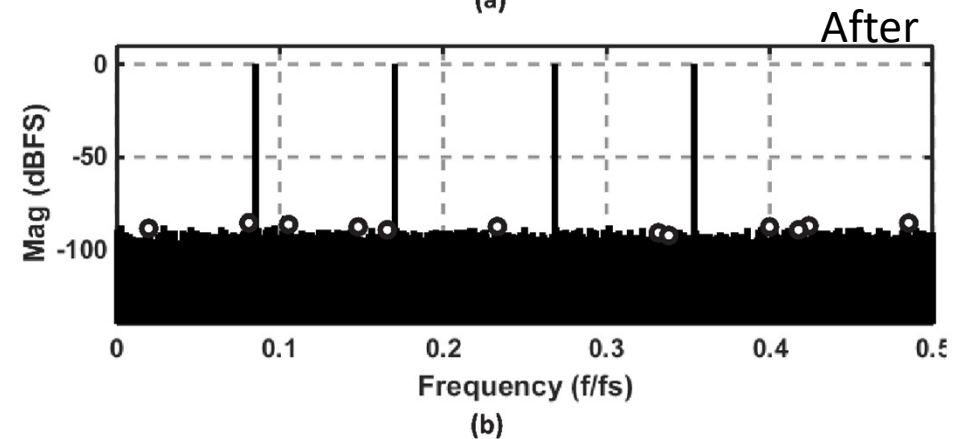
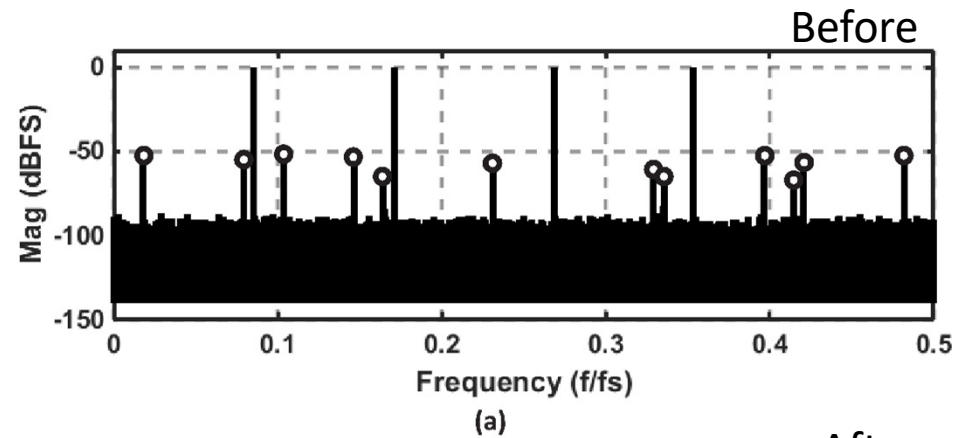
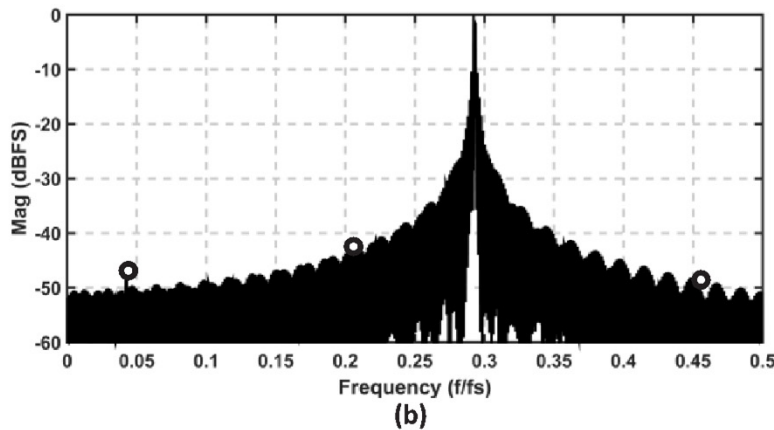
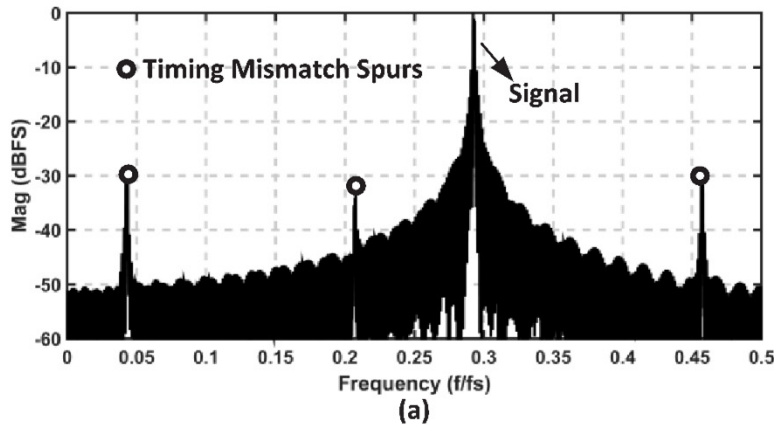
Simulation Results

- Simulation for 4xTI 12b 2GS/s ADC, $\Delta T_{1\sim 4} = [1ps, 4ps, 3ps, 2ps]$, $f_{in} = 0.41f_s$
- Behaviour matches theoretical expression over frequency until FIR bandwidth of $0.42f_s$



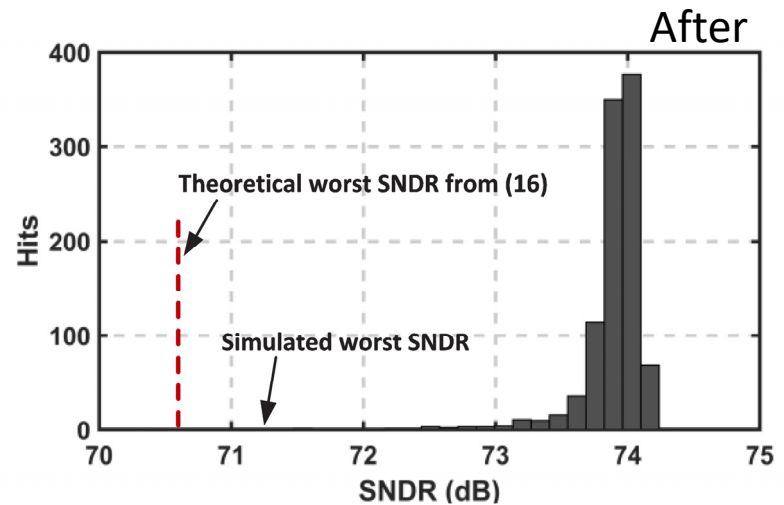
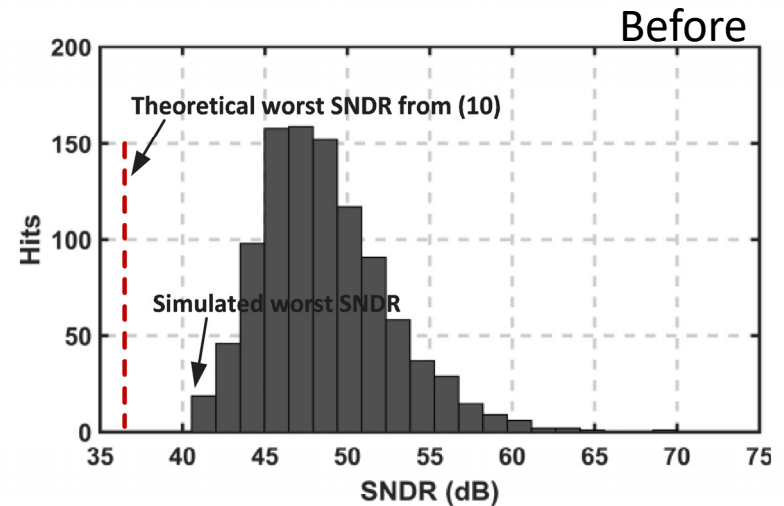
Simulation Results

- Calibration also verified with QPSK and multi-tone signal
- Background calibration is possible without restricting input to single tone



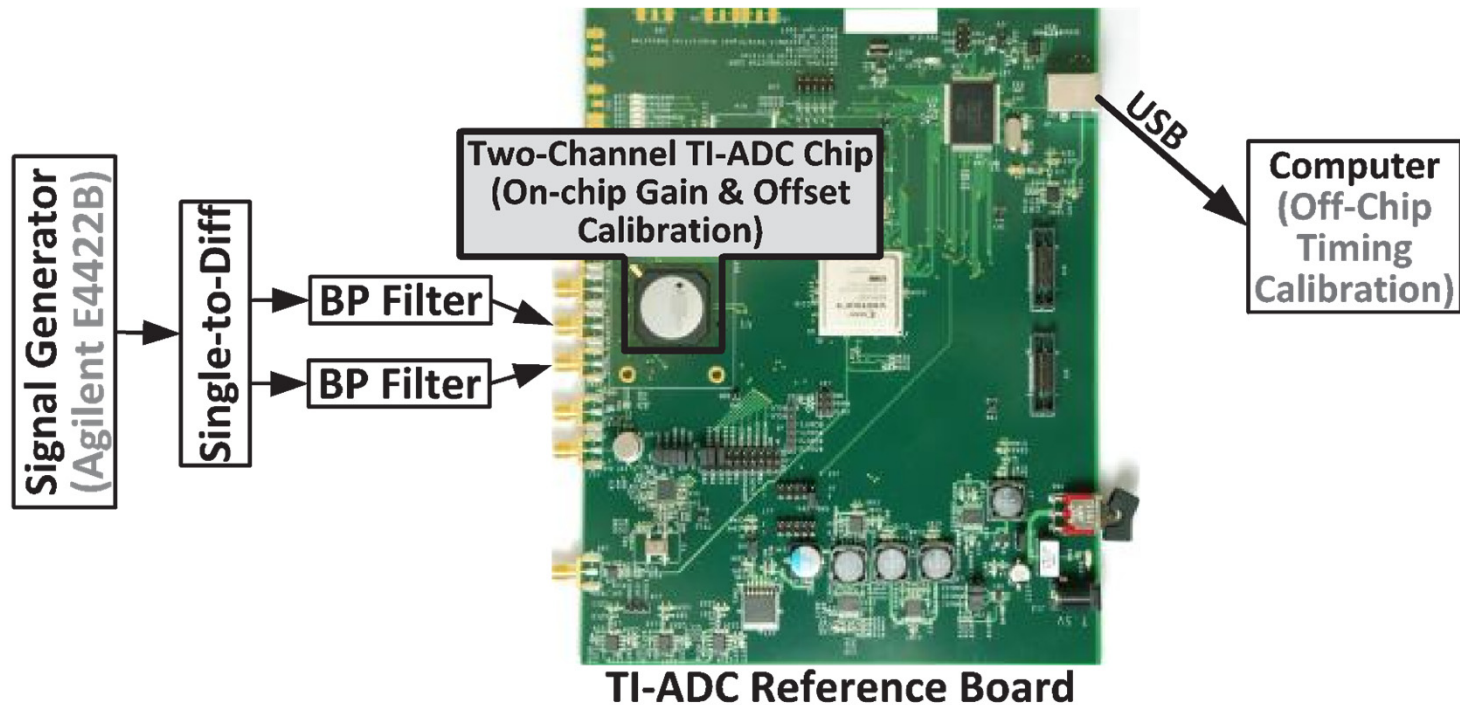
Simulation Results

- Worst-case SNDR expressions are verified using 1000 Monte-Carlo simulations, where $\Delta T_{1\sim 4}$ are iid Gaussian with $\sigma = 1\text{ps}$
- Theoretical limit shown here for $[\Delta T_{\min}, \Delta T_{\max}] = [-3\sigma, 3\sigma]$



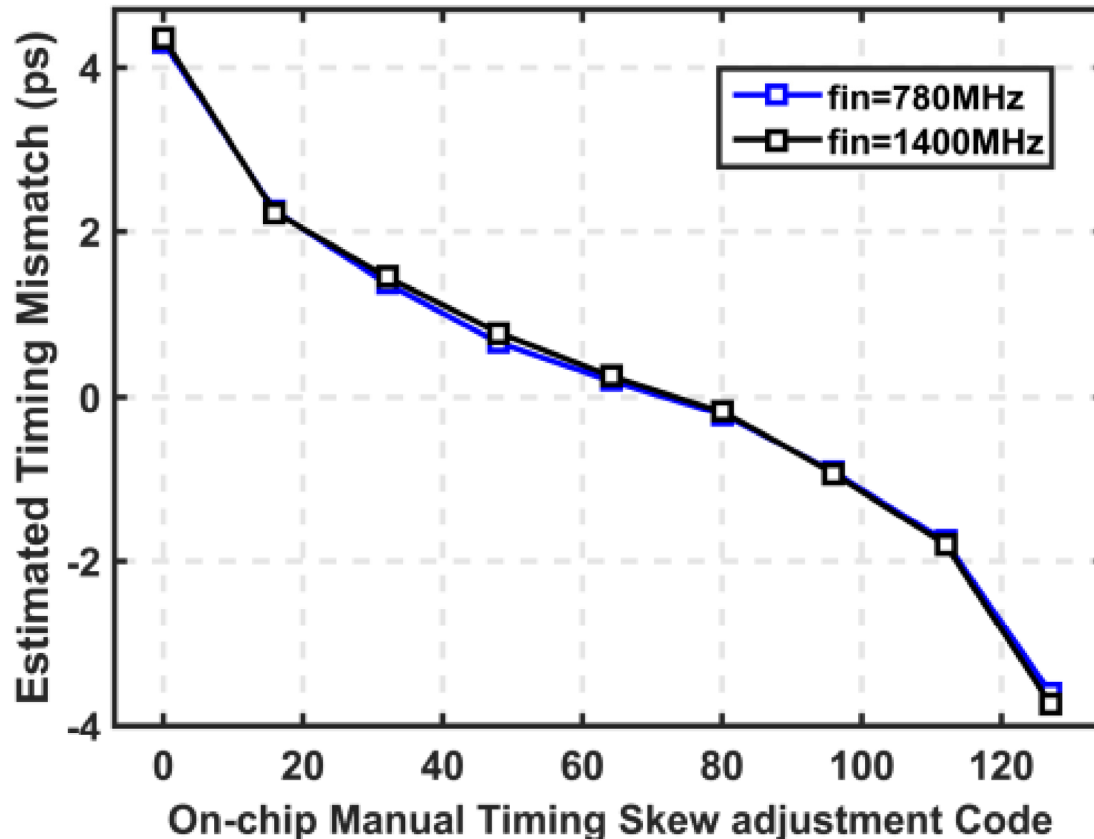
Measurement Results

- A commercial 12bit 3.6GS/s 2 channel TI-ADC [21] was also used to verify this work
- An on-chip manual timing skew adjustment code (analog delay) is available to compare with this work



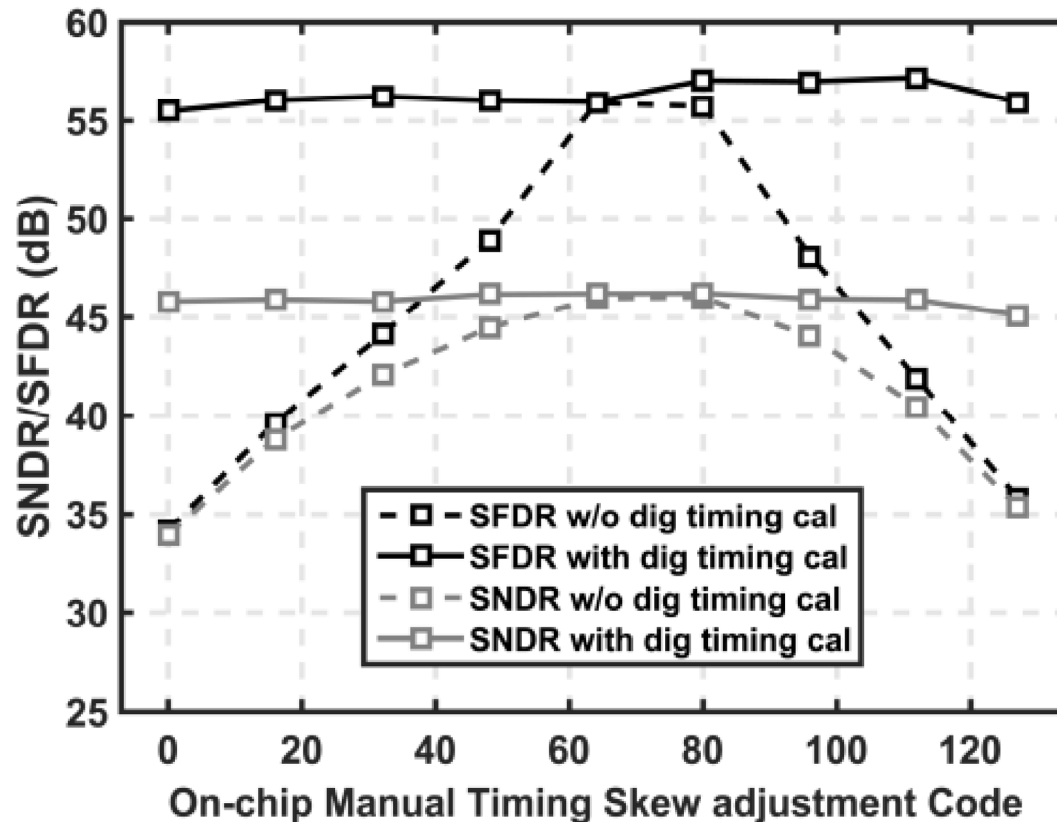
Measurement Results

- Using the on-chip delay code, we see the estimation does not vary with input frequency as expected for a single-tone input at 1400MHz and 780MHz.



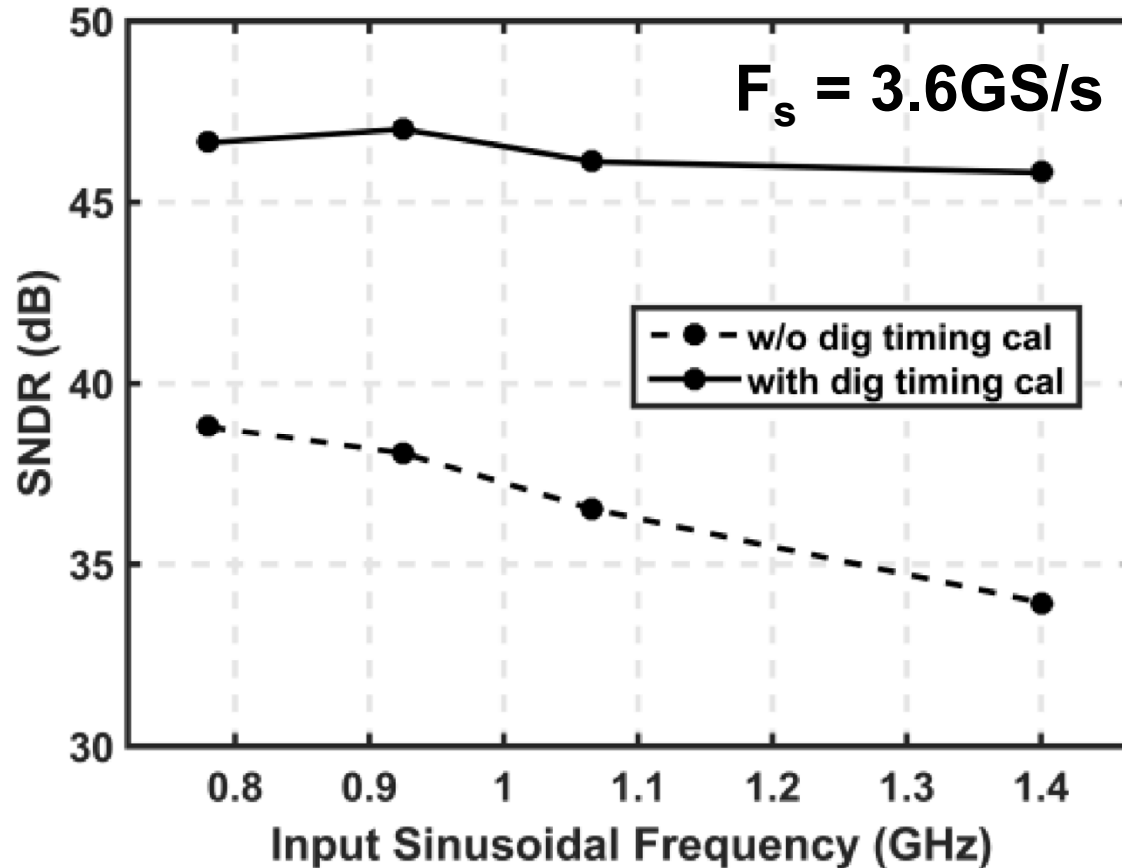
Measurement Results

- By varying the on-chip delay code, we converge the calibration for a single-tone input at 1400MHz, which improves SNDR for all delay range

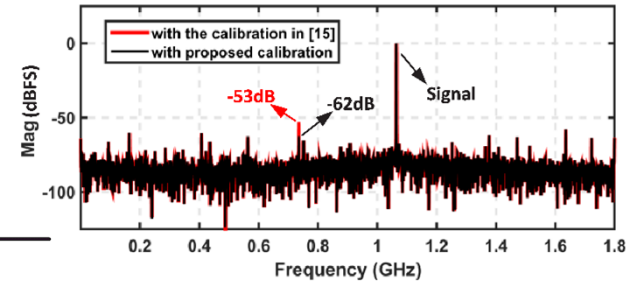


Measurement Results

- The calibration is also verified for other input frequencies



Comparison to Other Works



	This Work	N.L. Dortz ISSCC 2014	J. Matsuno TCAS-I 2013	H. Le Duc TCAS-II 2016	C.-Y. Lin ISSCC 2016
Derivative Generator	FIR filter	FIR filter	Polyphase FIR filter	Polyphase FIR filter	Auxiliary ADCs
Timing Mismatch Estimation	subtraction detection	open-loop calculation	FIR filter + correlator	FIR filter + correlator	auto-correlation detection
# of FIR filter	1	1	2	2	0
# of Multiplier^{1,2}	2	6	3	3	4
# of Adder^{1,2}	7	3	2	2	9
Timing Mismatch Tone³	-62dB	-53dB	-62dB	-62dB	-
Convergence Time (Samples)	80K	1M	60K	10K	32K

¹ for per sub-ADC channel

² for the correction and estimation of timing mismatch

³ for the 12bit 3.6GS/s two-channel TI-ADC with a single-tone input at 1065MHz

Conclusion

- Derivative-based digital correction and digital adaptive timing mismatch estimation are combined to achieve accurate closed-loop timing mismatch estimation and effective distortion tone suppression
- Explicit formulas (9), (10), (13) and (16) are also obtained accurately predicting SNDR and providing the bounds on the tolerable timing mismatch for four-channel TI-ADCs both before and after derivative-based digital correction, serving as useful guidelines for designers.

Acknowledgement

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