Welcome to

DesignCon® 2021
WHERE THE CHIP MEETS THE BOARD

Conference
August 16 – August 18, 2021

Expo
August 17 – August 18, 2021

San Jose McEnery Convention Center

Global Optimization of Wireline Transceivers for Minimum Post-FEC vs. Pre-FEC BER

Ming Yang, (University of Toronto)

Shayan Shahramian, Henry Wong, Peter Krotnev (Huawei Canada)
Anthony Chan Carusone (University of Toronto)

SPEAKER

Ming Yang

Ph.D. Candidate, University of Toronto

ming.yang@isl.utoronto.ca | https://isl.utoronto.ca/

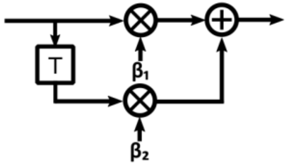
Ming Yang received the B.Eng. degree in aerodynamic engineering from the Department of Aeronautics, Xiamen University, Xiamen, China, in 2012, and the B.Eng. and M.Eng. degree in electrical engineering from the Department of Electrical and Computer Engineering, McGill University, Montreal, Canada, in 2013 and 2016, respectively. He is currently a Ph.D. candidate in the Edward S. Rogers Sr. Department of Electrical & Computer Engineering at University of Toronto. He is the recipient of the Alexander Graham Bell Canada Graduate Scholarships award (NSERC CGS D). His research interests are in analog integrated circuit design, on-chip analog signal processing and high-performance integrated circuit testing.

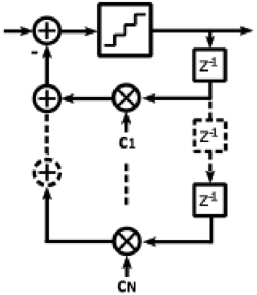
Outline

1. Motivation
2. Wireline Transceiver Model System Overview
   a. System Overview
   b. DFE Error Propagation
3. Pre-FEC and Post-FEC BER as Criteria for Optimizing Wireline Transceivers
   a. Pre-FEC vs Post-FEC BER Optimum
   b. Simulation Results: 1-Tap DFE
   c. Simulation Results: 2-Tap DFE
4. GA-Assisted Transceiver Optimization
   a. Genetic Algorithm Overview
   b. Optimization Framework
   c. Simulation Results
5. Conclusion

Motivation

- Common receiver DSP equalizer blocks in 100Gb/s+ wireline applications:

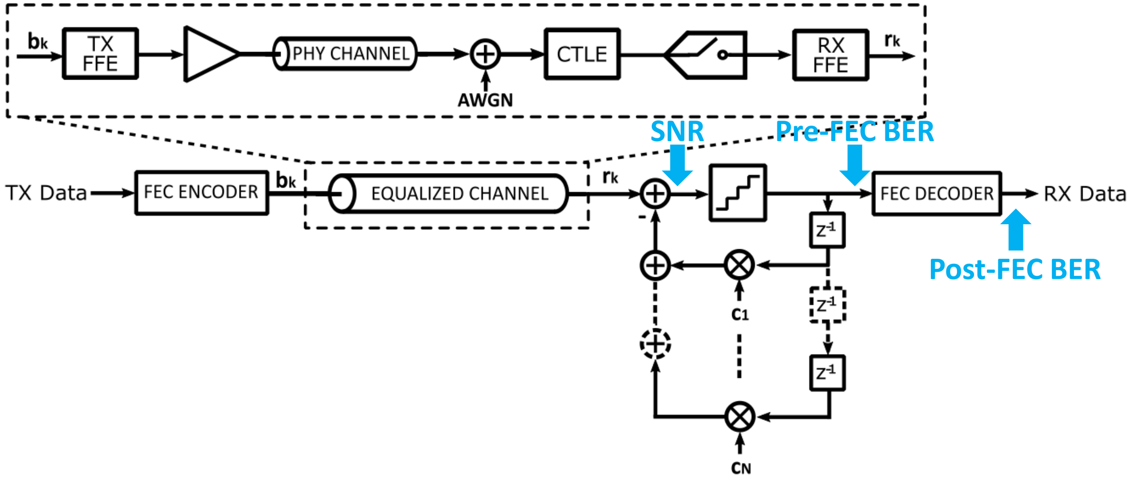




- Feed-forward Equalizer (FFE)
  - Noise amplification
  - High speed operation
  - No error propagation
- Decision-Feedback Equalizer (DFE)
  - Error propagation
  - Speed limited by critical feedback path
  - No noise amplification

- Forward-Error Correction (FEC) code have also become an integral part of the DSP
  - Standard Reed-Solomon (RS) to mitigate DFE error propagation
  - Ex: RS(544,514,15) KP4 code to achieve a targeted post-FEC BER $<10^{-15}$

Motivation



- Three performance metrics for optimizing equalizer coefficients in wireline transceivers:
  - SNR (Implicitly the optimization criteria when using LMS adaptation)
  - Pre-FEC BER
  - Post-FEC BER

Metric	FFE Noise Amplification	DFE Error Propagation	Sensitivity to Long Burst Errors at very low BER
SNR	✓	✖	✖
Pre-FEC BER	✓	✓	✖
Post-FEC BER	✓	✓	✓

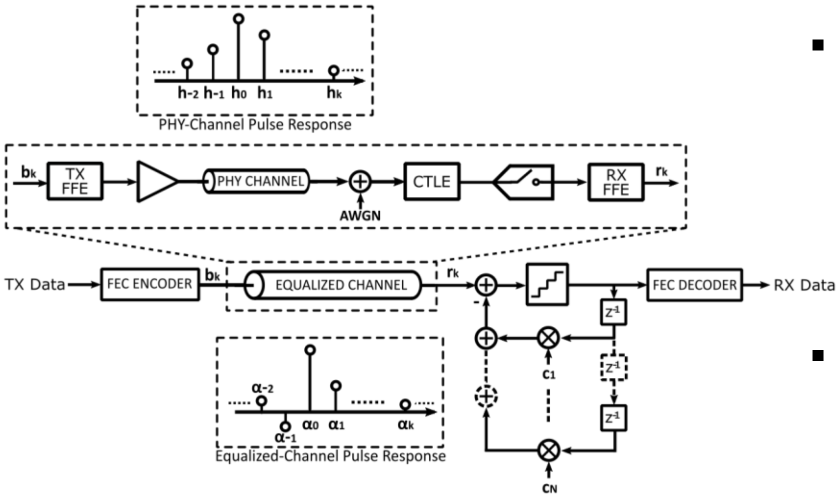
Motivation

- FFE and DFE tap coefficients are typically optimized to maximize signal-to-noise ratio (SNR) or to minimize the mean-squared error (MMSE) or pre-FEC BER [1-3]
- Equalizer parameters found by conventional methods do not necessarily minimize post-FEC BER
- This work presents an accurate and efficient methodology for finding transceiver parameters using Genetic Algorithm, based on post-FEC BER

Outline

1. Motivation
2. Wireline Transceiver Model System Overview
    a. System Overview
    b. DFE Error Propagation
3. Pre-FEC and Post-FEC BER as Criteria for Optimizing Wireline Transceivers
    a. Pre-FEC vs Post-FEC BER Optimum
    b. Simulation Results: 1-Tap DFE
    c. Simulation Results: 2-Tap DFE
4. GA-Assisted Transceiver Optimization
    a. Genetic Algorithm Overview
    b. Optimization Framework
    c. Simulation Results
5. Conclusion

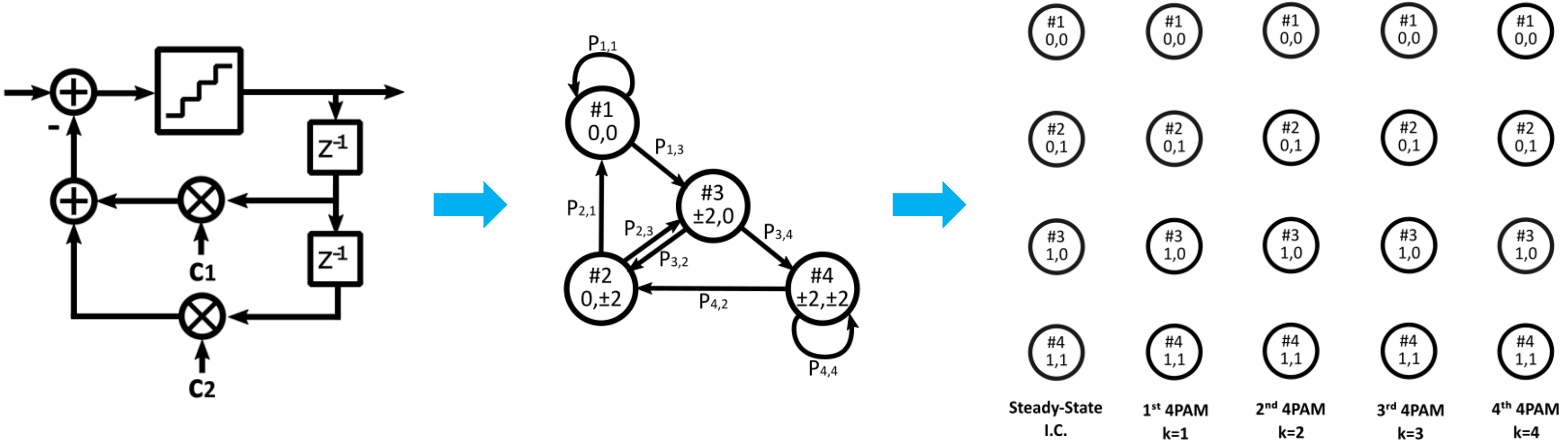
Transceiver Model – System Overview



- Equalized pulse response α(z) is generated by convolving the physical channel's pulse with the impulse response of other components in the link, such as the TX FFE, TX driver, CTLE and RX FFE

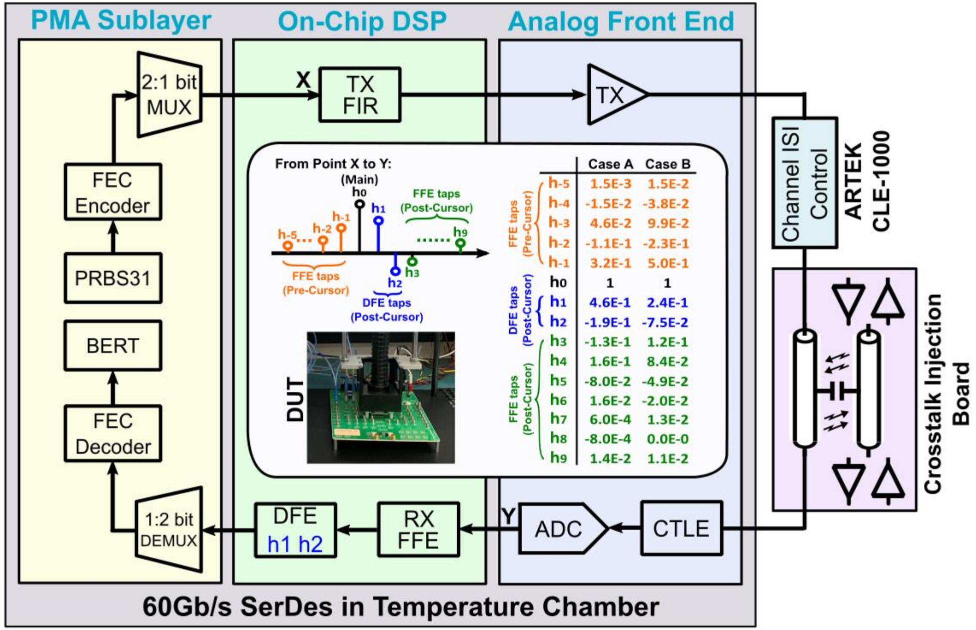
- Additive white Gaussian noise (AWGN) assumed at CTLE input, creating correlated noise samples after CTLE filtering

Statistical Model – DFE Error Propagation [Yang, TCAS-I, 2020]

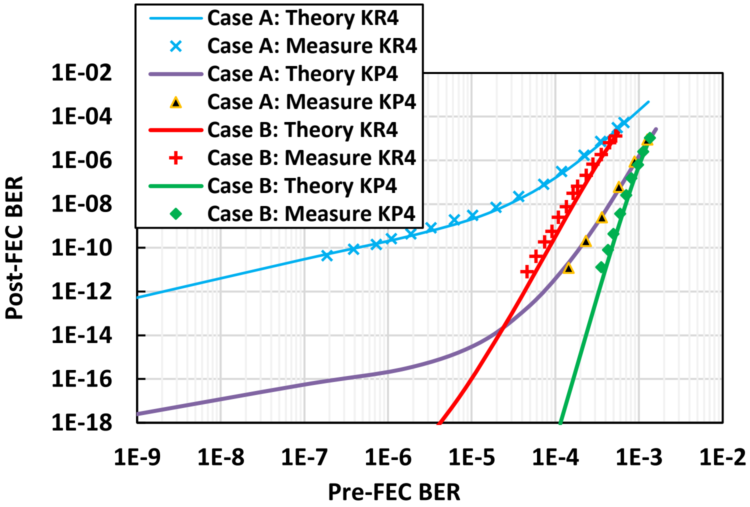


- Example of a 2-tap DFE represented by a simplified 4-state Markov model
- Time-unrolling the Markov DFE model to generate PAM trellis
- Apply trellis dynamic programming to the PAM trellis to efficiently collect all error patterns

Statistical Model – DFE Error Propagation [Yang, TCAS-I, 2020]

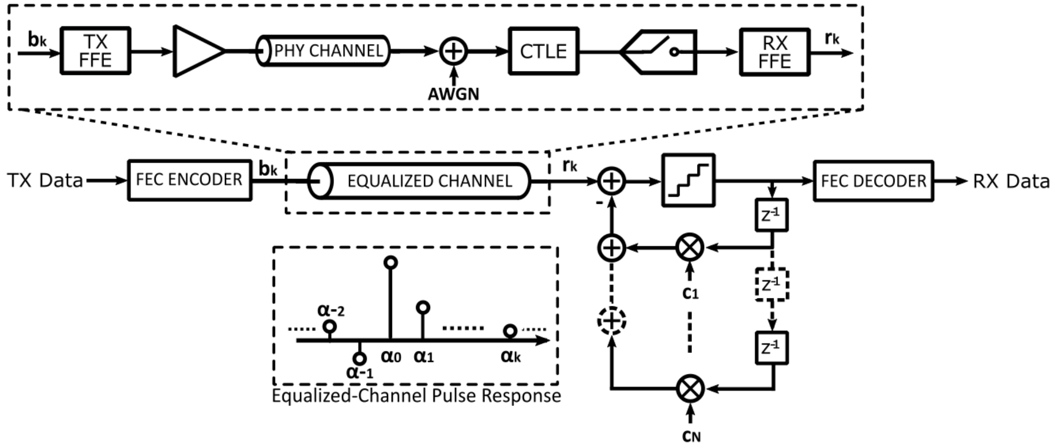


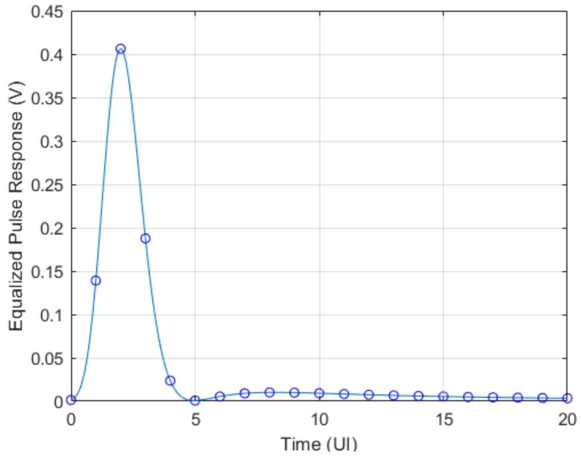
Measured and statistical pre-FEC vs post-FEC BER plot for RS(528, 514, 7) and RS(544, 514, 15) code



Outline

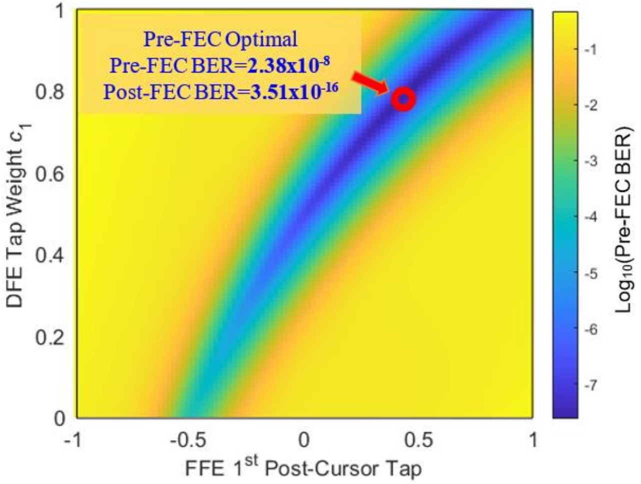
Pre-FEC vs Post-FEC BER Optimum - Link Setup

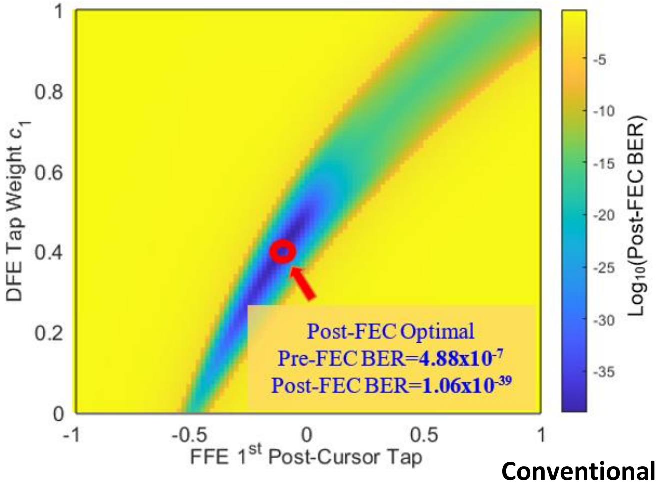




- A channel model with 30 dB insertion loss for a link communicating 4-PAM symbols at 56 GBaud/s subject to 0.55 VP-P swing at TX, 4.58 mV_{rms} integrated rms noise
- A simplified CTLE model provides 12 dB peaking gain with 0 dB gain at DC
- A 1-tap DFE and a 7-tap FFE with 2 pre-cursor and 4 post-cursor taps at RX
- The post-FEC BER is calculated assuming the standard KP4 RS(544,514, 15) code

Pre-FEC vs Post-FEC BER Optimum





- Vastly different optimal point with proposed optimization approach
- Tradeoff between FFE noise amplification and DFE error propagation

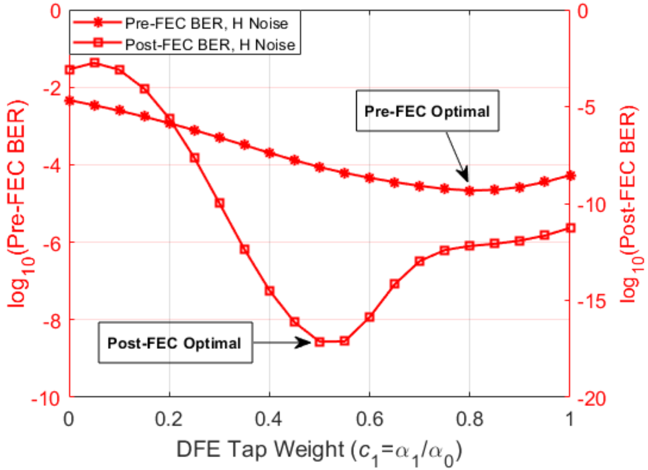
	Conventional: Pre-FEC Optimization	Proposed: Post-FEC Optimization
Pre-FEC BER	2.38×10^{-8}	4.88×10^{-7}
Post-FEC BER	3.51×10^{-16}	1.06×10^{-39}

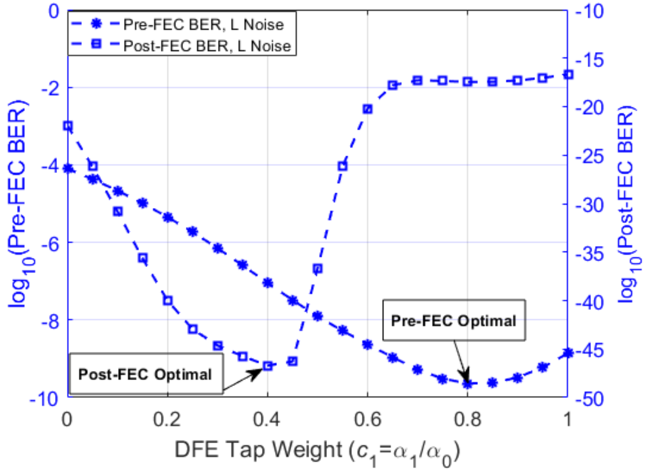
Significant improvement in post-FEC BER using proposed optimization approach

Simulation Results: 1-Tap DFE

- More extensive simulation results using six measured channel responses to validate our methodology using post-FEC BER
- TX has a 2-tap FFE providing 5 dB pre-emphasis, and the RX FFE has 15 taps, including 3 pre-cursor taps and 11 post-cursor taps
- An 8th-order CTLE model was applied to equalize all six channels having 30–40 dB insertion loss
- The equalized pulse responses including TX FFE, CTLE and PHY channel are tabulated in Table I of the paper

Simulation Results: 1-Tap DFE

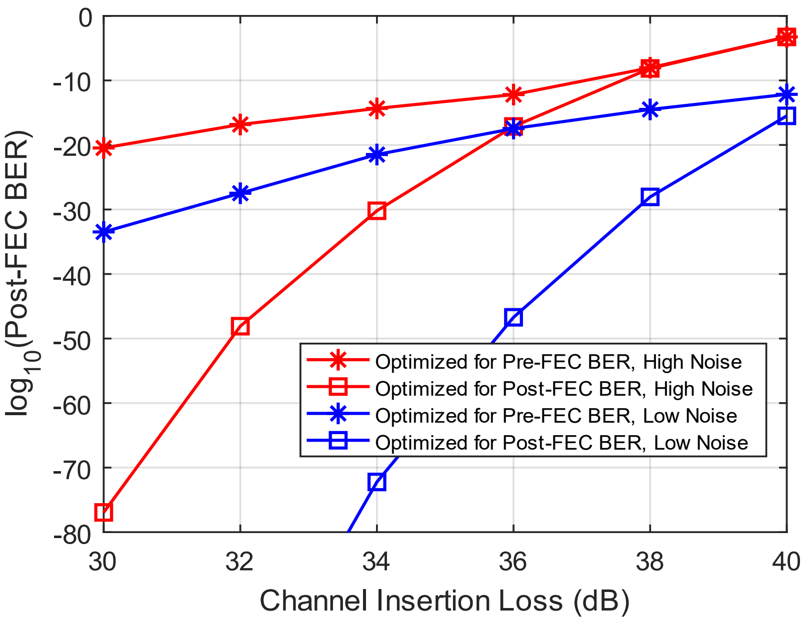




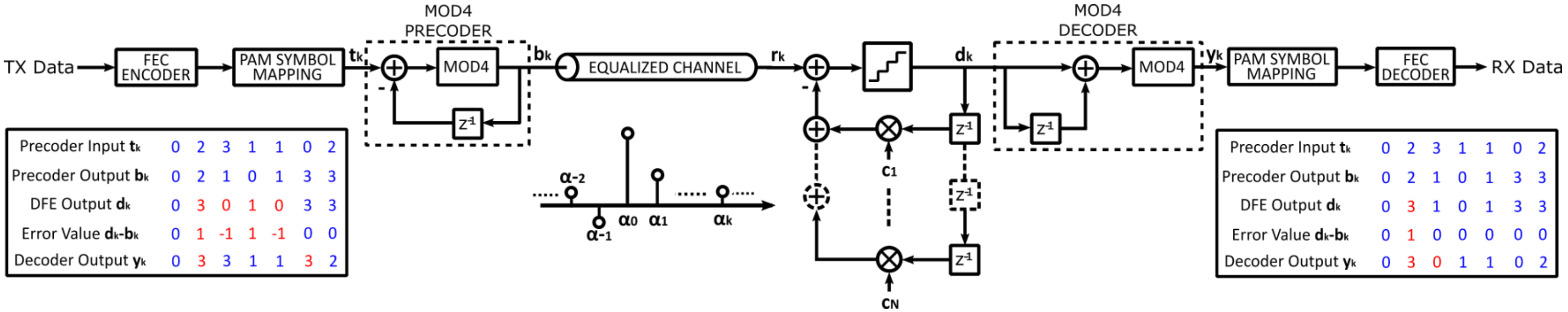
- Plot both the pre-FEC BER and post-FEC BER as a function of DFE tap weight α_1/α_0 for the 36 dB channel
- Simulated at two integrated rms noise levels: 1.62 mV_{rms} (low noise) and 2.42 mV_{rms} (high noise)
- Different DFE coefficients at pre-FEC and post-FEC optimal
  - Post-FEC BER is minimized at a lower α_1/α_0 than pre-FEC

Simulation Results: 1-Tap DFE

- Repeating the same analysis for all six measured channels
- The optimal post-FEC BER obtained by post-FEC optimization is always superior



1/(1+D) Pre-Coding [Yang, DesignCon, 2020]

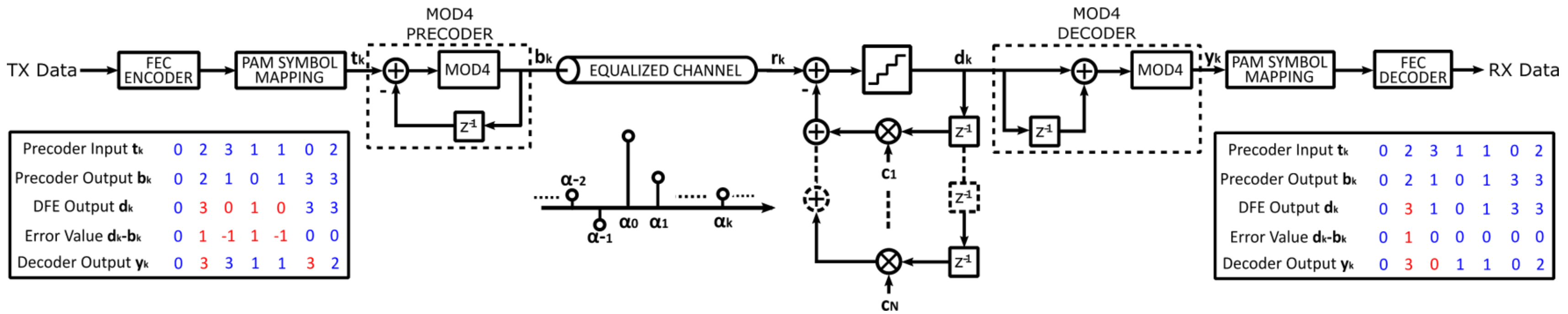


Precoder Input t_k	0	2	3	1	1	0	2
Precoder Output b_k	0	2	1	0	1	3	3
DFE Output d_k	0	3	0	1	0	3	3
Error Value d_k-b_k	0	1	-1	1	-1	0	0
Decoder Output y_k	0	3	3	1	1	3	2

Precoder Input t_k	0	2	3	1	1	0	2
Precoder Output b_k	0	2	1	0	1	3	3
DFE Output d_k	0	3	1	0	1	3	3
Error Value d_k-b_k	0	1	0	0	0	0	0
Decoder Output y_k	0	3	0	1	1	0	2

- A wireline transceiver model incorporating 1/(1+D) pre-coding to mitigate DFE error bursts
- 1/(1+D) decoder removes burst errors because the error d_k-b_k in the current received symbol is added to the error d_{k-1}-b_{k-1} in the previously received symbol
- Isolated individual symbol errors give rise to two consecutive symbol errors after decoding
- Method in [8] is used to generate the post-FEC BER results including 1/(1+D) pre-coding

Optimizing for (1+αD) Type of Partial Response

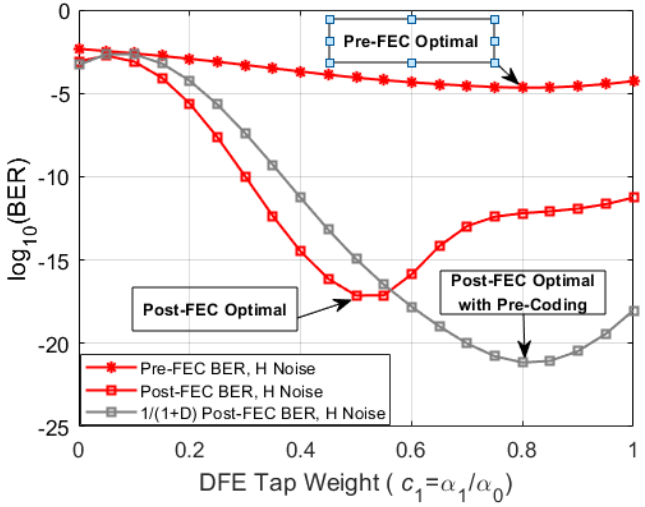


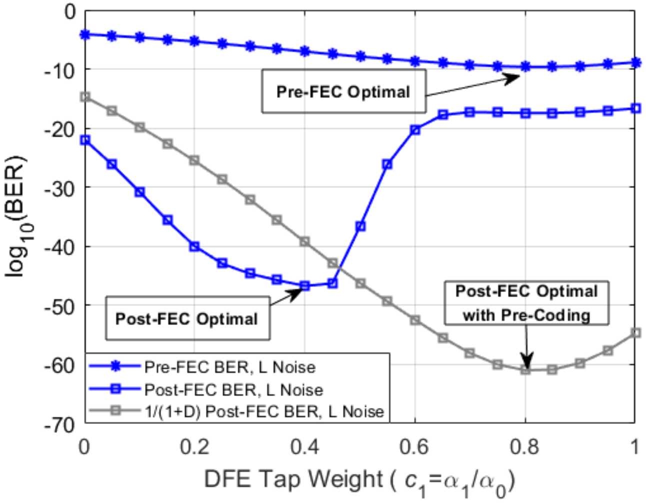
Precoder Input t_k	0	2	3	1	1	0	2
Precoder Output b_k	0	2	1	0	1	3	3
DFE Output d_k	0	3	0	1	0	3	3
Error Value d_k-b_k	0	1	-1	1	-1	0	0
Decoder Output y_k	0	3	3	1	1	3	2

Precoder Input t_k	0	2	3	1	1	0	2
Precoder Output b_k	0	2	1	0	1	3	3
DFE Output d_k	0	3	1	0	1	3	3
Error Value d_k-b_k	0	1	0	0	0	0	0
Decoder Output y_k	0	3	0	1	1	0	2

- Prior FFE+DFE equalization strategy:
  - Only use the *N*-tap DFE to equalize the first *N* post-cursor ISIs, the first *N* FFE post-cursor taps are set to zero. Here we denote the FFE-equalized pulse response as $\alpha_{k\text{-intrinsic}}$
- This work:
  - FFE-equalized pulse response is $(1+\alpha_1 \cdot D+\alpha_2 \cdot D^2+\ldots)$ where $\alpha_k > \alpha_{k\text{-intrinsic}}$ for $1 \le n \le N$. Extra SNR margin can be obtained by reducing FFE noise amplification. DFE taps are selected to cancel the new α_n and 1/(1+D) pre-coding is then applied to remove large DFE error propagation

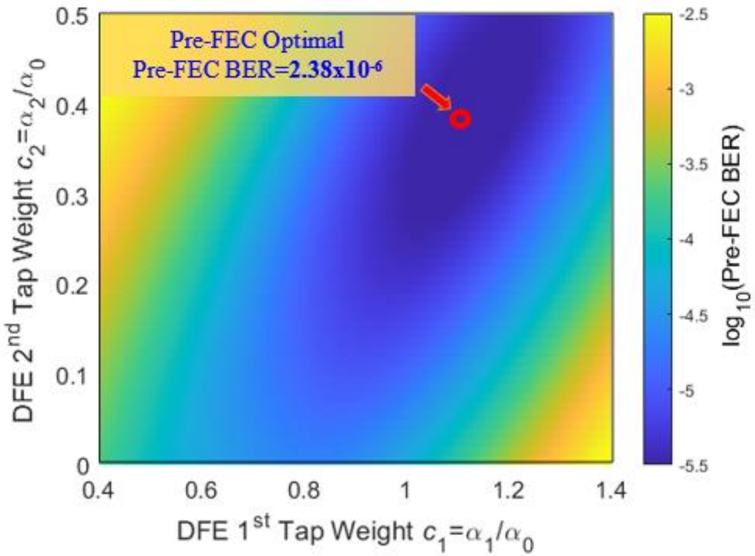
Simulation Results: 1-Tap DFE with 1/(1+D) Pre-Coding





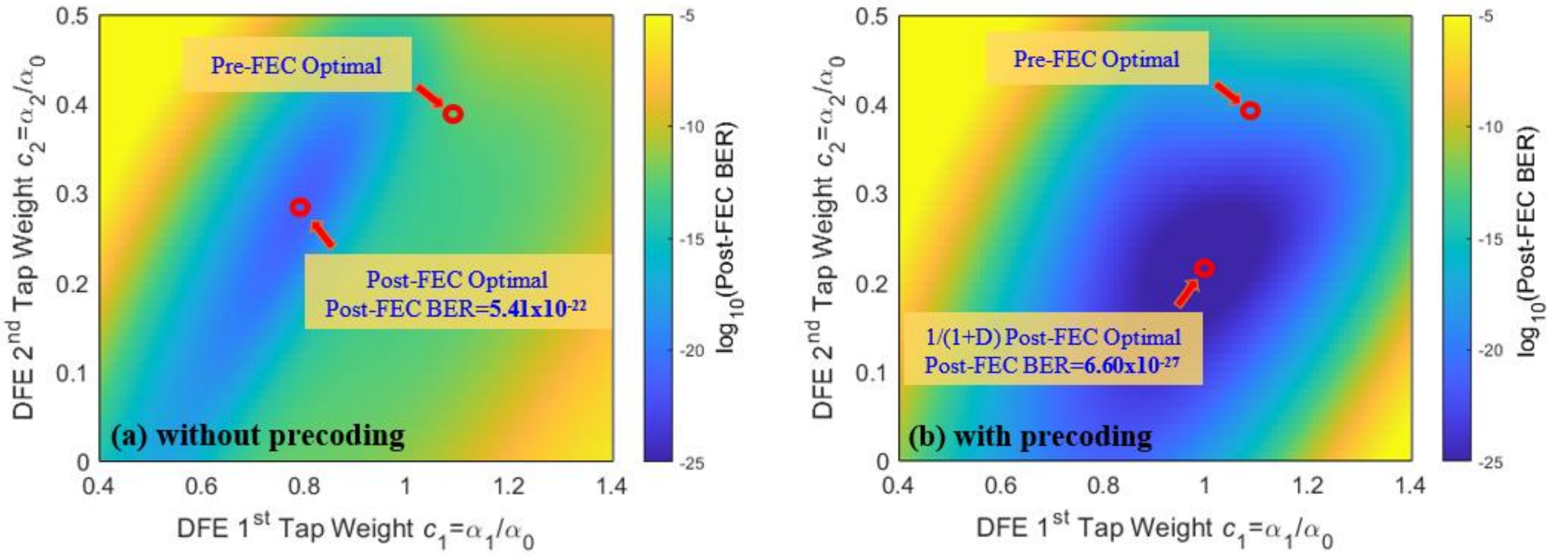
- Post-FEC BER of the previous 36dB channel case with and without 1/(1+D) pre-coding
- With pre-coding, both post-FEC and pre-FEC BER are minimized with the same equalizer coefficients

Simulation Results: 2-Tap DFE



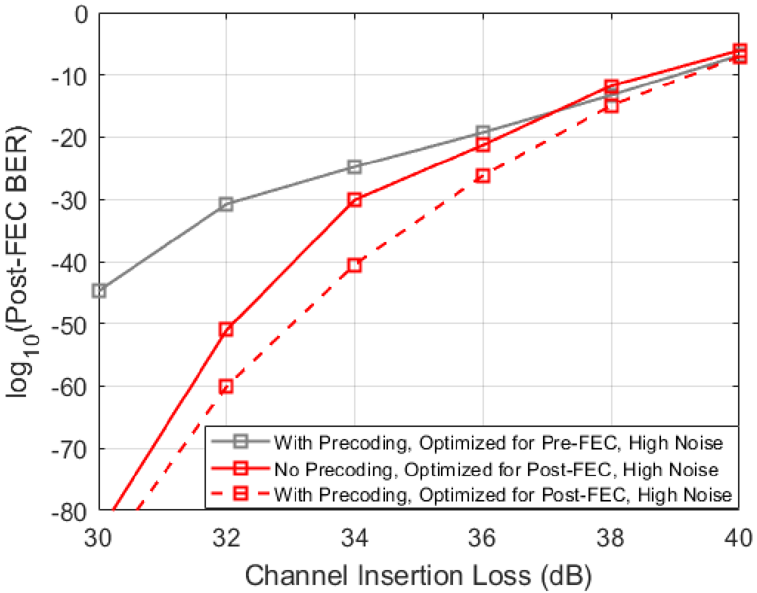
- Pre-FEC BER performance surface of the 36dB loss channel at 2.42 mV_{rms} noise level
- The 2-tap DFE affords the FFE post-cursor taps with one more degree of freedom to low-pass filtering the noise
  - significant BER improvement

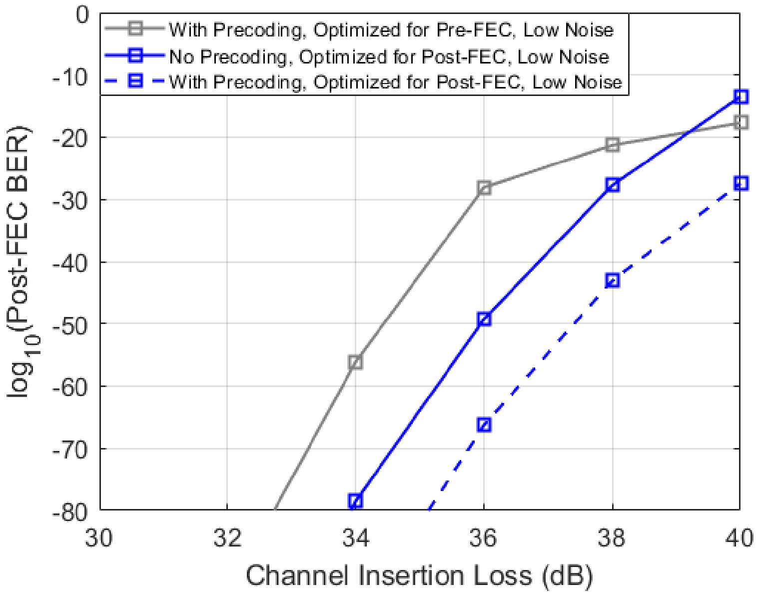
Simulation Results: 2-Tap DFE



- Vastly different optimal points identified on each performance surface

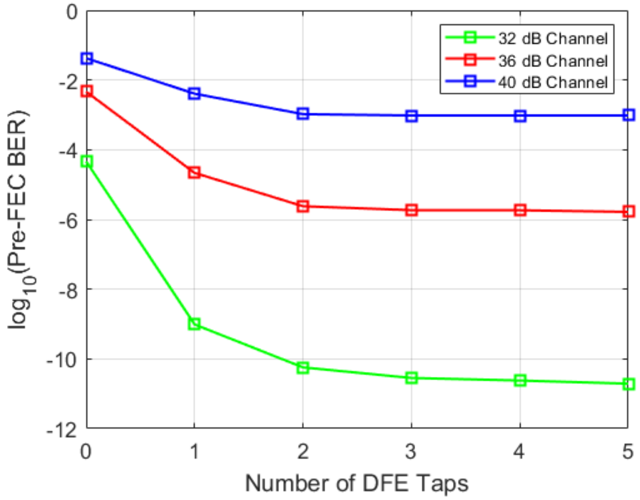
Simulation Results: 2-Tap DFE





- Contrary to the 1-tap DFE example, with precoding enabled the post-FEC BERs optimized for post-FEC is better than the post-FEC BERs optimized for pre-FEC
- The post-FEC BERs optimized for post-FEC with precoding are optimal

Summary

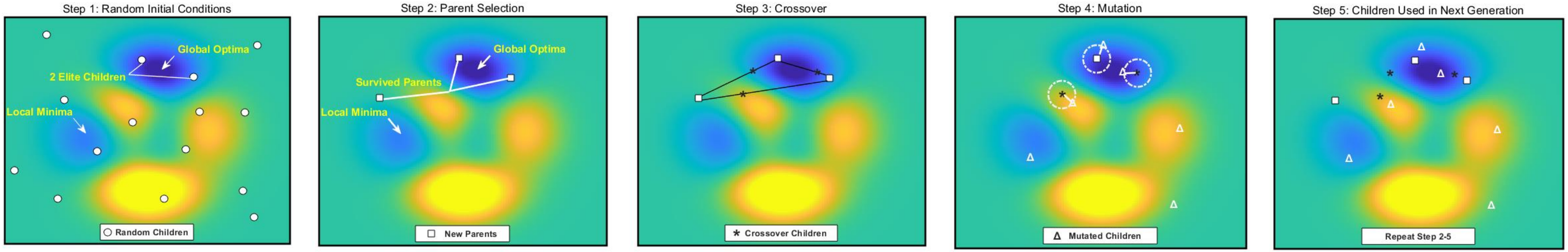


- Although *N* is typically limited to 1-2 due to the critical timing path in the DFE feedback loop, in this example near optimal results can be achieved using a 2-tap DFE
- Suggests that we should optimize for $1+\alpha_1 \cdot D+\alpha_2 \cdot D^2$ equalized pulse response in this example
- Only true if the post-cursor residual ISIs cancelled by the RX FFE are small

Outline

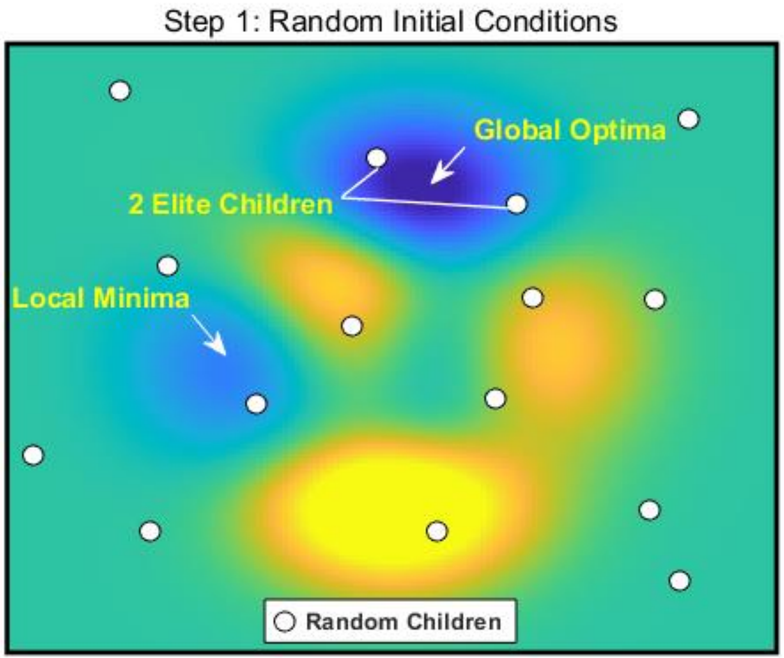
1. Motivation
2. Wireline Transceiver Model System Overview
   a. System Overview
   b. DFE Error Propagation
3. Pre-FEC and Post-FEC BER as Criteria for Optimizing Wireline Transceivers
   a. Pre-FEC vs Post-FEC BER Optimum
   b. Simulation Results: 1-Tap DFE
   c. Simulation Results: 2-Tap DFE
4. GA-Assisted Transceiver Optimization
   a. Genetic Algorithm Overview
   b. Optimization Framework
   c. Simulation Results
5. Conclusion

GA-Assisted Transceiver Global Optimization



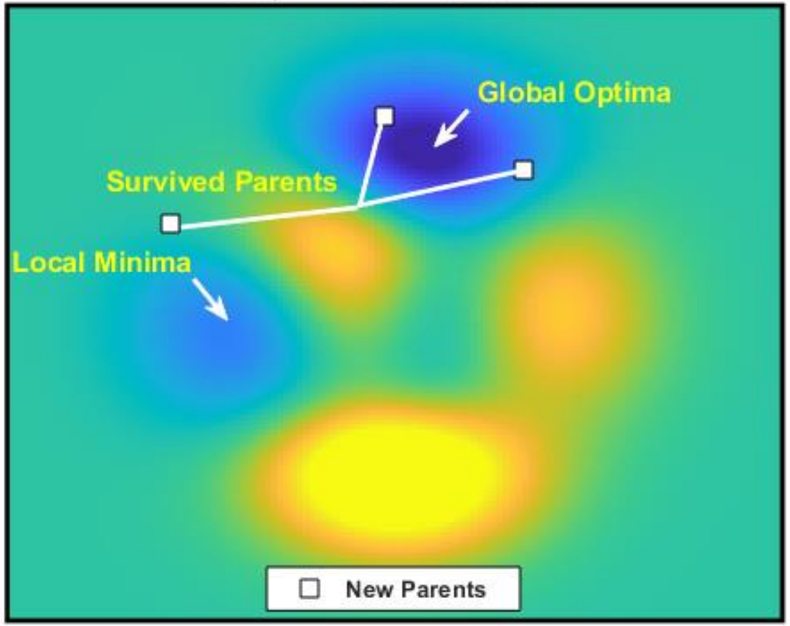
- Although LMS adaptation and other gradient-descent methods are commonly employed for optimizing FFE and DFE coefficients, they are ill-suited to CTLE optimization which has a non-unimodal performance surface
- The time required to accurately evaluate each CTLE setting through an exhaustive search grows exponentially as the number of CTLE control parameters increases
- A genetic algorithm (GA) is combined with the statistical model to obtain the best candidate settings for each transceiver block

Genetic Algorithm – Initial Condition Generation

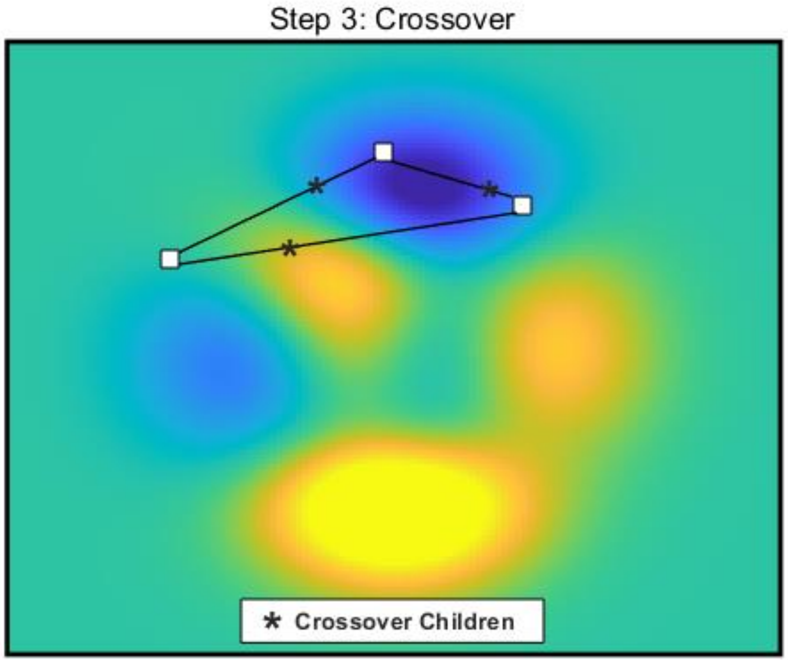


Genetic Algorithm – Parent Selection

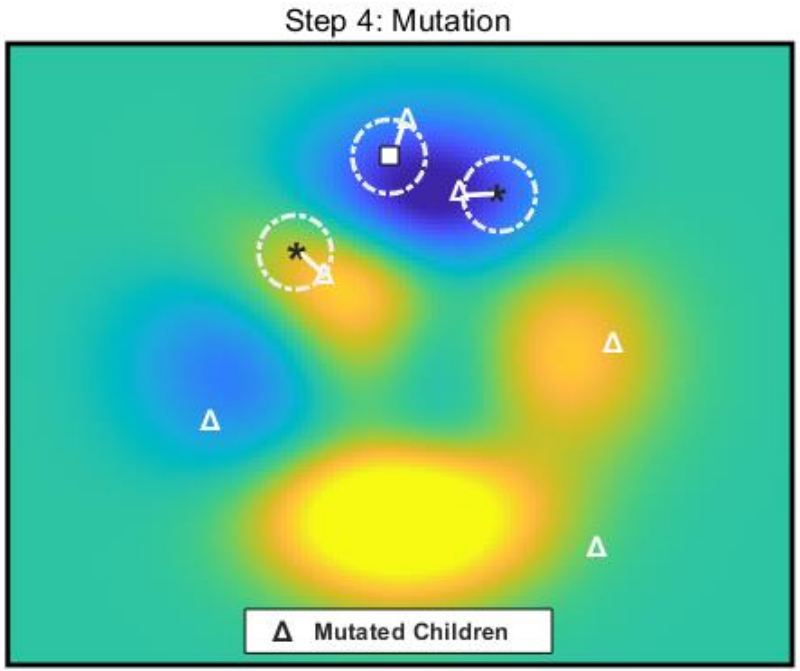
Step 2: Parent Selection



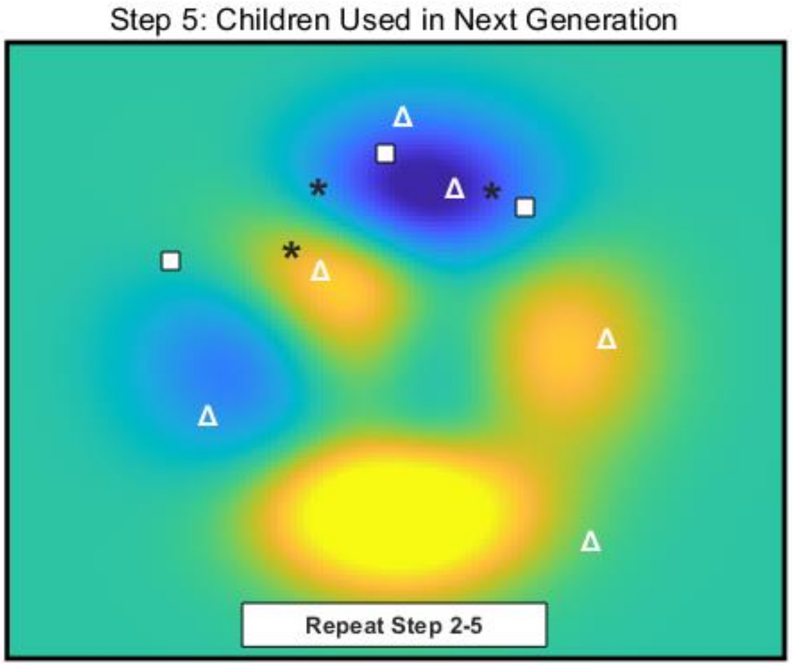
Genetic Algorithm – Crossover



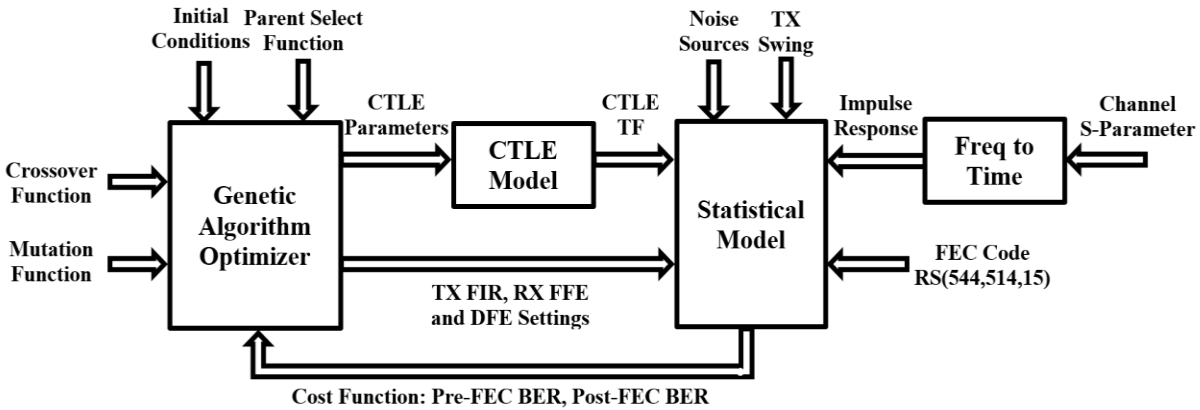
Genetic Algorithm – Mutation



Genetic Algorithm – Next Generation

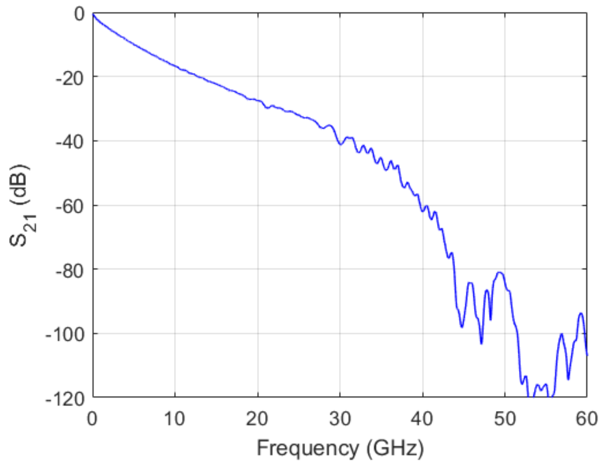


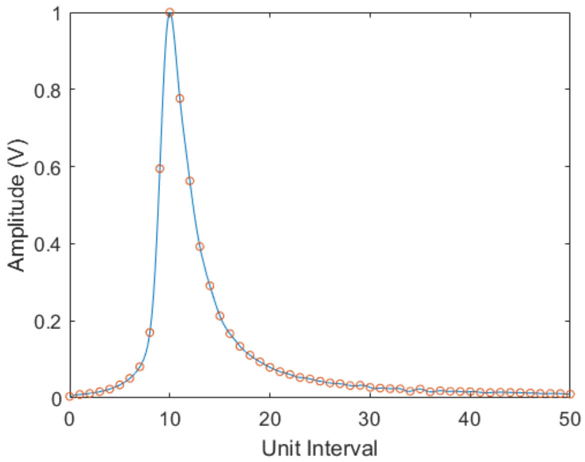
GA-Assisted Transceiver Global Optimization

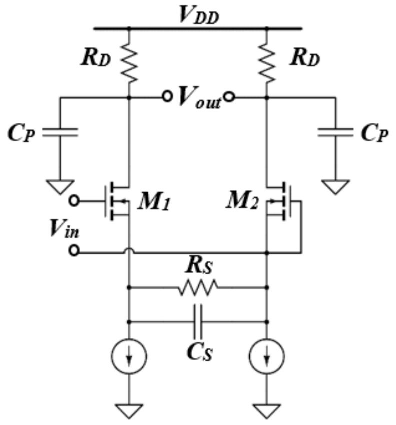


- The optimization framework shown in the diagram includes:
  - (1) a statistical model
  - (2) a genetic algorithm optimizer
- The FFE-DFE co-optimization method is employed by assuming the FFE equalized pulse response has taken the form $(1+\alpha_1 \cdot D+\alpha_2 \cdot D^2 +\ldots)$
  - (1) reduce search-space complexity and (2) achieve optimal noise filtering

Simulation Setup

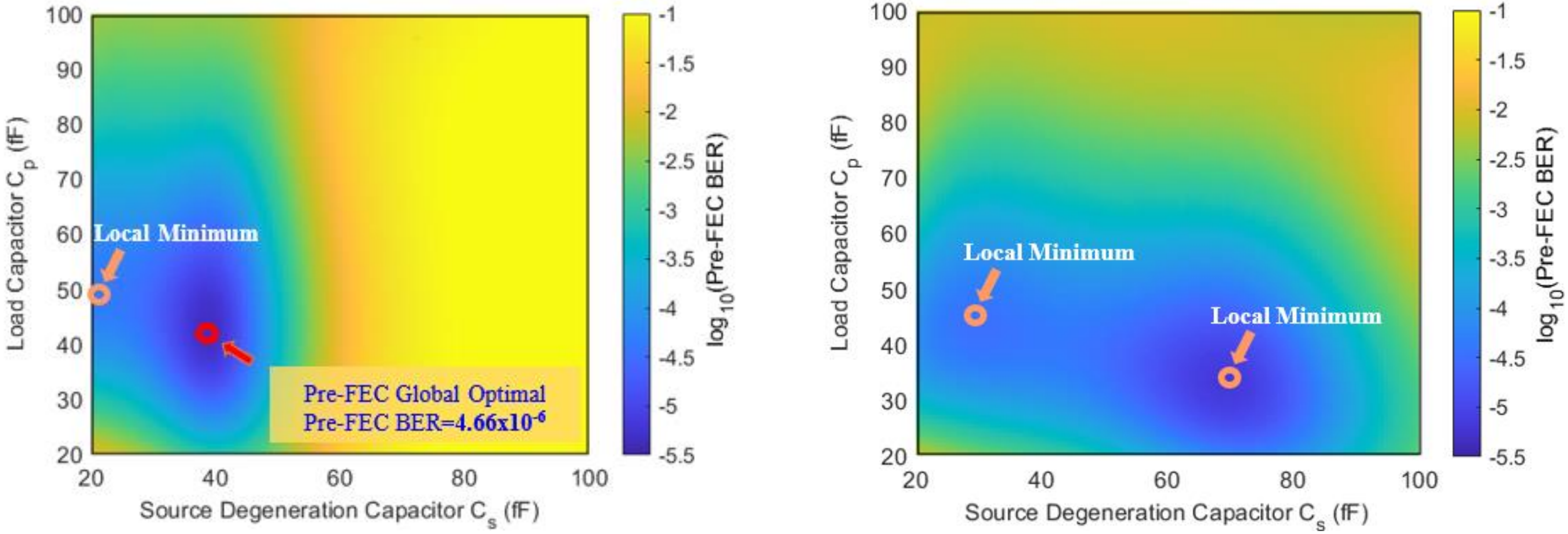






- A 14-inch orthogonal backplane channel from TE Connectivity [16] as the PHY channel model
  - Channel model has 35 dB insertion loss at 28 GHz
- A simple RC-degenerated differential pair reported in [17] is used as the reference CTLE design
  - A 5-bit digital control code is assigned to each CTLE component value

Non-Unimodal Performance Surface



- Pre-FEC BER surface plots are generated by sweeping C_s and C_P
- R_s and R_D set to global optimal (left) and suboptimal (right)

Simulation Results

Performance Metric	CTLE Settings				TX FIR		DFE		Pre-FEC BER	Post-FEC BER	
	R_s	C_s	R_D	C_p	β_{-1}	β_{-2}	c_1	c_2		No Pre-Coding	With Pre-Coding
Pre-FEC	18	8	6	10	-0.06	0.10	0.98	0.31	**4.66×10^{-6}**	7.12×10^{-15}	2.46×10^{-23}
Post-FEC	17	9	4	14	-0.06	0.10	0.69	0.22	1.44×10^{-5}	**5.44×10^{-24}**	2.95×10^{-22}
Pre-Coded Post-FEC	20	7	8	8	-0.06	0.10	0.92	0.21	5.42×10^{-6}	2.30×10^{-14}	**3.77×10^{-26}**

- Link communicates 4-PAM symbols at 56 GBaud/s subject to 1 $V_{P\text{-}P}$ swing at TX
- The transmitter has a 3-tap FIR filter equalizing only pre-cursor ISIs
- A 2-tap DFE and a 13-tap FFE with 1 pre-cursor and 11 post-cursor taps at RX
- GA is used to optimize 8 parameters
  - 4 CTLE component values, 2 TX FIR pre-cursor and 2 DFE tap weights

Outline

1. Motivation
2. Wireline Transceiver Model System Overview
   a. System Overview
   b. DFE Error Propagation
3. Pre-FEC and Post-FEC BER as Criteria for Optimizing Wireline Transceivers
   a. Pre-FEC vs Post-FEC BER Optimum
   b. Simulation Results: 1-Tap DFE
   c. Simulation Results: 2-Tap DFE
4. GA-Assisted Transceiver Optimization
   a. Genetic Algorithm Overview
   b. Optimization Framework
   c. Simulation Results
5. Conclusion

Conclusion

- Using SNR or pre-FEC BER as performance metrics may not be effective in minimizing post-FEC BER when architecting and optimizing wireline links
  - Links attain their minimum post-FEC BER with equalizer coefficients very different from those that minimize pre-FEC BER
  - The introduction of pre-coding mitigates the impact of error bursts, ensuring that both pre-FEC and post-FEC BER are minimized with the same equalizer coefficients for the 1-tap DFE example
  - Vastly different optimal equalizer settings with/without pre-coding for multi-tap DFE cases
- An optimization framework using Genetic Algorithm to find equalizer settings for minimum post-FEC BER on non-unimodal performance surfaces
  - 1+alpha·D type of partial responses are optimized by the GA to achieve optimal noise filtering and reduced search-space complexity

References

1. S. Kiran *et al*., "Modeling of ADC-Based Serial Link Receivers With Embedded and Digital Equalization," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 3, pp. 536-548, March 2019.
2. M. Yang, S. Shahramian, H. Shakiba, H. Wong, P. Krotnev and A. C. Carusone, "Statistical BER Analysis of Wireline Links With Non-Binary Linear Block Codes Subject to DFE Error Propagation," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 1, pp. 284-297, Jan. 2020, doi: 10.1109/TCSI.2019.2943569.
3. R. Narasimha, N. Warke and N. Shanbhag, "Impact of DFE error propagation on FEC-based high-speed I/O links," *GLOBECOM 2009 - 2009 IEEE Global Telecommunications Conference*, Honolulu, HI, 2009, pp. 1-6.
4. A. Szczepanek, I. Ganga, C. Liu, and M. Valliappan, "10GBASE-KR FEC tutorial," Website, http://www.ieee802.org.
5. *Transcoding/FEC Options and Trade-offs for 100 Gb/s Backplane and Copper Cable*, IEEE Standard 802.3bj, Nov. 2011.
6. *FEC Codes for 400 Gbps 802.3bs*, IEEE Standard 802.3bs, Nov. 2014.
7. X. Dong, G. Zhang and C. Huang, "Improved engineering analysis in FEC system gain for 56G PAM4 applications, "*DesignCon 2018*, Santa Clara, CA, 2018.
8. M. Yang, S. Shahramian, H. Shakiba, H. Wong, P. Krotnev and A. Carusone, "A Statistical Modeling Approach for FEC-Encoded High-Speed Wireline Links," *DesignCon 2020*, Santa Clara, CA, 2020.
9. K. Gopalakrishnan et al., "A 40/50/100Gb/s PAM-4 ethernet transceiver in 28nm CMOS," 2016 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2016, pp. 62-63.

References

10. A. Cevrero *et al*., "6.1 A 100Gb/s 1.1pJ/b PAM-4 RX with Dual-Mode 1-Tap PAM-4 / 3-Tap NRZ Speculative DFE in 14nm CMOS FinFET," *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2019, pp. 112-114, doi: 10.1109/ISSCC.2019.8662495.
11. M. Abdulrahman and D. D. Falconer, "Cyclostationary crosstalk suppression by decision feedback equalization on digital subscriber loops,", *IEEE J. Selected Areas Commun.*, vol. 10, no. 3, pp. 640–649, Apr. 1992.
12. Sheng Chen, L. Hanzo and B. Mulgrew, "Adaptive minimum symbol-error-rate decision feedback equalization for multilevel pulse-amplitude modulation," in *IEEE Transactions on Signal Processing*, vol. 52, no. 7, pp. 2092-2101, July 2004, doi: 10.1109/TSP.2004.828944.
13. Chen-Chu Yeh and J. R. Barry, "Adaptive minimum bit-error rate equalization for binary signaling," in *IEEE Transactions on Communications*, vol. 48, no. 7, pp. 1226-1235, July 2000, doi: 10.1109/26.855530.
14. S. Shahramian *et al*., "30.5 A 1.41pJ/b 56Gb/s PAM-4 Wireline Receiver Employing Enhanced Pattern Utilization CDR and Genetic Adaptation Algorithms in 7nm CMOS," *2019 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2019, pp. 482-484, doi: 10.1109/ISSCC.2019.8662421.
15. Bäck, Thomas, *Evolutionary Algorithms in Theory and Practice* (1996), Oxford Univ. Press.
16. N. Tracy, and A. Pachon, "Channel Simulations for 112G Backplane Analysis," Website, https://www.ieee802.org/3/ck/public/tools/.
17. S. Gondi and B. Razavi, "Equalization and Clock and Data Recovery Techniques for 10-Gb/s CMOS Serial-Link Receivers," in *IEEE Journal of Solid-State Circuits*, vol. 42, no. 9, pp. 1999-2011, Sept. 2007, doi: 10.1109/JSSC.2007.903076.

Thank you!

QUESTIONS?