A 1-Tap 40-Gb/s Look-Ahead Decision Feedback Equalizer in 0.18-μm SiGe BiCMOS Technology

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***Abstract*—This paper describes a fully differential 1-tap decision feedback equalizer in 0.18-μm SiGe BiCMOS technology. The circuit is capable of equalizing NRZ data up to 40 Gb/s. A look-ahead architecture is employed with modifications to reduce complexity in the high-speed clock distribution. An analog differential voltage controls the tap weights. The design is fabricated in 0.18-μm SiGe BiCMOS technology with a 160-GHz f_T. It occupies an area of 1.5 mm $\times$ 1 mm and operates from a 3.3-V supply with 230-mA current. It is the first feedback equalizer at 40 Gb/s.**

***Index Terms*—40 Gb/s, decision feedback equalizer, SiGe BiCMOS.**

I. Introduction

As THE DEMAND for bandwidth continues to grow, it is only a matter of time before OC-768 systems will be commonplace. The prolonged slowdown of the fiber optic market has allowed researchers to evaluate possible impairments limiting these high data rate systems. One such impairment in long-haul single-mode fiber systems is polarization-mode dispersion (PMD) [1]. Dispersion compensation of such systems is necessary to extend the range of communication and will usher in the widespread industrial adoption of OC-768.

Asymmetries along a fiber optic channel lead to an input pulse being split into pulses with different polarizations. To a first-order approximation, the impulse response of a PMD-limited channel is

$$h_{\mathrm{pmd}}(t) = \gamma\delta(t) + (1-\gamma)\delta(t-\Delta\tau) \tag{1}$$

where $\Delta\tau$ is the differential group delay (DGD) between the two modal pulses and γ is the proportional power split. The corresponding frequency response is

$$H_{\mathrm{pmd}}(f) = \gamma + (1-\gamma)e^{-j2\pi f\Delta\tau}. \tag{2}$$

The nonlinearities that occur when converting between the electrical and optical domains play an insignificant role in the overall channel response and are therefore ignored. Depending on the DGD and the proportional power split, the frequency response of the channel changes as seen in Fig. 1 for various values of γ. Deep nulls occur in the frequency response when the power is split evenly between the two pulses, making equalization considerably more difficult.

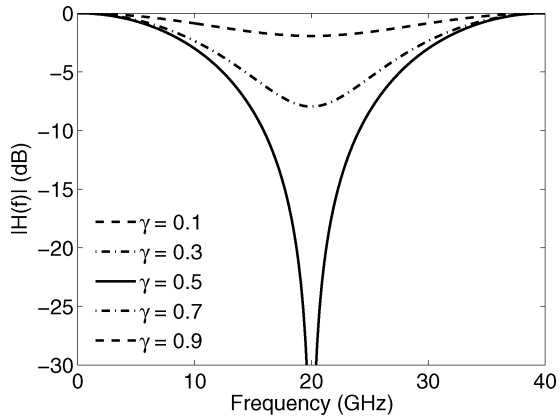

Fig. 1. Frequency response of PMD with varying γ and $\Delta\tau$ equal to one bit period (e.g., $\Delta\tau = 25$ ps at 40 Gb/s) [[2]].

Even though PMD compensation can be provided by both optical and electrical means, compelling arguments in [1] and [2] push towards an electrical solution involving a mixed-signal adaptive equalizer. Adaptive equalization is attractive since it allows for a higher level of system integration as well as the ability to adapt to the varying frequency response of a PMD-limited system.

A linear adaptive feedforward equalizer (FFE) is effective at compensating for a variety of dispersive channels and, if enough taps are provided, to correct for a large number of precursor and post-cursor inter-symbol interference (ISI) terms. The disadvantage of such a linear filter is that it is unable to equalize large signal losses, such as the deep nulls in a PMD channel. Electrical equalization of the deep nulls can be achieved with a decision feedback equalizer (DFE) due to its nonlinear nature. A DFE does not amplify the channel noise since it outputs a digital decision instead of an analog voltage. For most practical systems, a DFE is often paired with an FFE to correct for a variety of channels. A partial system-level view of the equalizer is presented in Fig. 2.

Previous work in [2] demonstrates that a 3-tap FFE paired with a 1-tap feedback equalizer (FBE) is sufficient to mitigate practical PMD-limited systems. More recently, the implementation of the FFE has been described in [3] and [4] at 40 Gb/s. This work focuses on the design of the 1-tap DFE.

Recent publications have reported operation of DFEs up to 10 Gb/s in both CMOS and SiGe BiCMOS technology [5]–[7].

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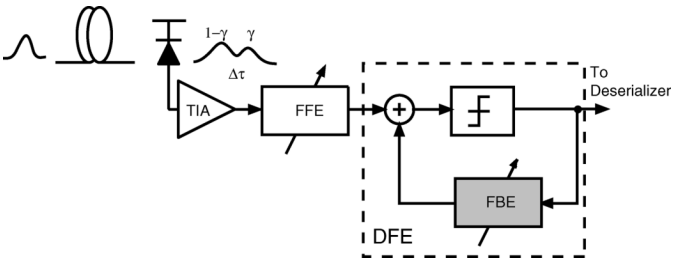


Fig. 2. System-level view of PMD equalization.

The fastest nonlinear equalizer to date is implemented in III-V technology at 40 Gb/s and utilizes a modified feedforward architecture with two delay paths having a delay difference of 1 unit interval [8]. The nonlinear architecture does not provide feedback prior to making a decision and therefore it is not suitable for PMD mitigation.

This work presents the first 40-Gb/s DFE [9]. It uses a well-known, proven full-rate look-ahead architecture originally proposed in [10]. A half-rate architecture was not implemented since a single-tap DFE is required and the additional loading on the analog front-end and clock overhead would have increased the DFE area and power consumption. The chip is fabricated in a BiCMOS technology, which allows for integration of adaptation algorithms on chip. The scope of the project, however, involves the implementation of the high-speed path and does not address the adaptation or clock recovery issues [7].

The following sections highlight the circuit design of the feedback equalizer and implementation issues, followed by the measurement results and verification performed at 40 Gb/s.

II. Architecture

There are two popular architectures for the implementation of a multi-Gb/s DFE: the direct feedback equalizer and the look-ahead architecture.

The direct feedback equalizer is the conventional approach to implementing the feedback equalizer (Fig. 3). The filter processing is performed in the feedback path and added at the summing node. The architecture allows for multiple taps to be added as shown in Fig. 3 by including the dotted components. From a system viewpoint, the clock and data recovery for the direct feedback equalizer would require similar circuitry to conventional clock and data recovery (CDR) circuits [7]. The major drawback, however, involves the timing bottleneck of the feedback path, which must have a delay of less than one bit period. Additional taps also cause significant loading at the high-speed node, limiting the performance of the circuit. Implementation of a direct feedback equalizer at 40 Gb/s is nontrivial even with 160-GHz transistors.

An alternate architecture uses a look-ahead topology [10] to achieve higher data rates. As seen in Fig. 4, parallelism is employed to remove processing from the feedback path, thereby relaxing the timing constraints. One path makes a tentative decision assuming the previous bit was a 1, while the other path assumes that the previous bit was a 0. The correct result is then selected and the other decision is discarded via the decision selective feedback (DSF) loop. As well as relaxing the timing constraint within the feedback path, this architecture eliminates

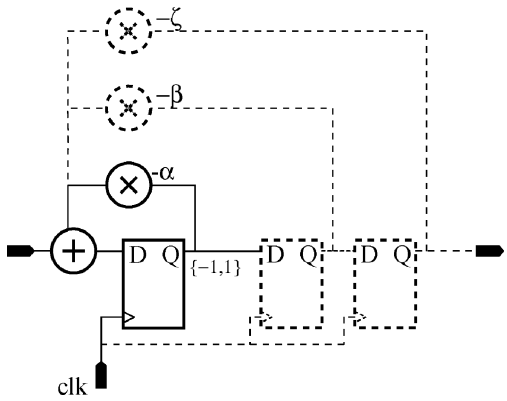


Fig. 3. Direct feedback equalizer architecture for single tap (solid) and multiple taps (dashed).

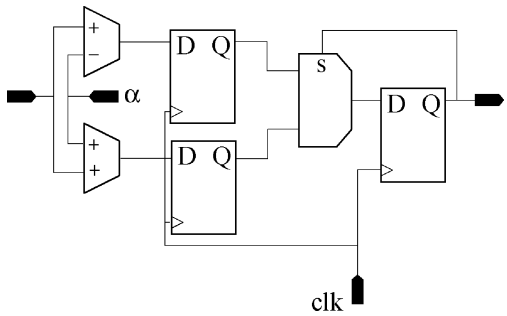


Fig. 4. One-tap look-ahead feedback equalizer architecture.

the large summing node for multiple tap designs, allowing for high-speed operation [11]. The look-ahead architecture, however, increases the hardware requirements and may complicate other blocks such as the clock recovery [12], resulting in an overall increase in area and power consumption.

For PMD compensation, the DFE only requires a single tap operating at 40 Gb/s [2], therefore, a look-ahead architecture is employed. The architecture, however, is different from the conventional high-speed implementation discussed in [10] since the retiming of the selector inputs has been replaced with slicers to remove considerable complexity in the clock path, clock skew management, and to reduce the overall power. A block-level view of the chip is shown in Fig. 5. It is estimated from simulations that a power savings of 278 mW is achieved by eliminating the retimers at the input to the selector and the associated clock network. This modification has little effect on the overall functional performance of the DFE.

III. Circuit Design

The block diagram of the implemented DFE is shown in Fig. 5 and is described next. Although all circuits are fully differential, the single-ended block diagram is shown for simplicity. The input is fed into the broadband front-end which features two stages: 1) the shunt–shunt feedback amplifier with local emitter degeneration and 2) a slicing threshold adjustment block which controls the differential DC offset of the output via the tap weight voltage α. The latter has two parallel paths and effectively changes the slicing threshold into the three cascaded emitter-coupled logic (ECL) inverters that limit the signal. Each

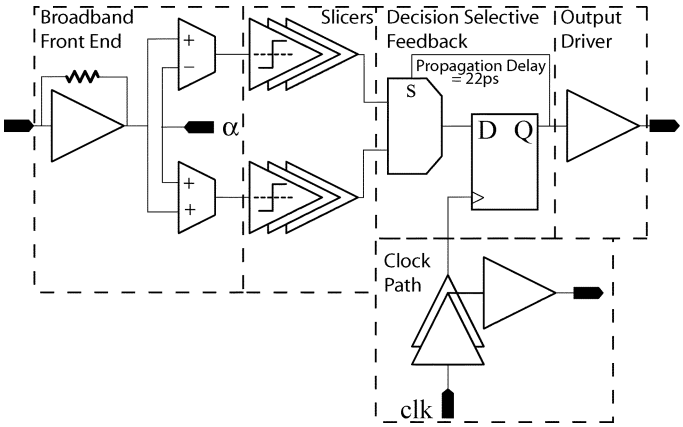


Fig. 5. Look-ahead DFE chip block level architecture.

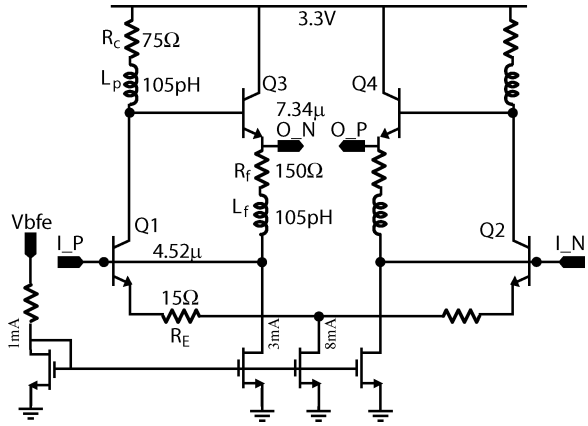


Fig. 6. Schematic of input shunt feedback (TIA) stage.

path acts as an equalizer to cancel one bit period of post-cursor ISI. The slicer output feeds into the decision selective feedback, which selects one of the paths based on the previous decision of the flip-flop. The feedback path from the clock input of the flip-flop to the data input of the flip-flop must have a delay which is smaller than one bit period. A 50-Ω output buffer with variable swing follows the flip-flop. The clock distribution network features two stages of E^2CL inverters and the clock signal is also made available externally for testing purposes.

A. Broadband Front-End

The broadband front-end is important in dictating the overall system performance of the DFE.

1) Shunt–Shunt Feedback Input Low-Noise Amplifier: The shunt–shunt feedback amplifier with emitter degeneration is used as a low-noise input voltage preamplifier. This circuit has the same topology as a transimpedance amplifier (TIA) and will therefore be referred to as a TIA. The TIA can be designed to provide simultaneous input and noise matching without limiting the circuit bandwidth [13]. Historically, a current mode logic (CML) inverter or ECL inverter stage is used as an input preamplifier with a 50-Ω on-chip resistor for input impedance matching purposes. This, however, causes degradation in the noise figure (sensitivity) of the system and limits the system bandwidth since large devices are required to provide the input noise matching. The use of the shunt feedback simultaneously decreases the optimum noise impedance $Z_{\rm sopt}$ and input impedance $Z_{\rm in}$, such that the concomitant noise and impedance matching can be achieved with a smaller bias current and device size than would be possible with other topologies [14].

The schematic of the implemented TIA is presented in Fig. 6. The design of the TIA is conducted using the methodology outlined in [14]. Resistively degenerated input transistors ($Q_{1,2}$) are biased at the optimum collector current density for low-noise operation ($J_{\rm minNF}$) at a frequency of 36 GHz. It is important to note that the optimum noise current density of a resistively degenerated transistor is different than the optimum noise current density of the transistor itself. The bias current, collector resistance R_C, and the emitter degeneration resistance R_E are used to set the loop gain using (3) and the output voltage swing of the TIA:

$$A_v = \frac{g_{m1,2}R_C}{1 + g_{m1,2}R_E}. \tag{3}$$

The output voltage swing is a product of the bias current and R_C and is set to 600 mV to maximize the input dynamic range. The loop gain determines the feedback resistor R_F required for input impedance matching from

$$R_{\rm in} = \frac{R_F}{1 + A_v} \tag{4}$$

where $R_{\rm in}$ is 50 Ω. R_F also provides a DC common-mode voltage drop to lower the base voltage of $Q_{1,2}$. This ensures that the output voltage swing is not limited by the collector-emitter voltage, V_{CE}, of $Q_{1,2}$ and thus avoids driving the transistor into saturation. Transistors $Q_{1,2}$ are sized to provide good noise matching to the 50-Ω source. The peaking L_P and feedback inductor L_F are added to increase the bandwidth. The feedback inductor also filters off the high-frequency noise caused by R_F [13].

2) Slicing Threshold Adjustment Buffer: The slicing threshold adjustment buffer is the physical implementation of the filter coefficients of the equalizer. The control voltage introduces a DC offset at the outputs, thereby shifting the slicing threshold of the following stages. One threshold adjustment buffer strengthens the transitions from 1 to 0 and the other strengthens the transitions from 0 to 1, in order to avoid missed bits due to ISI. The schematic of this block is illustrated in Fig. 7. It consists of an emitter-degenerated high-speed SiGe HBT inverter. The DC offset control of the outputs $O_{\rm P/N}$, is implemented with a MOS-HBT cascode ($Q_{3,4,5,6}$) whose differential input voltage controls the value of α.

The high-speed buffer is biased at peak f_T current density for maximum bandwidth and is degenerated to increase its linearity. Shunt peaking inductors are employed to further improve the bandwidth without increasing the power consumption. The high-speed outputs $O_{\rm P/N}$ are connected to the BiCMOS cascode pair which controls the differential offset current into the load resistors. The MOSFETs are buffered from the high-speed path by common-base HBTs ($Q_{3,4}$). SiGe HBT devices are used for this purpose because they provide lower collector-substrate capacitances than the MOFSET drain-bulk

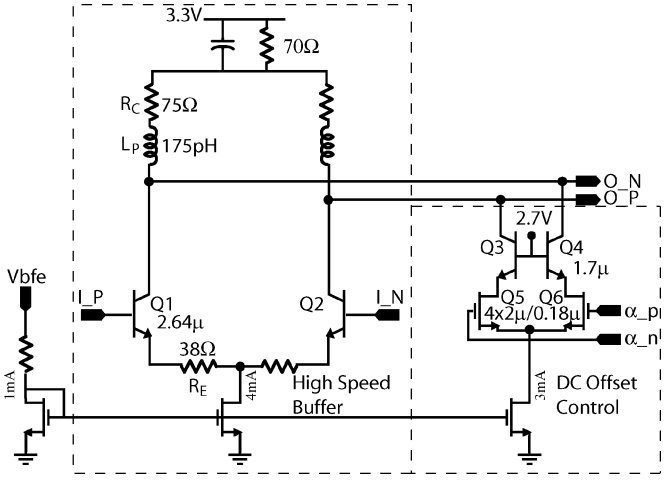


Fig. 7. Schematic of slicing threshold adjustment circuit for ISI cancellation.

capacitances. As well, the MOS-HBT cascode devices provide a wider linear range of the tap control voltage, due to their high output resistance and the constant V_{DS} which is maintained on $Q_{5/6}$, even for large changes in the DC offset voltages. The MOSFETs are employed for the differential pair $Q_{5,6}$ to further increase the linear tuning range of the α control voltage. Deep-submicron MOSFETs exhibit very linear transfer characteristics at gate voltages exceeding 0.65 V, making them the ideal linear device. When changing the gate voltage of the 180-nm MOSFETs between 0.65 V and 1.2 V, their transconductance remains practically constant. The DC offset block can adjust the slicing threshold by 225 $\mathrm{mV_{pp}}$.

B. Decision Selective Feedback

The DSF comprises a selector and a master–slave flip-flop (MS-FF). Schematics of the ECL implementation of these building blocks are presented in Fig. 8. Device sizes and bias conditions are chosen based on the criteria set in [15] for maximum high-speed operations. The output nodes of the slave latch of the MS-FF, prior to the emitter followers, are routed in the feedback path and connected to the selector inputs $\mathrm{Sel_{P/N}}$, as shown in Fig. 8(b). This lowers the fanout of the slave latch and adds the interconnect capacitance where it can be compensated for with shunt peaking. Bias currents in the selector and quads are set to the same value to maintain a fanout of one along the feedback path.

The critical path of the DSF is from the clock inputs, through the selector, and back to the data inputs of the MS-FF. The delay through this path sets the maximum data rate of the DFE, including the MS-FF setup time, and must be less than one bit period, i.e., 25 ps for 40-Gb/s applications.

The derivation of propagation delays of high-speed CML/ECL cells is extensively covered in [16] and [17]. These references provide methods to accurately estimate the propagation delay of the high-speed cells, however, the expressions are lengthy and difficult to use. To first order, the delay is dominated by the quad stage rather than the emitter-followers of the ECL latch and selector. Therefore, minimizing the delay through the quad is critical in the design of the feedback path.

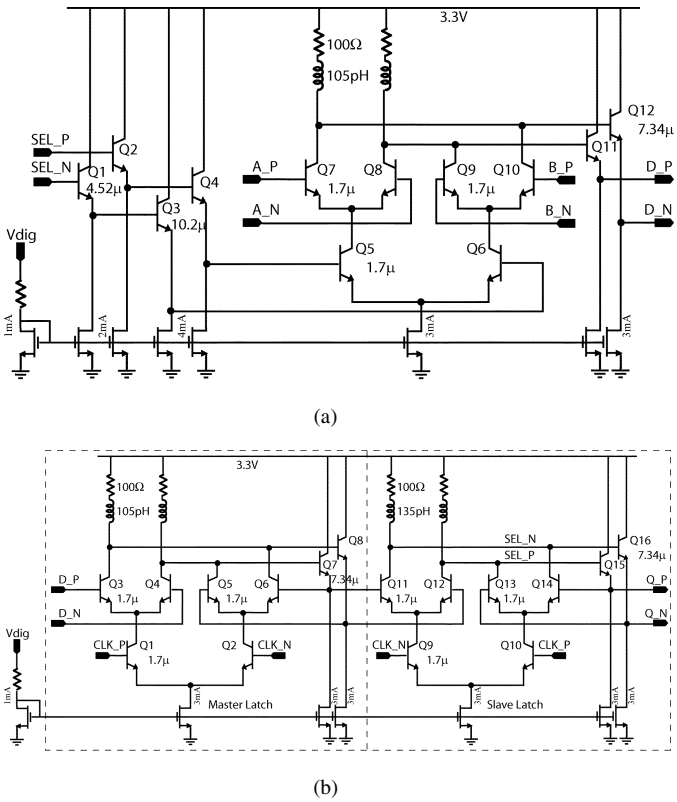


Fig. 8. ECL schematic. (a) Selector. (b) MS-FF.

The delay through the transistors of the selector and MS-FF quad is a strong function of the collector current density and can be minimized by biasing them at the peak-f_T collector current density J_{peakft} [15]. The effect of the interconnect capacitance on the overall propagation delay is decreased via layout and bias current. Using the top metal, the feedback path can be routed without adding significant parasitic capacitance at the output node. The tail current of the quad is set to 3 mA so as to not be slew-rate limited. Lastly, the voltage swing can be decreased for the same tail current to minimize the propagation time. There is a limit to how small the voltage swing can be made while still providing functionality. From [17], the minimum voltage swing required to switch the following differential pair is

$$\Delta V \geq 6V_t + I_C R_e \tag{5}$$

where $V_t = kT/q$ and R_e is the parasitic emitter resistance. To cover process and temperature variations as well as the DC voltage drop across R_e which exceeds 25 mV, the voltage swing is typically set larger than 200 $\mathrm{mV_{pp}}$ per side. The output logic swing here is set to 300 $\mathrm{mV_{pp}}$ to provide enough noise margin for the following ECL stages. The use of peaking inductors further decreases the propagation delay [18].

From simulations, the propagation delay through the critical path is 21 ps, without including the feedback interconnect. Using ASITIC, the feedback interconnect is modeled and found to have a distributed total inductance of 150 pH and capacitance of 15 fF. The interconnect model increases the propagation delay to 22 ps.

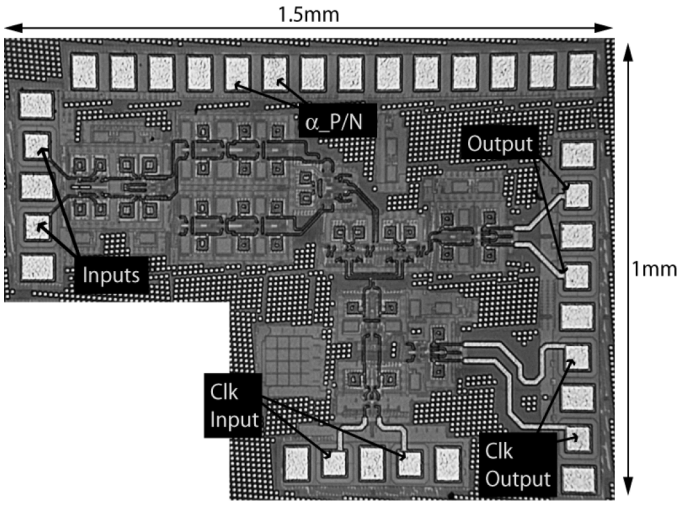
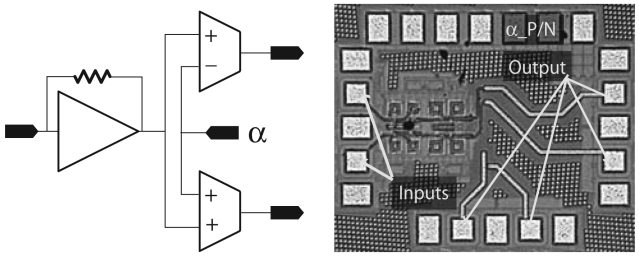


Fig. 9. DFE fabricated in Jazz Semiconductors' SBC18hx 0.18-μm SiGe BiCMOS technology with a 160-GHz f_T operating from a 3.3-V supply with 230-mA current.



(a) (b)

Fig. 10. Broadband front-end. (a) Block-level-schematic. (b) Die photo of breakout.

IV. Fabrication and Measured Results

The chip (Fig. 9) was fabricated in Jazz Semiconductor's SBC18HX 0.18-μm SiGe BiCMOS technology with an f_T of 160 GHz. The layout corresponds to the chip architecture in Fig. 5. It occupies an area of 1.5 mm $\times$ 1 mm and operates from a 3.3-V supply with 230-mA current. A breakout of the broadband front-end, including the TIA and slicing threshold adjustment circuit indicated in Fig. 10, was also fabricated to characterize the linear portion of the circuit.

The single-ended S-parameter measurements were performed using a Wiltron 360B VNA. One side of the differential inputs and outputs was connected to the network analyzer while the other side was terminated with 50 Ω. Measurements show the single-ended return loss [Fig. 11(a)] of all the high-speed ports of the DFE to be lower than -10 dB up to 50 GHz. Single-ended S-parameter measurements of the front-end breakout, through the TIA and one of the threshold adjustment circuits with the other outputs terminated, demonstrate a 3-dB bandwidth of 45 GHz up to the slicers. Since the measurements are single-ended, the actual gain is 6 dB higher than that presented in Fig. 11(b).

The 1-dB compression point ($P_{1\mathrm{dB}}$) was measured for the TIA and threshold circuit breakout to determine the maximum linear input power that can be applied. The measurement results

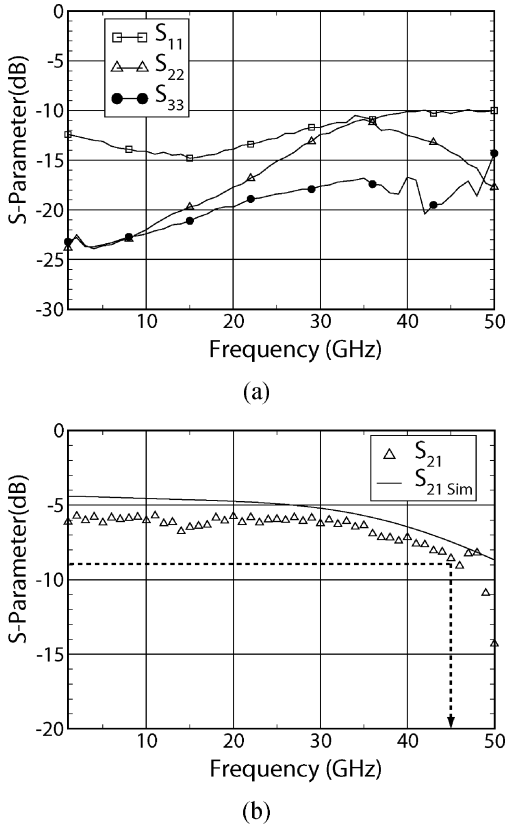


Fig. 11. (a) DFE return loss for the input (S_{11}), output (S_{22}), and clock input (S_{33}), and (b) measurements and simulation of S_{21} for front-end breakout.

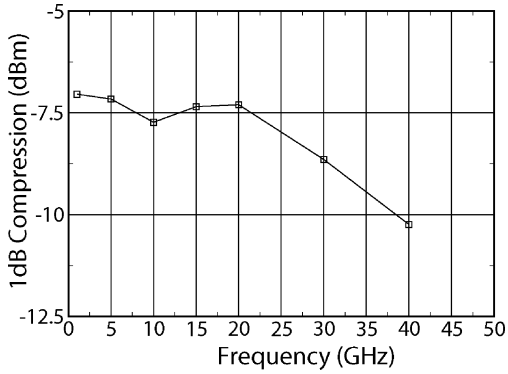


Fig. 12. Measured $P_{1\mathrm{dB}}$ over frequency.

up to 40 GHz can be seen in Fig. 12. The $P_{1\mathrm{dB}}$ is -7 dBm corresponding to a single-ended input of 135 $\mathrm{mV_{pp}}$. The measured DC offset voltage at the outputs of the threshold circuit is reproduced in Fig. 13 as a function of the DC control signal α. It is large enough to ensure ISI cancellation for all linear input amplitudes.

In the absence of a 40-Gb/s bit error tester (BERT) through an optical system, three large signal equalization tests were completed to verify functionality. The first measurement involved a bit error test performed through a PMD-emulating board at 5 Gb/s. The second measurement involved a bit error test performed through a 20-ft SMA cable at 10 Gb/s. Lastly, the third measurement involved equalization through a 9-ft SMA cable at

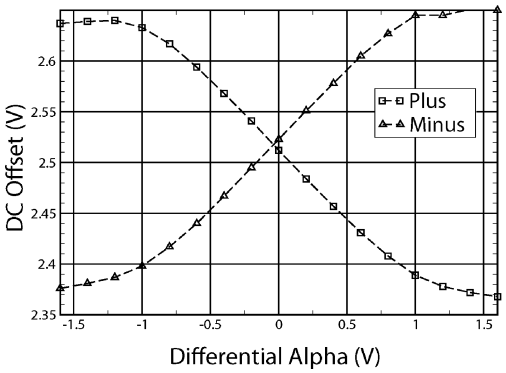


Fig. 13. Measured output offset voltage versus the differential DC control voltage for ISI cancellation.

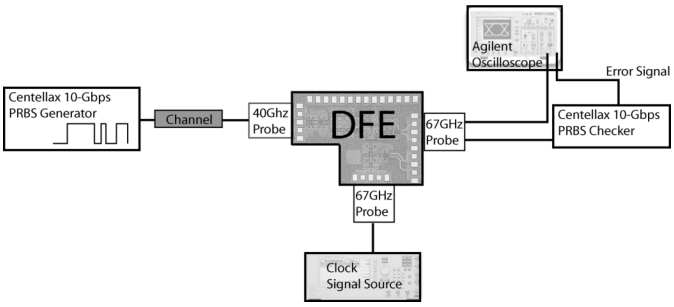


Fig. 14. BERT Measurement schematic setup.

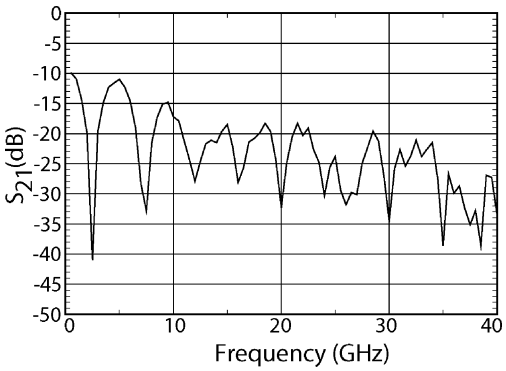


Fig. 15. PMD-Emulating board measured frequency response.

40 Gb/s with pattern waveform capture and hand error checking using the Agilent 8600C oscilloscope.

The measurement setup of the BERT is schematically represented in Fig. 14. The BERT runs off a single clock source, where one OTB3P1A Centellax 10-Gb/s board is configured as a $2^{31}-1$ pseudorandom bit sequence (PRBS) generator and the other is connected as a PRBS error checker. The PRBS data is either passed through a dispersive channel consisting of a PMD-emulating board, or through a 20-ft SMA cable, into the equalizer. One of the equalizer outputs is displayed on the oscilloscope and the other is connected to the error checker. The error trigger on the checker is also connected into the other remote head of the oscilloscope. A transition on the error trigger (ch. 4) indicates a bit error.

The PMD-emulating board reproduces an optical PMD limited channel with a γ of 0.5 and $\Delta\tau$ of 200 ps. The frequency

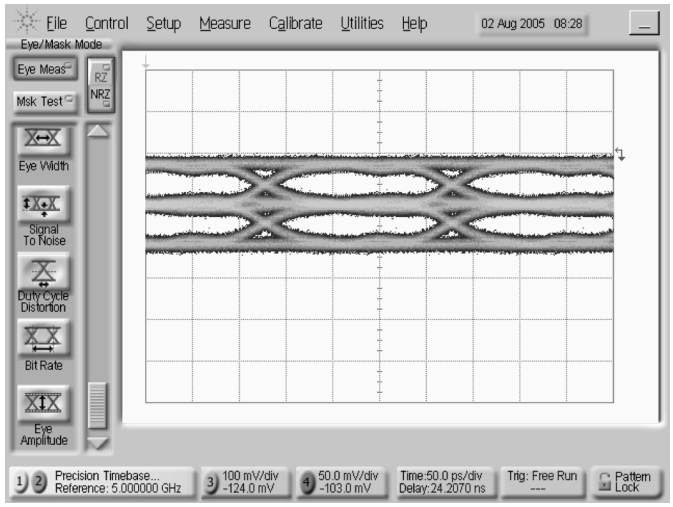


Fig. 16. Input eye diagram through the PMD board at 5 Gb/s.

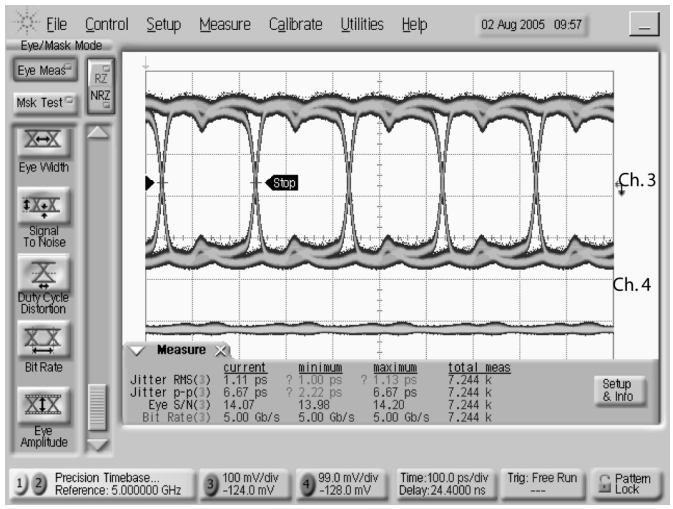


Fig. 17. Equalized output eye diagram through the PMD board at 5 Gb/s.

response of the channel (Fig. 15) shows a 30-dB null at 2.5 GHz. This measurement illustrates the DFE's ability to equalize deep nulls within the frequency spectrum similar to those seen in a PMD-limited channel. Fig. 16 shows the resulting eye diagram for a $2^{31}-1$ PRBS pattern at 5 Gb/s passed through this channel. The equalized single-ended output eye diagram, with an α of 0.2, is illustrated in Fig. 17. Fig. 17 shows no transition on the trigger, indicating error-free operation corresponds to a bit error rate (BER) lower than 10^{-12}. The 5-Gb/s single-ended output eye has a low peak-to-peak jitter of 6.7 ps, a signal-to-noise ratio (SNR) of 14, and a voltage swing of 2×340 $\mathrm{mV_{pp}}$.

The frequency response of the 20-ft multi-segment SMA cable, comprised of nine shorter SMA cables connected in series, is depicted in Fig. 18. It exhibits a linear (in dB) decrease versus frequency with 16 dB attenuation at 5 GHz. The input eye diagram at the input of the equalizer, after passing through the 20-ft cable, is shown in Fig. 19 for a $2^{31}-1$ PRBS sequence at 10 Gb/s. The equalized single-ended output eye diagram, with an α of 0.3, is presented in Fig. 20. No transition on the error trigger is seen for over 4K measurements (20 minutes), indicating fewer than 10^{-12} errors at 10 Gb/s. A peak-to-peak

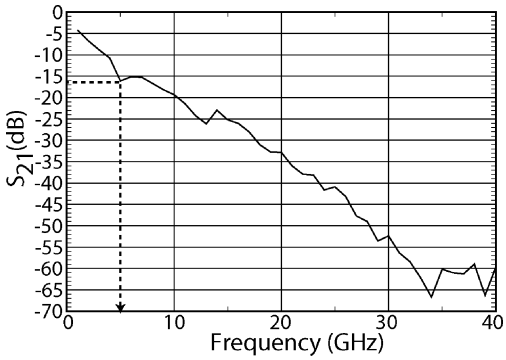


Fig. 18. 20-ft SMA cable measured frequency response.

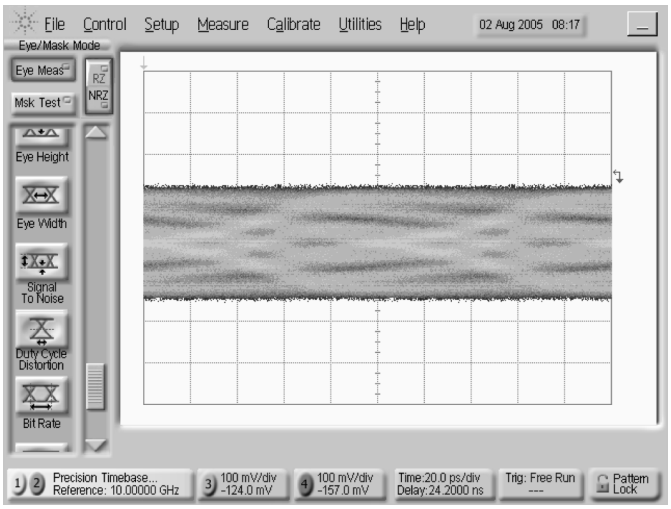


Fig. 19. Input eye diagram of a 10-Gb/s $2^{31}-1$ PRBS sequence through 20-ft SMA cable.

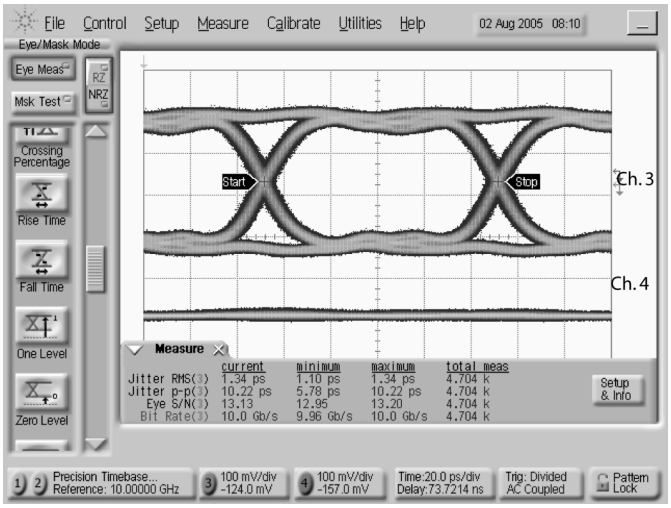


Fig. 20. Measured single-ended output eye diagram at 10 Gb/s through a 20-ft SMA cable.

jitter of 10.22 ps, an SNR of 13.13, and an amplitude of 290 mV_{pp} per side is seen at the output.

The test setup for 40-Gb/s measurements is described in Fig. 21. Two Centellax OTB3P1A boards produce 10-Gb/s PRBS data which are fed into a multiplexer (MUX) to generate

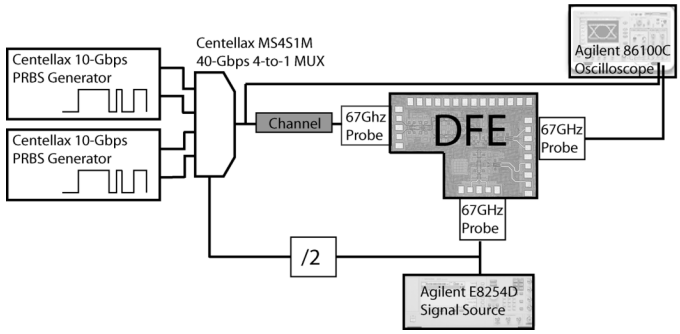
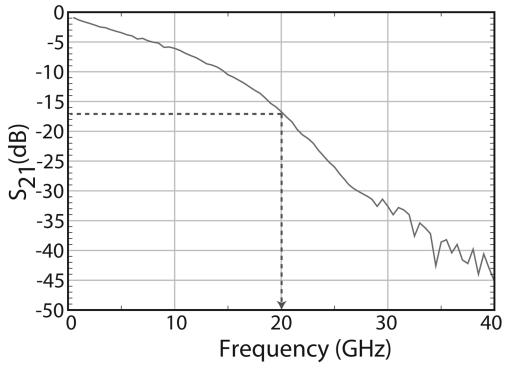
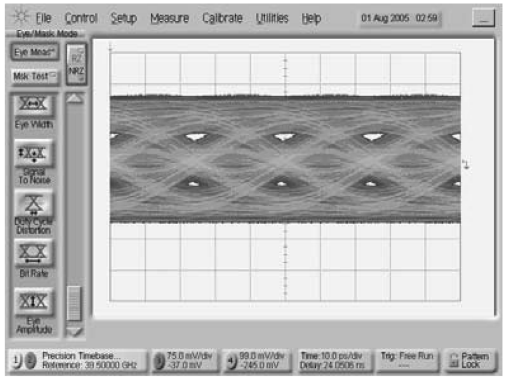


Fig. 21. Setup for large-signal 40-Gb/s measurements.



(a)



(b)

Fig. 22. 9-ft SMA cable (a) frequency response and (b) 40-Gb/s eye diagram at its output.

a broadband 40-Gb/s data stream with 4 times the bit length of the PRBS pattern of the boards (i.e., a 2^7-1 PRBS configuration results in a 508-bit repeating sequence). The oscilloscope displays the equalized single-ended output of the DFE as well as the ideal data pattern from the MUX. Error checking was performed on the bit sequence using the pattern lock feature in the oscilloscope.

The measured frequency response of the channel used for the 40-Gb/s measurement is shown in Fig. 22(a), along with a single-ended 40-Gb/s eye diagram at the input of the equalizer in Fig. 22(b). The single-ended output in Fig. 23 has an RMS jitter of 750 fs, peak-to-peak jitter of 5.11 ps, SNR of 9.1, and a swing of 340 mV_{pp}. The corresponding bathtub curve, generated by the Agilent 8600 C oscilloscope, in Fig. 24 indicates a timing margin of 0.75UI at an extrapolated BER of 10^{-12},

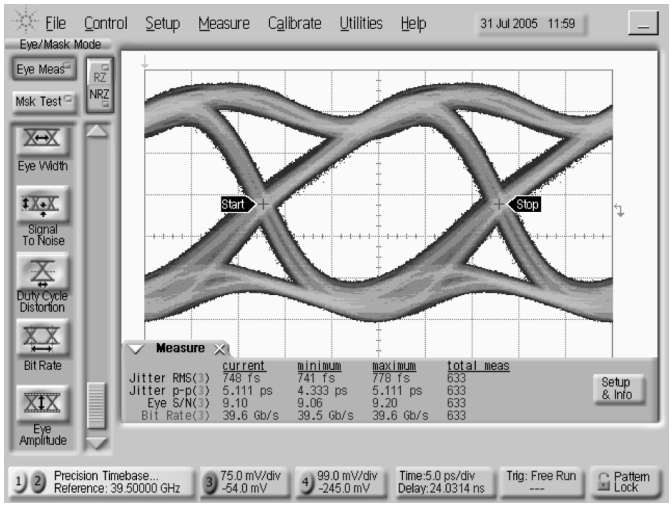


Fig. 23. Single-ended equalized output eye through 9-ft SMA cable at 39.5 Gb/s, board pattern of 2^7-1.

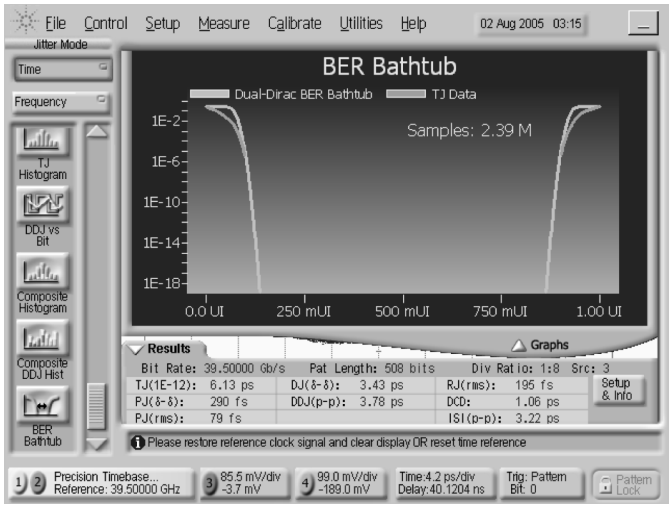


Fig. 24. Single-ended bathtub curve for single-ended output eye through 9-ft SMA cable at 39.5 Gb/s.

with a total jitter of 6.13 ps. A segment of the output bit sequence when the boards are configured for a 2^7-1 PRBS pattern (output of 508-bit length) is presented in Fig. 25, for ideal (top), unequalized (middle), and equalized outputs (bottom). Errors in the unequalized output are indicated with arrows above the sequence and are all corrected in the equalized trace.

V. Conclusion

The design of a 1-tap 40-Gb/s decision feedback equalizer has been investigated for PMD compensation of single-mode fibers. In order to meet the high-speed requirements, a look-ahead architecture was selected to decrease the propagation delay within the feedback path, while maintaining full functionality. Slight modifications to the architecture were made to ease the requirements on the clock distribution and reduce the overall power consumption of the DFE. A broadband front-end provides a low-noise linear input stage with a bandwidth of 45 GHz. A differential control voltage can shift the receiver's

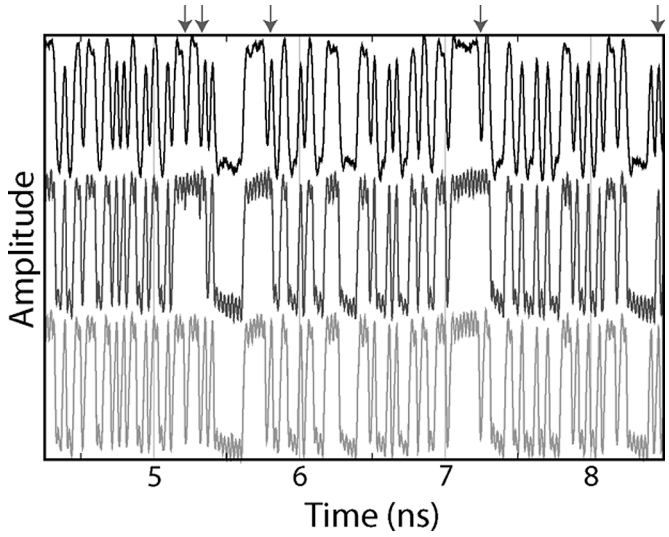


Fig. 25. Segment of 508-bit sequence (2^7-1 PRBS on each board) for an ideal (top), unequalized (middle), and equalized (bottom) output. Errors indicated by arrows above bit sequence.

decision threshold by up to 225 mV to compensate for one tap of post-cursor ISI. A propagation delay of 22 ps (simulated) is found through the critical path when interconnect parasitics are included. A BER of less than 10^{-12} was measured through a PMD emulating channel at 5 Gb/s and a 20-ft SMA cable at 10 Gb/s using a bit error checker. At 40 Gb/s, the DFE compensated for a 9-ft SMA cable and the functional verification was conducted with a 508-bit pattern. The return loss at the data inputs and outputs and at the clock inputs is lower than -10 dB up to 50 GHz, as needed for 40-Gb/s operation. The test chip occupies an area of 1.5 mm^2, operates from a 3.3-V power supply, and draws 230 mA of current.

To the authors' knowledge, this is the first fully functional 40-Gb/s DFE in any technology. It has been shown that using current commercially available technologies, equalizers at 40 Gb/s are feasible [4]. This work sets the stage to effectively eliminate PMD as a limitation in 40-Gb/s long-haul optical fiber systems.

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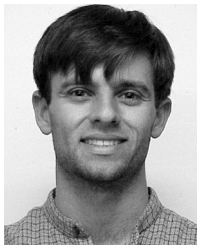

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