20 GHz Low Power QVCO and De-skew Techniques in 0.13µm Digital CMOS

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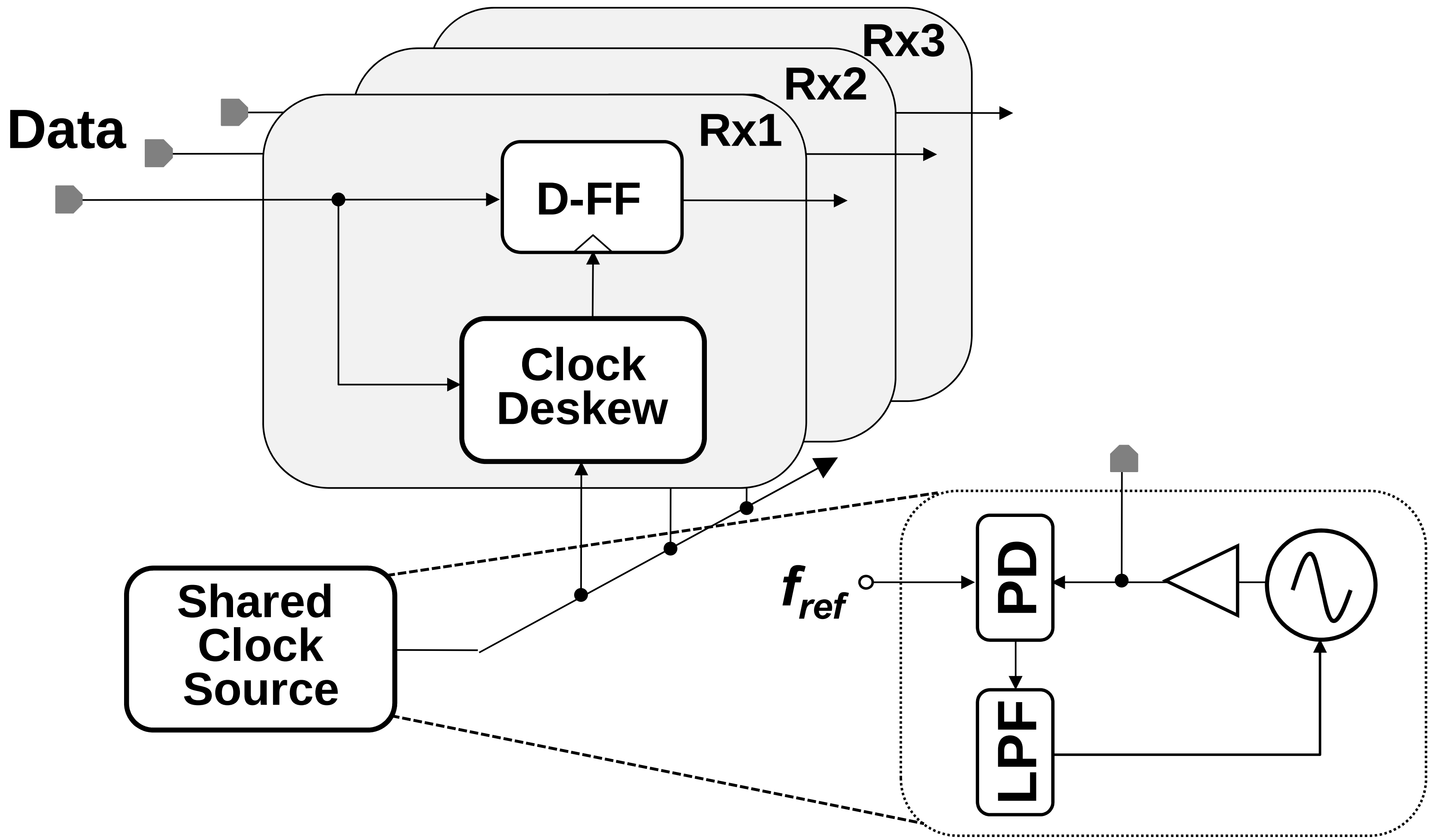
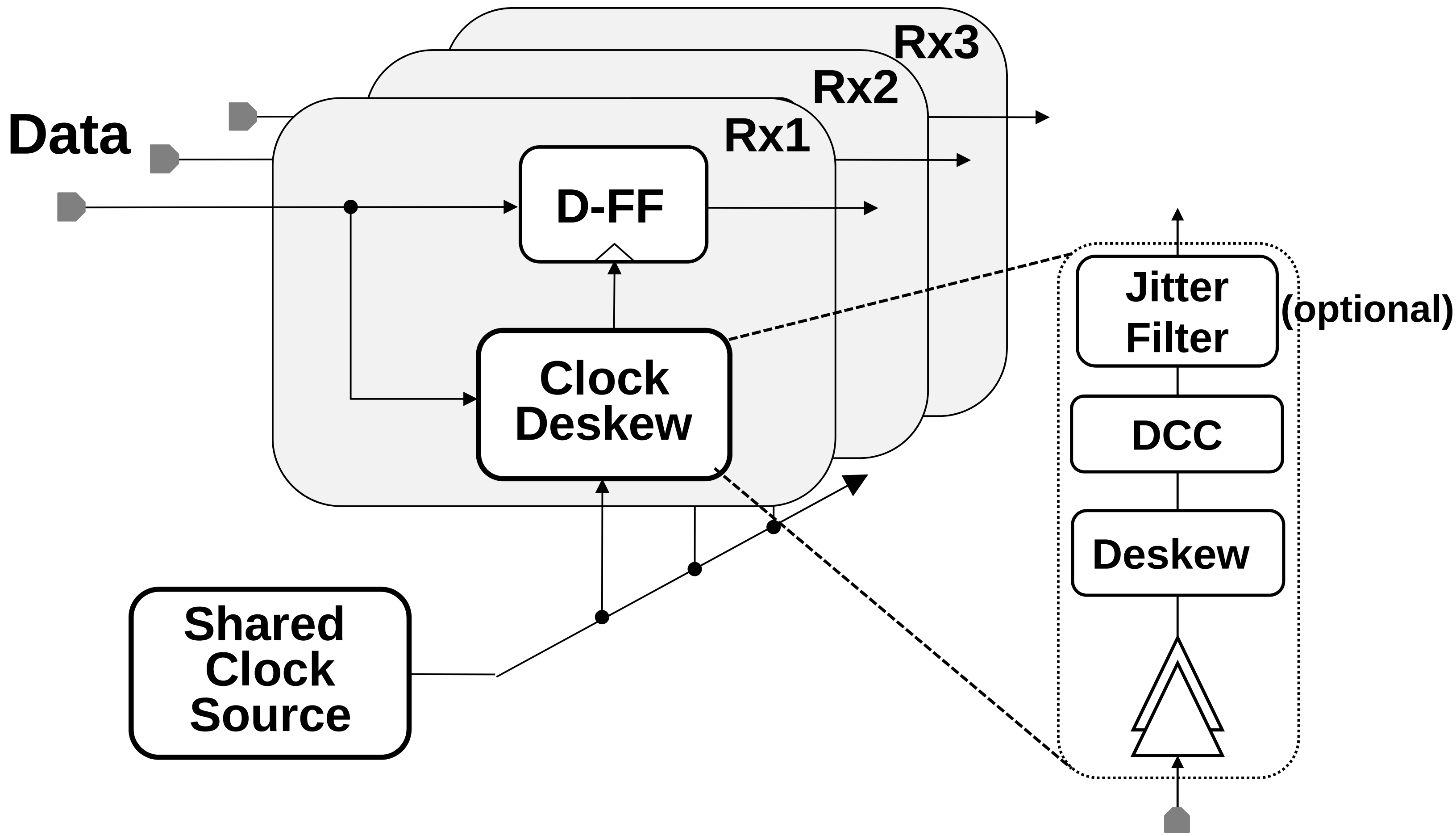
Motivation



Data
Rx3
Rx2
Rx1
D-FF
Clock Deskew
Shared Clock Source
f_{ref}
PD
LPF

Motivation



Data
Rx3
Rx2
Rx1
D-FF
Clock Deskew
Shared Clock Source
Jitter Filter
(optional)
DCC
Deskew

Outline

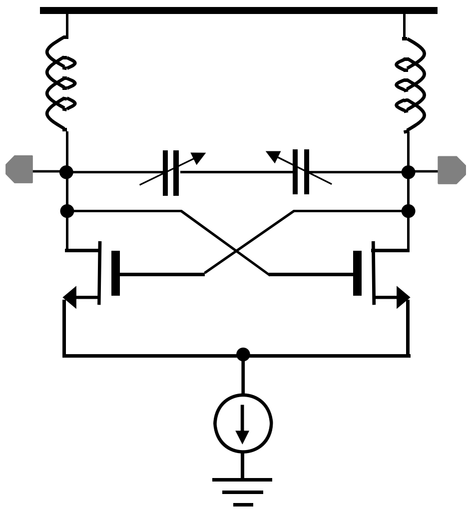
Low power clock source in Digital CMOS

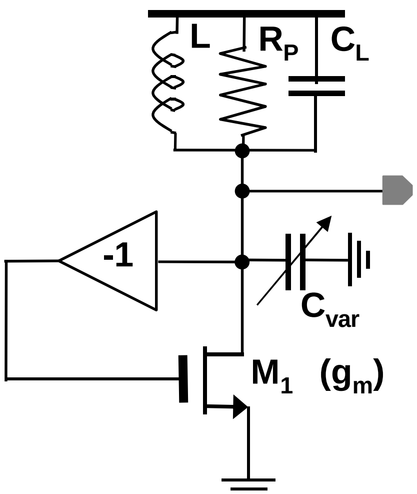
- Review of CMOS LC VCO topology
- Colpitts vs Cross-coupled
- Proposed VCO topology
- Experimental Results

Low power clock deskew technique CMOS

- Review of existing deskew techniques
- Proposed deskew technique
- Experimental Results

Cross-Coupled VCO





Oscillation condition:

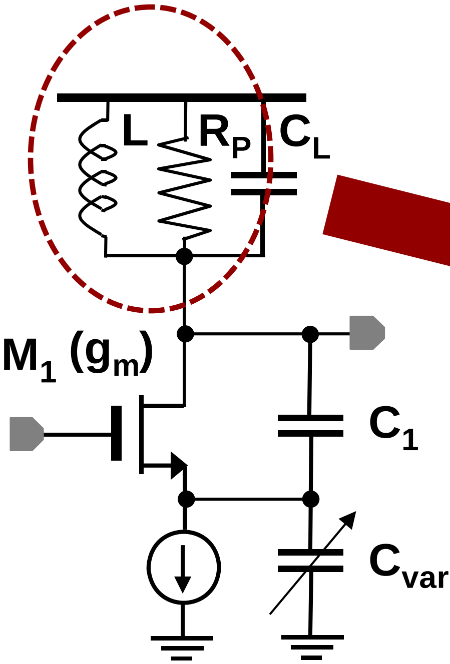
$$g_m \geq \frac{1}{R_P}$$

Oscillation frequency:

$$f_{OSC} = \frac{1}{2\pi\sqrt{L(C_{var} + C_L)}}$$

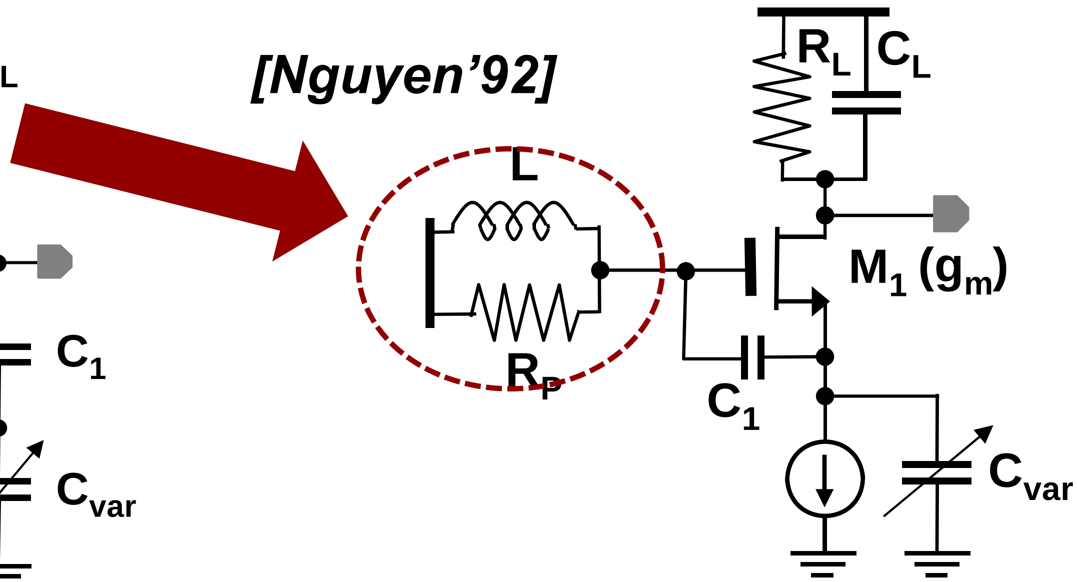
Colpitts VCO

Conventional Colpitts



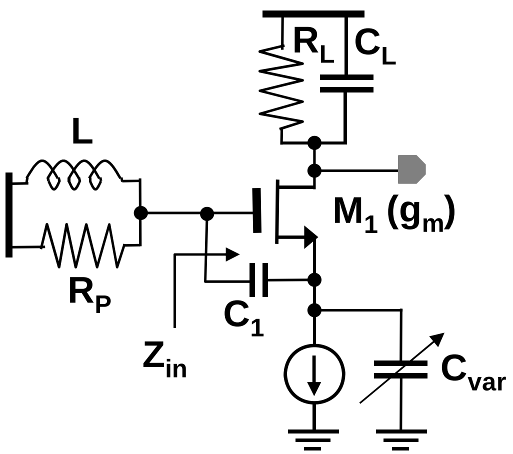
Modified Colpitts

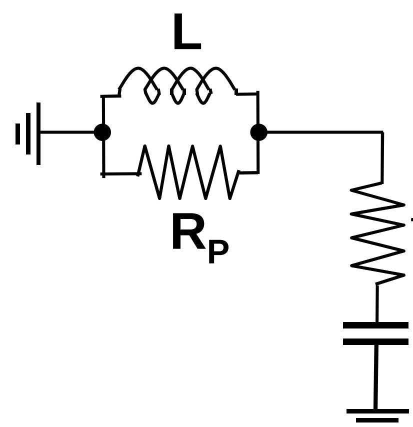
[Nguyen'92]



✓ **Decouples the tank from load**

Colpitts VCO





$$-R = \frac{g_m}{\omega^2 C_1 C_{var}}$$

$$C_{eq} = \frac{C_1 C_{var}}{C_1 + C_{var}}$$

Oscillation frequency:

$$f_{osc} \approx \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{L\frac{C_1 C_{var}}{C_1 + C_{var}}}}$$

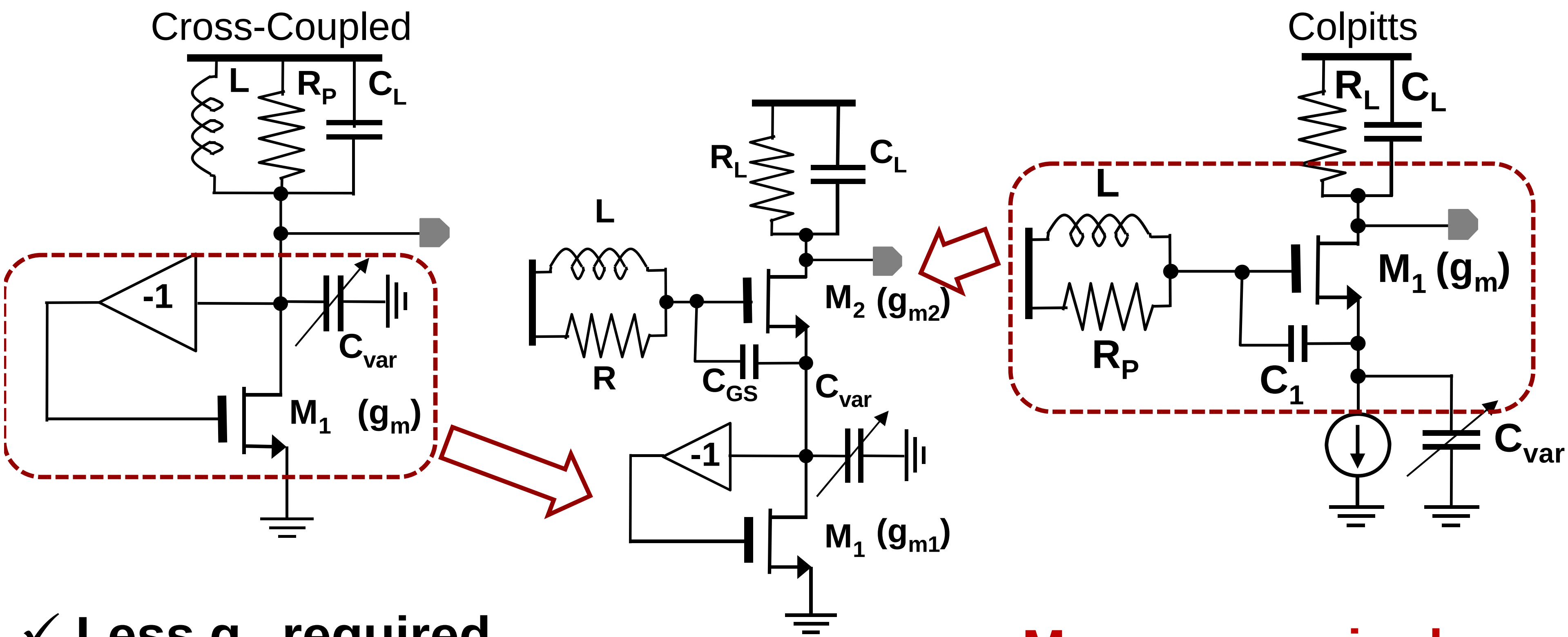
Oscillation condition:

$$g_m \geq \frac{1}{R_p}\left(\frac{(C_1 + C_{var})^2}{C_1 C_{var}}\right)$$

This can be minimized for C_1=C_{var} ,

$$g_m \geq \frac{4}{R_p}$$

Proposed VCO



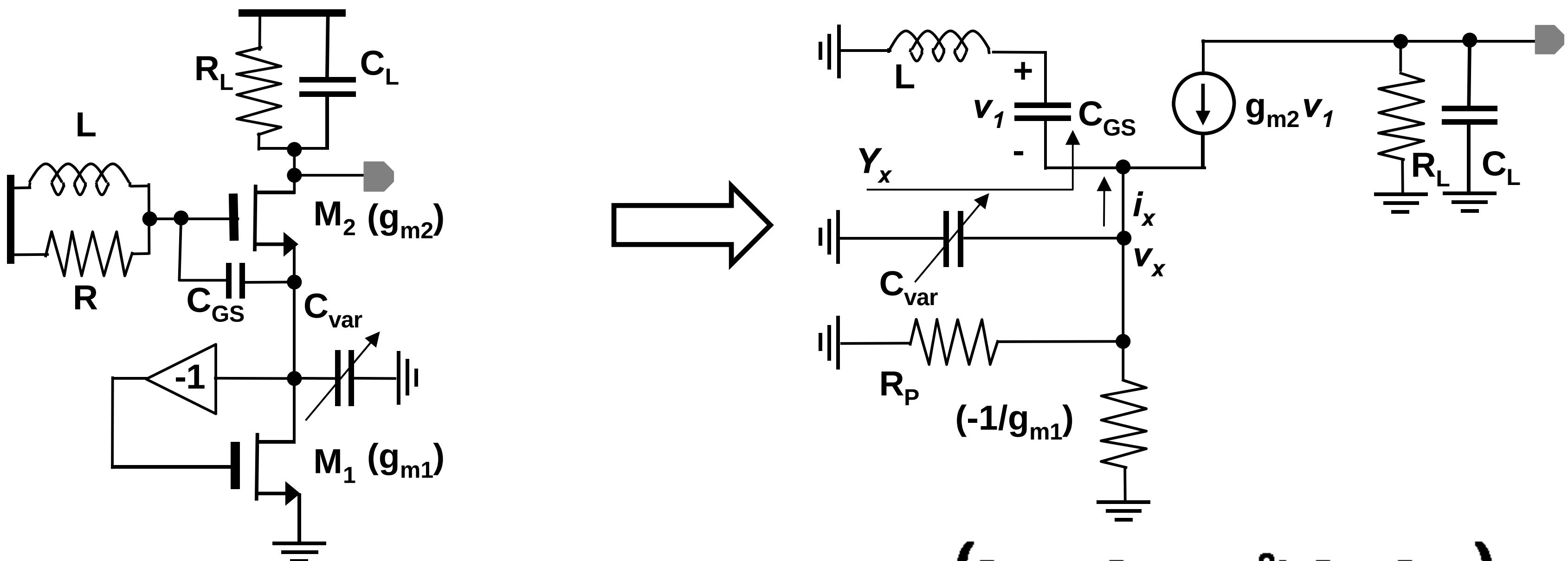
✓ **Less g_m required**

✖ **f_{osc} depends on C_L**

✖ **More g_m required**

✓ **f_{osc} independent of C_L**

Proposed VCO



Equivalent tank admittance

$$y_{tank} \approx \frac{g_{m2} + s\left(C_{GS} + C_{var} + s^2 L C_{GS} C_{var}\right)}{1 + s^2 L C_{GS}} + \frac{1}{R_P}$$

Oscillation frequency:

$$f_{osc} = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{L\dfrac{C_{GS}C_{var}}{C_{GS}+C_{var}}}}$$

Oscillation condition:

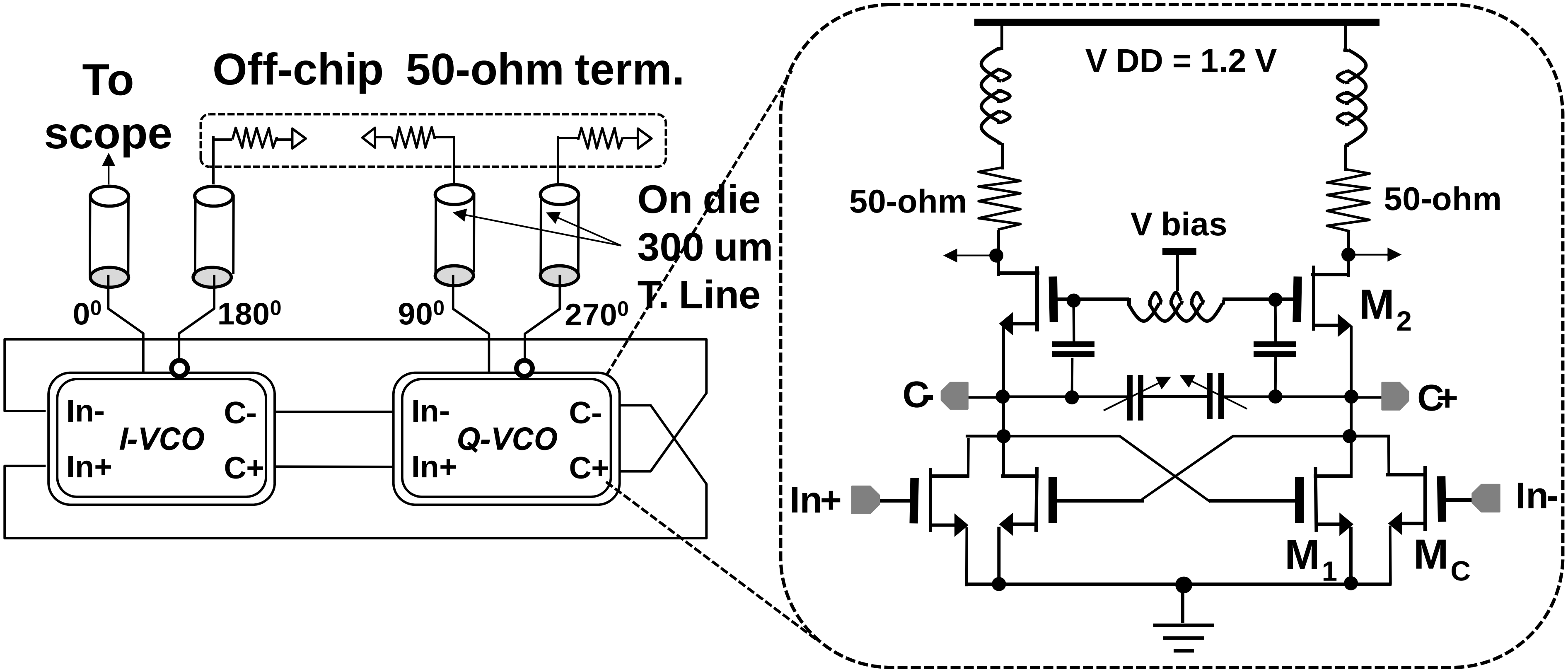
$$g_{m1} \geq \mathrm{Re}\{y_{tank}\} \approx -\frac{C_{var}}{C_{GS}} g_{m2} + \frac{1}{R_P}$$

VCO Summary

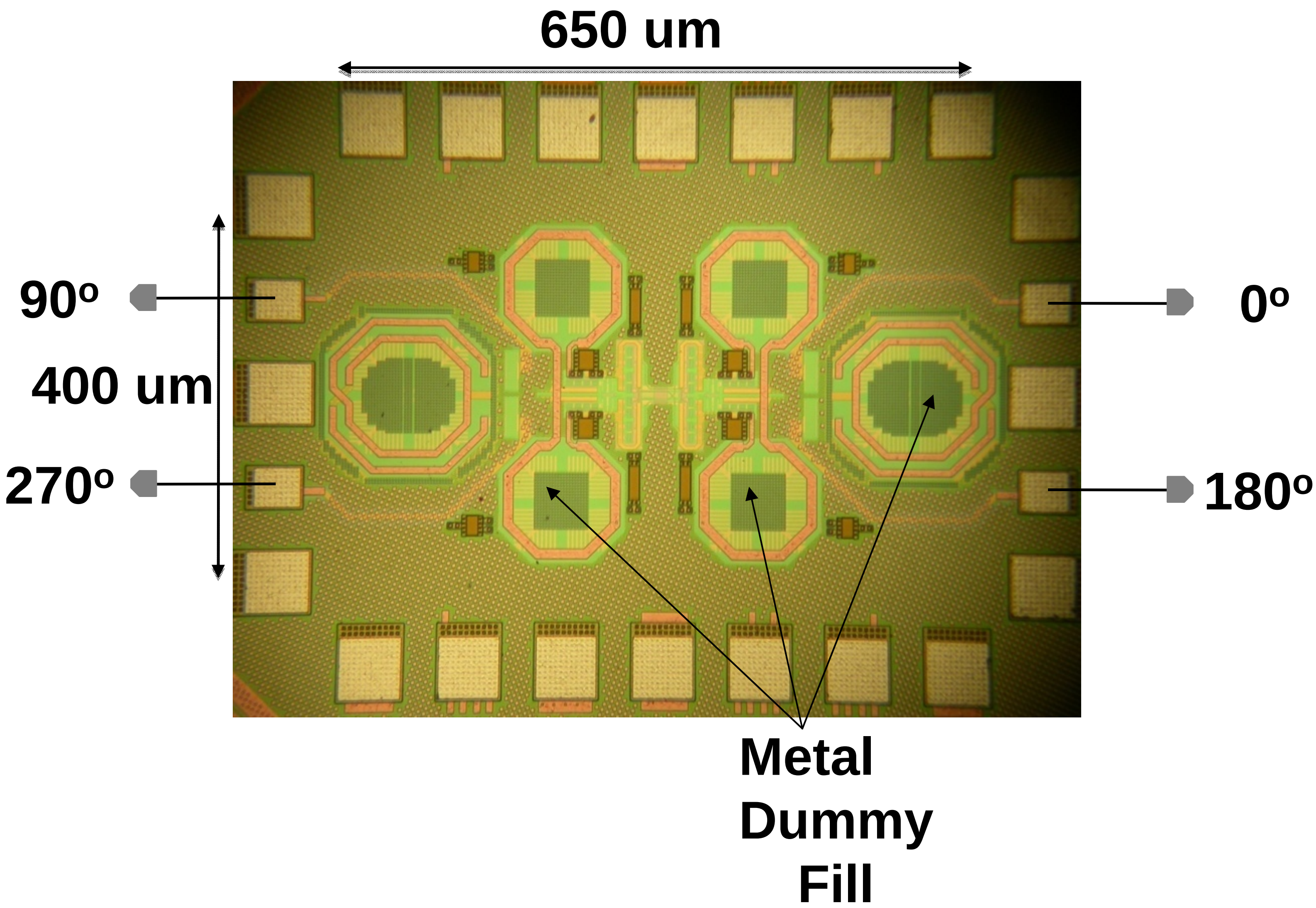
	Frequency of Oscillation	Minimum Required g_m
Cross-Coupled	$f_{osc} = \left(2\pi\sqrt{L\left(C_{var} + C_L\right)}\right)^{-1}$	$\geq \frac{1}{R_P}$
Colpitts	$f_{osc} = \left(2\pi\sqrt{L\frac{C_1 C_{var}}{C_1 + C_{var}}}\right)^{-1}$	$\geq \frac{4}{R_P}$
Proposed VCO	$f_{osc} = \left(2\pi\sqrt{L\frac{C_{GS} C_{var}}{C_{GS} + C_{var}}}\right)^{-1}$	$\geq \left(\frac{1}{R_P} - \frac{C_{var}}{C_{GS}} g_{m2}\right)$

Proposed oscillator combines the benefit of both topology !

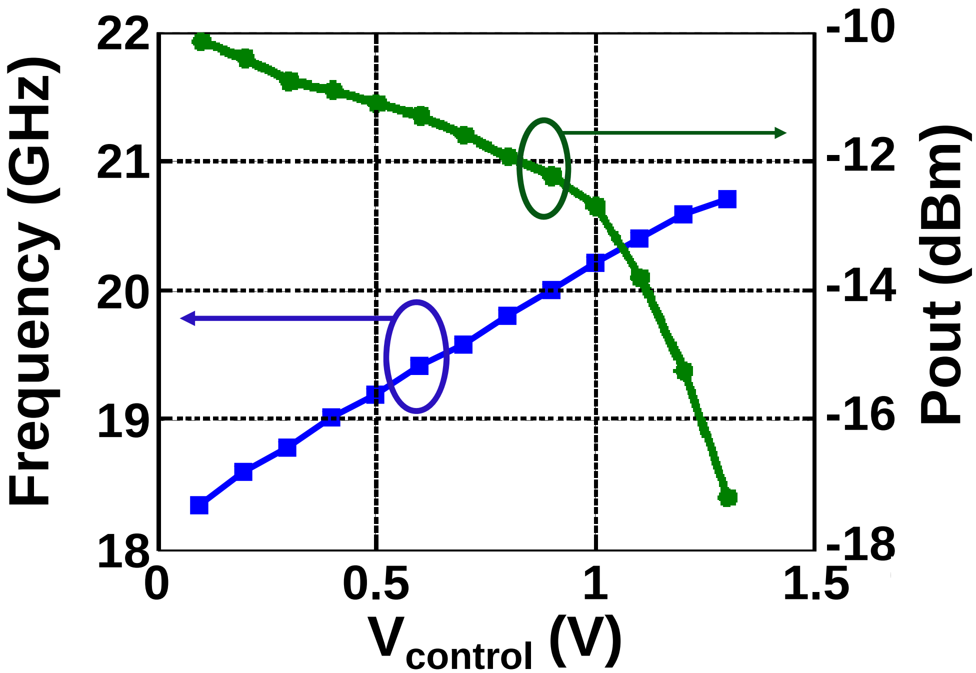
QVCO Implementation

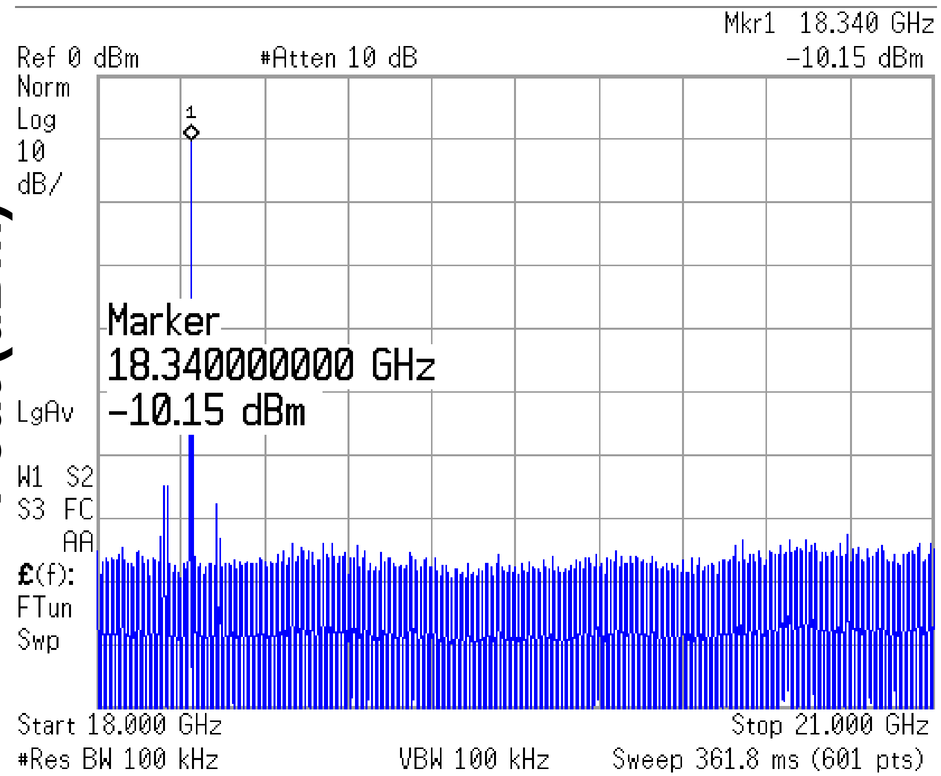


QVCO Implementation



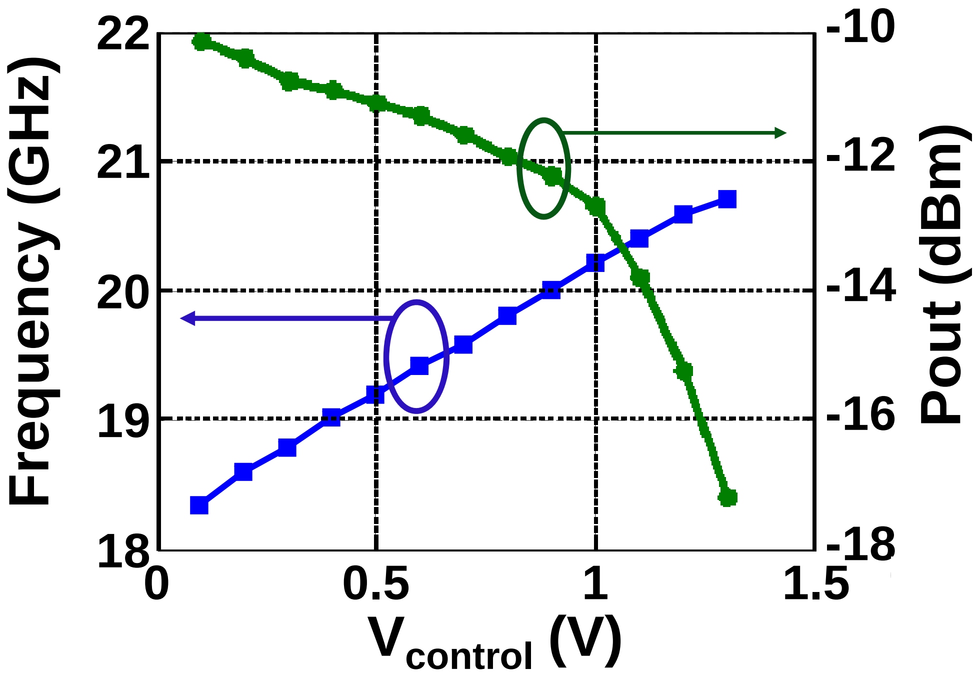
QVCO Performance

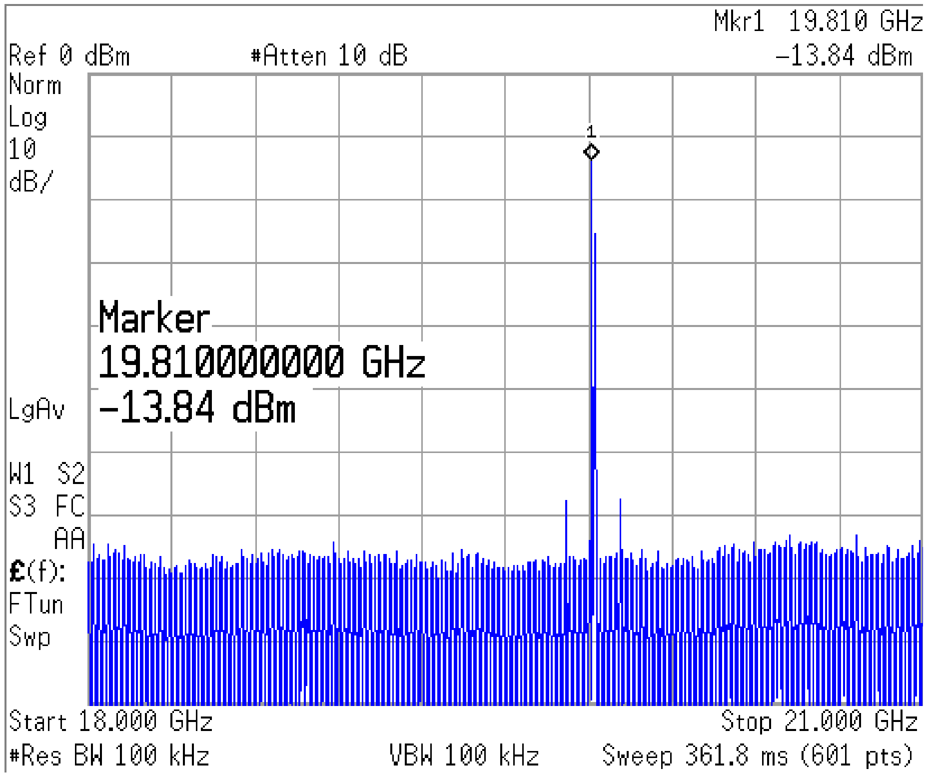




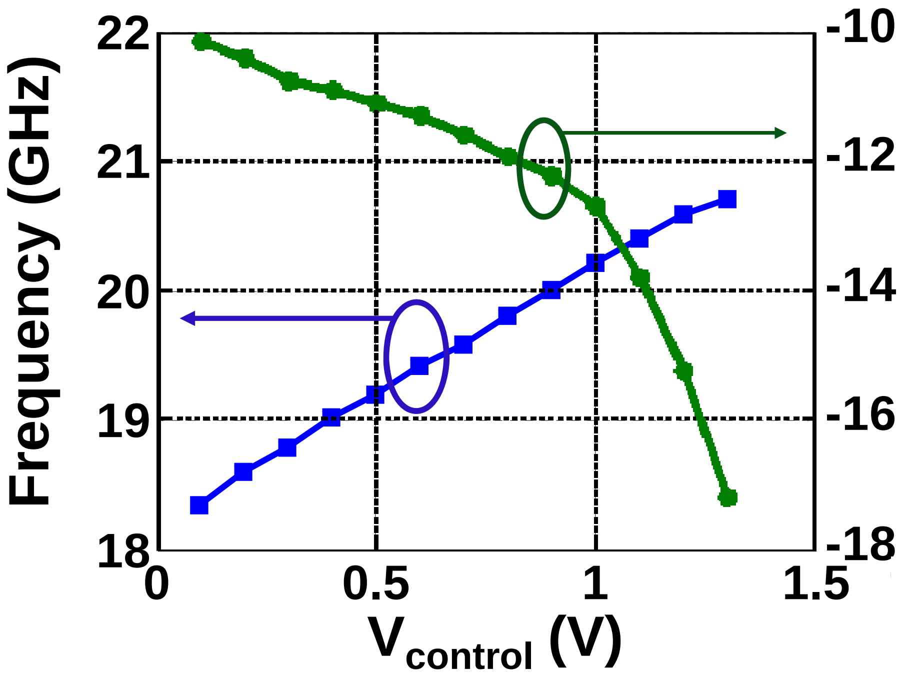
Tuning range 2.4 GHz (~12%)

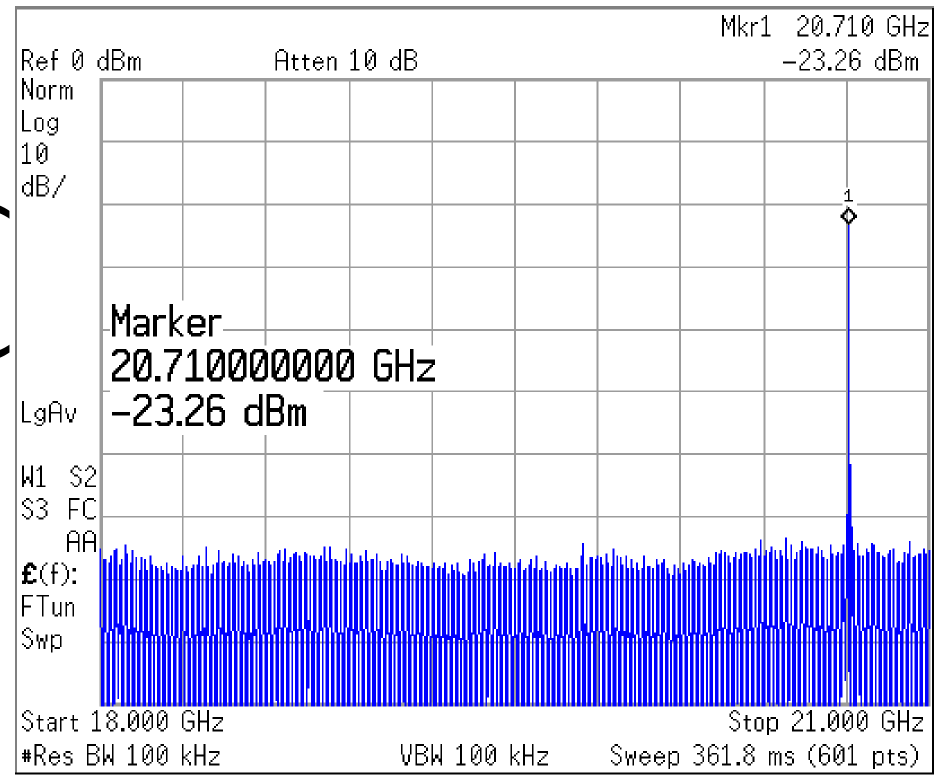
QVCO Performance





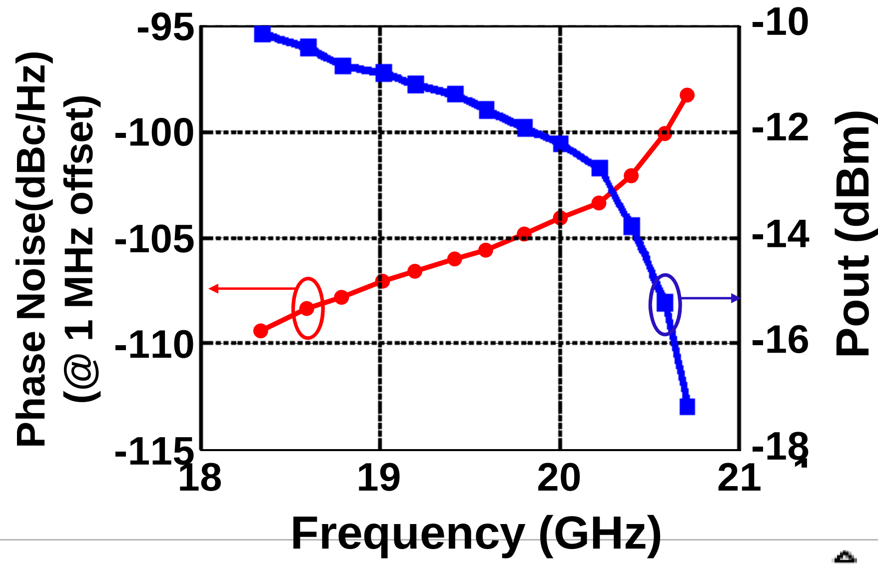
QVCO Performance

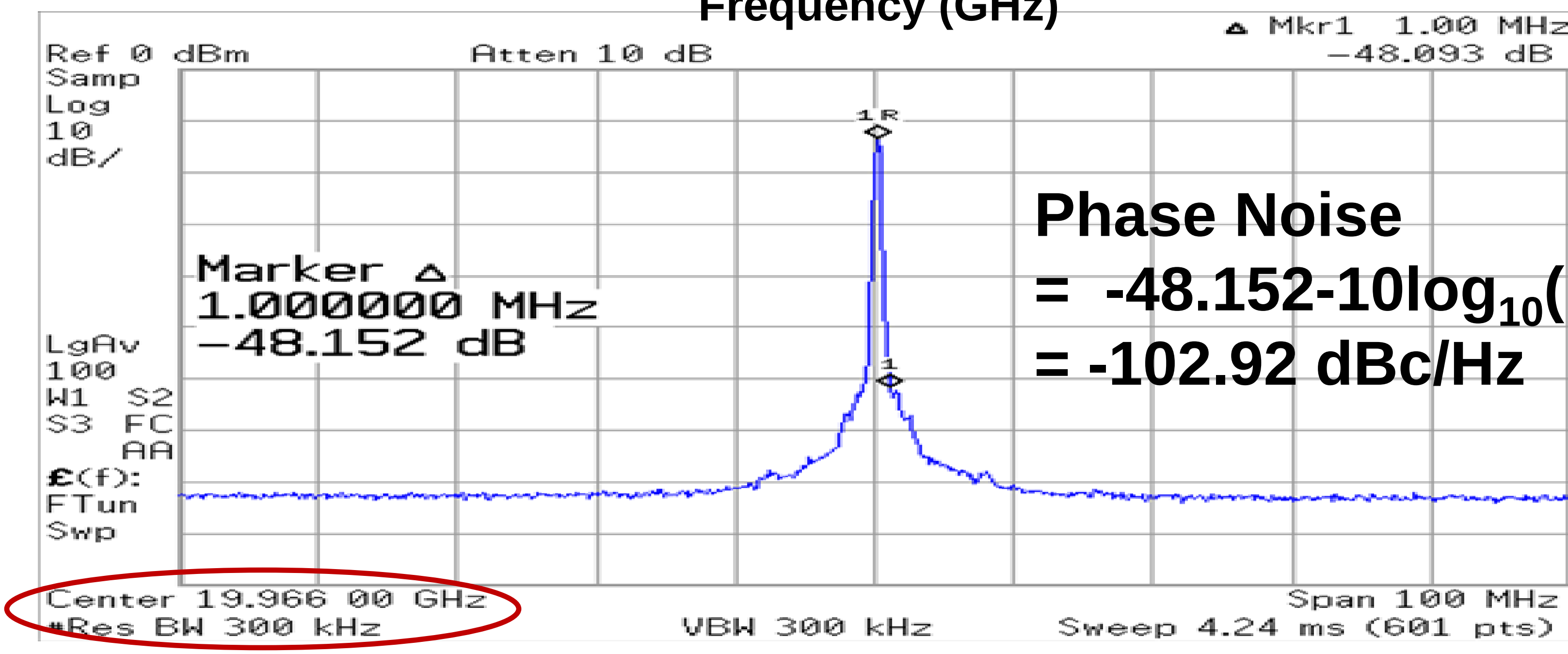




Cable loss was de-embedded

QVCO Performance



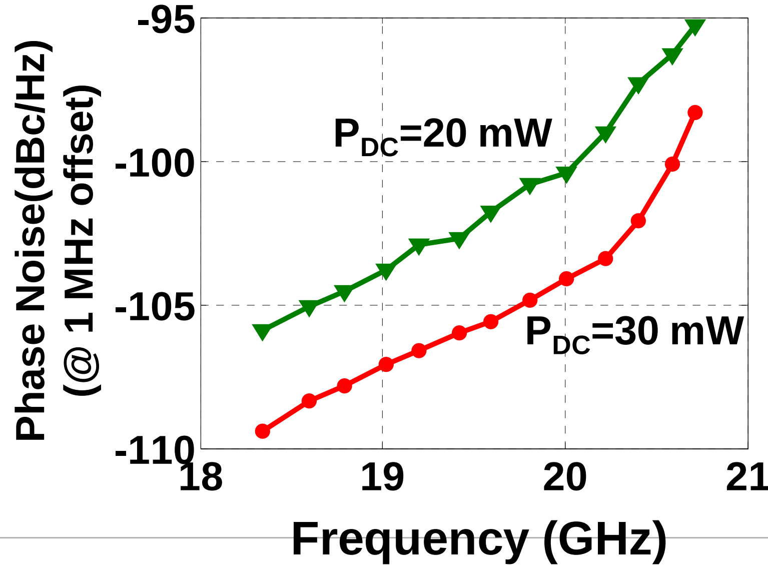


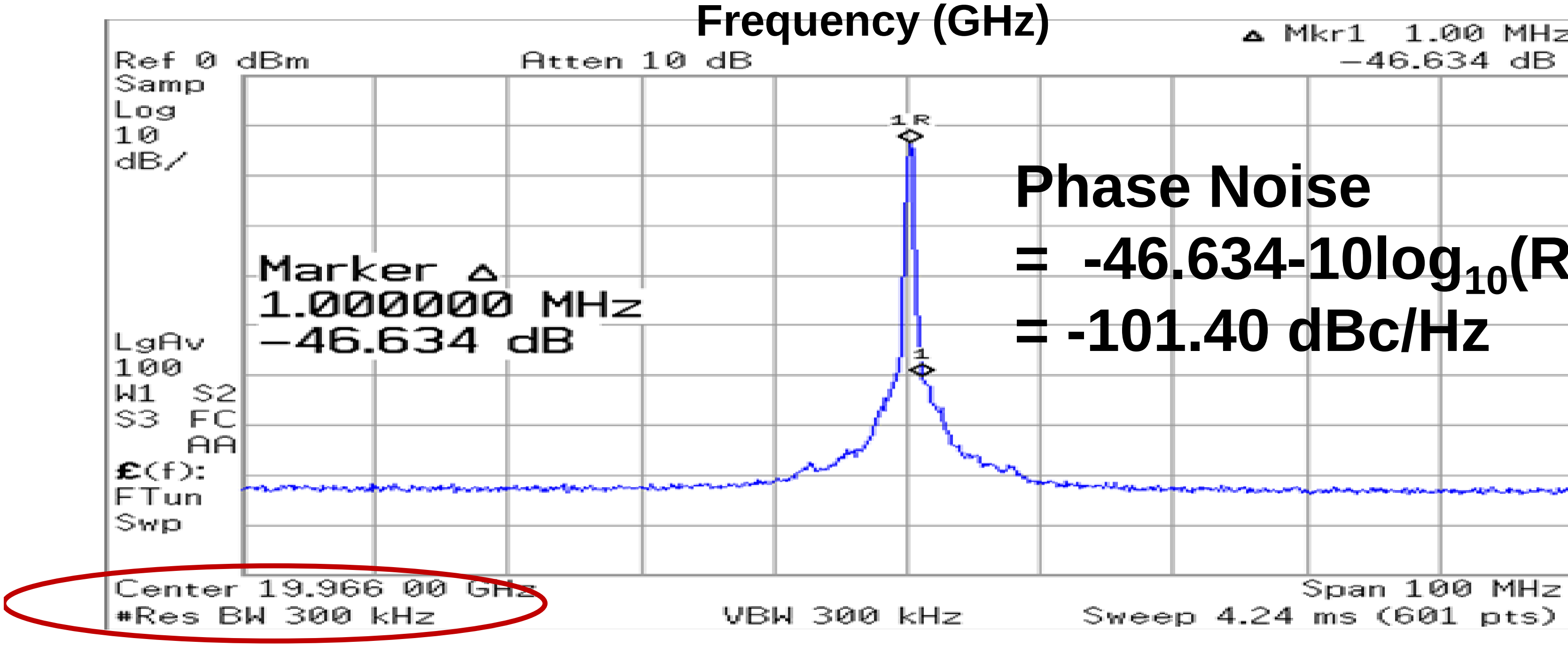
Phase Noise

$= -48.152 - 10\log_{10}(RBW)$

$= -102.92$ dBc/Hz

QVCO Performance





Phase Noise

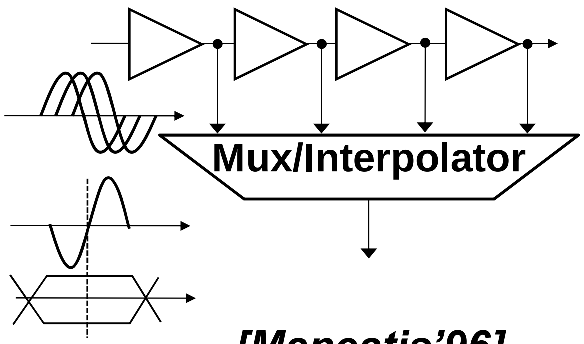
= -46.634-10log$_{10}$(RBW)

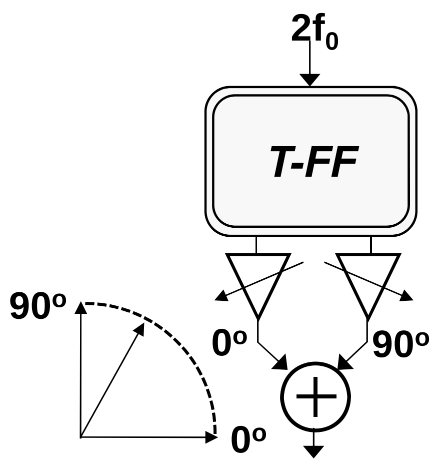
= -101.40 dBc/Hz

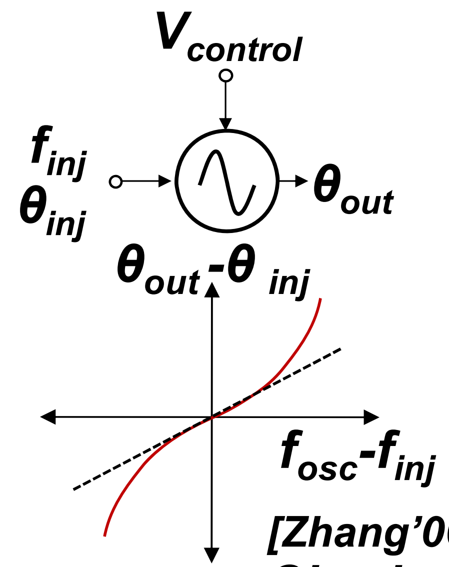
Performance Comparison

	CSICS'06	CSICS'06	JSSC'07	JSSC'04	VLSI'05	This work
Technology	90-nm CMOS	90-nm CMOS	0.13-um CMOS	0.13-um CMOS	90-nm SOI	0.13-um CMOS
Frequency	10 GHz	10 GHz	26 GHz	10 GHz	40 GHz	20 GHz
Topology	Colpitts	Cross-Coupled	G_m Tuned	Cross-Coupled	Cross-Coupled	Cross-Coupled
Diff./Quadrature	Diff.	Diff.	Diff.	Quad.	Quad.	Quad.
Tuning Range	12.2 %	15.8 %	23.6 %	15%	12.5 %	12 %
Inductor Q	10	10	18	-------	18	5
Phase Noise (dBc/Hz@1 MHz)	-117.5	-109.2	-92.6	-95	-87 @3 MHz	-102.41
VCO power VCO+ Buffer	36 mW	7.5 mW 17.5 mW	43.6 mW 50 mW	14.4 mW --------	--------- 81 mW	--------- 30mW
FOM (VCO) (dB) (VCO+ Buffer)	181.9 --------	180.4 176.5	163.9 163.3	163.4 --------	-------- 150.4	--------- 173.45

Deskew Techniques





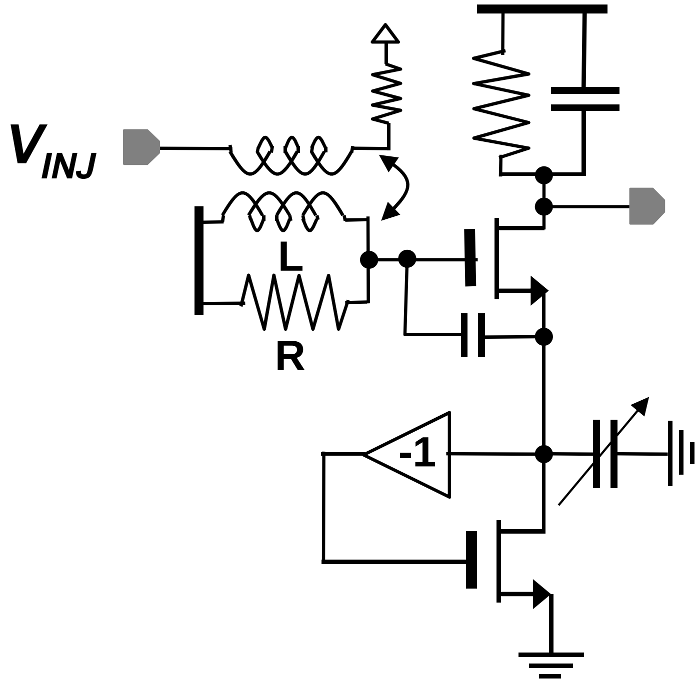


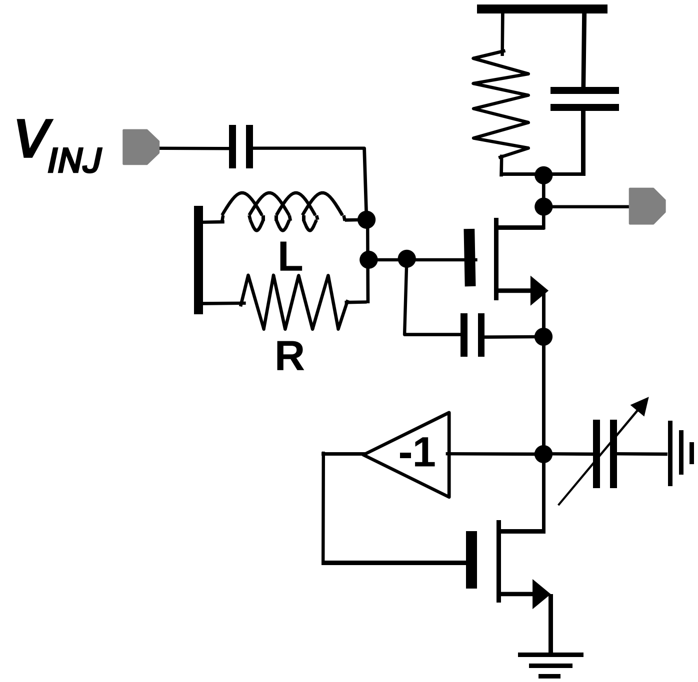
- ✓ 0-360⁰ deskew
- ✓ Moderate power
- ✖ Supply Noise
- ✖ Duty Cycle Dis.
- ✖ All pass JTF

- ✓ 0-360⁰ deskew
- ✓ Simple architecture
- ✖ Uses $2f_0$ or 4 phase
- ✖ Non-linearity
- ✖ All pass JTF

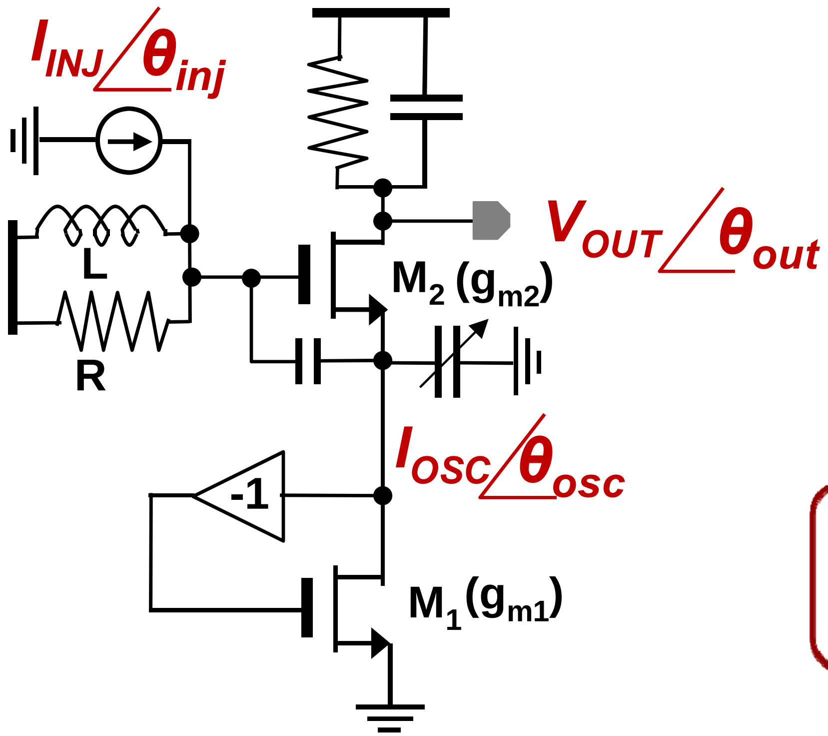
- ✓ Less supply noise
- ✓ Less DCD
- ✓ Low pass JTF
- ✓ Low power
- ✖ Limited deskew (<360)
- ✖ Non-linearity
- ✖ Skew dependent JTF

Passive Injection Technique





ILO based deskew

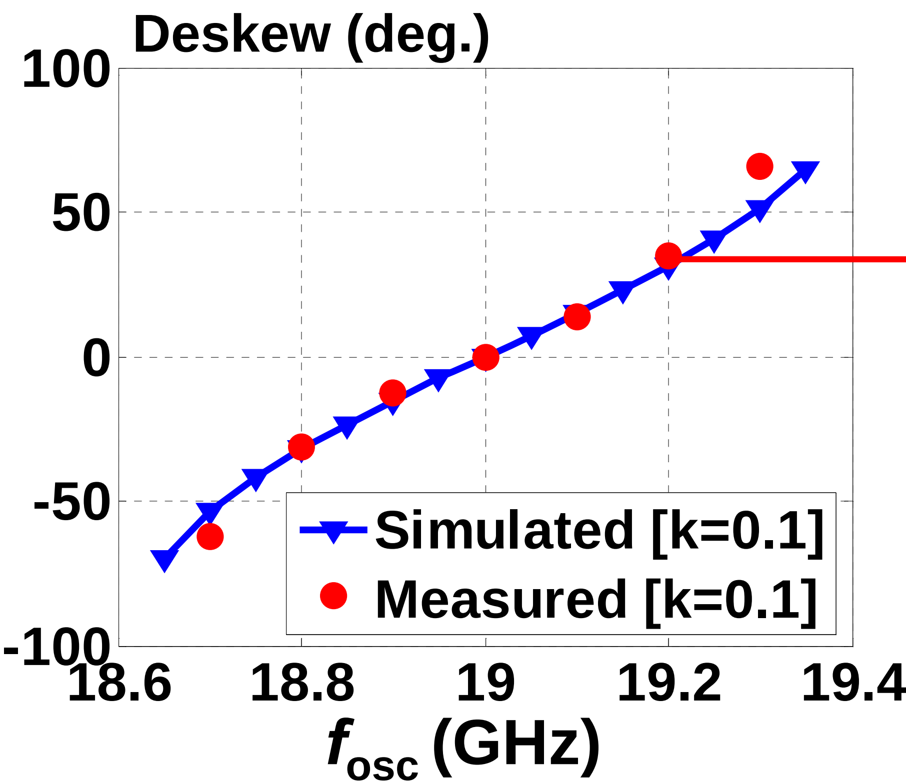


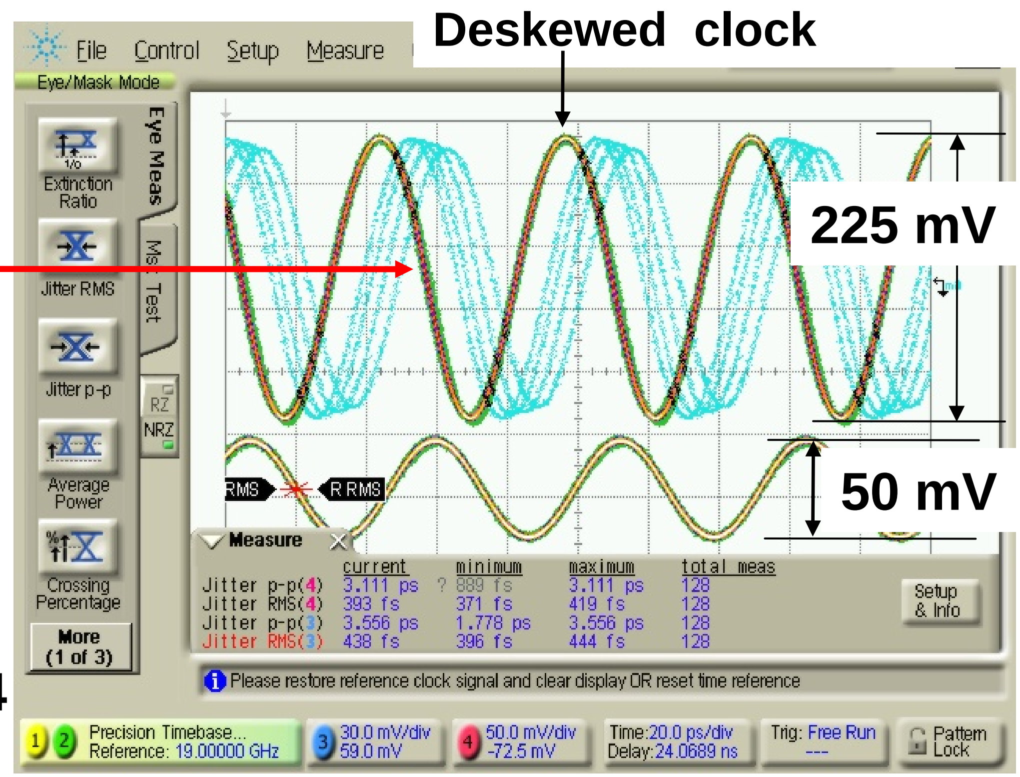
$$A_{CLOCK} = \frac{V_{OUT}}{V_{INJ}}$$

$$K = \frac{I_{INJ}}{I_{OSC}}$$

$$\theta_{out} - \theta_{inj} \approx \pi + \sin^{-1}\left(\frac{2Q}{K}\left(\frac{f_{osc} - f_{inj}}{f_{osc}}\right)\right)$$

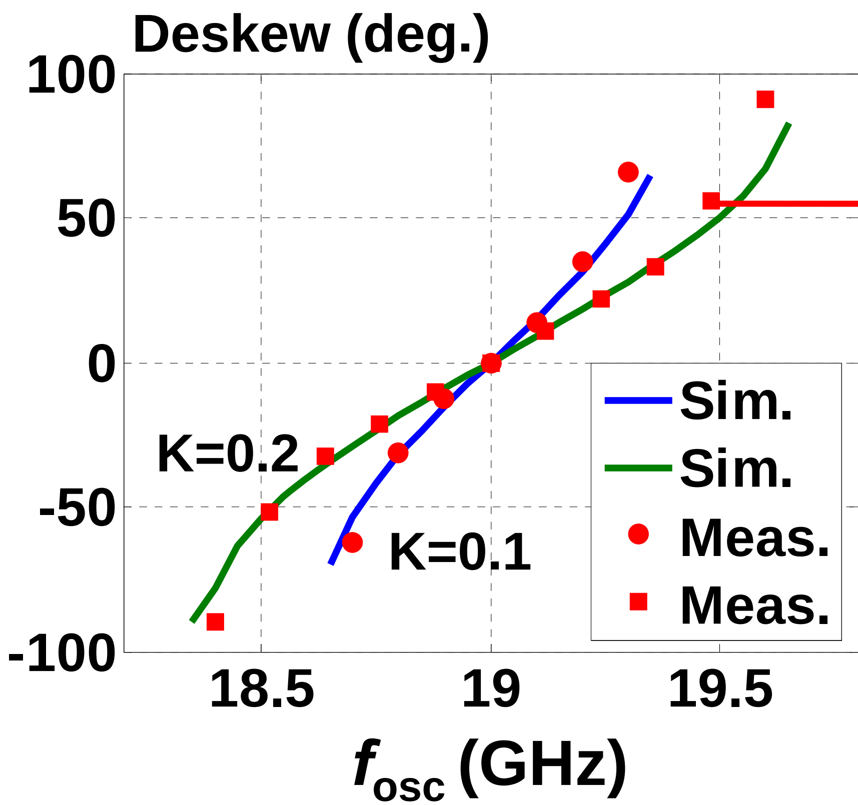
ILO based deskew (K=0.1)

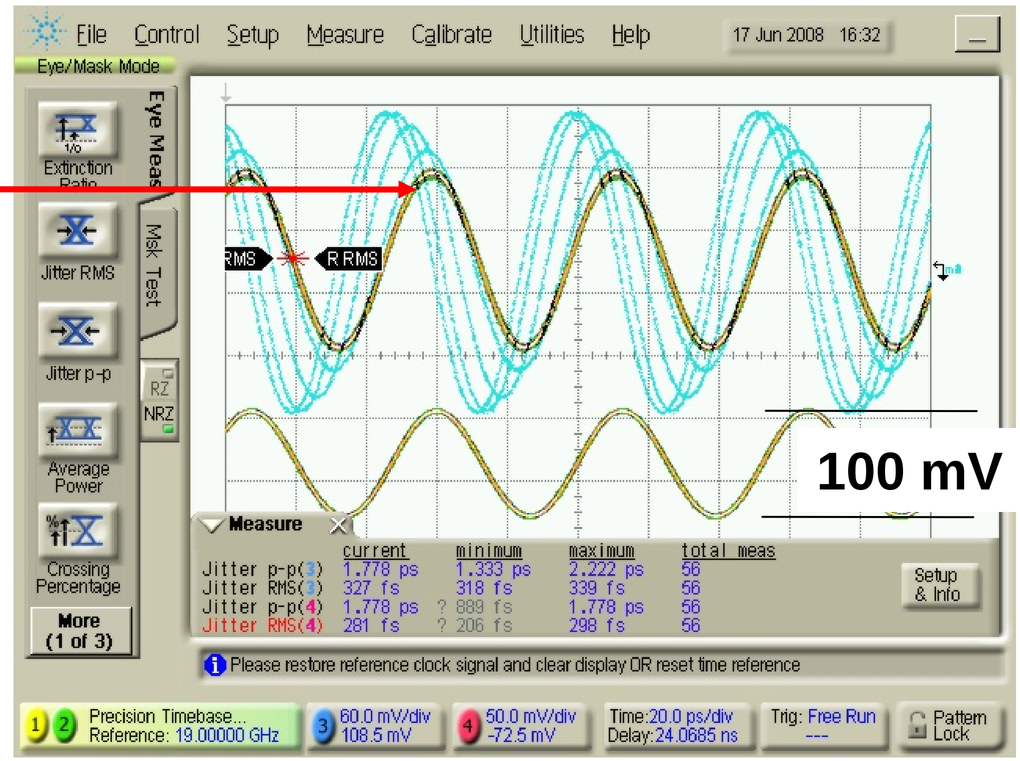




- 4.5 X Clock amplification
- Less than 10% amplitude variation
- 12 mW power consumption
- Deskew << 180°

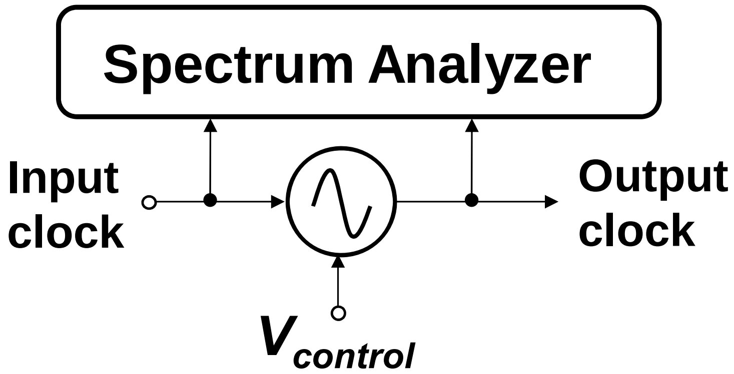
ILO based deskew (K=0.2)

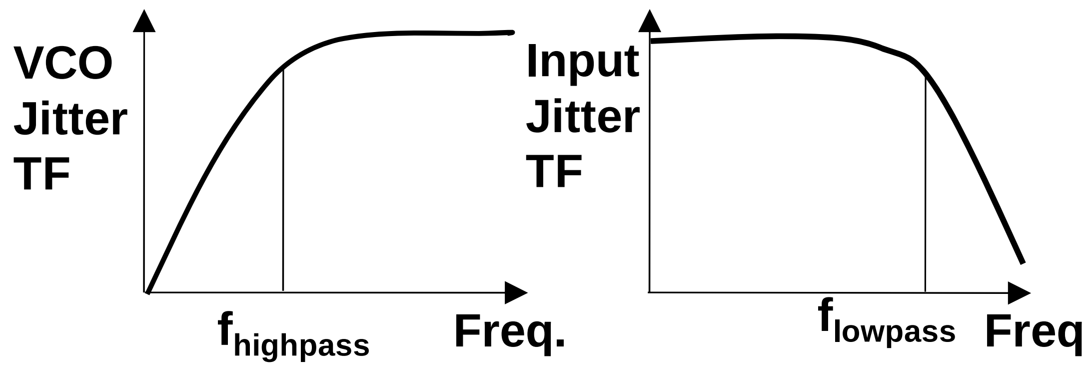


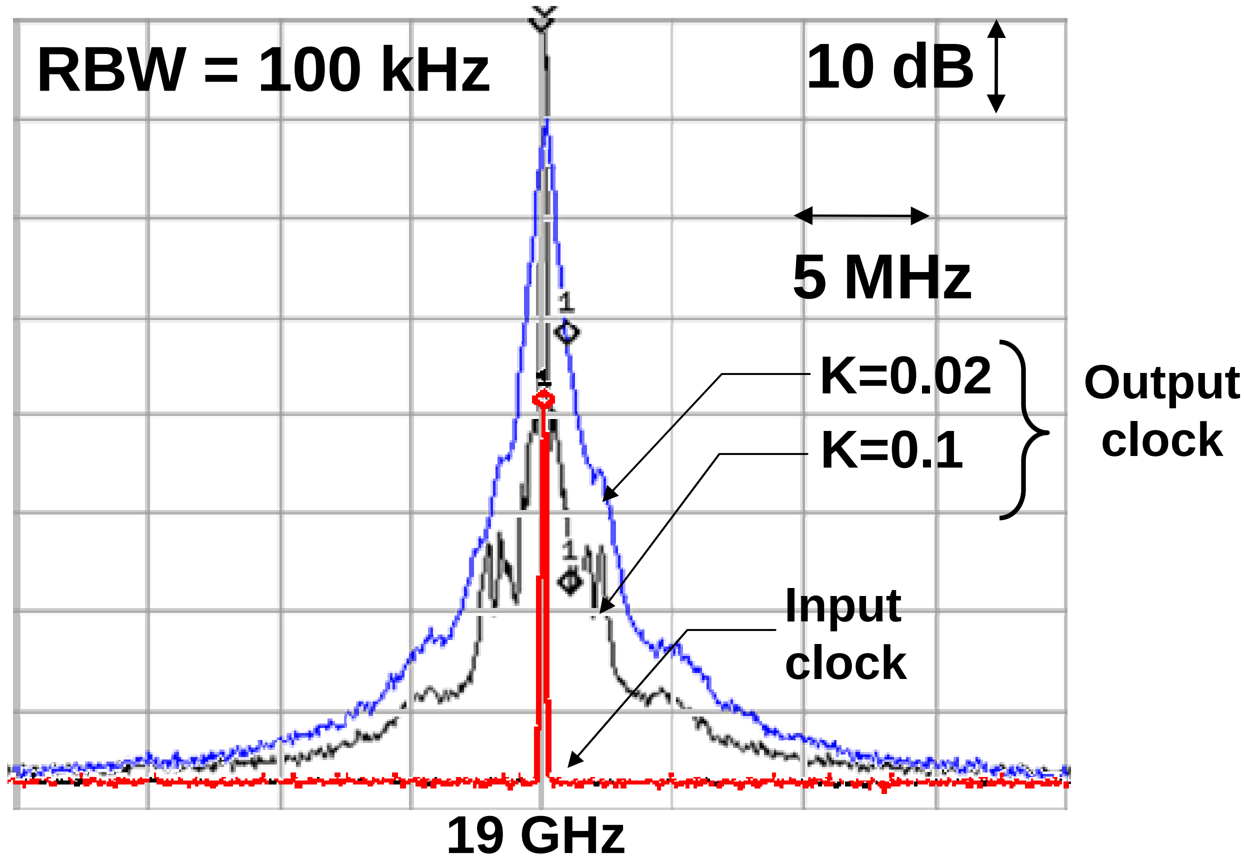


- **2.25 X Clock amplification**
- **More than 30% amplitude variation**
- **12 mW power consumption**
- **Deskew range increases but non-linear**

Jitter Transfer Function







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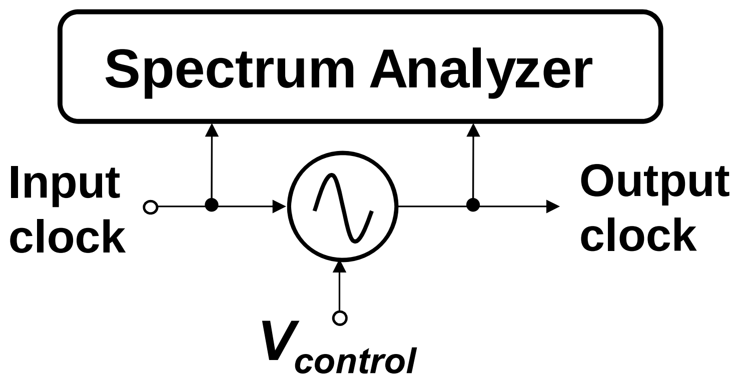
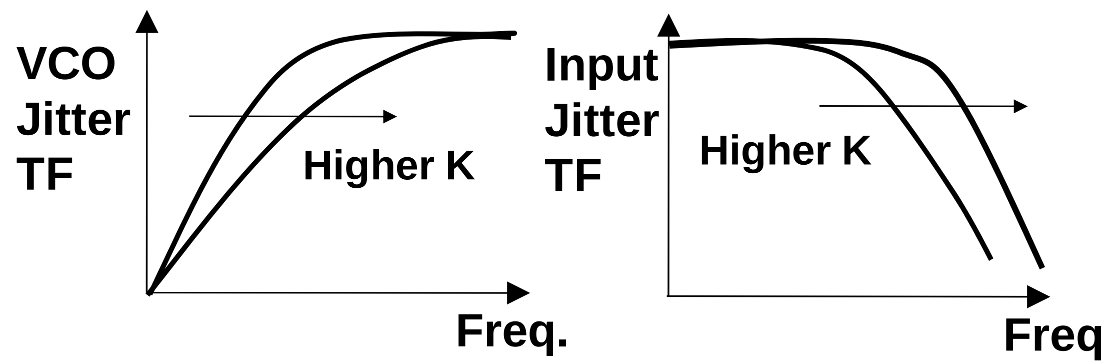
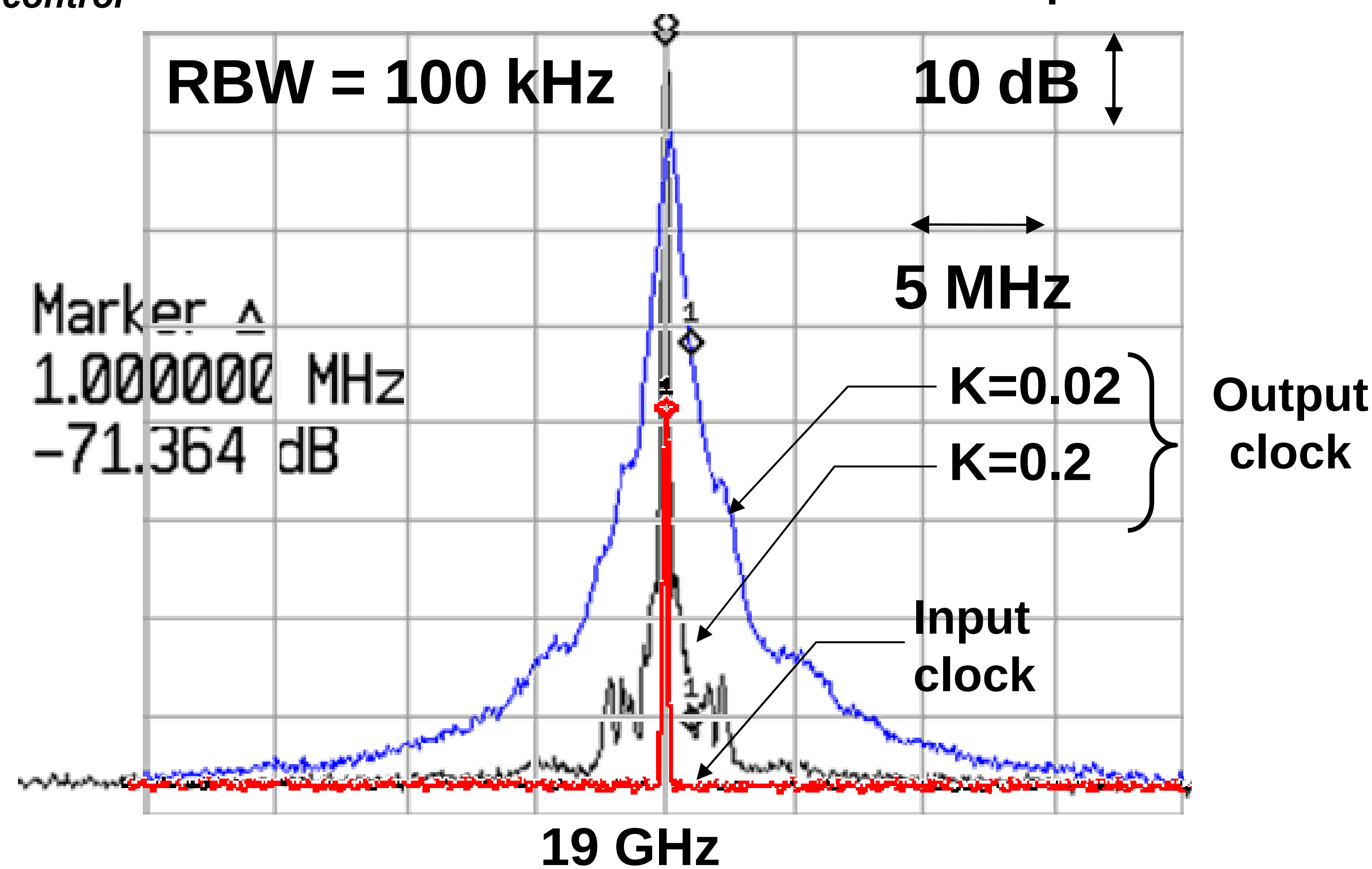
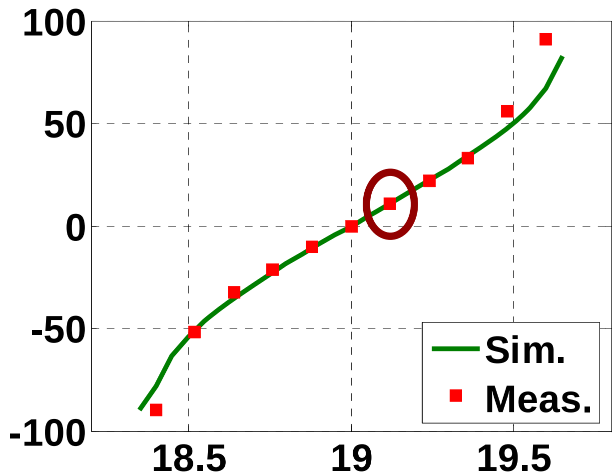
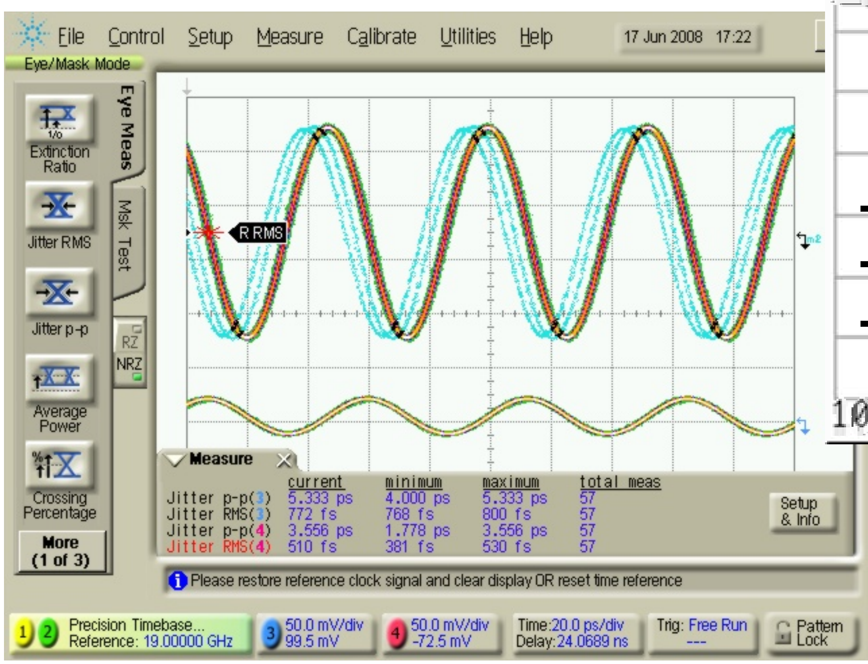


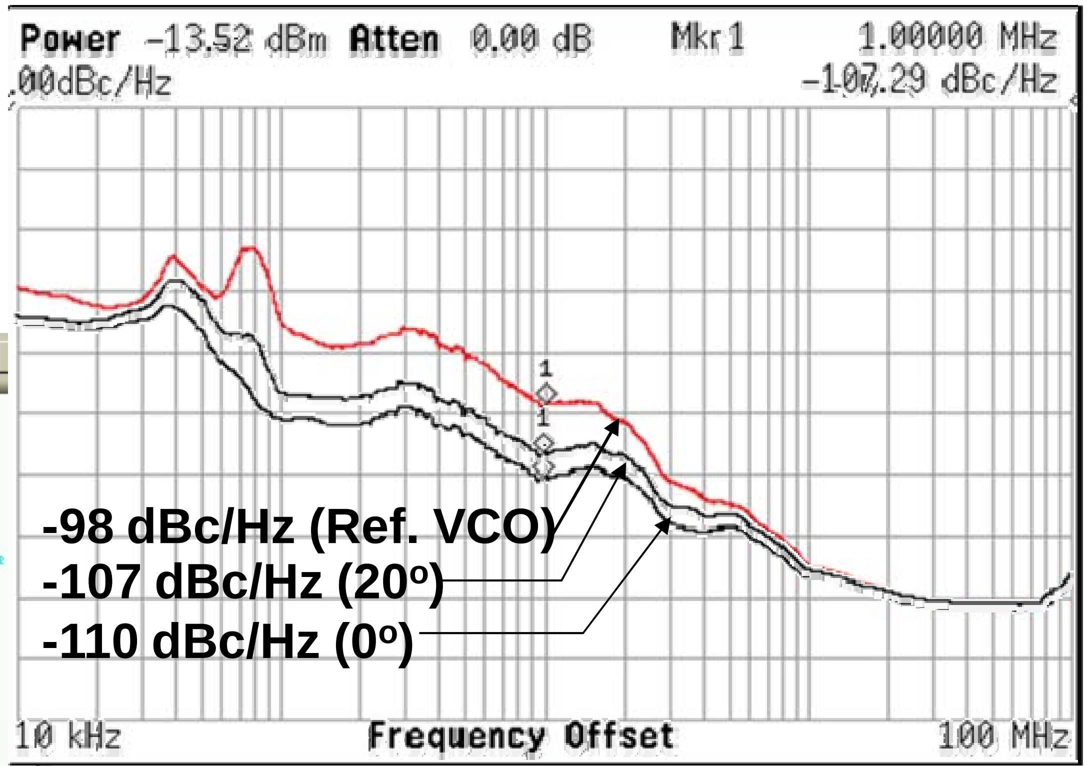




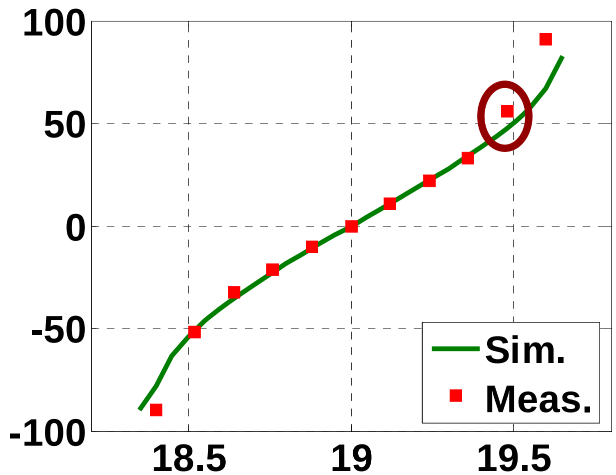
Jitter of Deskewed Clock

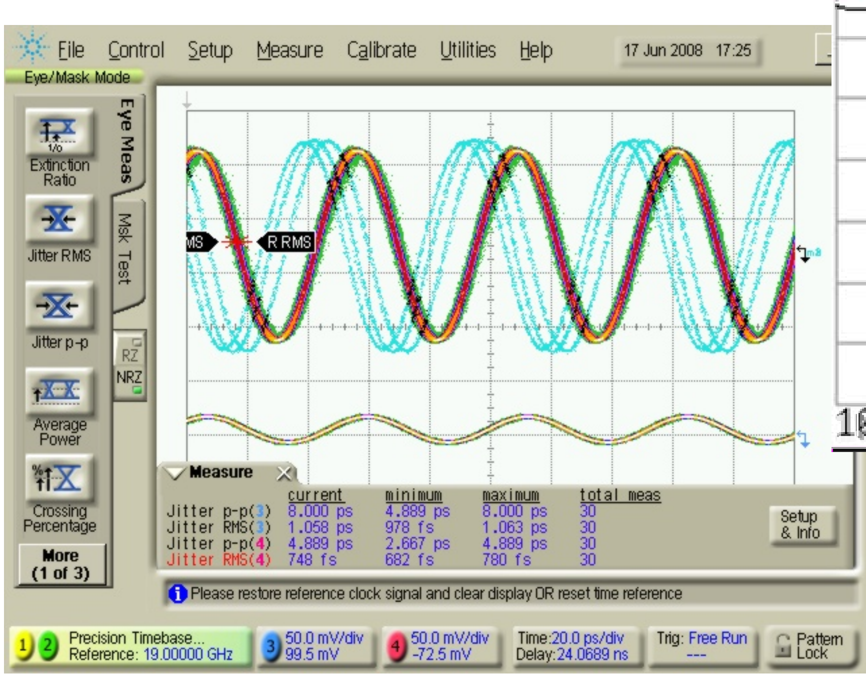


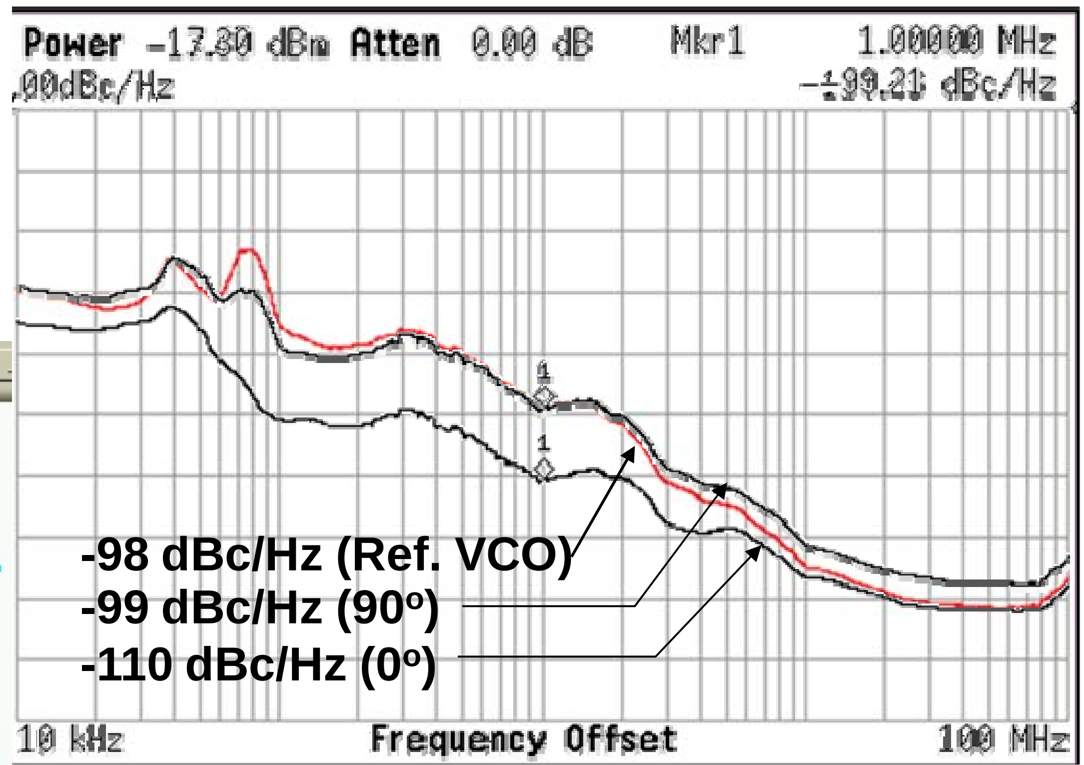




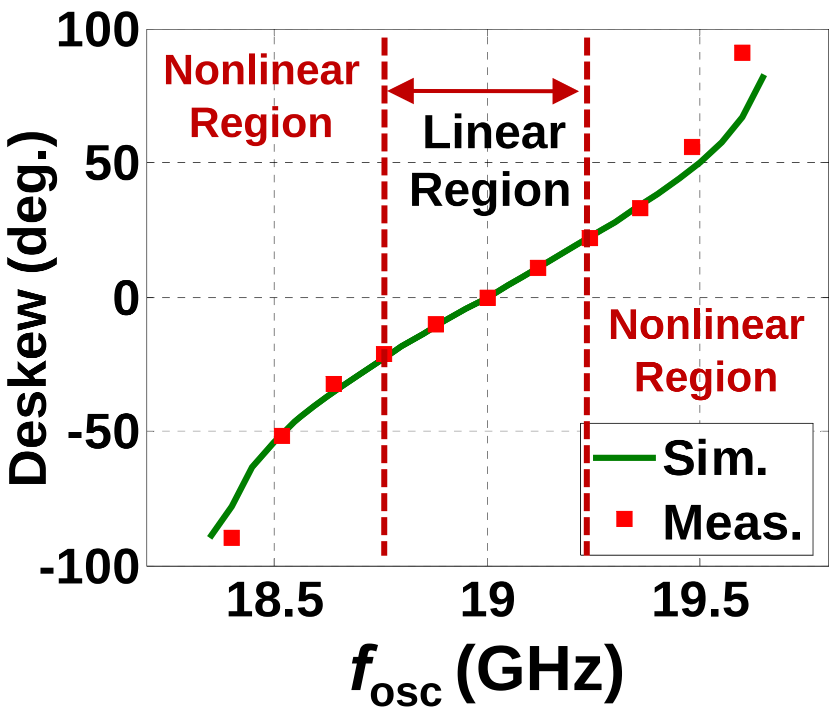
Jitter of Deskewed Clock







Summary: ILO Based Deskew



Linear Region (deskew< 50º)

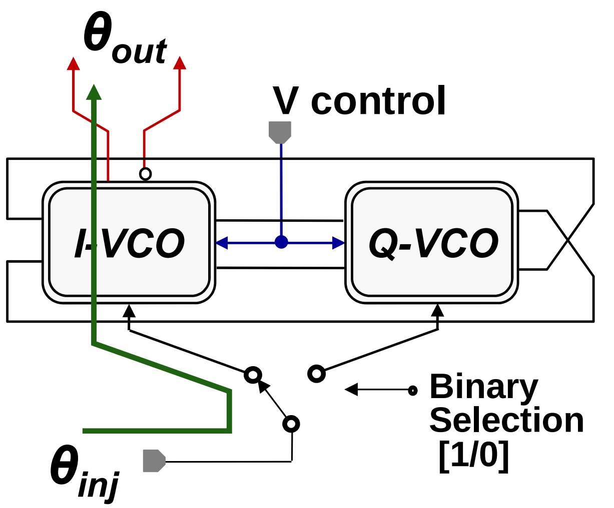
- ✓ Amplitude variation <10%
- ✓ Linear phase steps
- ✓ 12 dB jitter reduction @ 0º
  9 dB @ +/- 25º

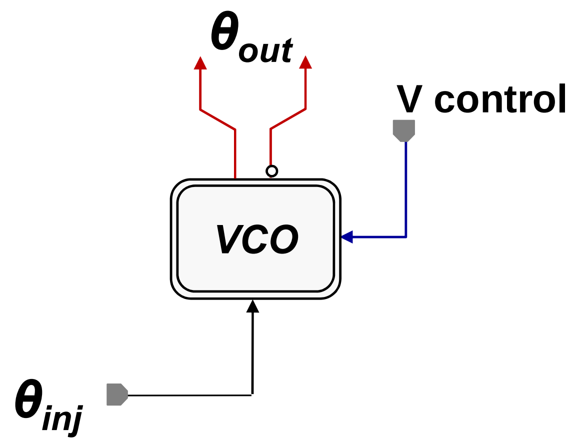
Nonlinear Region (deskew> 50º)

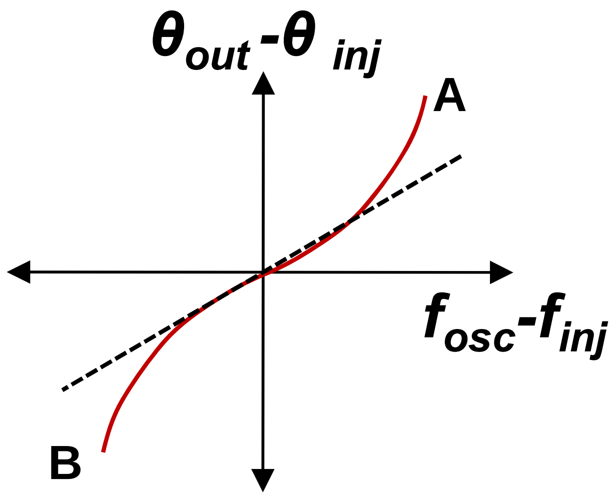
- ✖ Amplitude variation >20%
- ✖ Non-linear phase steps
- ✖ No jitter reduction at 90º

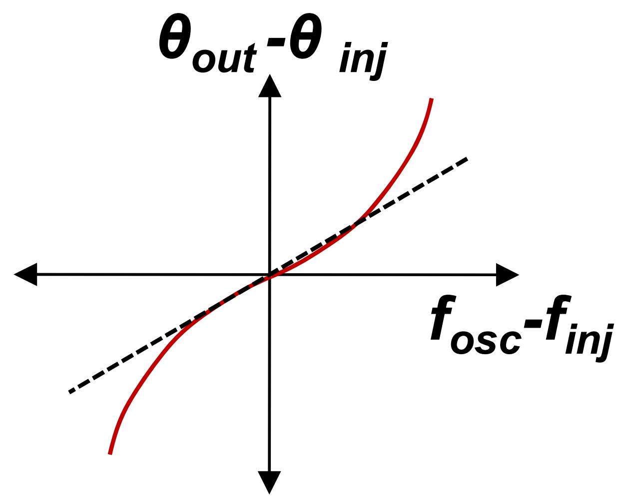
Motivation: Achieve 0-360º deskew range using only the linear region

Proposed Deskew Technique









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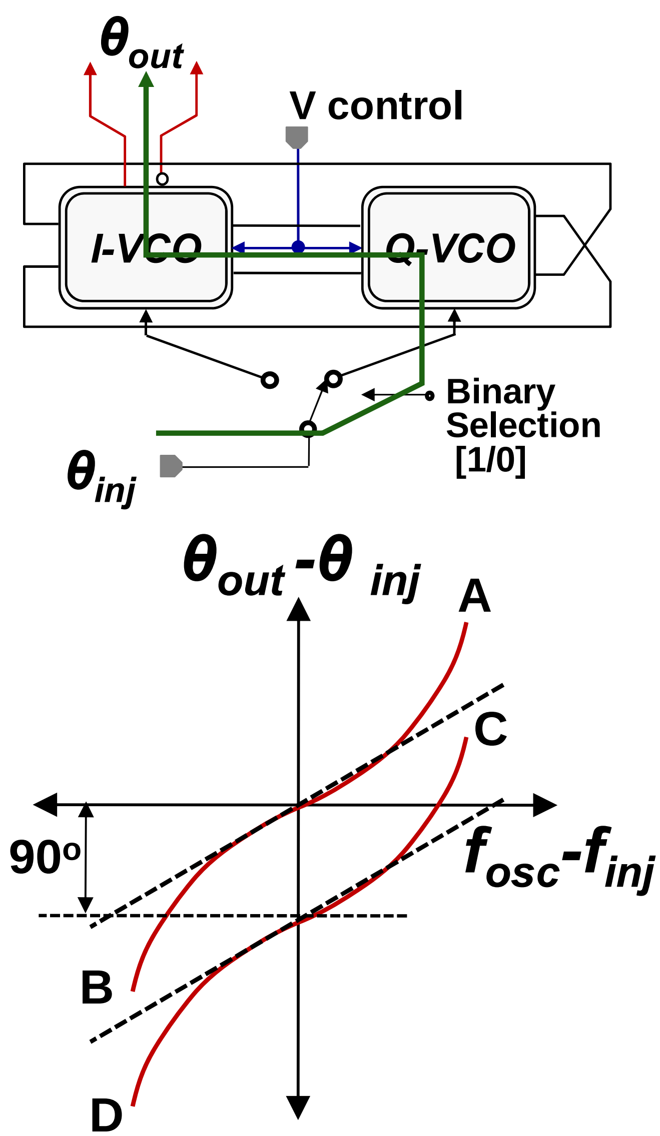

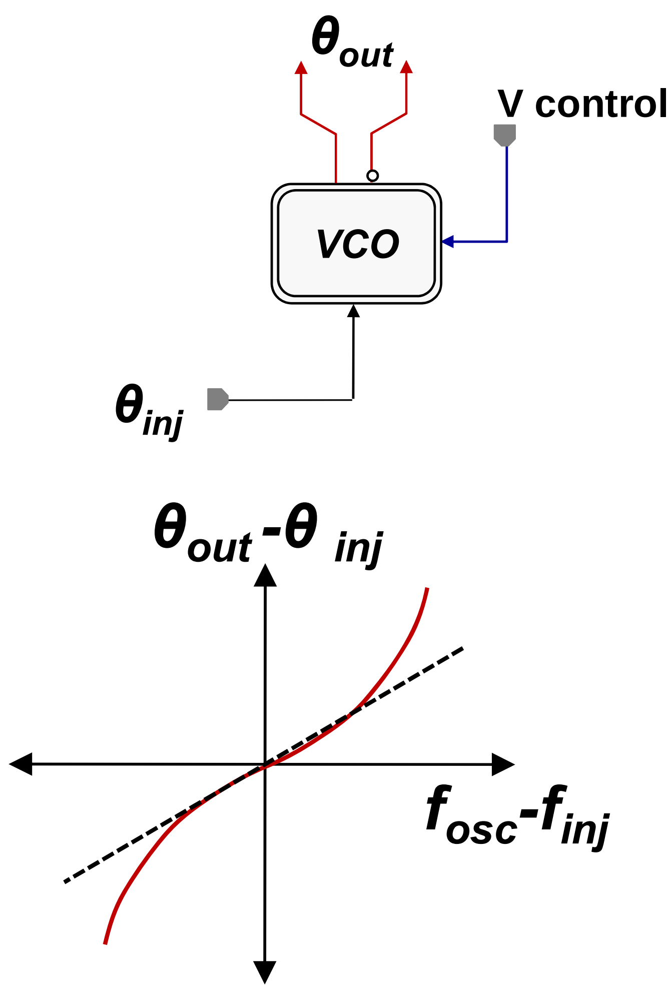

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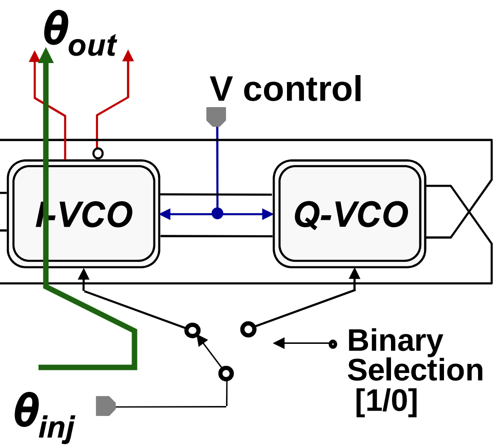
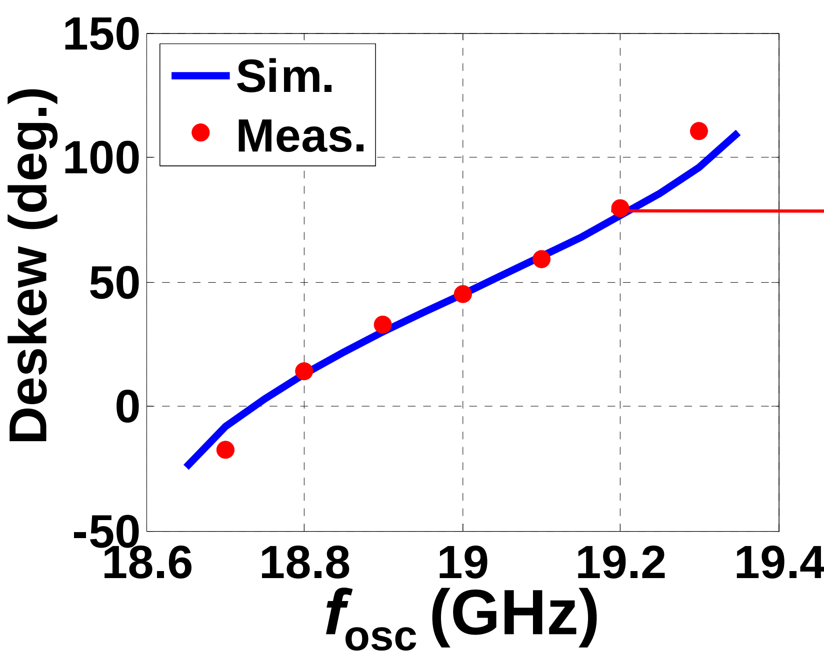
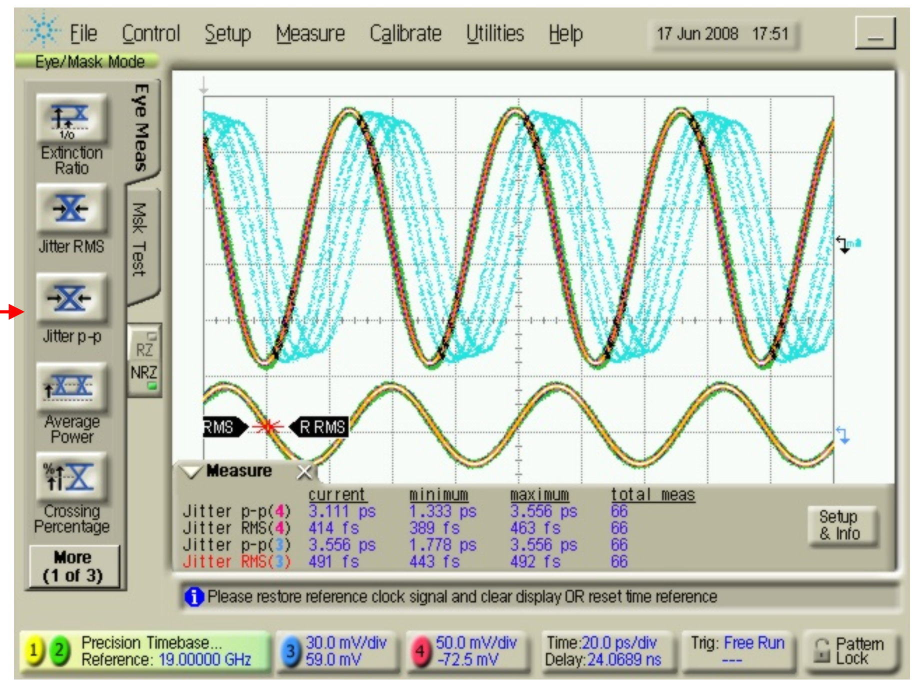
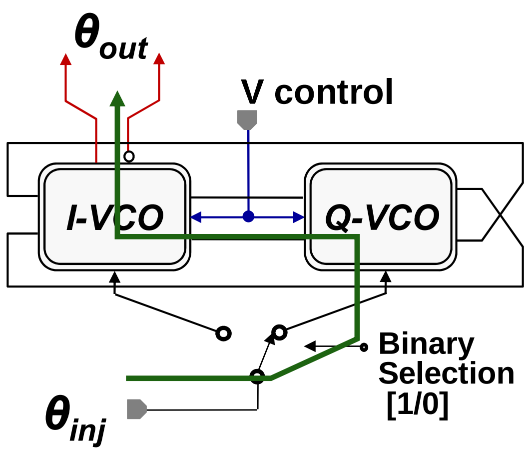


K=.125
Clock Amp=11.48 dB

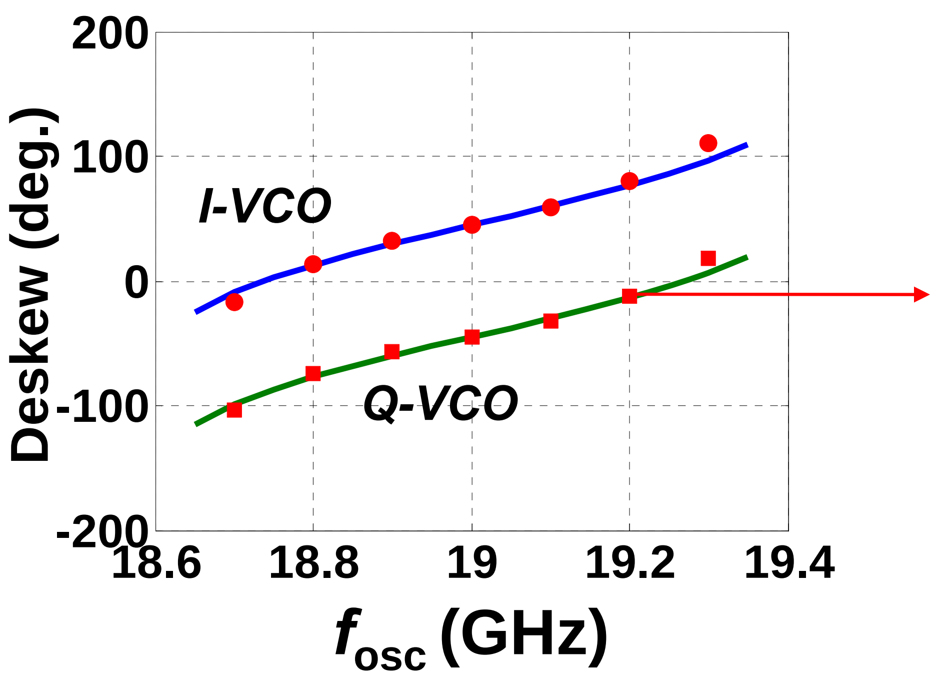


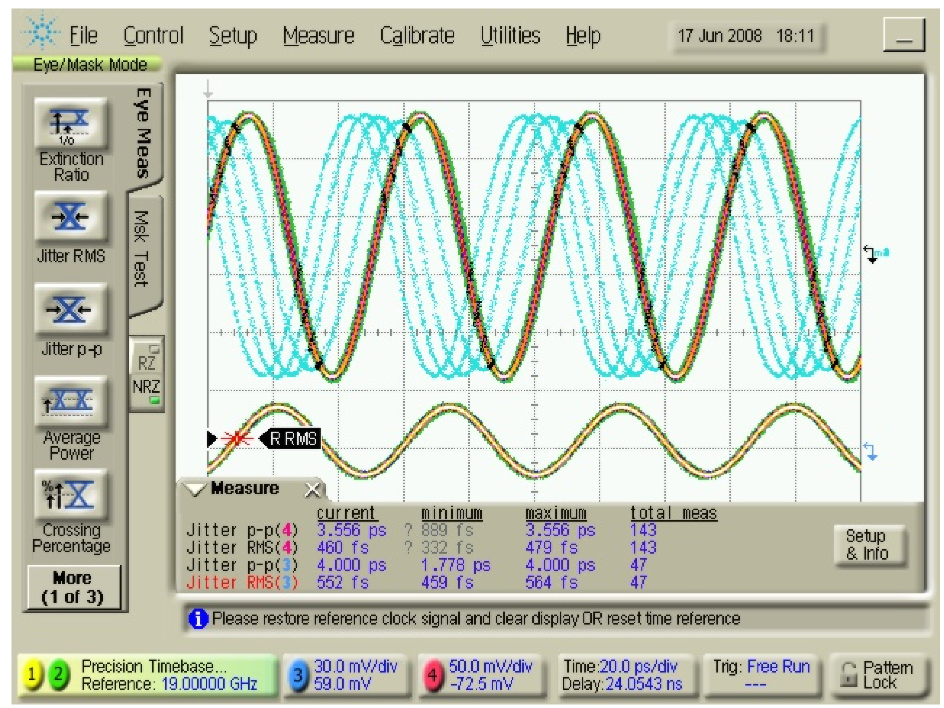


Proposed Deskew Technique

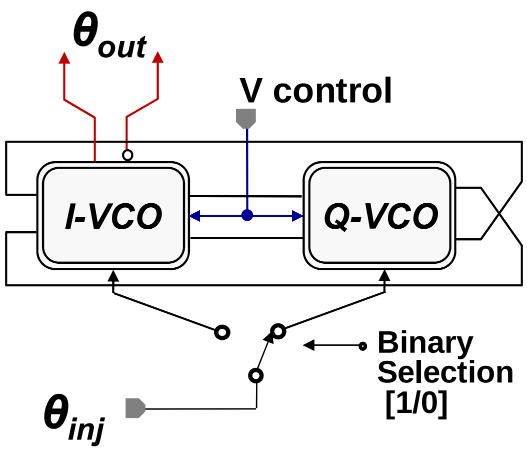


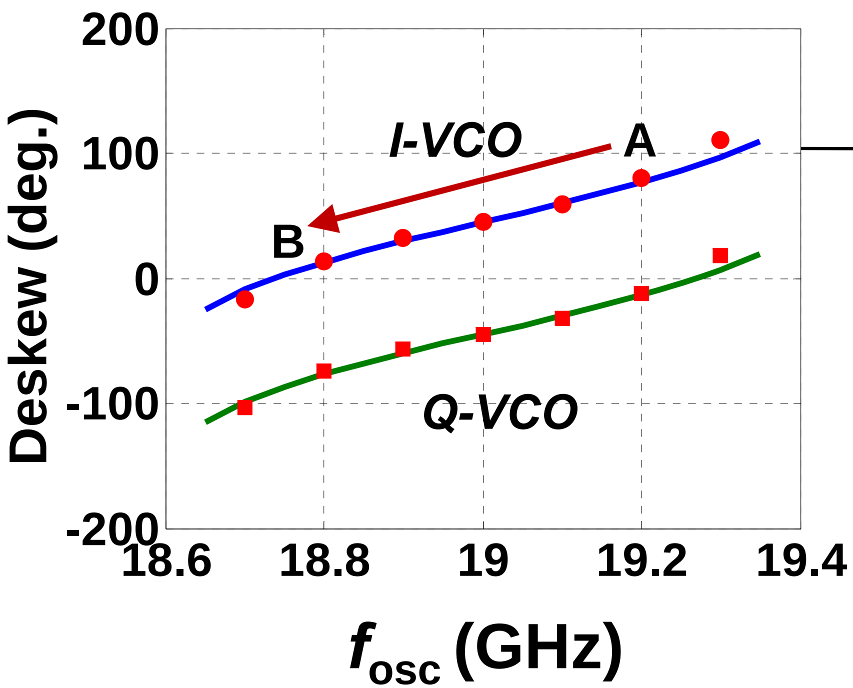
K=.125
Clock Amp=11.48 dB
Less Amplitude variation

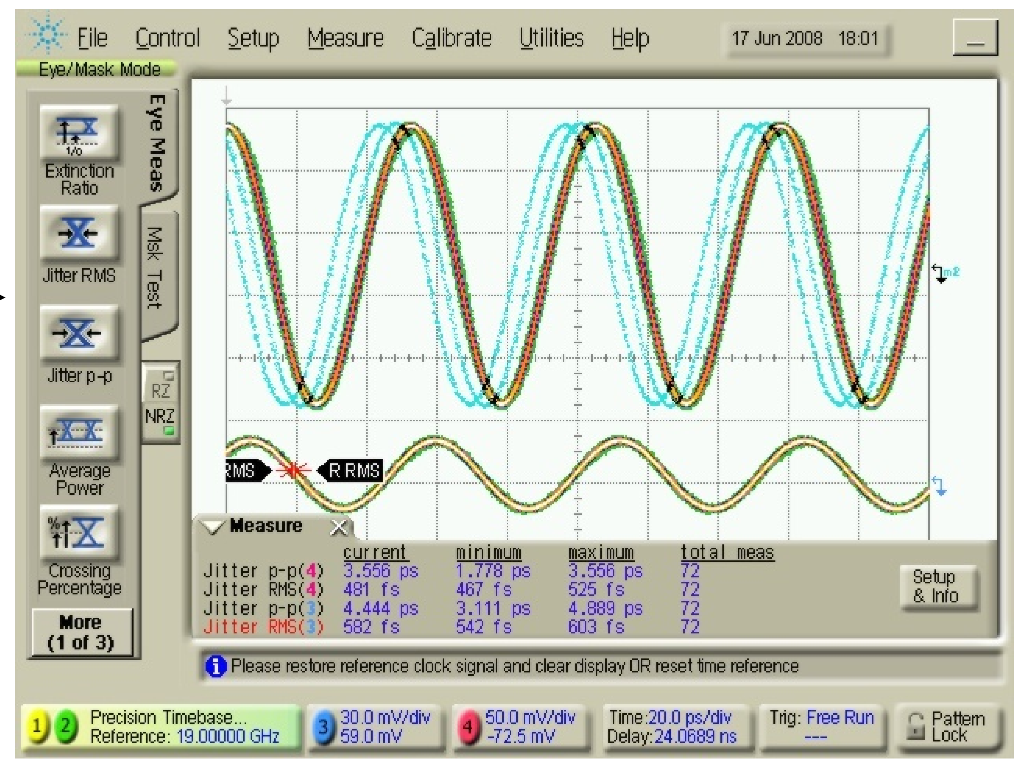




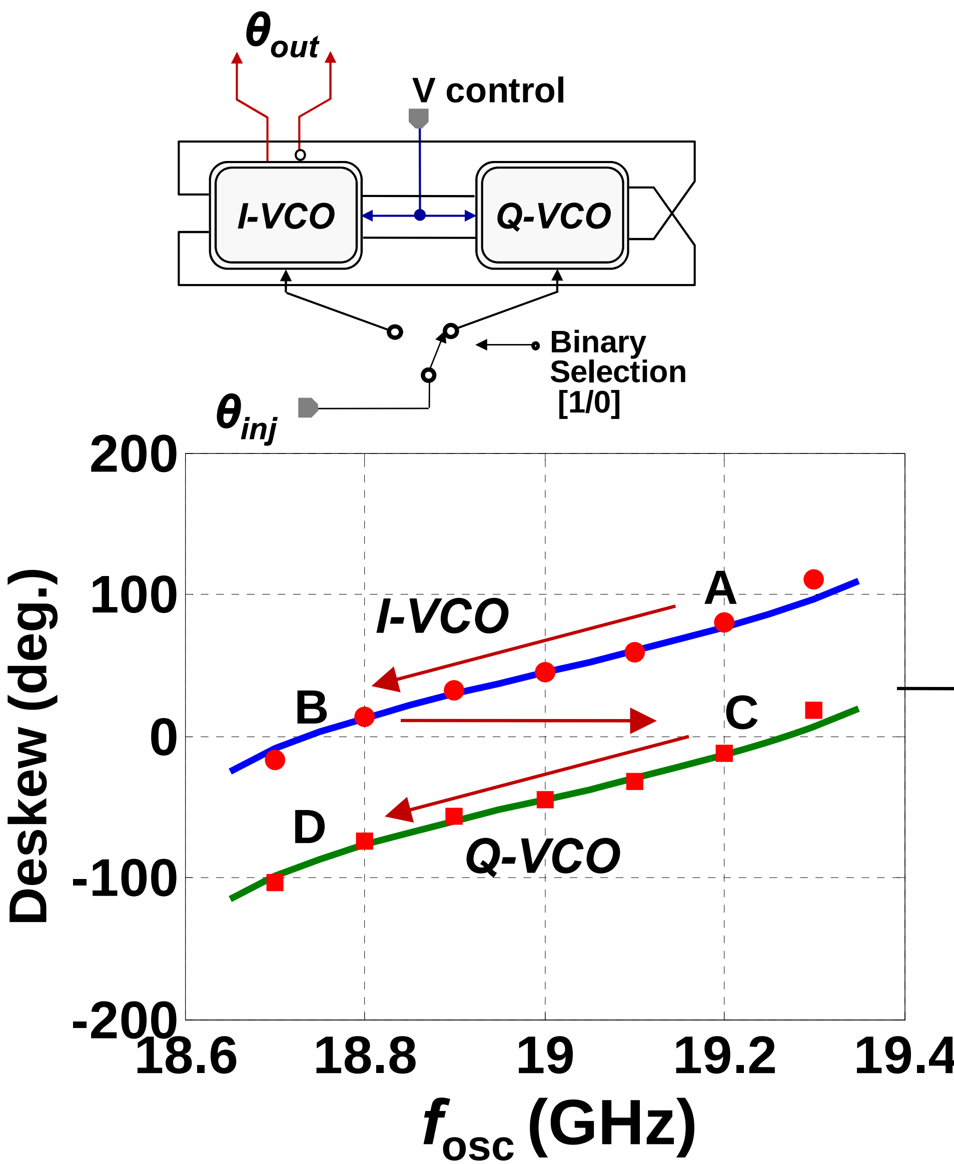
Proposed Deskew Technique

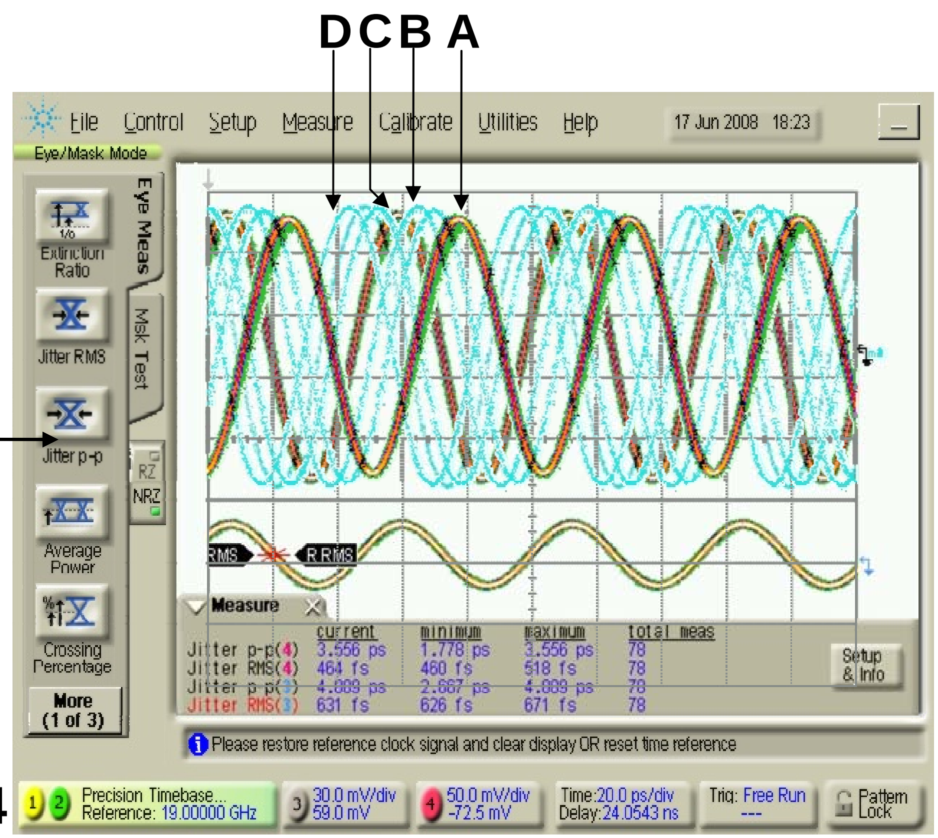




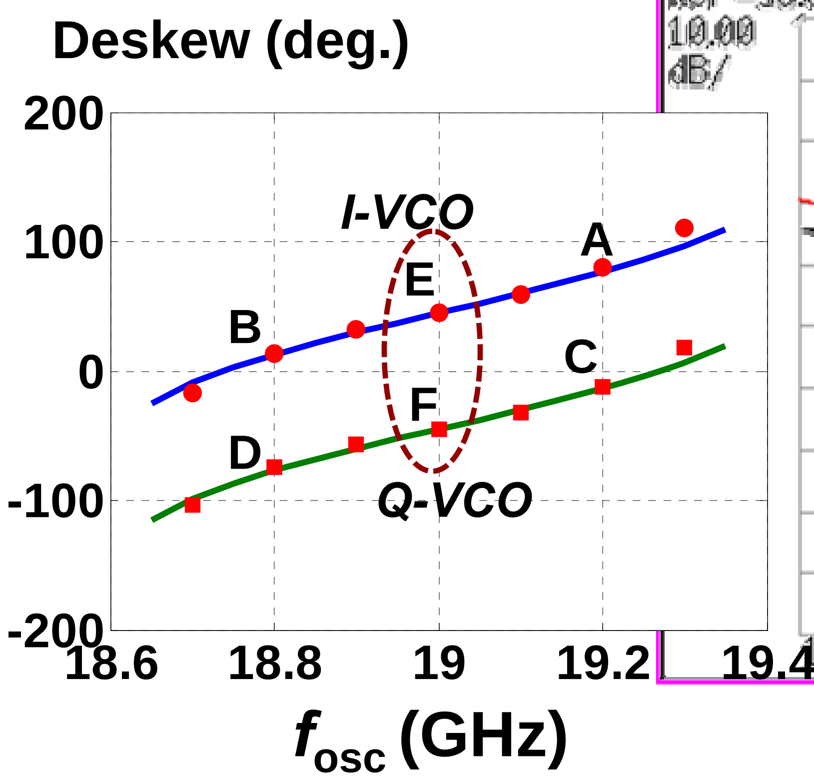


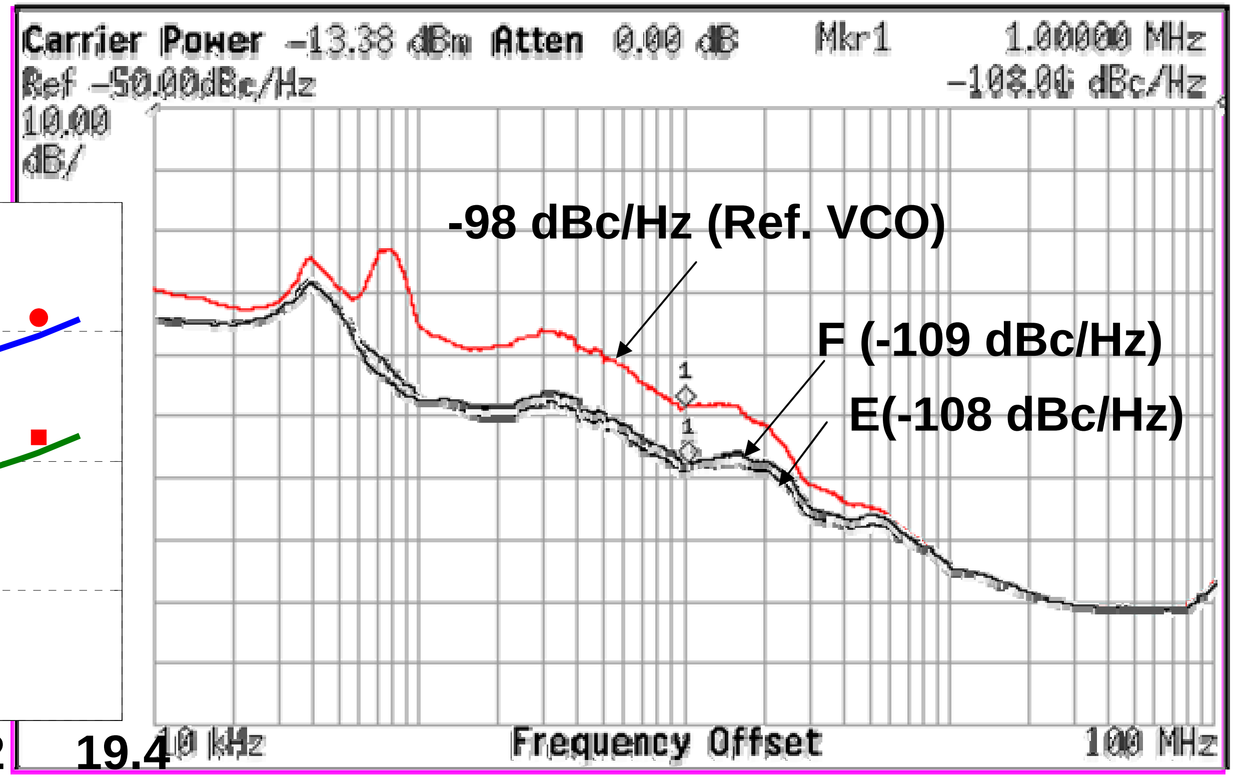
Proposed Deskew Technique



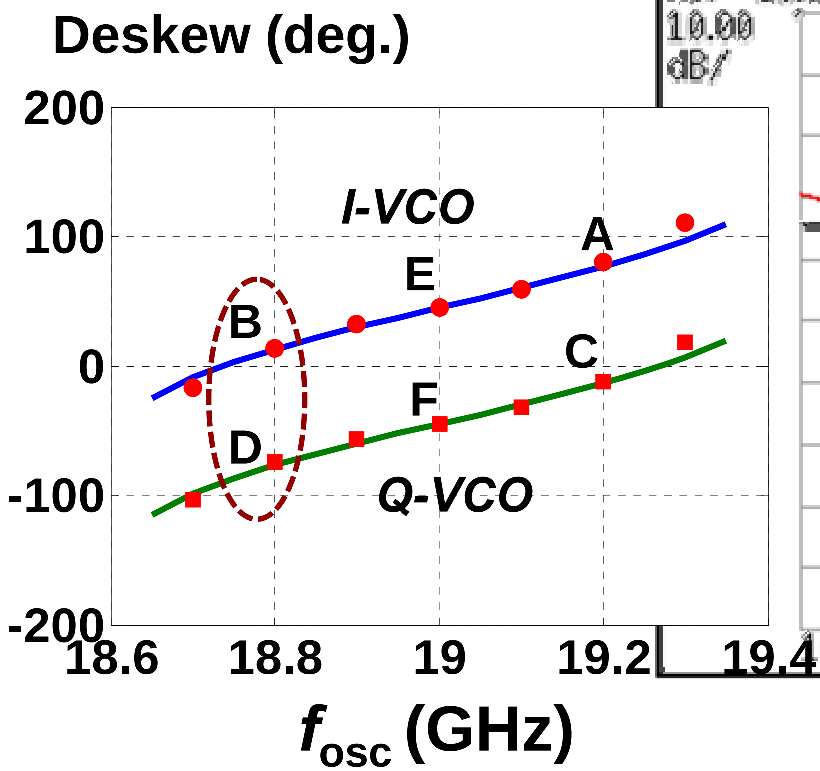


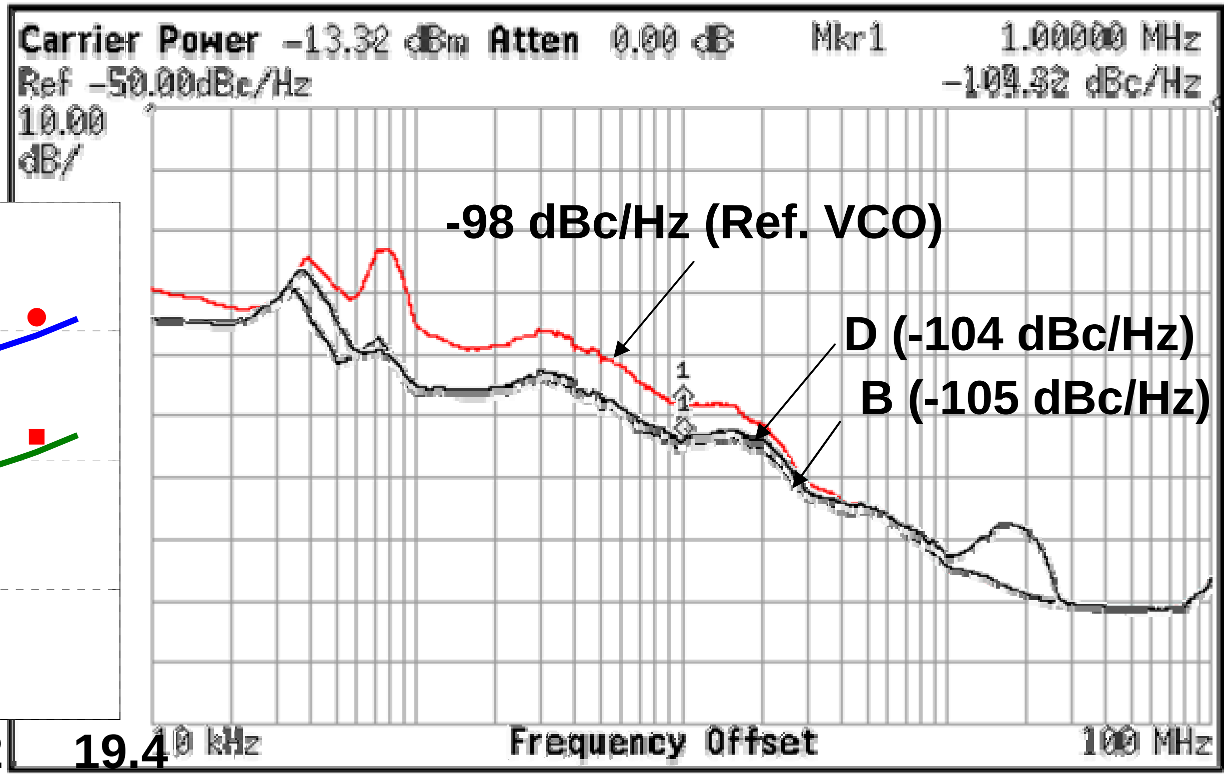
Proposed Deskew Technique



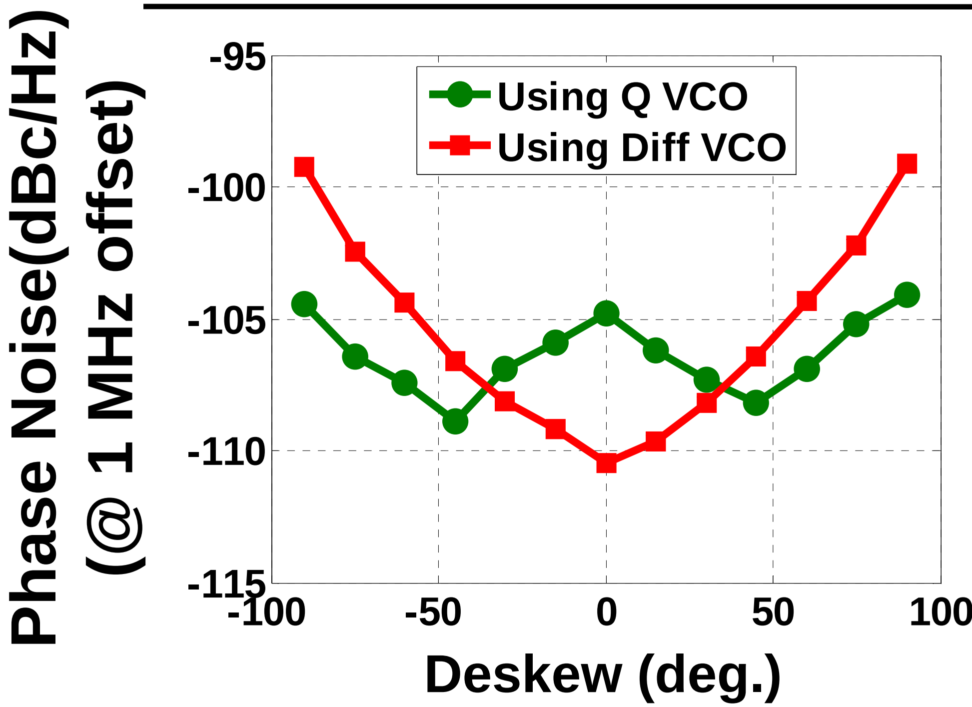


Proposed Deskew Technique





Comparison and Summary



We have introduced:

- **Low power Q-VCO topology for high-speed applications**
- **Utilize the QVCO based Deskew technique with inherent clock amplification and jitter filtering**

Acknowledgements

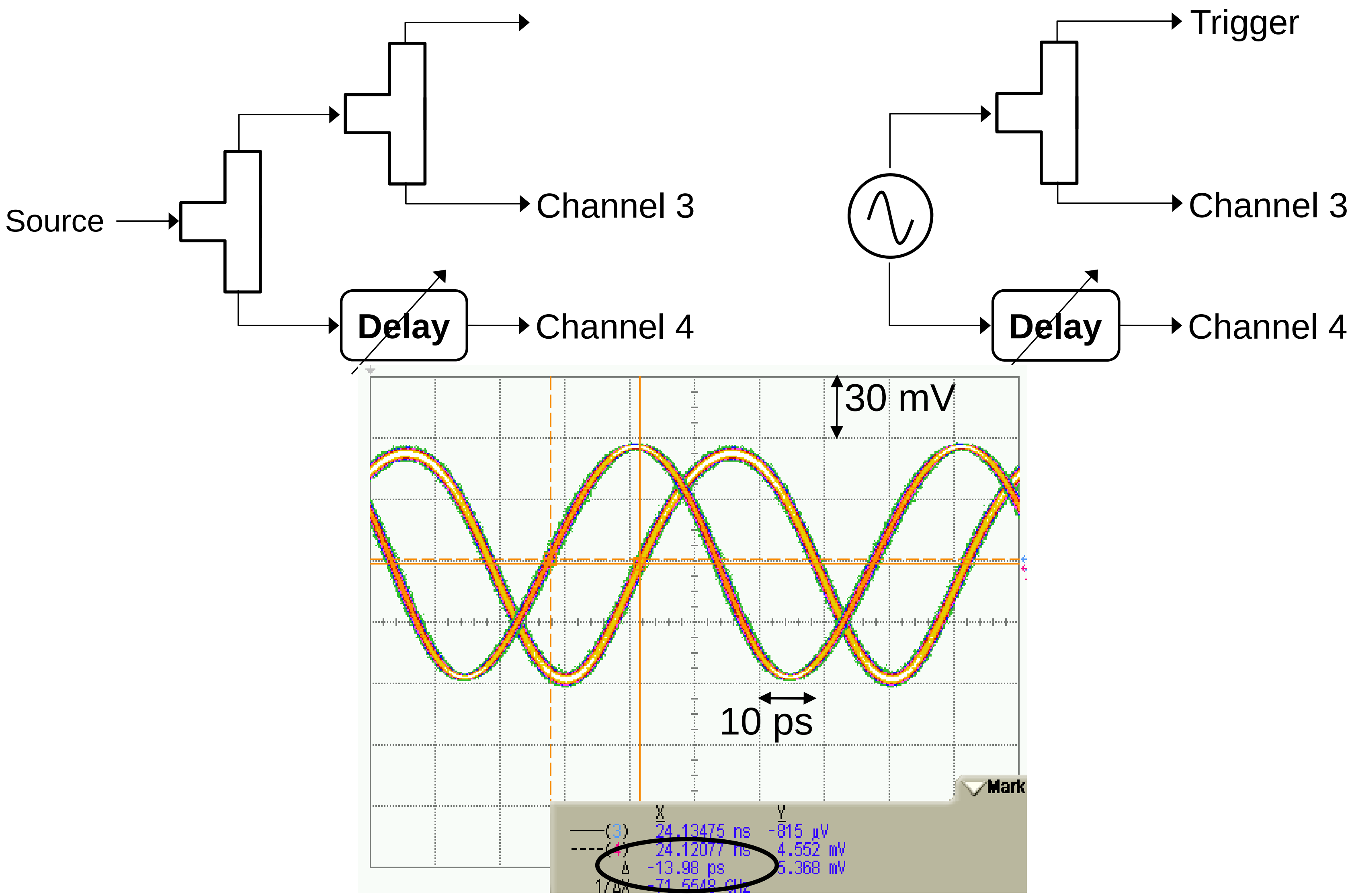
- **Intel Circuit Research Lab:**

  F. O'Mahony, M. Mansuri & B. Casper for their contribution in clock deskew technique presented in this work

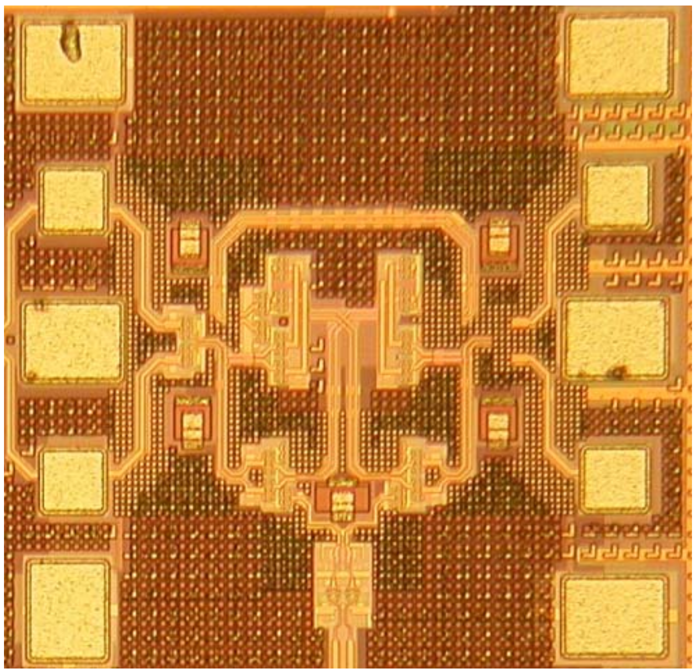
- **Gennum Corporation:**

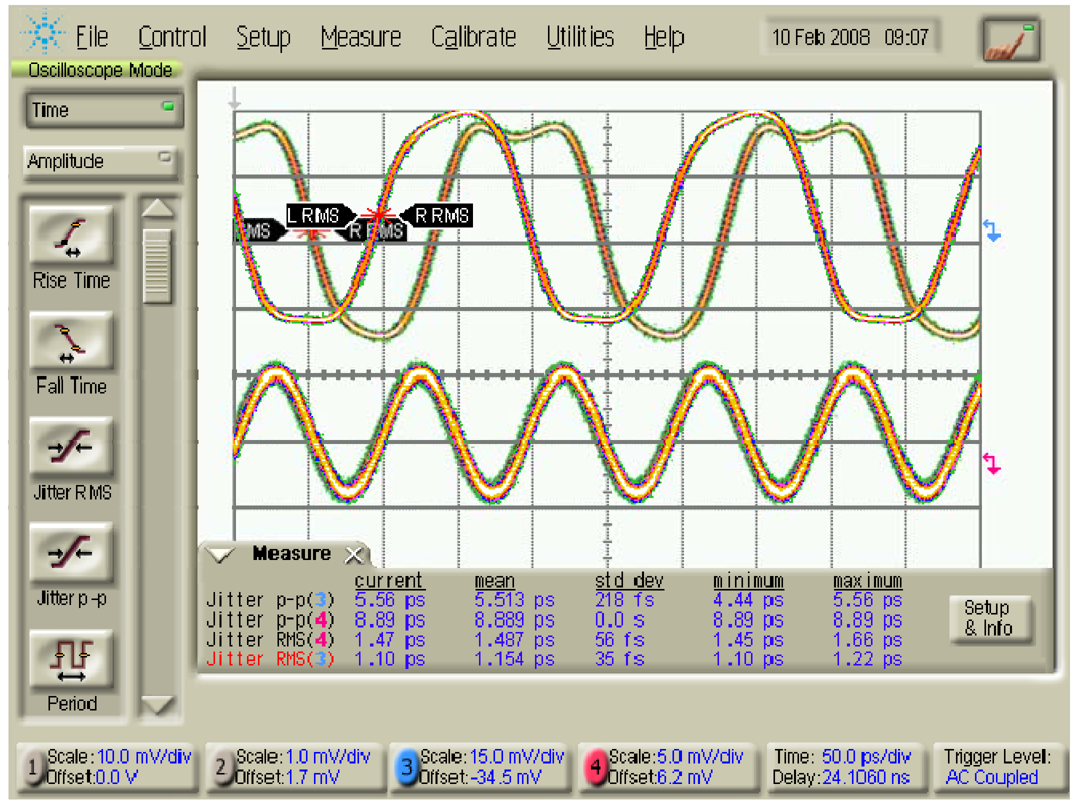
  For providing design & fabrication facilities

Backup Slide: Calibration



Backup Slide: Additional Verification





The same technique is also applicable with quadrature ring oscillator