A 5th Order Gm-C Filter in 0.25 mm CMOS with Digitally Programmable Poles and Zeros

Tony Chan Carusone, David A. Johns
tcc@eecg.utoronto.ca

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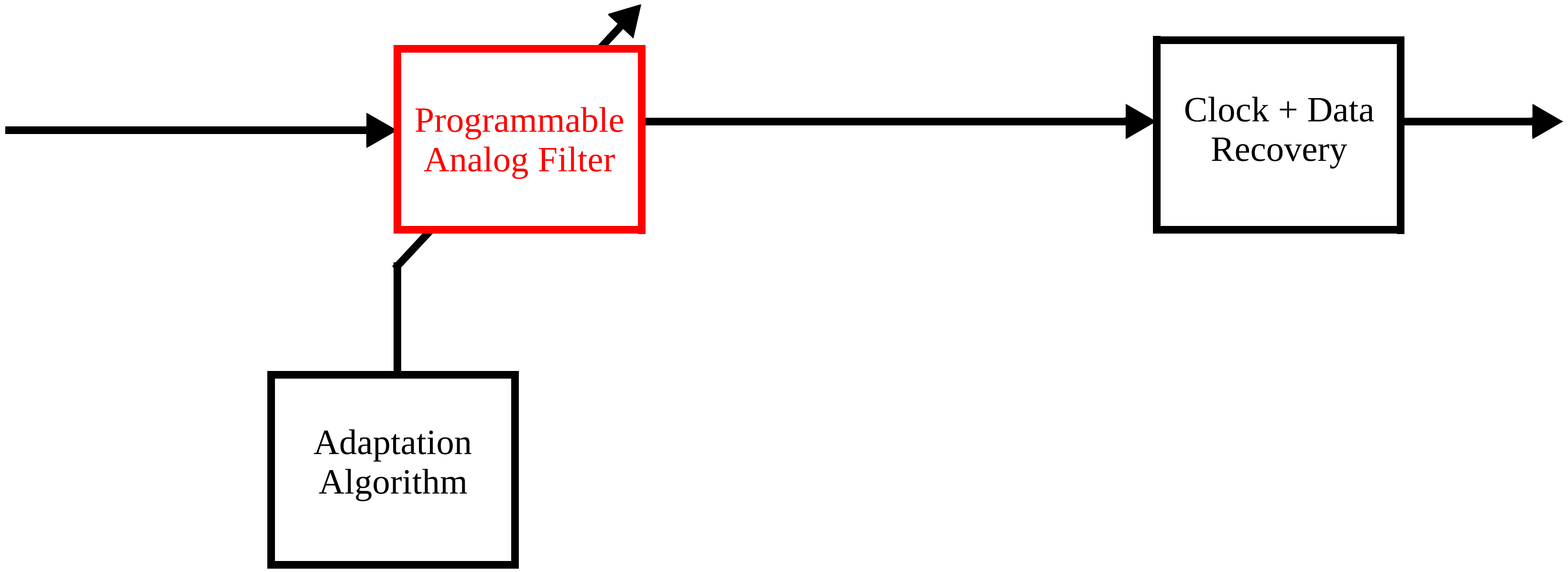
Outline

- Motivation - Analog Adaptive Filters
- Filter Design
  - filter structure
  - digitally programmable transconductor
- Results
- Conclusion

Motivation

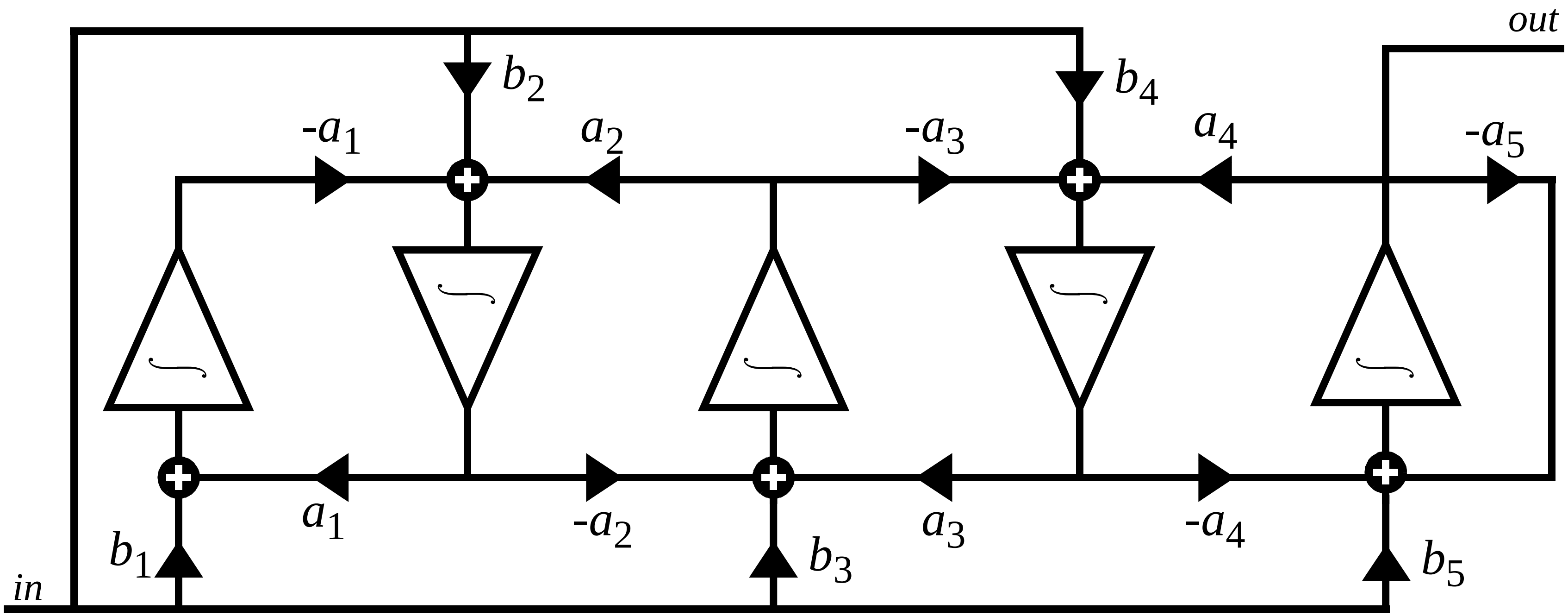
- Analog adaptive filters offer several important advantages in high speed mixed signal systems:
  - reduced specifications on the A/D converter
  - reduced specifications on the analog line driver (echo cancellation application)
  - moves the equalizer outside of the timing recovery loop
  - potential for power and area savings over digital filters (at high speeds and long impulse responses)



- Analog implementations of adaptation algorithms are not robust
  $\Rightarrow$ **digitally programmable analog filter**

Filter Structure

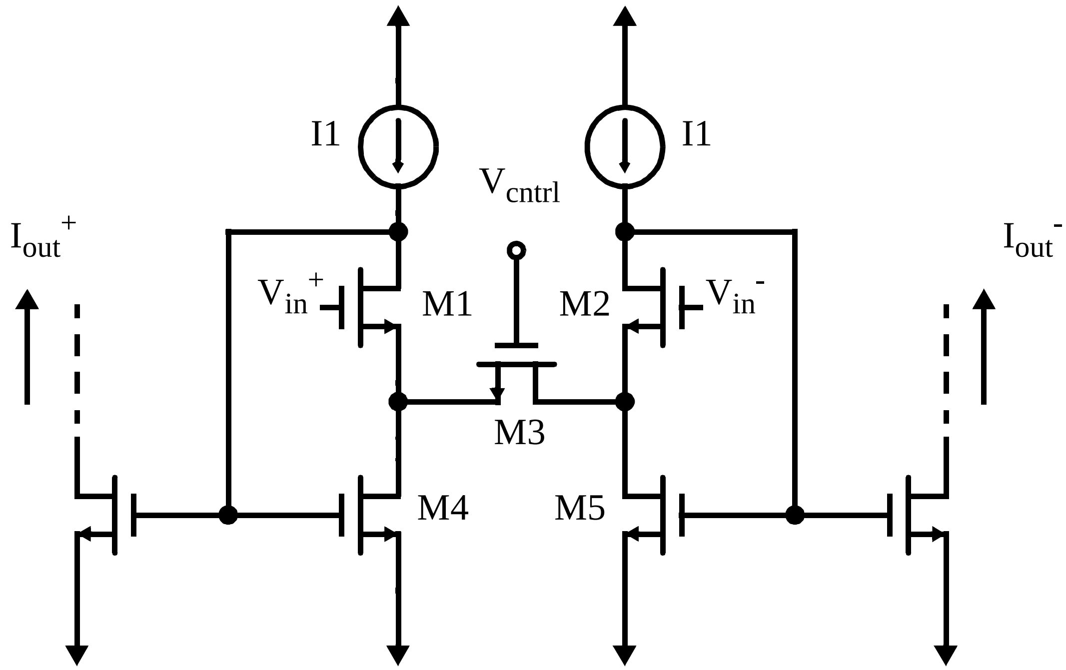
- continuous-time orthonormal ladder filter [Johns et al, *TCAS*, Mar '89]



- gains a_i and b_i are digitally programmable transconductors
  $\Rightarrow$ can realize any rational transfer function
- automatically scaled for optimum dynamic range

Digitally Programmable Transconductor

- fully-differential transconductor



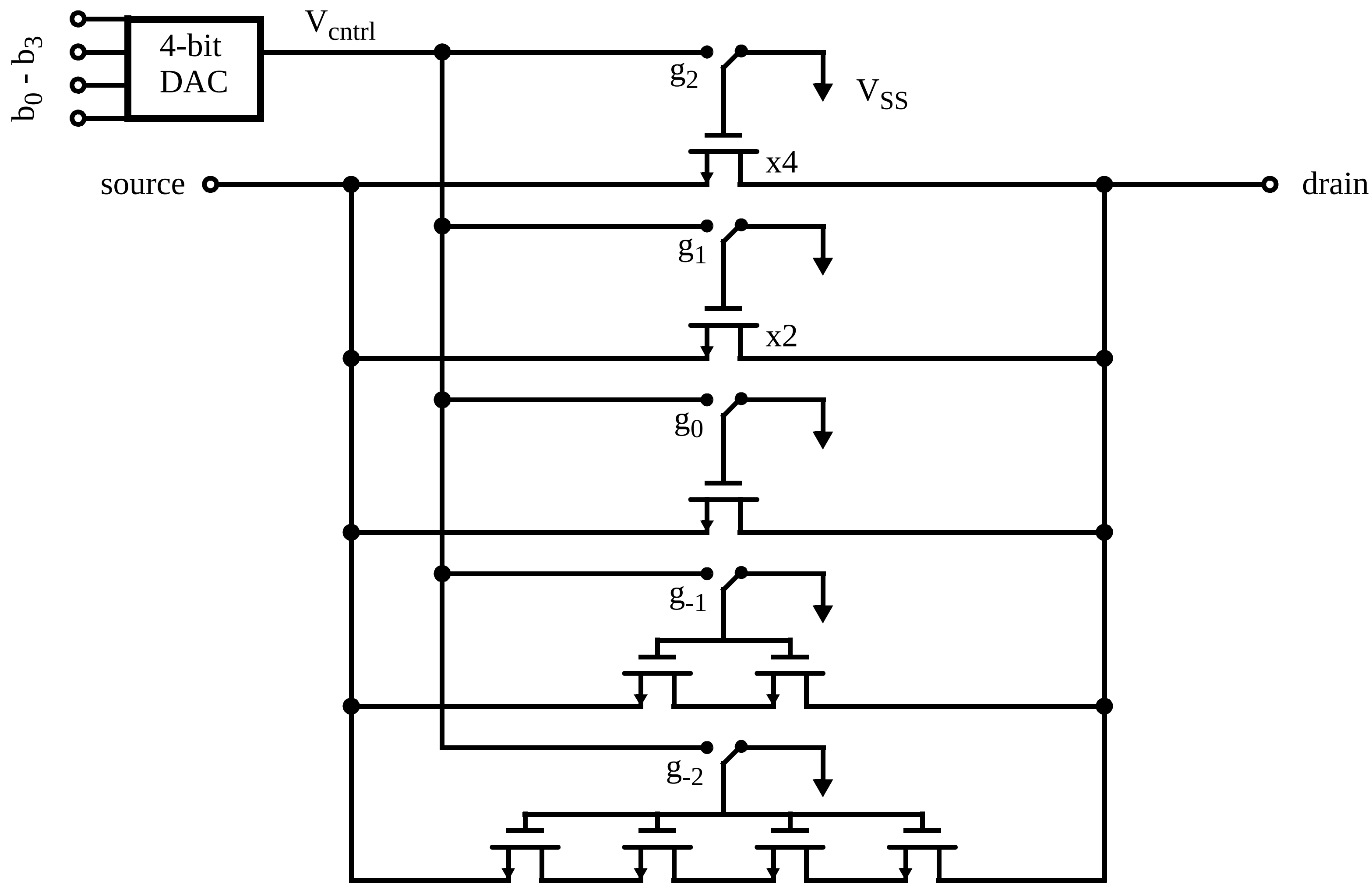
$$G_m = \frac{I_{out}^{+} - I_{out}^{-}}{V_{in}^{+} - V_{in}^{-}}$$

- G_m is proportional to triode-transistor, M3, conductance

$$G_{m(\mathrm{M3})} \propto \left(\frac{W}{L}\right)_{(\mathrm{M3})} \cdot V_{gs(\mathrm{M3})}$$

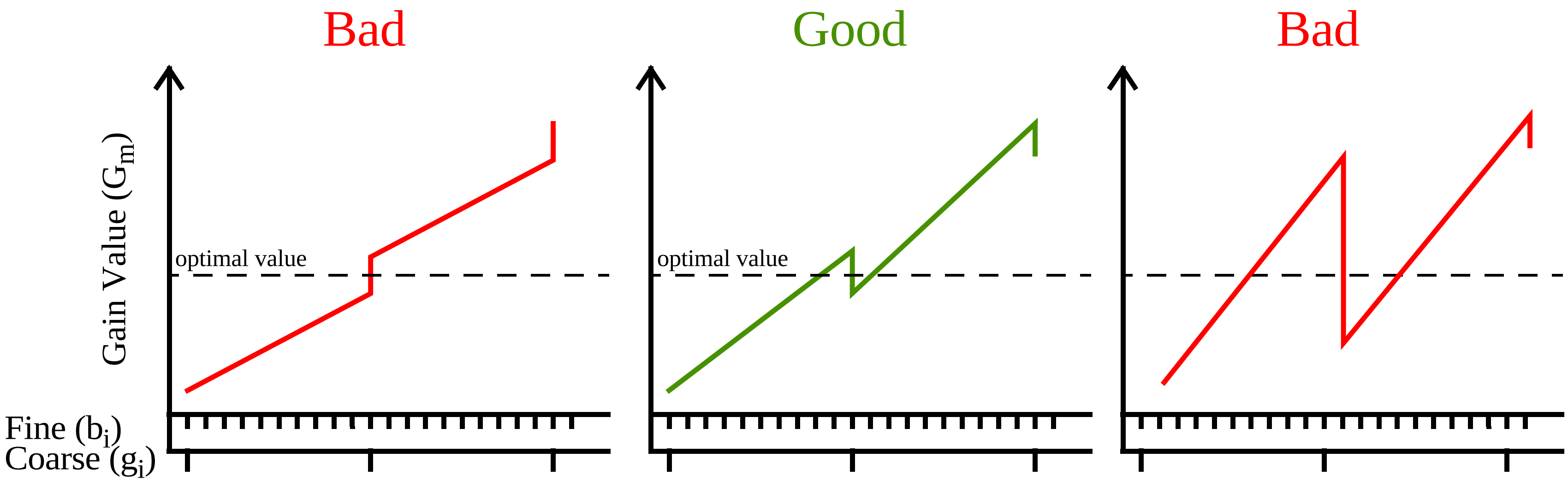
Digitally Programmable Transconductor

- 9-bit programmable conductance, M3

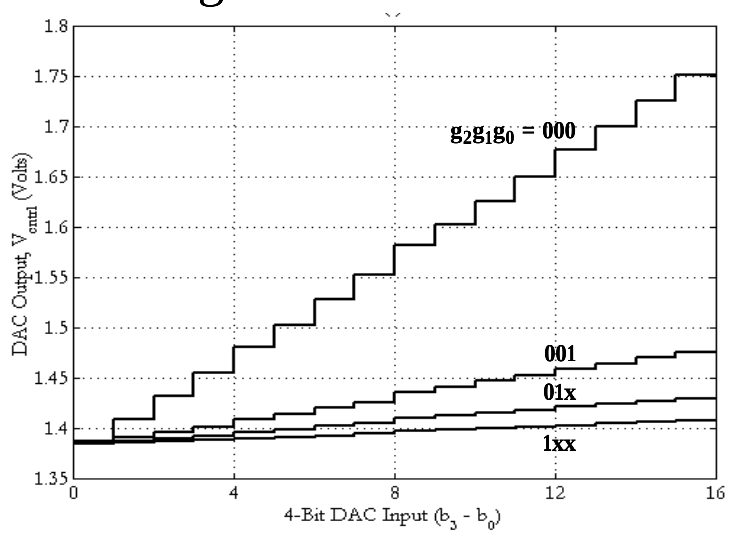


Digitally Programmable Transconductor

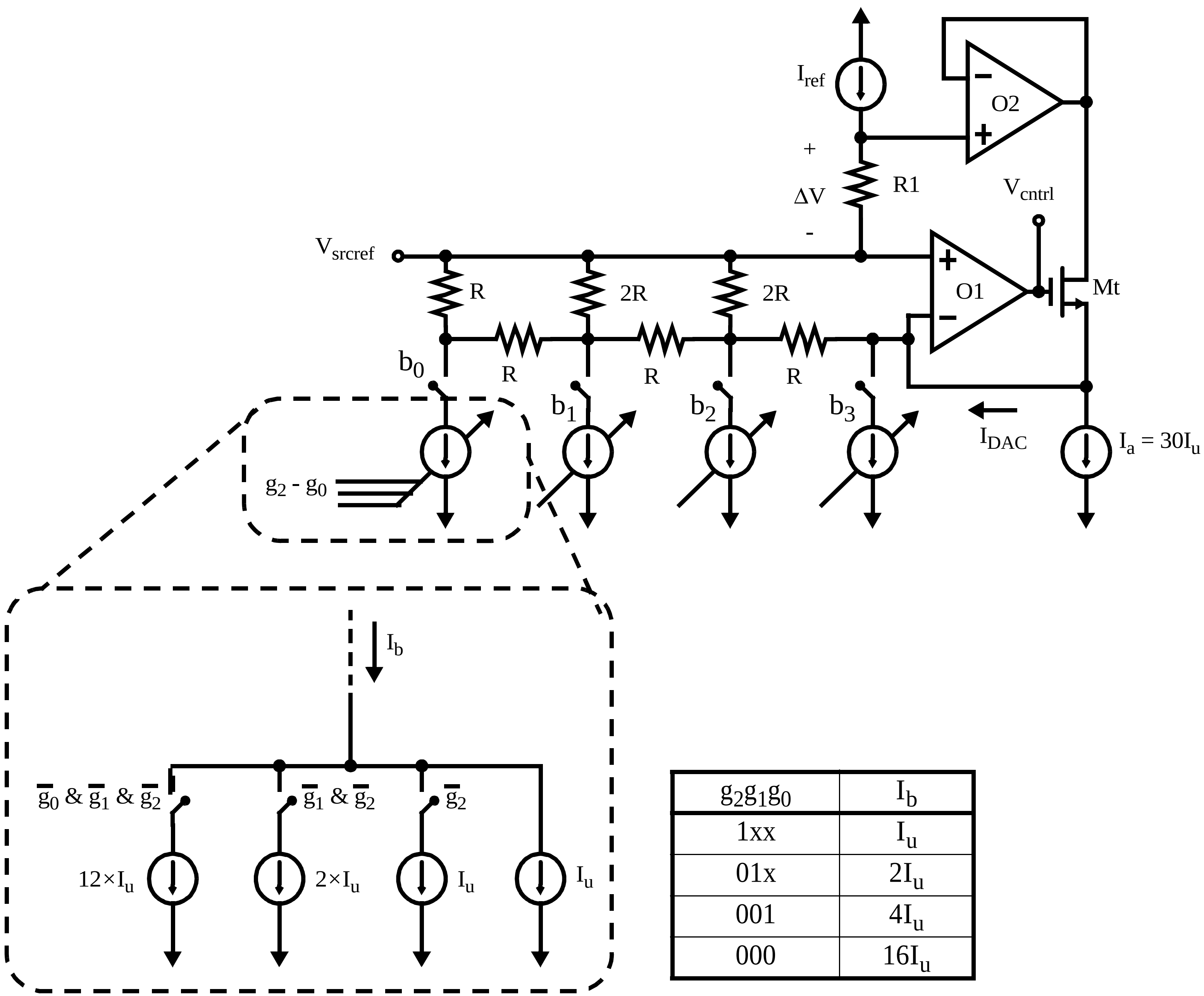
- hysteresis is required when two separate mechanisms control the same adapted parameter



- the fine control DAC range is a function of the coarse control bits

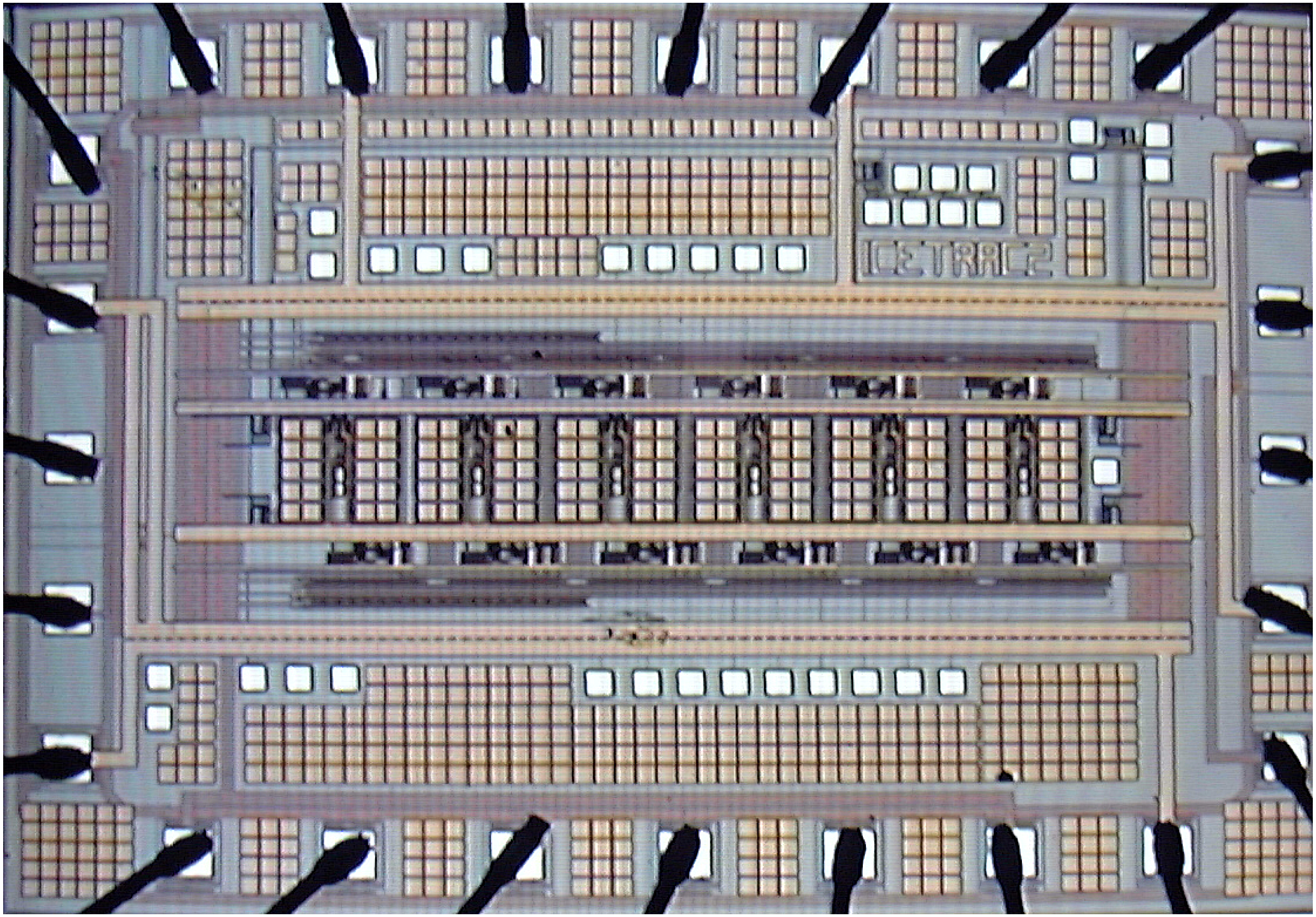


Details of the 4-bit DAC



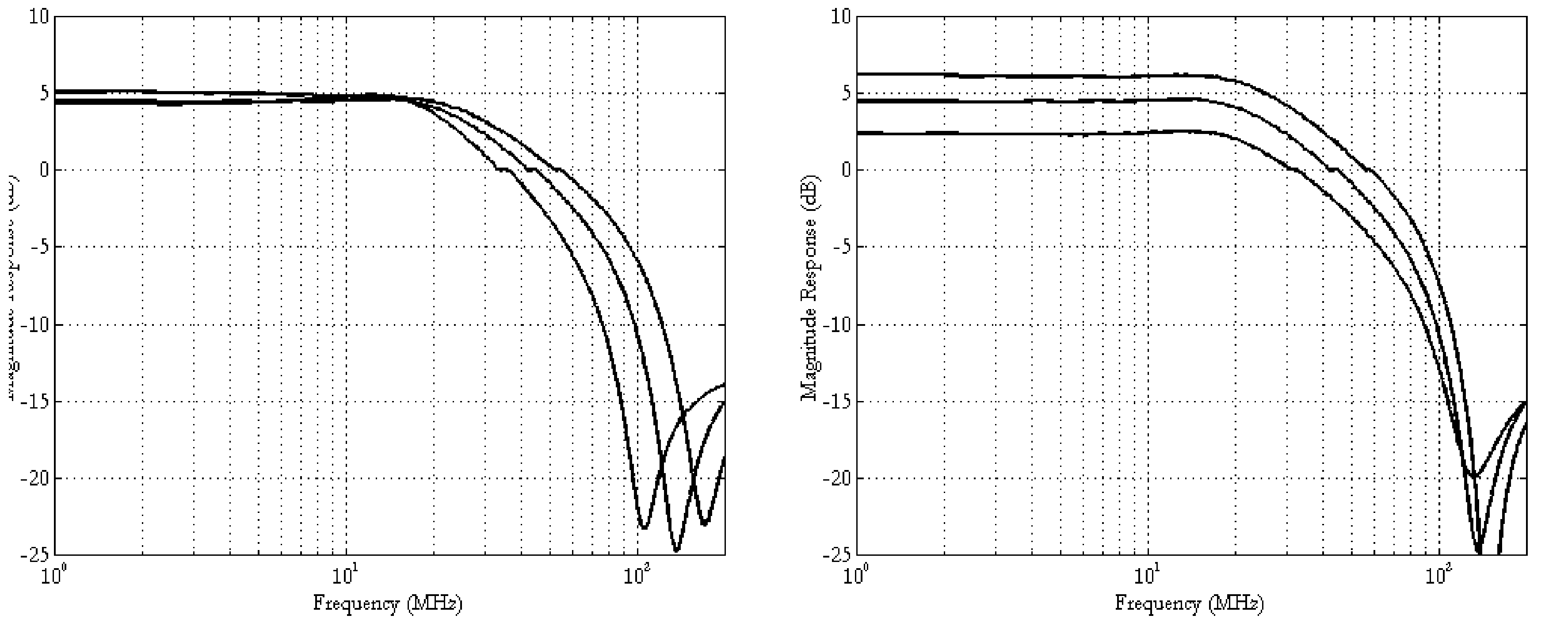
$g_2g_1g_0$	I_b
1xx	I_u
01x	$2I_u$
001	$4I_u$
000	$16I_u$

Die Photo



Experimental Results

- Lowpass filter with varying cutoff frequency and gain:



Experimental Results

Entire Prototype Gm-C Filter IC	
Technology	0.25 μm CMOS
Supply Voltage	2.5 V
Integrated Area	2.5 mm × 1.7 mm = 4.25 mm^2
Power	233 mW (Simulated) 250 mW (Measured)
First Order Filter Test Structure	
THD with 200 mVpp input, 120 mVpp output tone at 8 MHz	-41 dB
5th Order Lowpass Orthonormal Ladder Filter Core (40 MHz passband)	
Integrated Area	1.25 mm × 0.38 mm = 0.469 mm^2
Power with 9-Bit Programmable Coefficients	130 mW (Simulated)[a]
Power with 5-Bit Programmable Coefficients	87.5 mW (Simulated)[a]
Noise Power	1.656 mVrms
THD with 125 mVpp input, 170 mVpp output tone at $f_{3\,dB}/2$	-27.7 dB[b]
SFDR with input tone at $f_{3\,dB}/2$	30 dB[c]

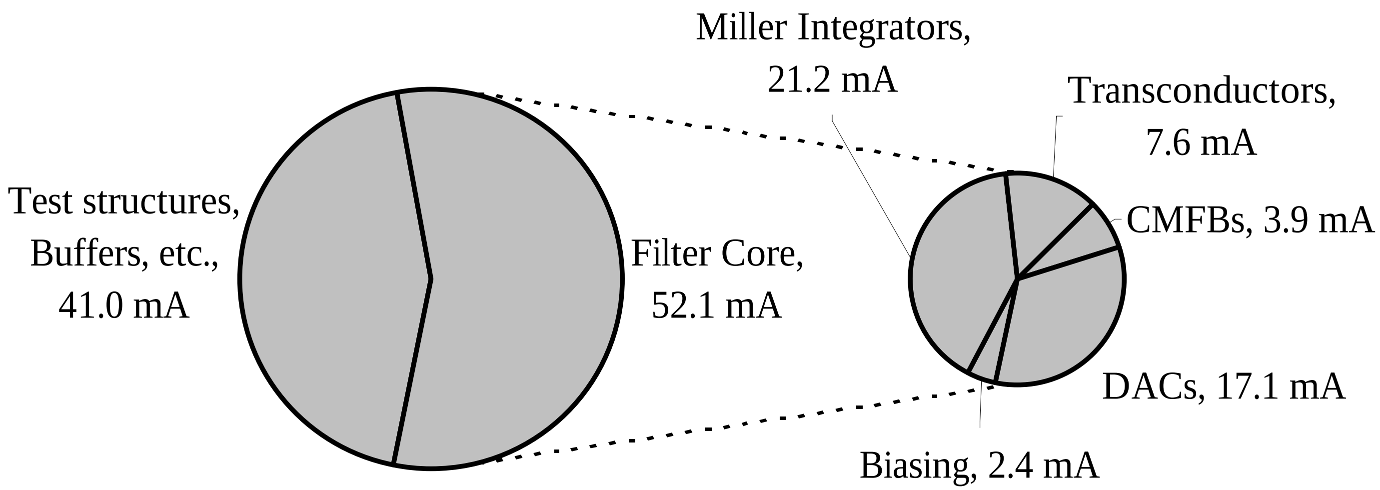
a. Includes shared bias circuitry.

b. Measurements for different transfer functions varied between -20 dB to -30 dB.

c. Corresponds to input amplitude of 105 mVpp and output amplitude of 145 mVpp.

Current consumption of the prototype by block

Entire Prototype IC = 93.1 mA



Conclusions

- circuit techniques for digitally programmable analog filters in CMOS were explored
- a 5th order filter with digitally programmable poles and zeros was developed
- the speed of operation is faster than any previously reported filter with this degree of programmability (although the linearity is limited)