A Baud-Rate Timing Recovery Scheme With a Dual-Function Analog Filter

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***Abstract*—This brief presents a baud-rate timing recovery scheme that is aided by signals generated from a dual-function analog filter. The analog filter functions as a simultaneous low-pass and bandpass filter to generate the data and its slope, respectively. Peaking is introduced in the low-pass data path to equalize a lossy channel. The timing recovery loop utilizes the equalized data and slope signals obtained from the dual-function analog filter to recover a clock based on a modified minimum mean squared error (MMSE) criterion. Unlike previously published baud-rate techniques for multigigabit per second nonreturn-to-zero data, this technique can lock to either random or alternating data patterns, even from a closed eye. As a proof of concept, a prototype dual-function analog filter was fabricated in a 0.18-μm CMOS process and used to recover a 2-GHz clock from a 2-Gb/s $2^{31}-1$ random data sequence based on the modified MMSE criterion.**

***Index Terms*—Analog filter, baud-rate timing recovery, CMOS, linear equalizer, minimum mean squared error (MMSE).**

I. Introduction

TIMING recovery (TR) is one of the most challenging receiver functions in modern serial data transmission systems. CMOS implementations of TR techniques can be divided into two categories: 1) deductive; 2) inductive. Deductive techniques generate a timing tone at the data rate by passing the received data waveform through a nonlinearity (such as a squarer) and a phase-locked loop (PLL) is used to lock a low jitter clock to this tone. An example is the nonlinear spectral line method [1]. However, this method requires a high excess bandwidth of the transmitted signal and a high Q filter for achieving an acceptable bit error rate (BER). Inductive methods simply comprise a PLL whose phase detector can extract timing information directly from edge samples of the incoming data [2] or from baud-rate samples [3].

Baud-rate techniques above 1-Gb/s have been reported in [3] and [4]. In [3], the baud-rate TR loop relies on an integrating receiver and requires specific 4-bit patterns for correct phase updates; thus resulting in low phase detector gain. Moreover, the low-pass characteristics of integrating front end receivers make them prone to intersymbol interference (ISI). In [4], the TR loop relies on the Mueller–Muller (MM) timing function [5]. Although hardware efficient, the MM function is only applicable for uncorrelated random data. Consequently, alternating data patterns may cause the timing loop to lose lock. This work focuses on removing these limitations by utilizing a modified version of minimum mean squared error (MMSE) TR.

MMSE TR [6], [7] basically uses the slope information of the incoming data signal to achieve lock between the data and the receiver clock. This scheme allows the TR loop to lock to either random or alternating data patterns. Also, MMSE possesses the unique property of tracking the maximum data eye opening instead of the midpoint between two transitions as in edge-sample based TR schemes [8]. Therefore, MMSE offers an excellent alternative to the baud-rate schemes reported in [3] and [4].

Detecting the slope of the input data is the main challenge in implementing MMSE for high-speed applications. Also, MMSE requires an extra latch to generate the error signal in the phase detector [8]. This brief presents a modified MMSE algorithm that excludes the error signal from the TR loop for nonreturn-to-zero (NRZ) data. It also presents an analog filter that performs continuous-time slope detection and linear equalization simultaneously and thus provides a hardware-efficient solution to baud-rate TR. This combined equalizer and slope detector based approach to baud-rate TR offers the advantage of recovering a clock from a closed eye. Also, this is the first continuous-time slope detection scheme for MMSE. Previous implementations for MMSE employ a discrete time approximation to the derivative [6], [7] which is prone to false lock for certain patterns [7] and may lead to larger jitter in the recovered clock [9].

II. Conventional MMSE TR

MMSE TR optimizes the sampling phase in a digital receiver by minimizing the expected value of the squared error e_k^2

$$E_k = E[e_k^2] = E[(R_k - y(kT+\tau_k))^2]. \tag{1}$$

Here, R_k represents the kth transmitted bit, $y(t)$ the received waveform, T the symbol period, and τ_k the sampling phase for the kth received bit. MMSE requires that the sampling phase τ_k be adjusted in the direction opposite the gradient $\delta E_k/\delta\tau_k$

$$\tau_{k+1} = \tau_k - \mu\left(\frac{\delta E_k}{\delta \tau_k}\right). \tag{2}$$

Here, μ is a parameter that is chosen to tradeoff acquisition time with jitter and determines how quickly τ_k is adjusted. Substituting (1) into (2) and dropping the expectation operator results in the following stochastic gradient update rule:

$$\tau_{k+1} = \tau_k + 2\mu e_k\left(\frac{\delta y(kT+\tau_k)}{\delta \tau_k}\right). \tag{3}$$

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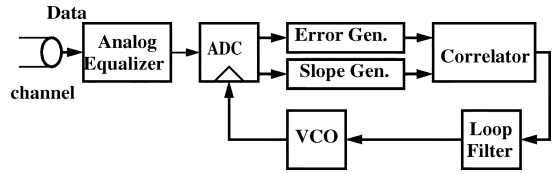

Fig. 1. Conventional MMSE TR scheme.

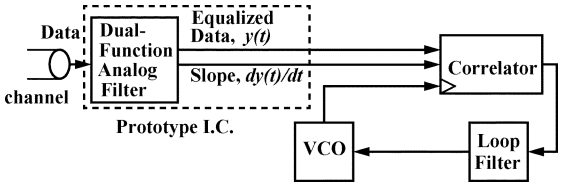

Fig. 2. Proposed MMSE TR scheme.

Practical high-speed implementations of the LMS algorithm often use only 1-bit representations of the sign of the error and the slope [10]. Applying this idea to MMSE TR results in the following sign–sign (SSMMSE) rule [8]:

$$\tau_{k+1} = \tau_k + 2\mu \mathrm{sgn}(e_k)\mathrm{sgn}\left(\frac{\delta y(kT+\tau_k)}{\delta \tau_k}\right). \quad (4)$$

III. Modified MMSE TR

Traditionally, MMSE has been implemented in discrete time. Fig. 1 shows a conventional MMSE method [11]. The correlator generates the timing gradient of (4). Note that the analog–digital converter (ADC) power limits the high-speed operation of this MMSE technique.

In recent years, analog MMSE techniques have become more popular due to their advantages in speed, power and area [6], [7]. However, previous analog slope detection techniques approximate the slope by comparing the current data sample with the data sample stored two bit periods earlier. This 2-tap approximation of the slope leads to large jitter [9] and results in false lock for certain patterns [7].

This work proposes a continuous-time approach to slope detection for MMSE TR. Fig. 2 shows the proposed scheme. Two important architectural differences are observed when compared to conventional MMSE (Fig. 1). Firstly, an analog filter is used to perform both linear equalization and slope detection. The design and implementation of this dual-function analog filter is discussed in Section IV. Secondly, no error signal is required by the correlator. The correlator basically attempts to adjust the sampling phase until the derivative is zero and is a modified implementation of the timing gradient in (4). In the digital domain, the correlator can be implemented by a simple exclusive-OR gate and in the analog domain the correlator can be implemented as a Gilbert cell mixer.

Assuming NRZ data and $R_k = +1$ (i.e., a positive level is received), the analog voltage $y(kT+\tau_k)$ will be between 0 and $+1$ most of the time, hence the sign of the error signal, e_k will be positive. Therefore, (4) can be modified for positive bits

$$\tau_{k+1} = \tau_k + 2\mu \mathrm{sgn}\left(\frac{\delta y(kT+\tau_k)}{\delta \tau_k}\right), \qquad y(kT+\tau_k) > 0. \quad (5)$$

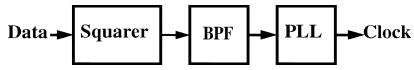

Fig. 3. Typical nonlinear spectral line method.

A similar argument can be made when a negative level is received, i.e., $R_k = -1$;. In this case, the sign of the error signal, e_k will be negative most of the time. Therefore, (4) can be modified for negative bits

$$\tau_{k+1} = \tau_k - 2\mu \mathrm{sgn}\left(\frac{\delta y(kT+\tau_k)}{\delta \tau_k}\right), \qquad y(kT+\tau_k) < 0. \quad (6)$$

Note that in both (5) and (6), the sign of the error has been replaced by the sign of the corresponding analog voltage $y(kT+\tau_k)$. Thus, combining (5) and (6)

$$\tau_{k+1} = \tau_k + 2\mu \mathrm{sgn}(y(kT+\tau_k))\mathrm{sgn}\left(\frac{\delta y(kT+\tau_k)}{\delta \tau_k}\right). \quad (7)$$

Equation (7) reveals that MMSE TR can be modified to exclude the error signal for NRZ data. From an implementation perspective, both the data and slope signals can be applied to clocked comparators and the results passed through an exclusive-OR gate. The number of clocked comparators can be reduced by directly multiplying the signal $y(kT+\tau_k)$ with its slope (by using a Gilbert cell mixer) and then retiming the output with a single clocked comparator

$$\tau_{k+1} = \tau_k + 2\mu \mathrm{sgn}\left(y(kT+\tau_k)\frac{\delta y(kT+\tau_k)}{\delta \tau_k}\right). \quad (8)$$

The proposed MMSE scheme has a strong resemblance to nonlinear spectral line methods [1]. This can be realized by rewriting (8) as follows:

$$\tau_{k+1} = \tau_k + 2\mu \mathrm{sgn}\left(\frac{1}{2}\frac{\delta [y(kT+\tau_k)]^2}{\delta \tau_k}\right). \quad (9)$$

Equation (9) shows that the proposed TR function can also be generated by taking the derivative of the input data squared. A practical implementation of a derivative block would be a bandpass filter since the circuit parasitics would eventually pull down the high frequency response. In nonlinear spectral line techniques (Fig. 3), the input data is squared and then passed through a high Q bandpass filter to extract a tone at the baud-rate. In our case, the input data is first passed through a bandpass filter (i.e., a practical derivative block) and then multiplied by the input data signal.

Several advantages show up as a result of this implementation. Firstly, the timing recovery loop locks to the maximum data eye opening since it tracks the slope of the incoming data waveform. We have verified this in our experimental results (Section V). Secondly, since the bandpass filter output is being multiplied by the signal, an equalizer can be placed in the signal path without interfering with the slope detection action of the bandpass filter. In cases where a linear equalizer is necessary to preserve signal integrity, the slope detector function can be integrated into the linear equalizer. An analog filter that performs

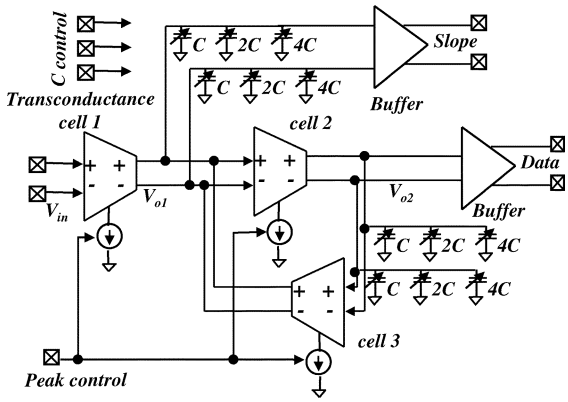

Fig. 4. Dual-function analog filter topology.

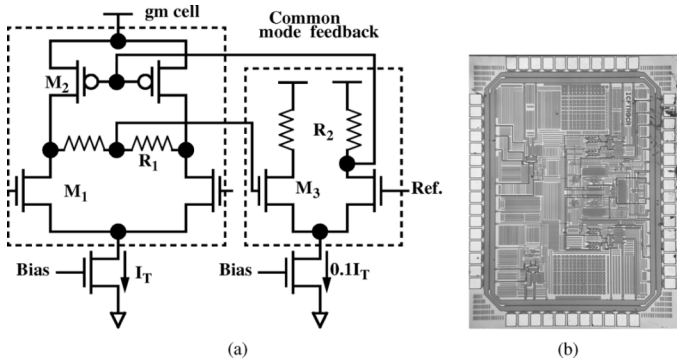

Fig. 5. Dual-function analog filter. (a) Schematic of transconductance cell. (b) Die photo.

the dual function of a linear equalizer and slope detector is described in Section IV.

Note that serial links need to work for both good and bad channels. For a "good" channel where the data eye is wide open, the slope goes to zero for a large fraction of each bit interval. To avoid this "zero-slope" condition, the analog filter front-end needs to band-limit the incoming data signal for a wide range of data rates. This is achieved by programming the filter parameters as discussed in Section IV.

It is also important to note that the nonlinearity in (9) will generate a timing tone even when the assumptions about the sign of the error are not true. Therefore, this technique works even when there is peaking in the data eye. In fact, this was experimentally verified. Certainly, for long strings of 1's or 0's or for channels with very high attenuation or channels with large reflections due to impedance discontinuities the recovered clock will have higher jitter (as with all TR techniques).

IV. Dual-Function Analog Filter

This section attempts to describe the architecture of the dual-function analog filter block of Fig. 2. Note that this block aids the TR loop by generating the slope and also performs linear equalization. Fig. 4 shows the architecture of the circuit. The circuit has two outputs: data and slope and it consists of three identical transconductance cells one of which is placed in negative feedback to realize a second order transfer function. The output impedance, R_o of the transconductance cells provides sufficient damping to ensure stability and avoid oscillations. Assuming g_m is the transconductance of each cell, C_{p1} the parasitic capacitance at V_{o1}, C_{p2} the parasitic capacitance at V_{o2}, C_{ext} the external capacitance (which is realized using a capacitor bank), Z_{o1} the impedance at node V_{o1} and Z_{o2} the impedance at node V_{o2} the transfer function in the data path can be expressed as

$$\frac{V_{o2}}{V_{\text{in}}} = \frac{g_m^2 Z_{o1} Z_{o2}}{1 + g_m^2 Z_{o1} Z_{o2}} \tag{10}$$

where $Z_{o1} = R_o/2 \| 1/sC_1$, $C_1 = C_{p1} + C_{\text{ext}}$, $Z_{o2} = R_o \| 1/sC_2$ and $C_2 = C_{p2} + C_{\text{ext}}$. The transfer function in the slope path can be expressed as

$$\frac{V_{o1}}{V_{\text{in}}} = \frac{g_m Z_{o1}}{1 + g_m^2 Z_{o1} Z_{o2}}. \tag{11}$$

Combining (10) and (11), we get

$$V_{o1} = \frac{1}{g_m Z_{o2}} V_{o2}. \tag{12}$$

Since Z_{o2} approaches $1/sC_2$ at high frequencies V_{o1} and V_{o2} are related as follows:

$$V_{o1} \approx s \frac{C_2}{g_m} V_{o2}. \tag{13}$$

To achieve linear equalization along the data path, some peaking has to be introduced into the transfer function in (10). The peaking frequency can be derived by computing the derivative of the data path transfer function in (10) and equating it to zero. If $\omega_o < \sqrt{(\omega_1^2 + \omega_2^2)/2}$ then there is no peaking, where $\omega_o = g_m/\sqrt{C_1 C_2}$, $\omega_1 = 2/(R_o C_1)$, $\omega_2 = 1/(R_o C_2)$. For this design, $\omega_o \gg \sqrt{(\omega_1^2 + \omega_2^2)/2}$. Hence, the peaking frequency can be approximated as

$$\omega_{\text{peak}} \approx \frac{g_m}{\sqrt{C_1 C_2}} = \omega_o. \tag{14}$$

Substituting ω_{peak} in (10) , the peaking amplitude can be approximated as

$$\left| \frac{V_{o2}}{V_{\text{in}}} (\omega = \omega_{\text{peak}}) \right| \approx \frac{g_m R_o}{\sqrt{\frac{C_1}{C_2}} + 2\sqrt{\frac{C_2}{C_1}}}. \tag{15}$$

Binary weighted capacitor banks in both the data and slope paths allowed programmable peaking frequencies and off chip tail current control of the transconductance cells facilitated peaking amplitude variation. Note that the programmability in peaking frequency and peaking amplitude provide the necessary band-limiting action that is essential for the proposed TR scheme to function for a wide range of data rates. Fig. 5(a) shows the schematic of the basic g_m cell along with its common-mode feedback (CMFB). Since cell 1 and cell 3 shared the same output nodes, a single CMFB circuit was used for both cells. To ensure greater flexibility in off chip tuning, both the CMFB bias and the g_m cell bias currents, I_T were controlled off chip. Spectre simulations show that as I_T is varied from 4.2 to 6.4 mA, g_m changes from 9 to 11 mA/V but R_o changes from 1 to 0.24 kΩ, thus causing the filter peak to fall from 10 to 0 dB. Since g_m does not change much with bias current, the change in the ratio of V_{o1} to V_{o2} is small.

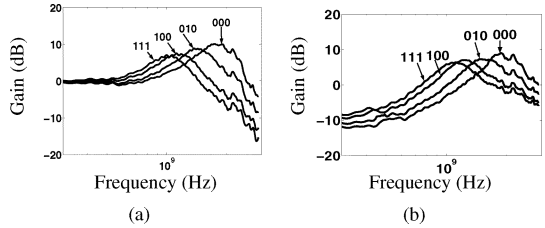

Fig. 6. Measured frequency response for four different digital control word inputs to the binary weighted capacitor bank of the dual-function analog filter. (a) Data path. (b) Slope path.

TABLE I
MEASURED RESULTS FOR DUAL-FUNCTION ANALOG FILTER

Technology	0.18μm CMOS
Core Area	0.4 mm^2
Max. Peaking Freq.	2 GHz (for both data and slope path)
Max. Peak Gain	10 dB (for data path); 9 dB (for slope path)
Maximum Quality factor	3.8 (for both data and slope paths)
1 dB Compression point (Input at 2GHz)	-11 dBm (for both data and slope paths)
IIP3 (Inputs: 2000.5 MHz 1999.5 MHz)	1.3 dBm (Data path) 3.8 dBm (Slope Path)

TABLE II
LINEAR EQUALIZER PERFORMANCE COMPARISON

Reference	Data Rate	Technology	Power
This work	2 Gb/s	0.18μm CMOS	39.6 mW
[13]	3.5 Gb/s	0.18μm CMOS	80 mW
[14]	2.5-3.5 Gb/s	0.25μm CMOS	95mW

V. MEASUREMENT RESULTS

The dual-function analog filter was fabricated in a 0.18-μm CMOS technology and occupied a core area of 0.4 mm^2. The die photo is shown in Fig. 5(b). An HP 8595E spectrum analyzer was used to measure the frequency response (Fig. 6) of the filter. With all the switches in the capacitor bank turned off (digital control word input $=$ 000), the transfer function in both the data and slope path peak at 2-GHz with peak gain at 10 and 9 dB, respectively. Turning all the switches on (digital control word input $=$ 111) shifts the peaking frequency to 1 GHz. In Fig. 6(a) and (b), the slight degradation in peaking amplitude with changing peaking frequency is attributed to the nonideality of the MOSFET switches used for the capacitor bank in the dual-function analog filter prototype. With all switches on, significant resistance shows up in series with the bank, thus degrading the peaking amplitude. As a result, the loss compensation capacity of the filter is slightly degraded at lower frequencies. Table I summarizes the performance of the filter. The filter consumed 39.6 mW from a 1.8-V supply. As shown in Table II, this is comparable to published designs in standard CMOS technologies although direct comparisons are difficult since each design accomodates different features and data rates.

An Agilent 8403A BER tester (BERT) was connected to the dual-function analog filter to test its functionality. Eye diagrams of data and slope outputs captured by an Agilent 86100B scope for a 2.7-Gb/s $2^{31}-1$ pseudorandom bit sequence (PRBS) sequence are shown in Fig. 7.

An external loop was used to demonstrate the proposed TR scheme (Fig. 8). The mixer, latch, VCO and loop filter were implemented on a separate board using commercial components.

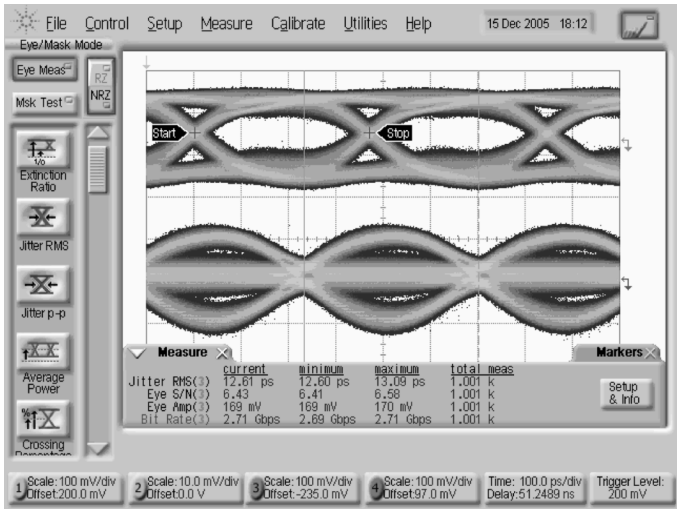

Fig. 7. Data (top eye) and slope (bottom eye) outputs of dual-function analog filter at 2.7-Gb/s (Vertical scale $=$ 100 mv/div ; Horizontal scale $=$ 200 ps/div).

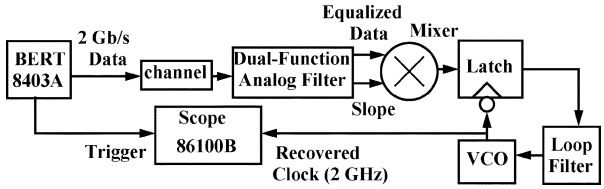

Fig. 8. Test set up for external TR loop using the dual-function analog filter.

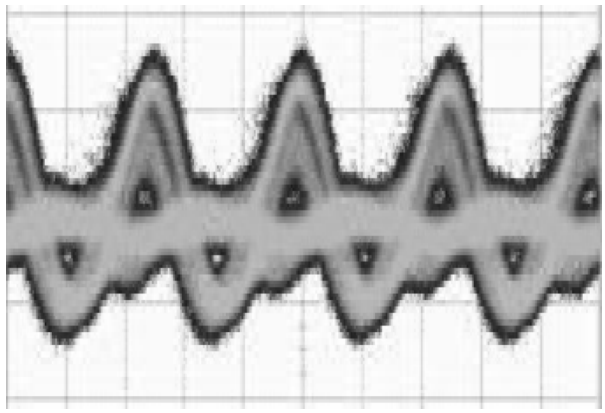

Fig. 9. Mixer output corresponding to a 2-Gb/s random data sequence (Vertical scale $=$ 20 mv/div ; Horizontal scale $=$ 200 ps/div).

For alternating data, the mixer output is a sinewave at the data rate. For random data, the mixer output basically consists of an alternating pattern superimposed on a zero dc level (Fig. 9). The zero dc level arises when consecutive 1's or 0's show up in the random data sequence at which time the slope is zero. The TR loop was initially tested with a 2-Gb/s alternating data pattern. The resulting RMS clock jitter was 2.6 ps. For the random data test, a 20-cm board to board channel and several coaxial cable sections were connected together to construct a lossy channel (Fig. 10) which was inserted between the BERT and the dual-function analog filter (Fig. 8). For a 2-Gb/s $2^{31}-1$ random data sequence, the eye at the channel output was barely

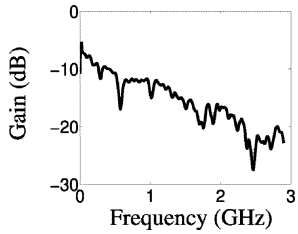

Fig. 10. Frequency response of lossy channel.

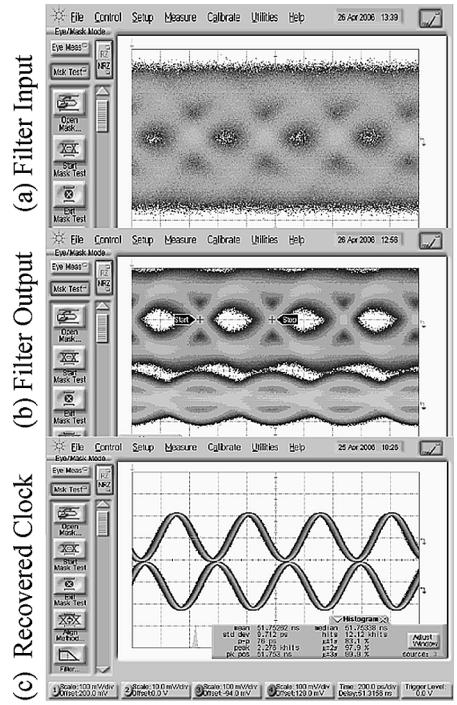

Fig. 11. Eye diagrams at different points of the TR loop. (a) Channel output/filter input at 2-Gb/s (Vertical scale = 25 mv/div ; Horizontal scale = 200 ps/div), (b) Equalized data (top) and slope (bottom) outputs of dual-function analog filter at 2-Gb/s (Vertical scale = 25 mv/div ; Horizontal scale = 200 ps/div), and (c) Recovered clock at 2-GHz (Vertical scale = 100 mv/div; Horizontal scale = 200 ps/div).

TABLE III
PERFORMANCE SUMMARY AND COMPARISON TABLE

Reference	Data Rate	Clock Freq.	Conditions	RMS Jitter
This work (Baud-rate)	2 Gb/s	2 GHz	Alternating data	2.6 ps
			2^{31}-1 PRBS; lossless channel	6.5 ps
			2^{31}-1 PRBS; lossy channel	9.7 ps
[3] (Baud-rate)	5 Gb/s	1 GHz	Random data; lossless channel	4.8 ps
[15] (Edge-sampled)	2.5 Gb/s	2.5 GHz	2^{23}-1 PRBS; lossless channel	17.4 ps

open [Fig. 11(a)]. Significant improvement in eye quality was observed at the analog filter output [Fig. 11(b)]. The TR loop extracted a 2-GHz clock from the equalized data and slope information obtained from the dual-function analog filter [Fig. 11(c)]. Note that the clock is aligned with the maximum data eye opening at the output of the dual-function analog filter; thus confirming MMSE TR. Table III summarizes the performance of the TR scheme.

VI. CONCLUSION

This brief presented a modified MMSE TR scheme that utilizes signals from a dual-function analog filter. Conventional MMSE is not hardware-efficient since it requires an extra latch to generate the error signal in addition to the slope information. The modified MMSE TR scheme proposed in this work eliminates the error signal from the TR loop for NRZ data without compromising the advantages of conventional MMSE. Also, to generate the slope information, a prototype dual-function analog filter that is capable of providing simultaneous low-pass and bandpass transfer characteristics is reported in this work. The bandpass transfer characteristic is utilized to provide the slope information and peaking in the low-pass path is introduced to perform linear equalization. To demonstrate the timing recovery concept, the prototype dual-function analog filter was used to recover a 2-GHz clock from a 2-Gb/s $2^{31} - 1$ random data sequence based on the modified MMSE criterion.

REFERENCES

[1] U. Moon and G. Huang, "CMOS implementation of nonlinear spectral-line timing recovery in digital data-communication systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 2, pp. 298–308, Feb. 2004.

[2] J. Alexander, "Clock recovery from random binary signals," *Electron. Lett.*, vol. 111, pp. 541–542, Oct. 1975.

[3] A. Emami-Neyestanak, S. Palermo, H. Lee, and M. Horowitz, "CMOS transceiver with baud-rate clock recovery for optical interconnects," in *Proc. VLSI Symp. Circuits*, 2004, pp. 410–413.

[4] V. Balan *et al.*, "A 4.8–6.4-Gb/s serial link for backplane applications using decision feedback equalization," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1957–1967, Sep. 2005.

[5] K. Mueller and M. Muller, "Timing recovery in digital synchronous data receivers," *IEEE Trans. Commun.*, vol. COM-24, no. 5, pp. 516–531, May 1976.

[6] P. Roo, R. Spencer, and P. Hurst, "A CMOS analog timing recovery circuit for PRML detectors," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 56–65, Jan. 2000.

[7] D. Sun, A. Xotta, and A. Abidi, "A 1-GHz CMOS analog front-end for a generalized PRML read channel," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2275–2285, Nov. 2005.

[8] F. Musa and A. Carusone, "Clock recovery in high-speed multilevel serial links," in *Proc. 2003 Int. Symp. Cirucits Syst.*, May 2003, pp. 449–452.

[9] E. Lee and D. Messerschmitt, *Digital Communication*, 2nd ed. Norwell, MA: Kluwer , 1997.

[10] M. Le, P. Hurst, and J. Keane, "An adaptive analog noise-predictive decision-feedback equalizer," *IEEE J. Solid-State Circuits*, vol. 37, no. 2, pp. 105–113, Feb. 2002.

[11] P. Aziz and S. Surendran, "Symbol rate timing recovery for higher order partial response channels," *IEEE J. Select. Areas Commun.*, vol. 19, no. 4, pp. 635–648, Apr. 2001.

[12] J. Choi, M. Hwang, and D. Jeong, "A 0.18-μm CMOS 3.5 Gb/s continuous-time adaptive cable equalizer using enhanced low-frequency gain control method," *IEEE J. Solid-State Circuits*, vol. 39, no. 3, pp. 419–425, Mar. 2004.

[13] X. Lin, J. Liu, H. Lee, and H. Liu, "A 2.5 to 3.5 Gb/s adaptive FIR equalizer with continuous-time wide-bandwidth delay line in 0.25 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1908–1918, Aug. 2006.

[14] S. Anand and B. Razavi, "A CMOS clock recovery circuit for 2.5-Gb/s NRZ data," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 432–439, Mar. 2001.