A CMOS Finite Impulse Response Filter With a Crossover Traveling Wave Topology for Equalization up to 30 Gb/s

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***Abstract*—This paper describes a fully differential 3-tap finite impulse response filter in 90-nm CMOS. A traditional traveling wave filter topology is modified to alleviate its inherent delay–bandwidth–gain tradeoffs. Each tap gain is comprised of two transconductors whose outputs superimpose with the same group delay, similar to a distributed amplifier. This doubles the bandwidth of the filter for a given tap spacing and gain. Digital control is provided for the tap gains, an integrated pre-amplifier, and tuning varactors. Coupled differential spirals are used in the delay lines to help the design fit into an area 600 μm $\times$ 500 μm. A 1-V supply voltage and 25-mW power consumption are enabled by the use of parallel differential pairs for sign control of the transconductances instead of Gilbert cell amplifiers. The input return loss is better than 16 dB and the output return loss is better than 9 dB up to 30 GHz. Equalization of NRZ data over a coaxial cable channel was demonstrated up to 30 Gb/s, making it faster than any previously reported CMOS equalizer.**

***Index Terms*—CMOS, distributed amplifier, equalization, finite impulse response filter, traveling wave filter.**

I. Introduction

THIS paper describes a fully differential 3-tap finite impulse response (FIR) filter in 90-nm CMOS capable of equalizing nonreturn-to-zero (NRZ) data up to 30 Gb/s. A traditional traveling wave filter (TWF) structure is modified so that each tap gain is comprised of two transconductors whose outputs superimpose with the same group delay, similar to a distributed amplifier. This doubles the bandwidth of the filter for a given tap spacing and gain. Differential (coupled) inductors are used to implement the delay lines passively with low power (25 mW from a 1-V supply) and relatively low area (600 μm $\times$ 500 μm). This is the first reported CMOS FIR filter operating on binary signals above 10 Gb/s.

Analog FIR filters with programmable coefficients are important building blocks in many communication systems. Currently, at data rates of 10+ Gb/s, the high power consumption of analog-to-digital converters [1] often makes analog FIR filters preferable to their digital counterparts. They are used on their own or with decision feedback for equalization in integrated receivers. The filters must adjust to different channels and environmental conditions, so their coefficients must be programmable.

The implementation of broadband, low power delay elements is a key challenge in the design of these analog FIR filters. Clocked switched capacitors can be used to provide the delays [2], but considerable power is required to recover and distribute a low-jitter clock for filters above 10 Gb/s. More often, continuous-time delays are provided by active filters [3], passive devices [4]–[6] or a combination of the two [7]. This work focuses on the use of passive continuous-time delay lines because they are low power, inherently linear, and offer the potential for very high bandwidth.

Most of the filters recently reported at 10–40 Gb/s use lumped-*LC* sections instead of microstrip or stripline transmission lines as passive delays. Microstrip or striplines would have to be very long (on the order of several millimeters) to achieve the required time delays, even at 40 Gb/s. As a result, the circuit area can become prohibitively large. In addition, long transmission lines may introduce significant series loss. By using artificial transmission lines made up of lumped inductors and capacitors, the total wirelength required to achieve a given delay is reduced. Thus, the chip area and resistive losses may be reduced. This work uses coupled differential spirals to keep both the chip area and series losses at a minimum.

The TWF topology that is the focus of this work dates back to the early 1970s [8] when it was demonstrated on a discrete prototype. Later, integrated circuit implementations of the general topology were described in [9] and [10]. More recently, the TWF topology has been shown to be robust to many typical integrated circuit nonidealities [11]. However, the use of lumped-*LC* sections in a TWF limits the bandwidth of the delay lines. In this work, the TWF topology is modified to increase the bandwidth of the delay lines for a given tap spacing and gain. The modified topology is particularly well suited to baud-rate equalizers.

Integrated circuit TWFs have been used for optical fiber, chip-to-chip, and coaxial cable communication up to 49 Gb/s. In [12], a 3-tap FIR filter was reported consuming 820 mW in an InP process at 40 Gb/s. In [4], a 7-tap FIR filter implemented in 0.18-μm SiGe BiCMOS was demonstrated up to 49 Gb/s. The filter has a tap spacing of 6.75 ps and a nominal power consumption of 750 mW. At 10 Gb/s, TWFs have been implemented with lower power consumption including a 7-tap design with 50-ps tap spacing in 0.18-μm SiGe BiCMOS consuming 40 mW [5] and a 4-tap equalizer with 33-ps tap spacing in 0.18-μm CMOS consuming only 7.3 mW [6]. The prototype

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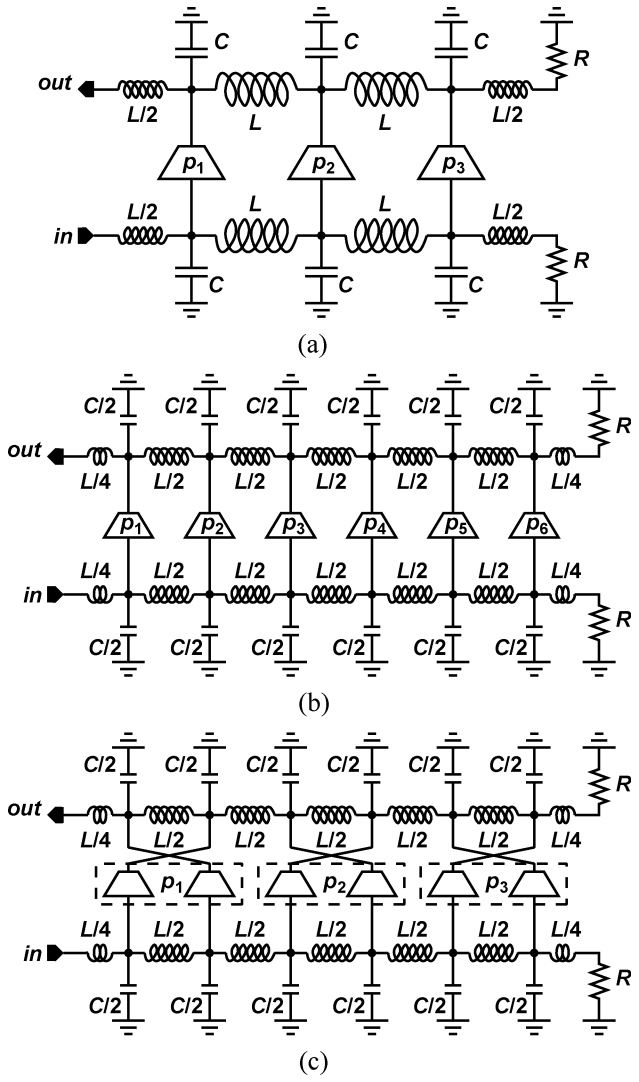

Fig. 1. Evolution of the crossover traveling wave filter topology: (a) a 3-tap traveling wave filter; (b) a 6-tap traveling wave filter with one-half the delay per tap; (c) a 3-tap crossover traveling wave filter.

described in this work is distinguished by its baud-rate tap spacing, the use of coupled differential spiral inductors, its digital programmability, the 1-V supply voltage, and operation up to 30 Gb/s in CMOS.

Section II will describe the traditional TWF topology and the inherent delay–gain–bandwidth tradeoffs it presents. Then, a crossover topology is introduced to increase the bandwidth. In Section III, the 3-tap prototype filter is described. Measurement results are presented in Section IV, followed by conclusions.

II. Filter Topology

A. Traveling Wave Filter

The basic TWF topology is shown in Fig. 1(a) (single-ended) for the case of a 3-tap filter. Ideally, it implements a finite impulse response using the *LC*-sections as passive delay elements.

The *LC* artificial transmission line is studied in detail in [13], where it is shown that group delay of each section, τ, with an inductance L and capacitance C per section is

$$\tau = \sqrt{LC}. \tag{1}$$

Furthermore, the *LC* delay line also forms a low-pass filter whose cutoff frequency is

$$f_c = \frac{1}{\pi\sqrt{LC}}. \tag{2}$$

For a traditional TWF, the tap spacing is equal to the delay through two *LC* sections, $\Delta T = 2\tau$. Hence,

$$\Delta T = 2\sqrt{LC}. \tag{3}$$

Combining (2) and (3) relates the maximum bandwidth and tap spacing of all TWFs with lumped-*LC* delay lines

$$f_c = \frac{2}{\pi\Delta T}. \tag{4}$$

For a 3-tap TWF with 25-ps tap spacing (one baud-interval at 40 Gb/s), (4) yields a cutoff frequency of 25 GHz. This is insufficient for a 40-Gb/s equalizer.

To extend the bandwidth, the *LC*-stages must be made smaller, thus making the delay line less "lumpy." Fig. 1(b) shows an equalizer which is half as lumpy as the equalizer in Fig. 1(a). The bandwidth of the delay line is doubled to $f_c = 2/\pi\sqrt{LC}$, but the tap spacing is halved to $\Delta T = \sqrt{LC}$, so the same delay–bandwidth tradeoff expressed in (4) is maintained.

Plots of the simulated magnitude response and group delay for 3- and 6-section lumped delay lines are given in Fig. 2, showing the bandwidth doubling from 25 to 50 GHz. Also, notice that the group delay is flat only within the bandwidth of the delay line, another important reason for making the delay line more distributed.

Unfortunately, the 6-tap TWF has several drawbacks compared with the 3-tap TWF for equalizer applications. Since the node capacitances include the transistor parasitic capacitances, when they are decreased the transistor device sizes and bias currents must scale accordingly. Therefore, the gain through each tap of a 6-tap TWF is only half of that in a 3-tap TWF (6 dB less) for the same total filter delay. This has a negative impact on receiver sensitivity when used as an equalizer. Also, increasing the number of taps and decreasing the tap spacing increases the complexity of the adaptation algorithm required, making it more difficult to achieve convergence of the tap values.

B. Crossover Traveling Wave Filter

The filter topology described in this subsection was motivated by a desire to obtain the increased bandwidth of the 6-tap TWF

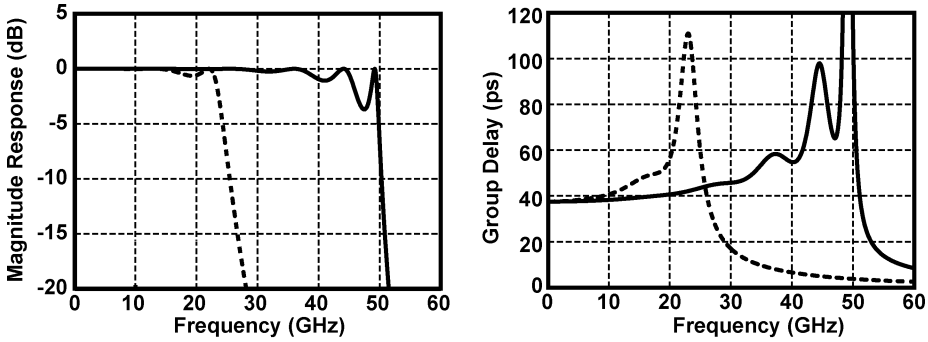

Fig. 2. Comparison between 3- and 6-element delay lines: (a) magnitude response; (b) group delay.

TABLE I
DELAY–BANDWIDTH–GAIN TRADEOFFS FOR THE TRAVELING WAVE FILTERS IN FIG. 1

	Tap spacing τ	Delay line bandwidth f_c	Max. gain per tap
3-tap TWF	$2\sqrt{LC}$	$\frac{1}{\pi\sqrt{LC}}$	$\propto C$
6-tap TWF	$\sqrt{LC}$	$\frac{2}{\pi\sqrt{LC}}$	$\propto \frac{C}{2}$
3-tap CTWF	$2\sqrt{LC}$	$\frac{2}{\pi\sqrt{LC}}$	$\propto C$

while maintaining the same tap spacing and tap gain as the 3-tap TWF.

A trivial method of increasing the tap spacing of the 6-tap TWF is to eliminate every other transconductor in Fig. 1(b), replacing them with appropriately sized capacitors. Such a filter would have the same bandwidth as the 6-tap TWF, and the same tap spacing as the 3-tap filter, but still 6 dB less gain.

Alternatively, by crisscrossing the outputs of neighboring transconductors in a TWF, their gains add with equal group delay. This topology will be referred to as a crossover traveling wave filter (CTWF) and is illustrated in Fig. 1(c). Each pair of transconductors is actually a small distributed amplifier whose input and output transmission lines are the same ones used to generate the filter's tap delays. The tap delay is now formed by four lumped sections (instead of two). Hence, the 3-tap CTWF topology in Fig. 1(c) maintains the same tap spacing and gain as the 3-tap TWF in Fig. 1(a), but with the bandwidth of the less lumpy 6-tap TWF in Fig. 1(b). There is no power penalty and only a small area overhead compared with the traditional topologies. These results are summarized in Table I for ideal (lossless) delay lines.

The simulated frequency responses of one tap in the 6-section TWF in Fig. 1(b) and the 3-tap CTWF in Fig. 1(c) including skin effect and dielectric loss are shown in Fig. 3. The CTWF provides approximately 5 dB more gain through a single tap than the conventional TWF. This is slightly less than the ideal doubling (6 dB increase) because of the additional series loss introduced by the crossover topology. In order for the outputs of neighboring transconductors to add in phase, the mismatch between the two path delays must be significantly less than the tap spacing. Therefore, attention is required during layout to ensure symmetry in the crossover routing.

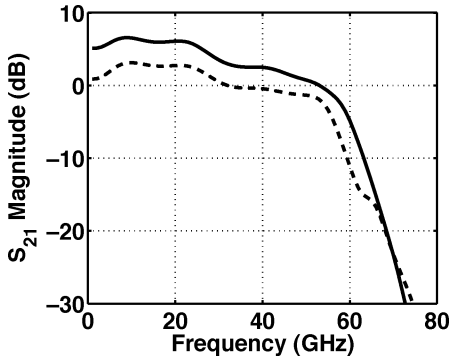

Fig. 3. Simulation results comparing the gain of a single tap in the 6-section TWF of Fig. 1(b) (dashed line) and the 3-tap crossover TWF in Fig. 1(c) (solid line).

III. CIRCUIT DESIGN

A block diagram of the entire circuit is given in Fig. 4. A 3-tap 40 Gb/s baud-rate equalizer was targeted to eliminate polarization mode dispersion as a length limitation in long-haul single-mode optical fiber links [14]. However, the topology and design techniques are applicable to many other optical and wireline applications. The circuit is fully differential and has been designed for use with a 100-Ω (differential) system impedance.

A preamplifier stage accepts differential inputs and provides a variable gain to maximize the dynamic range of the equalizer. It also performs single-ended-to-differential conversion when the circuit is driven by an unbalanced input. The preamplifier drives the differential input delay line. Six transconductors tap this delay line at equal intervals and drive an output differential delay line. All delay lines are made up of lumped capacitors and differential inductors.

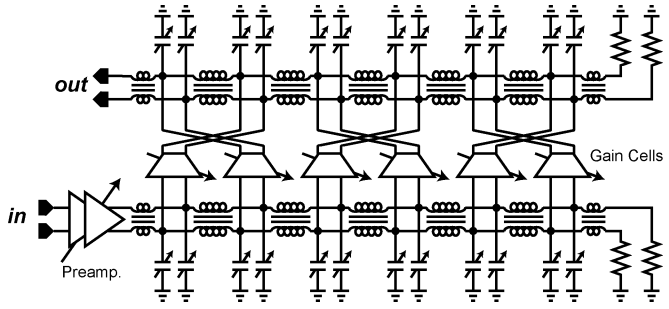

Fig. 4. Symbolic top-level schematic of the fabricated 90-nm equalizer IC.

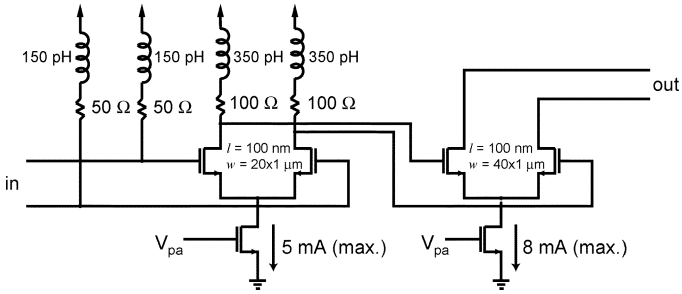

Fig. 5. Circuit schematic of preamplifier block.

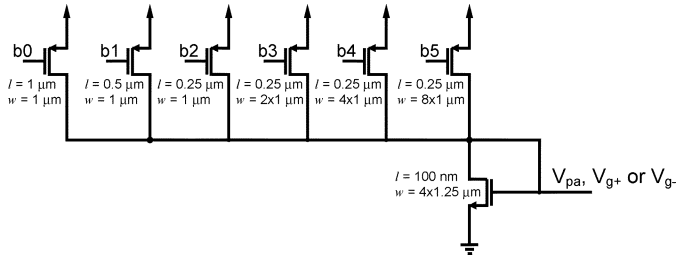

Fig. 6. Circuit schematic of the digitally controllable 6-bit switched-resistor current mirror. Copies of this circuit are used to bias the preamplifier and each tap gain separately.

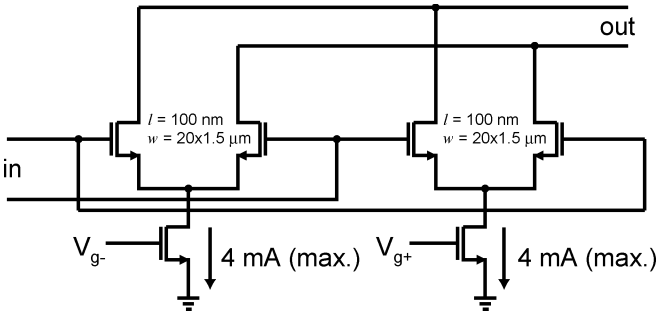

Fig. 7. Circuit schematic of a variable gain cell.

Not shown in Fig. 4 is the digital control path. The capacitances, preamplifier and tap gains are controllable through a set of registers which can be loaded serially.

This 90-nm CMOS technology has nMOS threshold voltages of approximately 0.35 V. The same techniques could, of course, be applied to any CMOS technology. To obtain the same tap gains in a technology with greater minimum gate length, greater parasitic capacitances would appear along the delay lines. To maintain the same characteristic impedance the delay line inductors would have to increase proportionately, thereby increasing the tap spacing and decreasing the circuit bandwidth. The bandwidth of the lumped preamplifier would also decrease in such a technology.

A. Preamplifier

A schematic of the lumped preamplifier stage is given in Fig. 5. The preamplifier consists of two cascaded differential pairs. The inputs of the first differential pair are terminated by 50-Ω loads for input matching to the 100-Ω (differential) system impedance. A differential inductor is placed in series with the 50-Ω loads to partially compensate for the large input capacitance, allowing a better input match over a larger bandwidth. The first differential pair is loaded with 100-Ω resistors, which allow it to provide reasonable gain. Another differential inductor is used in series with the 100-Ω resistors to extend the bandwidth of the first stage to over 30 GHz (simulated).

The second differential pair acts as an open-drain line driver, driving the input signal onto the 50-Ω input delay lines. The open-drain configuration was chosen over a doubly terminated configuration for several reasons. First, it offers a power savings because it allows the bias current to be halved for the same voltage gain. Second, since it requires a lower bias current, the transistors in both stages can be made smaller, making it easier for the first stage to achieve high bandwidth and a good input match. Third, since the devices have very short channel lengths, the output resistance of the differential pair is on the order of a few hundred ohms, such that partial matching is achieved at this node without any termination. Finally, any energy traveling back to the preamplifier along the transmission line would be attenuated somewhat by the lossy nature of the transmission lines, reducing the magnitude of the reflections resulting from the open-drain configuration.

The gain of the preamplifier stage is digitally controllable. The current sources of both differential pairs in the preamplifier are set by a digitally controllable 6-bit switched-resistor current mirror, shown in Fig. 6.

B. Gain Cell

The design of the gain cell is complicated by the low supply voltage. Recent integrated circuit traveling wave filters have used Gilbert cell multipliers as transconductors to provide sign and magnitude control over the gain [4]–[6], [15]. However, stacking the additional transistors required for a Gilbert cell is not possible within the 1-V supply voltage of this design. Not even series switches could be tolerated as in [7]. Therefore, simple differential pairs were used.

A schematic of the gain cell is given in Fig. 7. Each gain cell is composed of two differential pairs. Their outputs are connected with opposing polarity to enable both positive and negative tap weights. The bias voltages V_{g+} and V_{g-} are each controlled individually with a copy of the bias circuit in Fig. 6. To implement a positive tap weight, the bias current for the differential pair connected with negative polarity is zeroed by decreasing V_{g-} leaving only the positive path from input to output. Therefore, each tap gain is controlled with 6 bits plus one sign bit.

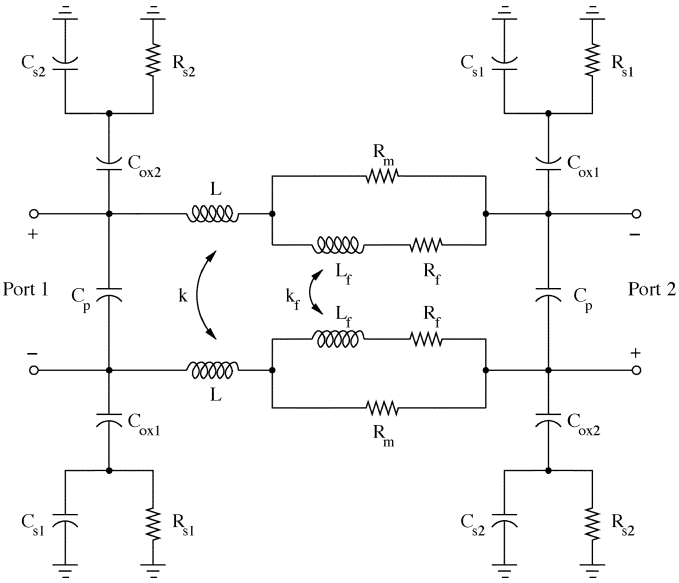

Fig. 8. Spice model used for the delay line differential spirals [17].

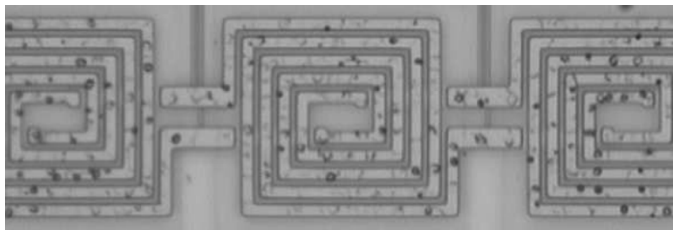

Fig. 9. Close-up of the lumped-*LC* delay line with differential spirals. Each spiral is 47 μm × 47 μm with an inductance of 312.5 pH per side.

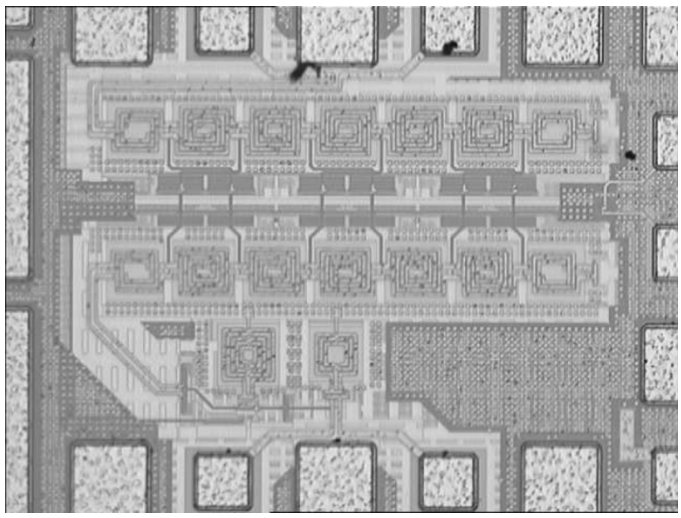

Fig. 10. Die photo of the prototype equalizer.

The size of the differential pair transistors has been chosen to balance the competing objectives of maximizing gain and maximizing tuning ability. The capacitance at each node is determined by the characteristic impedance and tap spacing. A variable capacitance at each node can compensate for variations in the device and wiring capacitances. For large gain, the transistors should make up a large portion of the node capacitance. However, to maximize the tuning ability it is desirable for the varactors to be large. For this circuit, the transistors are sized to provide approximately 65% of the total node capacitance, with the remainder provided by the varactors.

The maximum current that can be drawn by all three taps is limited to 8 mA to ensure that the output common-mode voltage does not drop below 0.8 V. Therefore, the current through any particular gain cell can range from 0 when the tap is off to 4 mA when the tap is fully on (two gain cells drawing 4 mA each).

C. Input and Output Delay Lines

The input and output delay lines are designed to achieve a characteristic impedance, $Z_0 = \sqrt{L/C}$, of 50 Ω per side and a nominal tap spacing of 25 ps. Therefore, an inductance of $L/2 = 312.5$ pH per section per side and a node capacitance of $C/2 = 125$ fF per side is required. Additional inductors of $L/4$ are added to each end of the transmission line so that the total inductance of the line is $3L$, to match the total capacitance of $3C$.

Differential spiral inductors are used to reduce the area compared with two separate paths of uncoupled inductors. They also reduce the wirelength for a given inductance, thereby reducing series losses along the delay line. Thick top-layer metal is used for the spirals. Each is designed using the ASITIC software package [16]. The inductors are modeled in Spice using the circuit model given in Fig. 8 [17]. The parameters for these models are found by fitting the network parameters of the model to the network parameters generated by ASITIC. The inductors' series losses are estimated at over 1.5 Ω per spiral per side at low frequencies. This results in roughly 10 Ω of series resistance for each complete lumped-*LC* delay line. A photo of the fabricated inductors appears in Fig. 9. Since each inductor was characterized by ASITIC in isolation, any coupling between adjacent spirals was not characterized. In a compact layout like this one, the coupling can be significant. A more accurate simulation would model the entire delay line together.

The capacitances at each node include a digitally controllable varactor to allow tuning of the transmission line characteristic impedance and delay. These varactors are composed of switched capacitors built using the top four metal layers of the IC process. On each layer, two interdigitated metal structures form the two capacitor plates. Between each consecutive layer, the orientation of the two plates is reversed. This capacitor achieves high capacitance per unit area because it makes use of both the horizontal capacitance between the interdigitated structures, and the vertical capacitance between adjacent metallization layers [18]. A total of 31 unit-sized capacitors were connected in a binary weighted array to provide 5 bits of control for the input and output delay lines separately.

Each side of the differential delay lines is terminated using a fixed 50-Ω poly resistor.

D. Circuit Layout

The circuit was fabricated in a TSMC 90-nm CMOS process. A die photo of the circuit layout is provided in Fig. 10. The two transmission lines are easily discerned, with the transconductors appearing between them. The differential input enters at the bottom of the circuit and the output is taken from the top, with

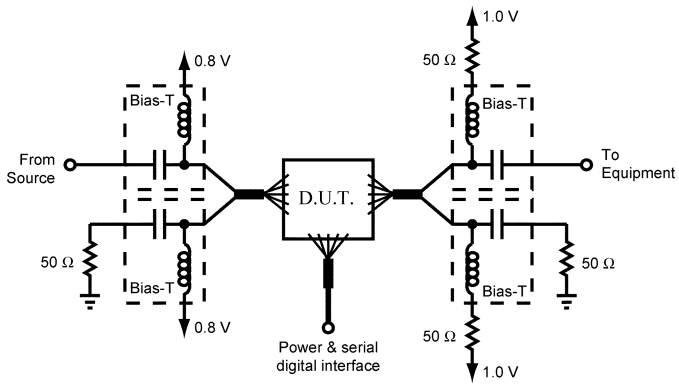

Fig. 11. On-wafer measurement setup including external biasing components.

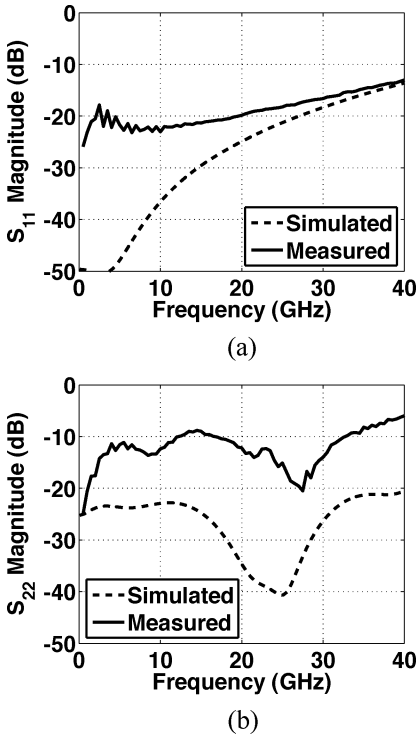

Fig. 12. Return loss of the prototype equalizer measured single-endedly: (a) input return loss; (b) output return loss.

power and digital control provided from the right. The overall dimensions of the equalizer IC are 600 μm $\times$ 500 μm including the pads.

IV. Measurement Results

All circuit measurements were made on-wafer. Fig. 11 shows the measurement setup including external bias-tees at the input and output. These were de-embedded for the S-parameter measurements during calibration, but could not be de-embedded for the eye diagram measurements. All measurements are single-ended because it was not possible to make differential connections without introducing significant skew between the positive and negative signal paths above 10 GHz. Therefore, the preamplifier must convert the single-ended input to a fully differential signal to drive the differential input delay line in a balanced fashion. Since it has finite common-mode rejection, the single-ended-to-differential conversion is imperfect, degrading the measurement results.

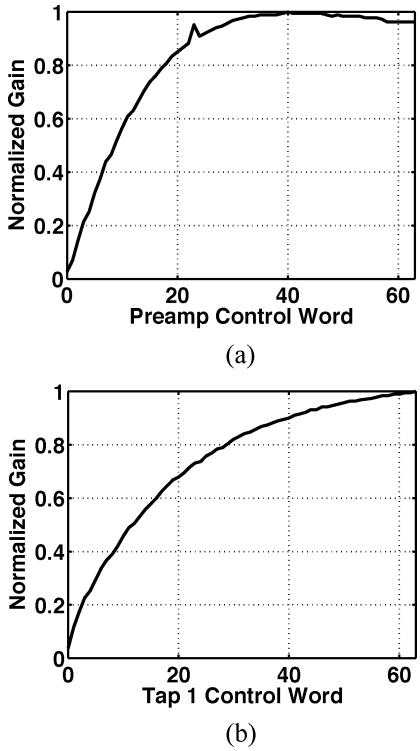

Fig. 13. Normalized gain as a function of the 6-bit digital control word for: (a) the preamplifier, and (b) tap 1 of the equalizer.

Fig. 12 shows the simulated and measured input and output return losses. Input matching is provided by integrated 50-Ω resistors, and is therefore very good at low frequencies. The measured input return loss is better than 16 dB up to 30 GHz. Since the prototype's output terminals are directly connected to a delay line, the measured output return loss is determined by the characteristic impedance of the integrated delay lines. The on-chip digital varactors were manually tuned to provide the best possible output return loss. An output return loss of better than only 9 dB was achieved up to 30 GHz. These results were obtained by minimizing the capacitance of all digital varactors, indicating that the internal node capacitances had been underestimated during simulation. The digital varactors for both the input and output return loss were fixed at this setting for the remainder of the testing.

The gain of the preamplifier was measured as a function of the 6-bit word that controls it. These measurements were made with a 1-GHz sinusoidal input, tap 1 turned on (with its gain control set to 31), and taps 2 and 3 turned off. The results are plotted in Fig. 13(a). Notice that the gain decreases with high control words corresponding to total bias currents in the preamplifier above the maximum of 13 mA. This is because the preamplifier's output common-mode voltage decreases and subsequent stages are no longer biased in saturation. The preamplifier gain control was set to 27 for the remainder of the testing.

The gain tuning characteristic of tap 1 was also measured with a 1-GHz sinusoidal input, and taps 2 and 3 off. It is plotted in Fig. 13(b). Although nonlinear, the tuning curve is monotonic,

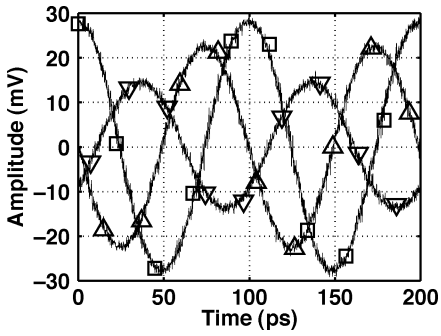

Fig. 14. Measured tap response for a 10-GHz sinusoidal input: □—tap 1, ▽—tap 2, △—tap 3.

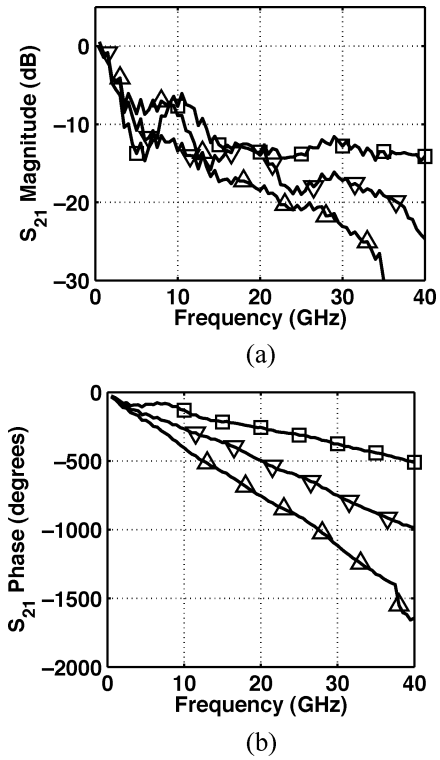

Fig. 15. Single-ended S_{21} measurements for each tap (For differential $|S_{21}|$, add 6 dB): □—tap 1, ▽—tap 2, △—tap 3.

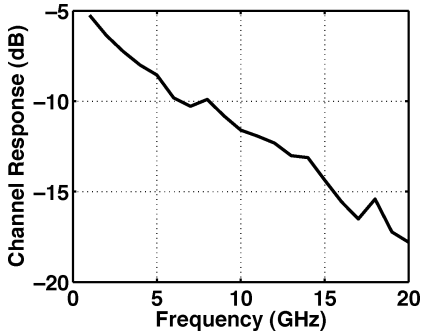

Fig. 16. Measured response of the channel used for eye diagram testing.

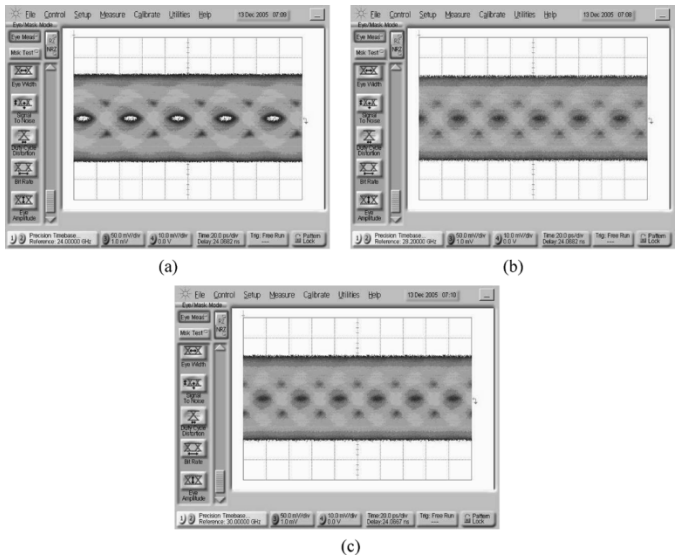

Fig. 17. Eye diagrams at the input to the equalizer at: (a) 24 Gb/s, (b) 28 Gb/s, and (c) 30 Gb/s.

which is all that would be required if a gradient-descent adaptation algorithm (such as the LMS algorithm) were used to optimize the equalizer tap weights.

Fig. 14 shows the tap spacing measured at 10 GHz. The response of each tap was measured separately on an oscilloscope, then the traces were superimposed to measure the tap spacing. Based on these measurements, the taps spacing is 37 ps, considerably larger than the 25 ps designed for, further evidence that the internal node capacitances were underestimated during simulation.

Fig. 15(a) shows the magnitude response of each tap measured with a two-port network analyzer. Since the measurements are single-ended, the differential gains would be 6 dB greater than shown here. The increase in tap gains near dc is partly due to the transmission lines' series losses which appear as an additional resistive load in series with the termination resistors at low frequencies. From 2 to 20 GHz, considerable ripple is observed on the magnitude response of each tap. This can be attributed to relatively poor matching on the delay lines, evidenced by the output return loss measurements. The resulting standing waves cause the observed ripple. Above 20 GHz, the increasing series losses of the delay lines are evident going from tap 1 to tap 2 to tap 3. Fortunately, it has been shown that the performance of equalizers based on traveling wave filters is robust to mismatch, series losses, and other nonidealities [11].

Fig. 15(b) shows the phase response of each equalizer tap. The group delay is constant over the frequency range 10–30 GHz, but deviates outside of that range. These measurements indicate a tap spacing of 35 ps, in close agreement with the sinusoidal measurements in Fig. 14.

The filter's 1-dB input compression point is −7 dBm (280 mV peak-to-peak) measured single-endedly at both 2.5 and 5 GHz with any one tap turned on at its maximum gain setting. A total harmonic distortion (THD) of −28 dB was measured through tap 1 at 5 GHz with an input power equal to the 1-dB compression point. The THD measured through taps 2 and 3 were significantly better since the signals through these paths are attenuated by longer lengths of lossy delay line at the input and output.

Equalization experiments were performed at data rates from 24 to 30 Gb/s. An input pattern was generated by multiplexing

TABLE II
PROTOTYPE SUMMARY AND COMPARISON WITH OTHER RECENTLY REPORTED INTEGRATED CIRCUIT TRAVELING WAVE FILTERS

	This work	[7]	[4]	[6]	[5]
Technology	90 nm CMOS	0.13 μm CMOS	0.18 μm SiGe BiCMOS	0.18 μm CMOS	0.18 μm SiGe BiCMOS
Data rate (Gb/s)	30	10	49	10	10
Tap spacing (ps)	35	75	6.75	33	50
Number of taps	3	7	7	4	7
Supply voltage (V)	1	2.5	5	1.8	—
Power (mW)	25	287	750	7.3	40
Area (mm $\times$ mm)	0.6 $\times$ 0.5	4.8 $\times$ 1.5	2.0 $\times$ 1.0	—	3.0 $\times$ 1.5

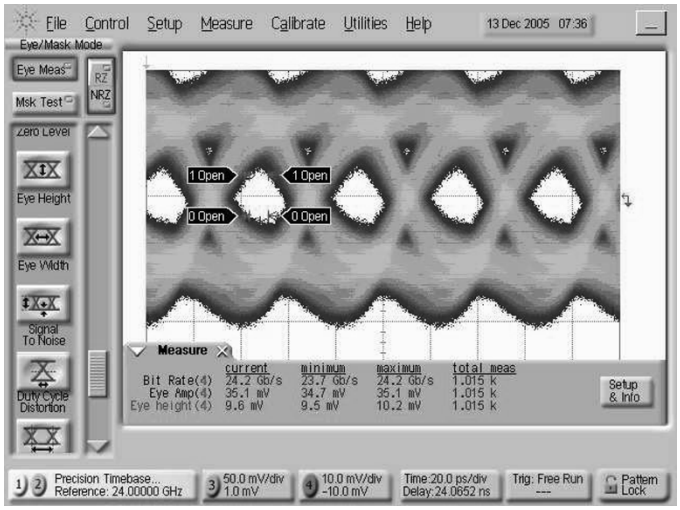

Fig. 18. Equalizer output eye diagram at 24 Gb/s with the coaxial cable channel.

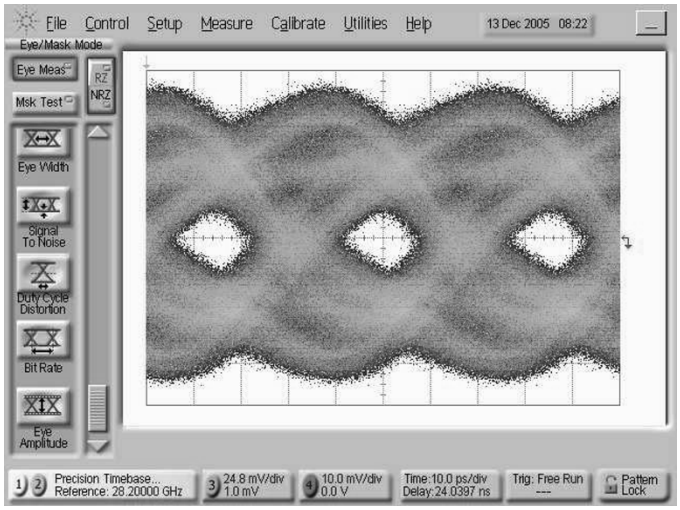

Fig. 19. Equalizer output eye diagram at 28 Gb/s with the coaxial cable channel.

together four independent PRBS $2^{31}-1$ patterns. Although the resulting pattern is not necessarily a PRBS sequence, its broadband spectrum was verified on a spectrum analyzer. The data was passed through a combination of coaxial cable, an attenuator, and connectors whose frequency response is plotted in Fig. 16. The eye diagrams that appeared at the end of this channel (the filter input) are shown in Fig. 17 at 24, 28, and 30 Gb/s.

Figs. 18, 19, and 20 show the filter output at the same data rates. In each case, the tap gains were manually adjusted via trial-and-error to open the eye at the equalizer output (i.e., the tap gains for each data rate were chosen separately). No adaptation circuitry was integrated in this design. A FIR equalizer can compensate for channel losses up to a frequency of $1/2\Delta T$. Since most of the energy in random binary NRZ data appears at frequencies well below the bit rate, it is possible to perform some equalization even at bit rates beyond $1/2\Delta T$, as demonstrated.

In Fig. 20, an eye mask test is used to demonstrate a modest 10 mV per side (20 mV differential) eye opening with no violations. Since the maximum gain of each tap is approximately 0 dB in this design, the channel is equalized by attenuating low-frequency signal content resulting in a small output swing. A low noise amplifier would be required between this circuit and a practical clock and data recovery system.

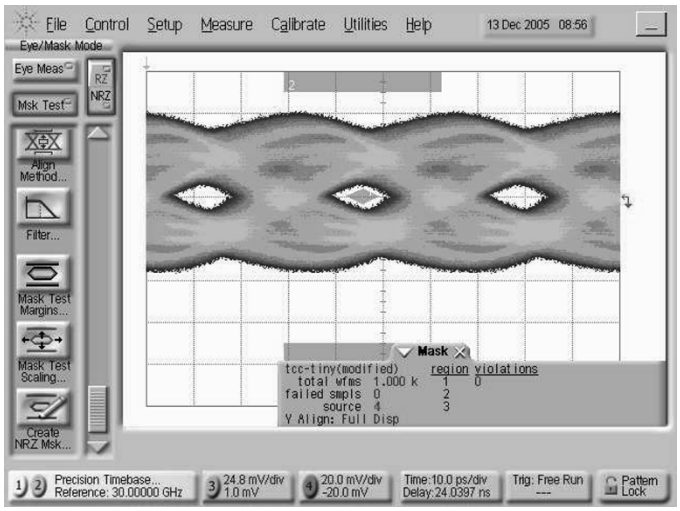

Fig. 20. Equalizer output eye diagram at 30 Gb/s with the coaxial cable channel. The eye mask is 10 mV in height per side (20 mV differential) with no violations observed.

V. Conclusion

The design of a fully differential 3-tap transversal filter in 90-nm CMOS was described. A traditional traveling wave filter topology was modified to increase the filter's bandwidth. A tap spacing of 35 ps is provided by a passive *LC* delay line with differential inductors and digitally programmable capacitors for tuning. The tap weights and an integrated preamplifier have individually digitally programmable gains. The input return loss is better than 16 dB and the output return loss is better than 9 dB up to 30 GHz. The design is 600 μm $\times$ 500 μm and consumes 25 mW.

Table II provides a summary and comparison with other recently reported analog FIR filters. Equalization of NRZ data over a coaxial cable was demonstrated up to 30 Gb/s, making it faster than any previously reported CMOS equalizer. A 1-V supply voltage is enabled by the use of parallel differential pairs for sign control of the transconductances instead of Gilbert cell amplifiers. Finally, the use of coupled differential spirals in the delay lines resulted in a relatively small area (0.3mm^2).

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