HIGH-SPEED BAUD-RATE CLOCK RECOVERY

by

Faisal A. Musa

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Graduate Department of Electrical and Computer Engineering
University of Toronto

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Abstract

Baud-rate clock recovery (CR) is gradually gaining popularity in modern serial data transmission systems since these CR techniques do not require edge-samples for extracting timing information. However, previous baud-rate techniques for high-speed serial links either rely on specific 4-bit patterns or uncorrelated random data. This work describes the modeling and design of analog filter front-end aided baud-rate CR schemes. Unlike other baud-rate schemes, this technique is not constrained by the properties of the input random data.

Firstly, the thesis develops a hardware-efficient baud-rate algorithm that requires only the slope information of the incoming random data. Called modified sign-sign minimum mean squared error (SSMMSE), this algorithm adjusts the clock sampling phase until the slope is zero through a bang-bang control loop. Secondly, the performance of a modified SSMMSE phase detector is investigated and compared with a conventional edge-sampled phase detector. It is shown that, at severe noise levels, the proposed modified SSMMSE method has better performance compared to the edge-sampled method for equal loop bandwidths.Thirdly, the thesis investigates different hardware-efficient slope detection techniques. Both passive and active filter based slope detection techniques are demonstrated in this work. In addition to slope generation, the active filter performs linear equalization as well. However, the passive filter generates the slope information at higher speeds than the active filter and also consumes less power. The two filters are used to recover a 2-GHz clock by using an external bang-bang loop.

In short, the thesis demonstrates that area and power savings can be achieved by utilizing slope information from front-end filters without compromising the performance of the CR unit.

Acknowledgments

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Chapter 1

Introduction

1.1 Motivation

Clock and data recovery (CDR) is one of the most challenging receiver functions in modern serial data transmission systems. Fig. 1.1 shows the physical location of a CDR in a typical serial link [1],[2]. Parallel bit streams supplied by a set of parallel channels are converted into a single bit stream by time division multiplexing. Since the receiver side lacks an explicit timing reference, a CDR is required to recover the timing information and retime the incoming bit stream in the presence of different deterministic and random noise sources.

CDR techniques have been extensively studied in the literature [3]. Although a large variety of CDR architectures exist, CMOS implementations of CDR techniques can be

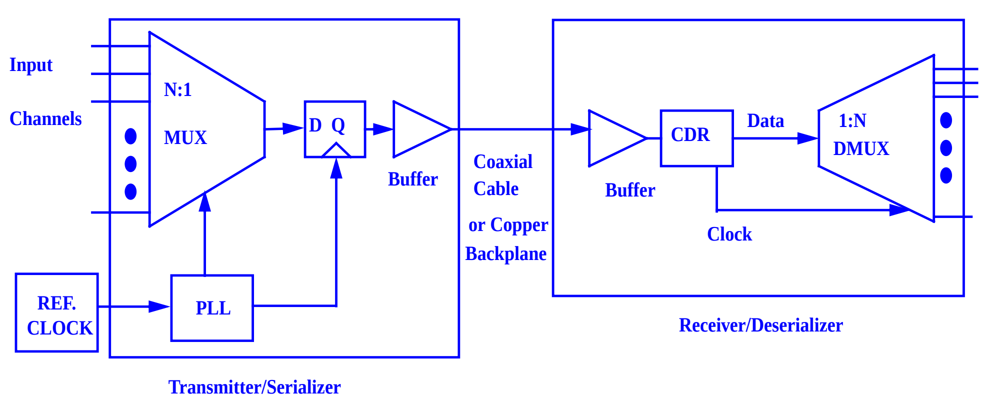


Figure 1.1: Blockdiagram of typical serial link

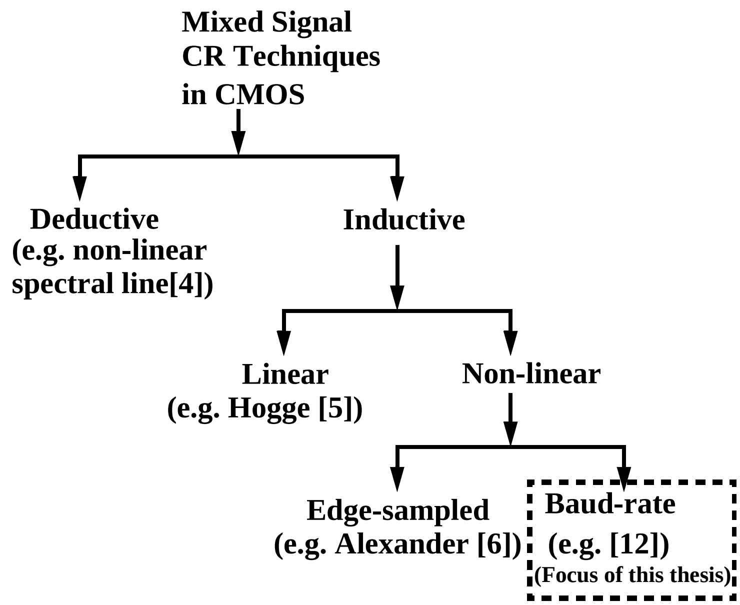


Figure 1.2: Classification of CMOS clock recovery schemes.

divided into two basic categories [1] as shown in Fig. 1.2: (1) deductive and (2) inductive. Deductive techniques generate a timing tone at the data rate by passing the data waveform through a nonlinearity (such as a squarer) and a PLL is used to lock a low jitter clock to this tone. An example is the nonlinear spectral line method [4]. In this case the input data is squared and then passed through a high Q bandpass filter to extract a tone at the baud-rate. The similarity between this technique and one of the clock recovery schemes presented in this work will be discussed later.

Inductive methods simply comprise a PLL whose phase detector (PD) can extract timing information directly from the input data. Based on the technique of extracting timing information, inductive CDR architectures are subdivided into: (1) Linear (e.g. Hogge PD [5]) and (2) Nonlinear (e.g. Alexander PD [6]). Fig. 1.3 shows examples of the two techniques.

In the presence of data transitions, the Hogge PD in Fig. 1.3(a) generates pulses whose width are proportional to the phase error between the data and clock, and compares them to fixed-width reference pulses. The average difference between the proportional and reference pulses indicates the magnitude and polarity of the phase error. Under

[1]It is important to note that the clock recovery schemes shown in Fig. 1.2 are not technology dependent and can be applied to any technology. This is due to the fact that the basic building blocks for these clock recovery schemes can be fabricated in any technology.

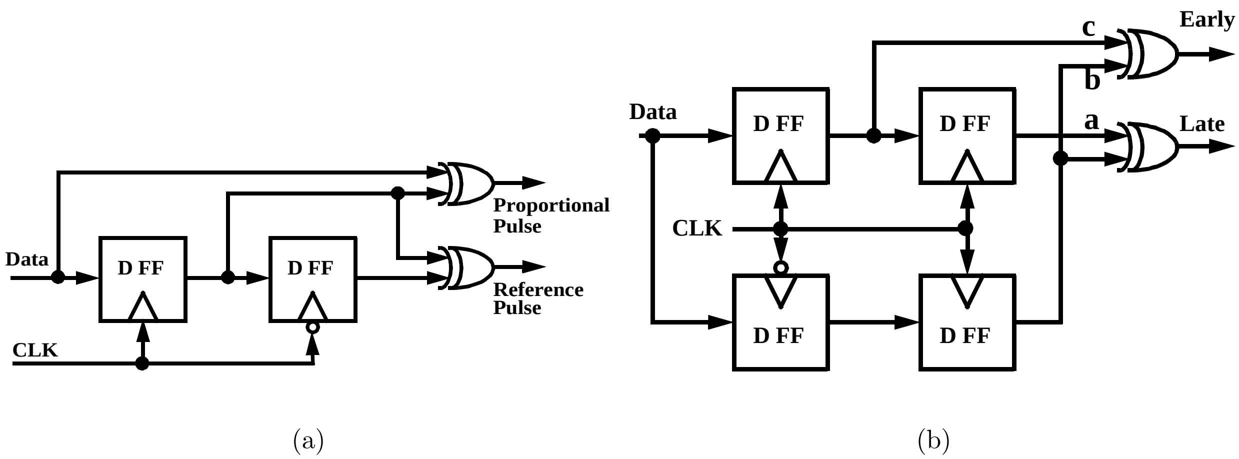


Figure 1.3: Inductive PD schemes. (a) Linear (e.g. Hogge PD). (b) Non-linear (e.g. Alexander PD).

locked conditions, the average width of the proportional pulses approximately equals that of the reference pulses[11],[12]. Phase acquisition can also be achieved using the Alexander PD in Fig. 1.3(b) where data samples are compared with transition samples to determine whether the clock is early or late. Since this PD only detects the polarity of the phase error it is inherently nonlinear and results in larger jitter under locked conditions. However, bang-bang CDRs are more robust than linear (Hogge) CDRs since they are less demanding on the "analog" features of the IC technology [7]. As shown in Fig. 1.3(a), the Hogge PD needs to generate narrow pulses in the proportional path, thus requiring a wide bandwidth exclusive-OR gate. In contrast, the bang-bang PD generates only fixed width pulses and thus the maximum speed requirement for its logic gates is similar to the input data rate. Also, a bang-bang PD allows for a complete digital CDR implementation; e.g. [8]. Examples of 10-Gb/s bang-bang CDRs for SONET applications were reported in [7],[9] and for a 40-Gb/s application in [10]. Most nonlinear inductive CDRs in CMOS employ Alexander phase detection scheme which relies on edge samples for clock recovery.

Another class of inductive schemes are called "baud-rate" schemes. In this work, the term "baud-rate" implies a nonlinear inductive CDR scheme that does not use edge samples (or transition samples) in its PD. This thesis focuses on baud-rate schemes because of the potential advantages over their edge-sampled counterparts. Firstly, the number of clock sampling phases can be reduced by half if the PD employs a baud-rate architecture instead of an edge-sample PD as shown in Fig. 1.4. Thus baud-rate schemes

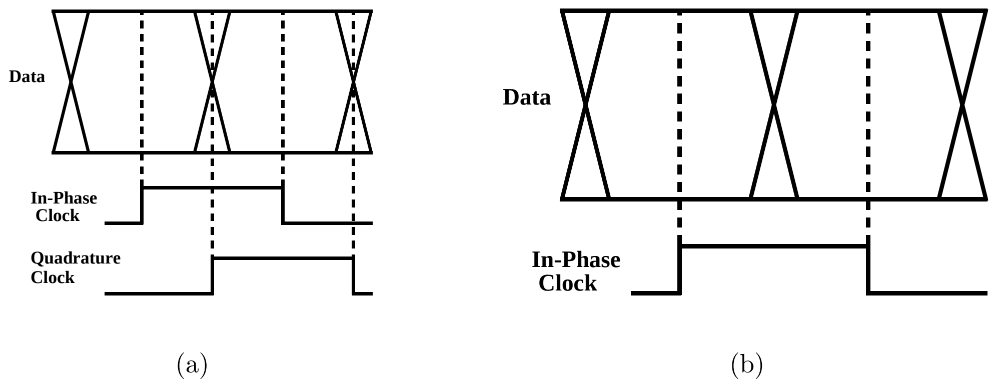


Figure 1.4: Timing diagrams for two nonlinear inductive CDRs (a) Edge-sample (or Alexander) PD based CDR. (b) Baud-rate PD based CDR.

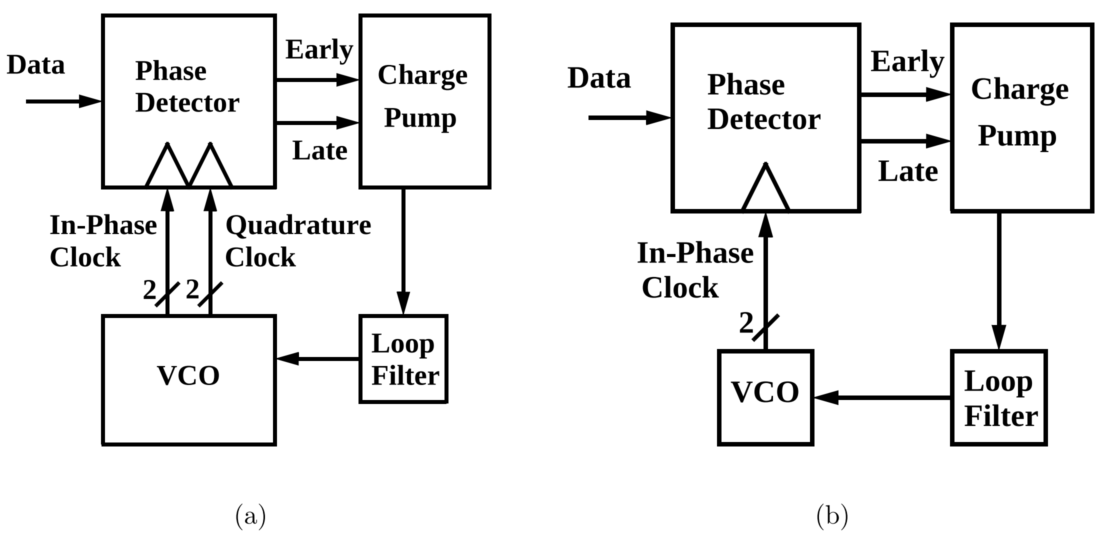


Figure 1.5: Block diagrams for half-rate CDRs. (a) Edge-sample (or Alexander PD) based CDR. (b) Baud-rate CDR.

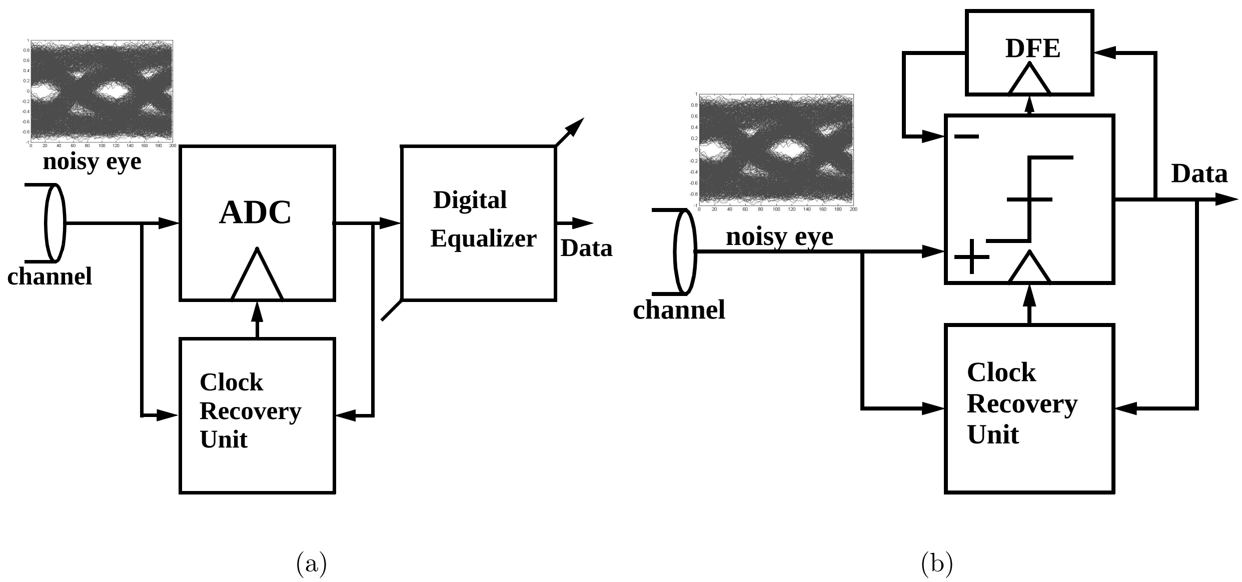


Figure 1.6: Extracting timing information from a noisy eye with two different front-ends. (a) Front-end consisting of an ADC and digital equalizer. (b) Front-end consisting of a decision circuit and DFE.

have the potential to save power in CDRs by simplifying the VCO (as shown in Fig. 1.5 for a half-rate clock [9]) and possibly the phase detector. Secondly, as will be shown in this thesis, baud-rate CDRs have the potential for better performance when recovering a clock from a noisy input. Fig. 1.6 depicts two instances where clock recovery is required from data that is severely corrupted by deterministic and random noise sources. In Fig. 1.6(a), an ADC is placed at the receiver front end to utilize a digital equalizer. Proper operation of the ADC requires a low jitter clock. In Fig. 1.6(b), a Decision Feedback Equalizer (DFE) is used to compensate for channel non-idealities and also requires a low jitter clock for proper operation. As will be shown later, a certain class of baud-rate schemes perform better under these circumstances (i.e. low signal-to-noise ratios), since they infer the timing phase without edge samples.

To summarize, the objectives of this thesis are:

(1) Investigate different baud-rate techniques and select a robust[2] architecture suitable for high-speed[3] serial links in CMOS. Both binary and multilevel PAM links are considered

[2]The term “robust” implies a technique that can handle the widest variety of data statistics.

[3]In this work, the term “high-speed” implies link speeds greater than 1Gb/s with simple binary NRZ or N-PAM modulation.

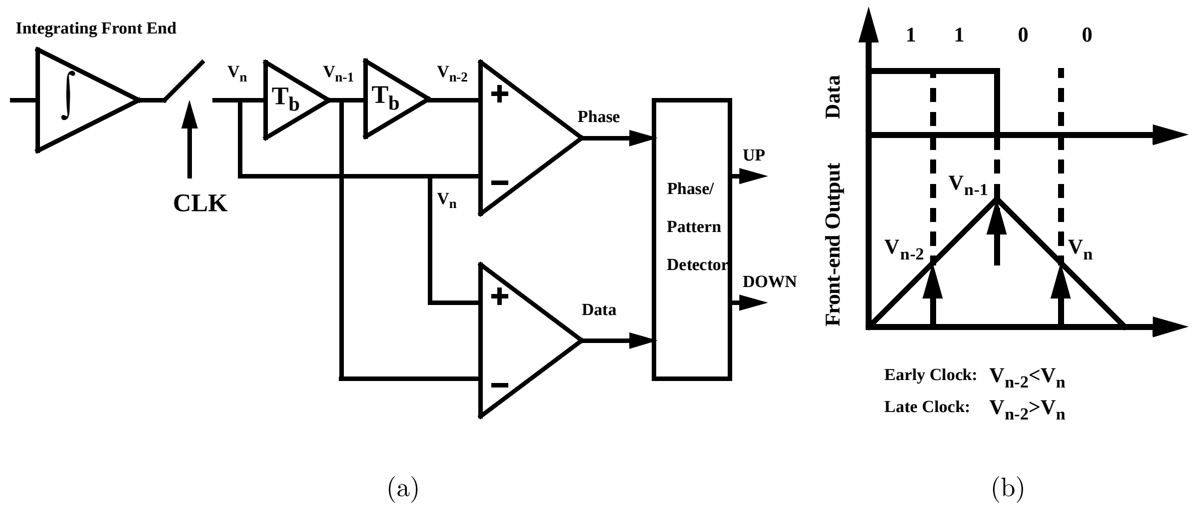


Figure 1.7: Integrating front-end based baud-rate clock recovery (a) Block diagram. (b) Timing diagram.

since both are being used in high speed serial link research.

(2) Compare the performance of the selected technique to that of a typical bang-bang type architecture (e.g. an Alexander PD based CDR) in the presence of deterministic and random noise.

(3) Implement the technique for a high-speed serial link.

1.2 Overview of different Baud-Rate CDR techniques

This section reviews different baud-rate techniques reported in the literature for high-speed serial links and discusses their pros and cons.

1.2.1 Integrating front-end based baud-rate clock recovery

This method utilizes an integrating front-end to extract timing information from the data samples [13]. As shown in Fig. 1.7(a), the integrator output is fed to data samplers which are followed by two sets of comparators: one set for data recovery and the other set for clock recovery. Data recovery is achieved by comparing each bit sample V_n with its one-bit older sample V_{n-1}. However, clock recovery is achieved by comparing each bit sample, V_n with its two bit older sample, V_{n-2}. As shown in Fig. 1.7(b), this comparison only produces correct phase information for a 1100 pattern or a 0011 pattern. Other patterns can give incorrect phase updates. In fact, an alternating pattern (i.e. 10101010.. pattern) always gives incorrect phase information for this architecture and therefore may cause the loop to lose lock. Therefore, some logic is required to deactivate the PD when such patterns are encountered.

This technique is hardware-efficient compared to the Alexander PD based CDR since it requires half the number of samplers and half the number of clock sampling phases. However, since the PD requires specific 4-bit patterns for correct phase updates, the PD can be inactive for long periods of time while waiting for the correct bit sequence [13]. Also, the scheme requires an integrating front-end architecture. Alexander PDs work with or without an integrating front-end. The low-pass characteristics of integrating front-ends make them prone to intersymbol interference (ISI) thus limiting the maximum allowable data rate for this scheme.

1.2.2 Mueller-Muller PD based CDR

The purpose of Mueller-Muller (MM) timing recovery is to infer the channel response from baud-rate samples of the received data and then to align the sampling clock to the center of the pulse response [14]. Denoting the pulse response by $h(t)$ and the bit interval by T_b, the sampling phase τ_k may be considered centered when $h(\tau_k - T_b) = h(\tau_k + T_b)$ as shown in Fig. 1.8(a). Therefore, the clock will be early when $h(\tau_k - T_b) < h(\tau_k + T_b)$ and it will be late when $h(\tau_k - T_b) > h(\tau_k + T_b)$. Hence, all that is required is an estimate of the difference between $h(\tau_k - T_b)$ and $h(\tau_k + T_b)$. Assuming A_m are the data symbols, the received signal can be expressed as,

$$x(t) = \sum_m A_m h(t - mT_b) \tag{1.1}$$

For the k^{th} sample taken at time $t = kT_b + \tau_k$,

$$x_k = x(kT_b + \tau_k) = \sum_m A_m h[(k-m)T_b + \tau_k] = \sum_i A_{k-i} h(iT_b + \tau_k) \tag{1.2}$$

Multiplying both sides by A_{k-1} and taking the expectation,

$$E[x_k A_{k-1}] = \sum_i E[A_{k-i} A_{k-1} h(iT_b + \tau_k)] \approx A^2 h(\tau_k + T_b) \tag{1.3}$$

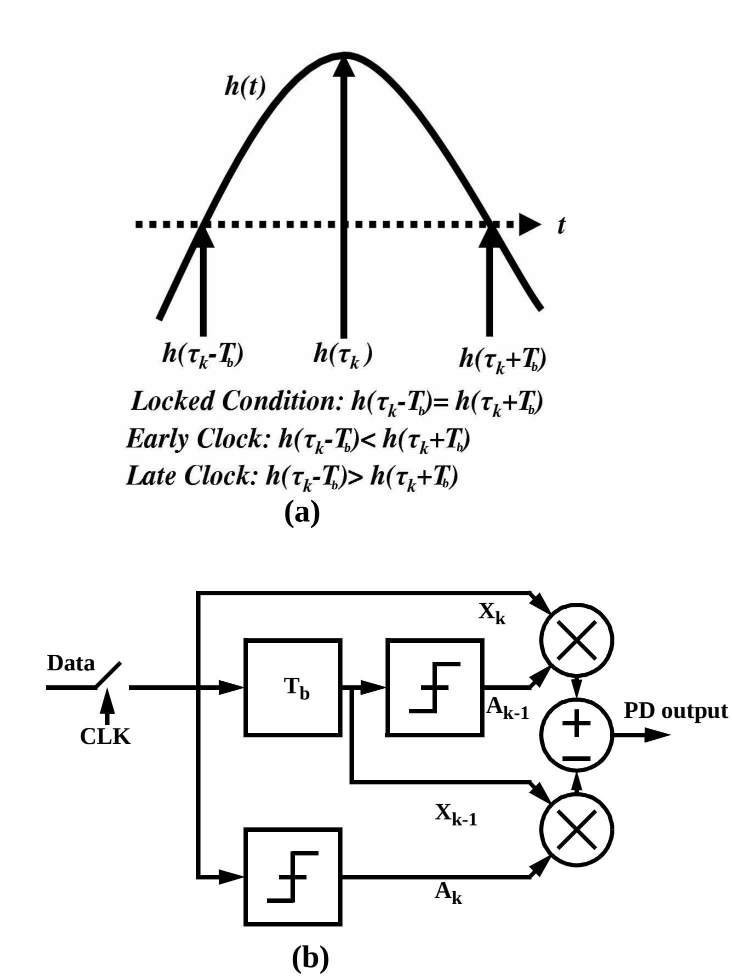


Figure 1.8: Principle of Mueller-Muller (MM) timing recovery. (a) Concept of obtaining timing information from the pulse response. (b) Block diagram.

where $A^2 = E[A_{k-1}^2] = E[A_k^2]$. The approximation in Eq. (1.3) assumes independent and equiprobable data. Similarly,

$$E[x_{k-1}A_k] \approx A^2 h(\tau_k - T_b) \tag{1.4}$$

Combining Eq. (1.3) and (1.4),

$$E[x_k A_{k-1} - x_{k-1}A_k] \approx A^2[h(\tau_k + T_b) - h(\tau_k - T_b)] \tag{1.5}$$

Fig. 1.8(b) shows a block diagram of the MM PD implementing Eq. (1.5). The expected value is obtained by averaging the PD output in the CDR's loop filter.

Instead of using the signal samples x_{k-1} and x_k, the error signal, $e_k = x_k - A_k$ can also be used [14]. This algorithm has been implemented in a 4.8-6.4 Gb/s serial link with a 4-tap DFE [15].

The major drawback of the MM technique is that it is applicable only to independent and equiprobable random data[14]. Consequently, an alternating data pattern may cause the timing loop to lose lock. Also, this algorithm locks the sampling phase to the center of a symmetric pulse response [14],[15]. Therefore, the clock sampling phase may be skewed to one side of the data eye for an asymmetric pulse response.

1.2.3 Minimum mean squared error (MMSE) PD based CDR

Minimum mean squared error (MMSE) timing recovery ([16],p.748) optimizes the sampling phase in a digital receiver by minimizing the expected value of the squared error, e_k^2:

$$E_k = E[e_k^2] = E[(A_k - y(kT_b + \tau_k))^2] \tag{1.6}$$

Here A_k represents the kth data bit, $y(t)$ the received waveform, T_b the symbol period,τ_k the sampling phase for the kth data bit and $e_k = A_k - y(kT_b + \tau_k)$. MMSE requires that the sampling phase, τ_k be adjusted in the direction opposite the gradient, $\delta E_k/\delta\tau_k$:

$$\tau_{k+1} = \tau_k - \mu\left(\frac{\delta E_k}{\delta\tau_k}\right) \tag{1.7}$$

Here μ is a parameter that is chosen to tradeoff acquisition time with jitter and determines how quickly τ_k is adjusted. Substituting Eq. (1.6) into Eq. (1.7) and dropping the expectation operator results in the following stochastic gradient update rule:

$$\tau_{k+1} = \tau_k + 2\mu e_k\left(\frac{\delta y(kT_b + \tau_k)}{\delta\tau_k}\right) \tag{1.8}$$

The MMSE algorithm has been used for timing recovery in magnetic storage channels [17],[18].

Generation of the slope and error signals are the major challenges in implementing MMSE at high speeds. Although a two-tap approximation to the slope is normally used in magnetic storage applications, it leads to large clock jitter ([16],p.760) which can be a major problem in high-speed serial links.

1.2.4 Choice of baud-rate MMSE CDR

This work focuses on MMSE baud-rate timing recovery:

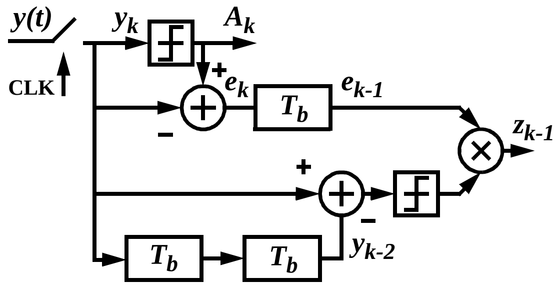


Figure 1.9: Typical block diagram of MMSE timing recovery that uses a 2-tap slope detector.

(1) MMSE is more robust than the baud-rate schemes based on the integrating front end [13] & MM methods [15].

(2) Being a baud-rate scheme, it does not require edge samples for clock recovery and thus is an attractive alternative to the Alexander PD based CDR.

However, it is necessary to seek more hardware efficient implementations to MMSE timing recovery for high speed serial links. Moreover, it is unclear whether MMSE will perform better than an Alexander PD based CDR in a noisy environment. Therefore, a generic model that includes the effect of different noise sources has to be developed and then utilized to perform a fair comparison of the two PDs.

1.3 MMSE PD schemes for high-speed serial links

1.3.1 Review of published MMSE schemes

Currently, the biggest application area for MMSE is disk drive systems [17],[18]. The phase update equation used in these implementations is

$$\tau_k = \tau_{k-1} + 2\mu e_{k-1}\mathrm{sgn}\,(y_k - y_{k-2}) \tag{1.9}$$

Note that the phase update equation requires an error signal in addition to the slope. Note also that the second term in Eq. (1.9) uses a 2-tap approximation to the slope. This 2-tap approximation may not always produce correct slope information and is valid under the assumption that the sampling phase is varying slowly enough such that it can be considered constant ([16], p.760) over many bit periods. Fig. 1.9 shows the block diagram of MMSE timing recovery that uses Eq. (1.9) .

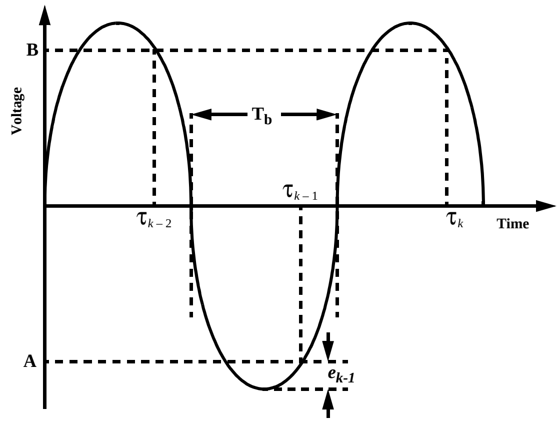


Figure 1.10: Slope estimation using a two-tap filter.

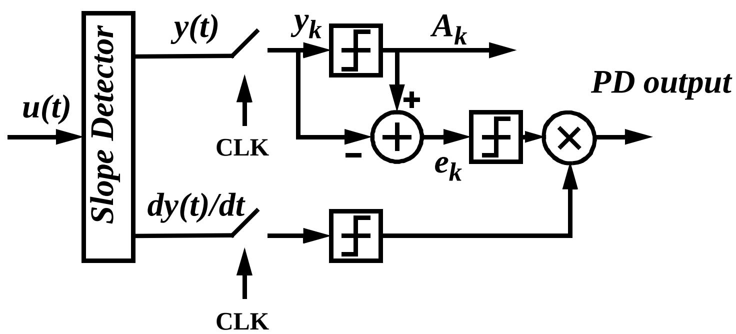


Figure 1.11: Block diagram of sign-sign MMSE (SSMMSE).

Fig. 1.10 shows a periodic pattern with a bit period equal to T_b. Assuming the current sampling phase is τ_k, the sampled voltage at τ_{k-1} is A. The polarity of the slope depends on the sampled voltages at τ_k and at τ_{k-2}. Since the sampled voltages at these two instants are so close to each other, the polarity of the slope has an equal probability of being either +1 or -1 whereas the true sign of the slope at τ_{k-1} is +1.

Obviously, a more accurate estimation of the slope at high-speeds would be a continuous-time slope detector which would permit an exact implementation of Eq. (1.8) instead of the approximation in Eq. (1.9).

1.3.2 Sign-Sign MMSE (SSMMSE)

Practical high-speed implementations of adaptation algorithms often use only 1-bit representations of the sign of the error and the gradient signals [21]. Applying this idea

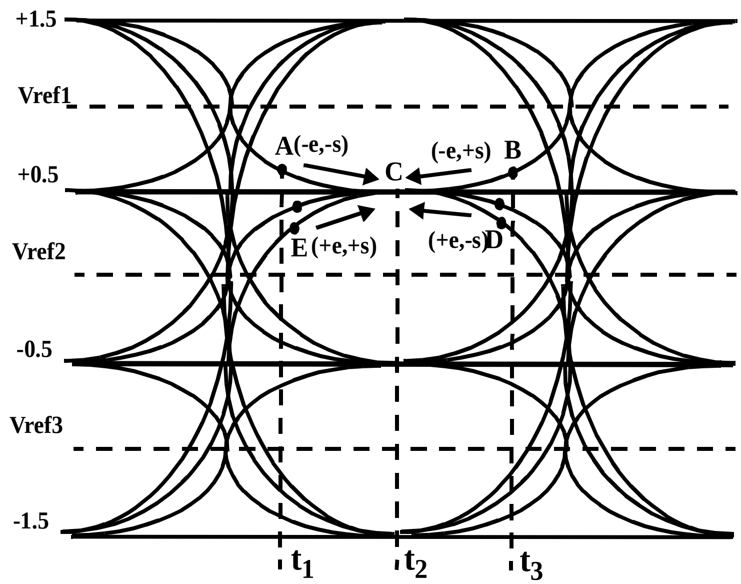


Figure 1.12: 4-PAM eye

Table 1.1: SSMMSE PD Truth Table

Sampling Point (Fig. 1.12)	Error (e)	Slope (s)	PD decision
A	0	0	Early
B	0	1	Late
D	1	0	Late
E	1	1	Early

to MMSE TR results in the following Sign-Sign MMSE (SSMMSE) rule [22]:

$$\tau_{k+1} = \tau_k + \theta_{bb}\mathrm{sgn}(e_k)\mathrm{sgn}\left(\frac{\delta y(kT_b + \tau_k)}{\delta \tau_k}\right) \tag{1.10}$$

where the bang-bang phase update, θ_{bb} replaces 2μ. As shown in Fig. 1.11, this scheme proposes a continuous time approach to slope detection. Considering the 4-PAM signal shown in Fig. 1.12, let A be the sampled data due to a clock sampling phase of t_1. The sampling phase being incorrect, the sampled data deviates from the desired signal level (which is +0.5 in this case) thus producing a finite negative error. The slope of the received signal is negative. To decrease the mean squared error, the VCO frequency must decrease so that the sampled data point is C instead of A. If the sampling phase is t_3 (i.e. point B) the error is still negative but the slope is positive. The VCO frequency must increase to advance the clock phase to t_2. The decision to advance or delay the sampling phase can be based on the signs of the error and the slope at the sampling point as shown in Table 1.1. Here a positive error/slope is denoted by 1 and a negative error/slope by 0. Therefore, the early/late pulses can be generated as follows:

$$Early = D(e \odot s); Late = D(e \oplus s) \tag{1.11}$$

where $\oplus$ and $\odot$ denote the exclusive-OR operation and the exclusive-NOR operation respectively and D is high whenever the 4-PAM signal is in between V_{ref1} and V_{ref2}. In addition to the data and slope slicers, this technique requires an extra slicer for the error signal. Therefore, a simpler phase update equation needs to be developed to eliminate the error signal.

1.3.3 Modified SSMMSE

The SSMMSE method can be simplified to exclude the error signal. For example, consider binary NRZ data over a low pass channel with no overshoot. If $A_k = +1$ (i.e. a positive level is received), and there is no overshoot in the channel pulse response, the sampled analog voltage $y(kT_b + \tau_k)$ will be between 0 and +1, hence the sign of the error signal, e_k must be positive[4]. Therefore Eq. (1.10) can be modified for positive bits,

$$\tau_{k+1} = \tau_k + \theta_{bb}\mathrm{sgn}\left(\frac{\delta y(kT_b + \tau_k)}{\delta\tau_k}\right),\ y(kT_b + \tau_k) > 0 \tag{1.12}$$

A similar argument can be made when a negative level is received, i.e. $A_k = -1$. In this case, the sign of the error signal, e_k will be negative. Therefore Eq. (1.10) can be modified for negative bits,

$$\tau_{k+1} = \tau_k - \theta_{bb}\mathrm{sgn}\left(\frac{\delta y(kT_b + \tau_k)}{\delta\tau_k}\right),\ y(kT_b + \tau_k) < 0 \tag{1.13}$$

Note that in both Eq. (1.12) and Eq. (1.13), the sign of the error has been replaced by the sign of the corresponding analog voltage $y(kT_b + \tau_k)$. Thus combining Eq. (1.12) and Eq. (1.13),

$$\tau_{k+1} = \tau_k + \theta_{bb}\mathrm{sgn}(y(kT_b + \tau_k))\mathrm{sgn}\left(\frac{\delta y(kT_b + \tau_k)}{\delta\tau_k}\right) \tag{1.14}$$

Eq. (1.14) reveals that SSMMSE can be modified to exclude the error signal for NRZ

[4] Recall that $e_k = A_k - y(kT_b + \tau_k)$.

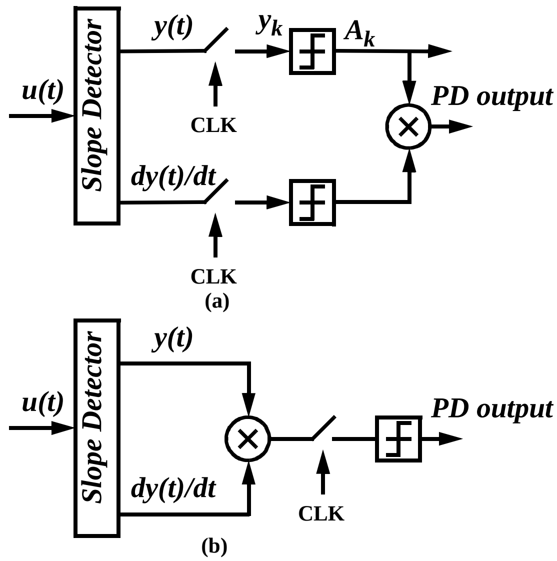


Figure 1.13: Modified SSMMSE. (a) With two slicers and digital logic. (b) With one slicer and a Gilbert Cell.

data. From an implementation perspective, both the data and slope signals can be applied to slicers and the results passed through an exclusive-OR gate. This is shown in Fig. 1.13(a). Although derived for NRZ data, this algorithm can work for 4-PAM signals when the phase detector monitors maximum or minimum levels. This will be discussed in chapter 2. Note that this is similar to"error-free MMSE" or the "sampled derivative algorithm" first proposed in [23].

The number of slicers can be further reduced by directly multiplying the signal $y(kT_b + \tau_k)$ with its slope (for example, a Gilbert cell mixer) and then retiming the output with a single slicer as shown in Fig. 1.13(b):

$$\tau_{k+1} = \tau_k + \theta_{bb}\text{sgn}\left(y(kT_b + \tau_k)\frac{\delta y(kT_b + \tau_k)}{\delta \tau_k}\right) \tag{1.15}$$

The proposed MMSE scheme has a strong resemblance to nonlinear spectral line methods [4]. This can be realized by rewriting Eq. (1.15) as follows:

$$\tau_{k+1} = \tau_k + \theta_{bb}\text{sgn}\left(\frac{1}{2}\frac{\delta[y(kT_b + \tau_k)]^2}{\delta \tau_k}\right) \tag{1.16}$$

Eq. (1.16) shows that the proposed TR function can also be generated by taking the derivative of the input data squared. A practical implementation of a derivative block

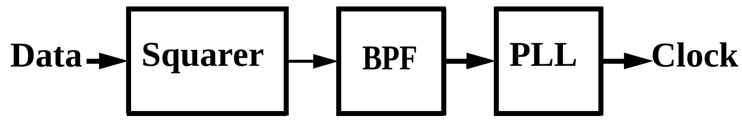


Figure 1.14: Typical nonlinear spectral line method.

would be a bandpass filter since the circuit parasitics would eventually pull down the high frequency response. In nonlinear spectral line techniques (Fig. 1.14), the input data is squared and then passed through a high Q bandpass filter to extract a tone at the baud-rate. In the modified SSMMSE case, the input data is first passed through a bandpass filter (i.e. a practical derivative block) and then multiplied by the input data signal.

Several advantages show up as a result of this implementation. Firstly, the timing recovery loop locks to the maximum vertical data eye opening since it tracks the slope of the incoming data waveform. Secondly, in cases where a linear equalizer is necessary to preserve signal integrity, the slope detector function can be integrated into the linear equalizer thus saving power and area. An analog filter that performs the dual function of a linear equalizer and slope detector is described in chapter 4.

Note that if there is peaking in the data eye, the assumptions about the sign of the error upon which Eq. (1.15) is based are no longer true. Nevertheless the nonlinearity in Eq. (1.16) generates a timing tone in the presence of peaking in the data eye which the TR loop can lock to. This is experimentally verified in section 4.4.

1.3.4 Effect of zero-ISI channel

For a zero-ISI channel, the data eye is wide open and consequently the slope goes to zero for a large fraction of each bit interval. Hence, MMSE timing recovery may cause the recovered clock phase to wander across the eye resulting in large jitter. To avoid this "zero-slope" condition, an analog filter front-end needs to band-limit the incoming signal for a wide range of data rates. This can be achieved by using a programmable filter as was done for the dual-function analog filter described in chapter 4.

To have an estimate of the bandwidth requirement of the front-end filter, the normalized mean squared error vs. sampling phase is plotted in Fig. 1.15 for an MMSE PD with an infinite bandwidth front-end and a 6-GHz bandwidth front-end. Note that for the infinite bandwidth front-end case, the mean squared error is zero for a larger interval of time than the 6-GHz bandwidth case. Consequently, the clock phase will be confined

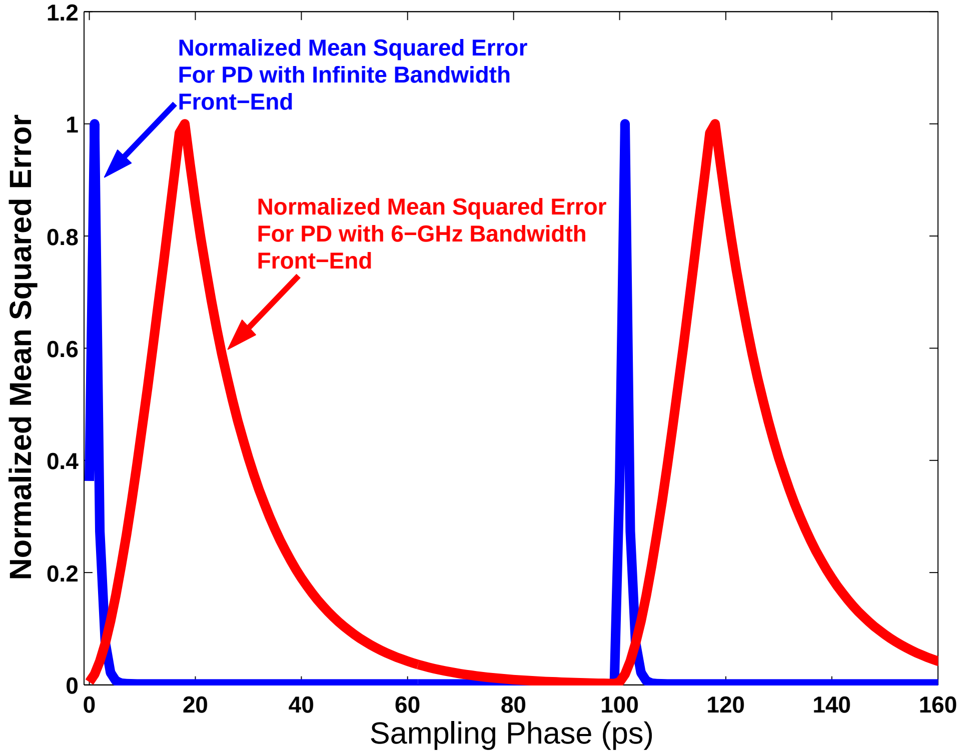


Figure 1.15: Normalized mean squared error vs. sampling phase for 10-Gb/s MMSE PD with two different front-end bandwidths.

to a narrow region for the 6-GHz front-end bandwidth case resulting in lower jitter. As a rule of thumb, the over-all bandwidth at the receiver front-end (including PCB traces, pads, metal layer parasitics and device parasitics) should be 70-60 % of the desired data rate.

It is important to note the contradictory requirements of the front-end amplifier in an Alexander PD and an MMSE PD. For an Alexander PD the front-end amplifier is designed for a large bandwidth to ensure fast rise and fall times [1]. For the MMSE PD, the front-end amplifier needs to bandlimit the input signal, thus relaxing the design of the front-end amplifier. Moreover, a bandlimited front-end limits the random noise input to the receiver,thus improving the SNR.

1.3.5 High-speed slope detection

Due to problems encountered in the two-tap approximation to the slope signal, this work proposes a continuous time approach to slope detection.

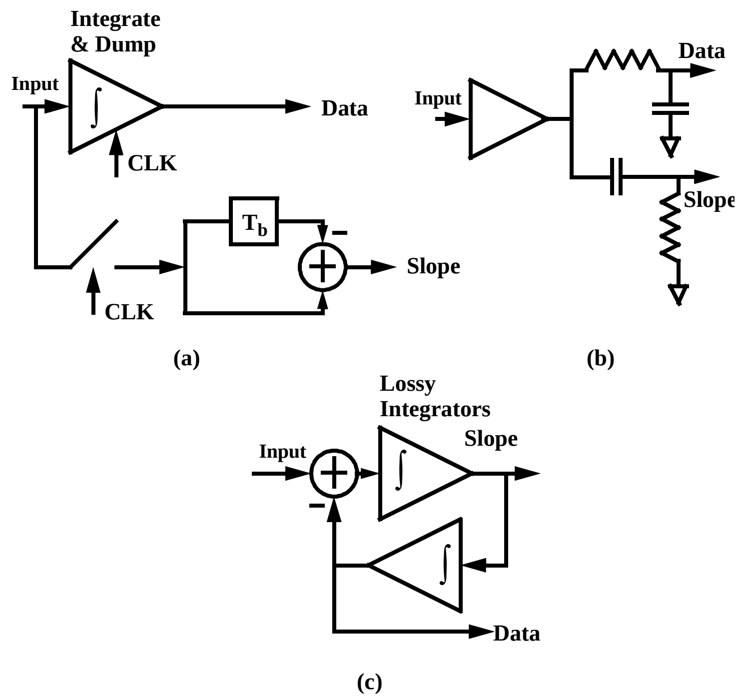


Figure 1.16: Slope detection. (a) Integrate and Dump. (b) Passive Filter. (b) Active Filter.

Integrate and Dump

As shown in Fig. 1.16 (a) slope detection can be simplified if an integrate and dump circuit is present, which is commonly used to perform approximate matched filtering in many receivers [24]. This has the following input-output relationship [22]:

$$y(kT_b + \tau_k) = \int_{(k-1)T_b+\tau_{k-1}}^{kT_b+\tau_k} u(t)\, dt \tag{1.17}$$

where $u(t)$ is the input and $y(t)$ is the output. Taking the derivative of both sides,

$$\left(\frac{\delta y(kT_b + \tau_k)}{\delta \tau_k}\right) = u(kT_b + \tau_k) - u((k-1)T_b + \tau_{k-1}) \tag{1.18}$$

This approach is simple and provides a low power solution to slope detection. However, the low-pass characteristics of integrating front-ends make them prone to intersymbol interference (ISI) thus limiting the maximum allowable data rate for this scheme.

Passive Filter

The data can be passed simultaneously through a low-pass and a high-pass first order passive filter section as shown in Fig. 1.16(b). This will align the slope signal with the data eye over a broad bandwidth. However, there is a trade-off between the passive filter bandwidth and sensitivity of the phase detector. This technique is considered in chapters 2 and 3.

Active Filter

An active filter can be utilized to provide data and slope information simultaneously as shown in Fig. 1.16(c). The active filter path can be designed to include linear equalization as well. This technique is considered in chapter 4.

1.4 Organization of the thesis

Chapter 2 discusses modeling and performance comparison of Alexander and modified SSMMSE PD based CDRs. Chapter 3 discusses how a passive filter may be used to aid modified SSMMSE timing recovery. Chapter 4 describes the design and implementation of an active filter that performs linear equalization with slope detection. Chapter 5 concludes the thesis with recommendations and future work.

Chapter 2

Analysis and modeling of bang-bang CDRs

2.1 Introduction

In this chapter, a modified SSMMSE PD is modeled using a stochastic analysis and its performance compared with a typical Alexander PD-based CDR [25]. To permit a fair comparison, the two CDRs must be designed for equal loop bandwidths. Therefore, a method to linearize the nonlinear PD in the presence of input noise and ISI is introduced. The linearized model is verified for a 4-PAM coaxial cable link by comparing its predicted jitter transfer to simulations. The RMS jitter of the CDRs in the presence of input noise and ISI are predicted using a linear CDR model and a Markov chain and the predictions are verified using behavioral simulations. Jitter tolerance simulations are also employed to compare the two CDRs. Both analytical calculations and behavioral simulations predict that at equal loop bandwidths, the modified SSMMSE PD architecture is superior to the Alexander type CDR when large ISI and/or low signal to noise ratios are present.

2.1.1 Background

Analysis of bang-bang phase-locked or clock recovery loops is complicated due to the inherent nonlinearity of the phase detector (PD). An attempt to linearize a bang-bang phase locked loop in [26] by using an approximation to Gaussian input noise resulted in a square-root dependence of output jitter on input jitter. In [27], a linear regime for a

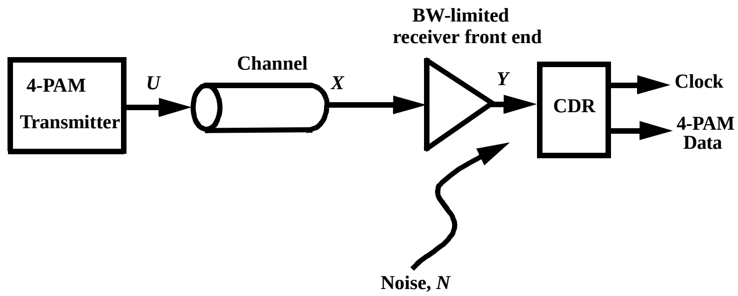


Figure 2.1: 4-PAM system model

bang-bang CDR loop is defined by considering the effect of PD metastability and Gaussian noise. In [28], the effect of ISI, transmitter noise and receiver noise on the performance of a bang-bang loop is analyzed leading to the conclusion that ISI dominates the low-BER analysis. However, none of these references provide an analysis of how deterministic and random noise sources influence the gain of the bang-bang PD and how the CDR should be designed in the presence of these noise sources to meet given specs (such as loop bandwidth, jitter peaking, etc.). Here this is addressed by defining the PD gain as the slope of the average PD output with respect to sampling phase. This PD gain can be analytically determined from knowledge of the channel and noise statistics. The analysis is applicable to binary or multilevel PAM. Two CDRs based on Alexander and a modified SSMMSE PD are analyzed using the model. VCO noise and transmitter noise are introduced in behavioral simulations to verify the loop bandwidth predicted by the model and to estimate the jitter tolerance.

The techniques developed in this work allow us to model the effects of noise and ISI on nonlinear phase detectors. This allows us to choose the phase detector with the best performance (lowest jitter, higher jitter tolerance) for a particular channel. Effects such as ISI and input-referred random noise are emphasized here since these are dominant in high speed serial links [28]. Fig. 2.1 shows the example system to be modeled. A 4-PAM signal is transmitted through a bandlimited channel which leads to ISI. At the receiver end, the signal is further corrupted by additive noise and then fed into the receiver front end which may exacerbate the ISI. The CDR recovers the clock signal which is used to sample the received signal and recover the transmitted data.

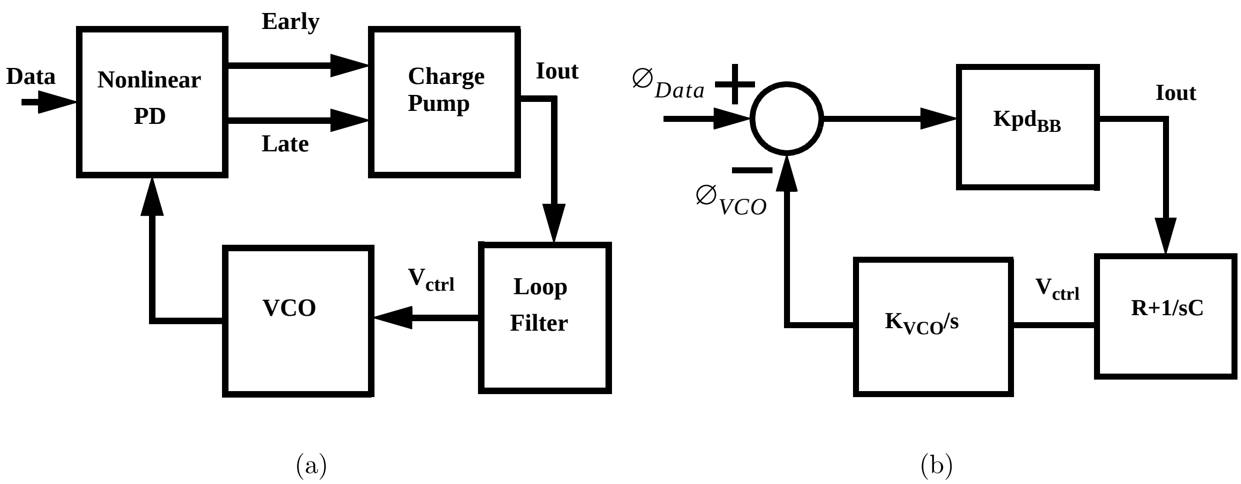


Figure 2.2: Bang-bang PLL. (a) Block diagram. (b) Linearized model.

2.1.2 Chapter Outline

Section 2.2 discusses relevant background concepts and introduces a linear jitter model. Section 2.3 derives a sampling phase dependent probability density function (PDF) for a multilevel serial link. The PDF is used to model Alexander PDs in section 2.4.1. Approximate SSMMSE timing recovery is analyzed, discussed and modeled in Section 2.4.2. In Section 2.5, the two CDRs are compared with respect to non idealities such as ISI, random noise, VCO jitter and jitter tolerance. Finally, the chapter concludes with comments on VLSI realizations of the two CDRs (Section 2.6).

2.2 Concept of linearizing a bang-bang loop

A block diagram of a nonlinear (bang-bang) CDR loop is shown in Fig. 2.2. From the analysis of bang-bang loops described in [26] the bang-bang phase update is defined as,

$$\theta_{bb} = \frac{IRK_{VCO}}{f_{clk}} \tag{2.1}$$

where I is the charge pump current in Amps, f_{clk} is the clock frequency in Hz, K_{VCO} is the VCO gain in Rad/V-s and R is the resistance of the loop filter in ohms. The complete expression for loop bandwidth is given as [29],

$$\omega_{-3dB} = \omega_n[\sqrt{(2\zeta^2+1)+\sqrt{(2\zeta^2+1)^2+1}}] \tag{2.2}$$

Thus for large damping factors, $\zeta \gg 1$, the loop bandwidth can be approximated as,

$$\omega_{-3dB} \approx 2\zeta\omega_n \tag{2.3}$$

For $\zeta = 4$, the loop bandwidth using Eq. 2.2 is equal to $8.13\omega_n$ and the loop bandwidth using Eq. 2.3 is equal to $8\omega_n$. Thus the error is approximately 1.6% for $\zeta = 4$. To meet SONET jitter peaking specifications, ζ needs to be larger than 4.66 [29]. Thus for large damping factor ($\zeta = (R/2)\sqrt{K_{pd}CK_{VCO}}$), the loop bandwidth of a second order linear loop can be approximated as [29],

$$\omega_{-3dB} \approx K_{pd}K_{VCO}R \tag{2.4}$$

where K_{pd} is the gain of the PD and charge pump in A/rad ($K_{pd} = I/2\pi$ for a linear PLL [29]). Eq. (2.4) is accurate within 1.6% for $\zeta > 4$. Substituting Eq. (2.1) in Eq. (2.4), the loop bandwidth of a bang-bang PLL can be expressed as:

$$\omega_{-3dB_{BB}} = 2\pi f_{-3dB_{BB}} = \frac{\theta_{bb}f_{clk}}{I}K_{pd_{BB}} \tag{2.5}$$

Here $K_{pd_{BB}}$ is the gain of the bang-bang PD which has yet to be defined. Since the bang-bang PD drives a charge pump, the average output of the charge pump ($= E[I_{out}]$) can be expressed in terms of the charge pump current, I, and sampling phase, τ:

$$E[I_{out}(\tau)] = -IP_{early}(\tau) + IP_{late}(\tau) = I - 2IP_{early}(\tau) \tag{2.6}$$

where P_{early} denotes the probability of obtaining an early pulse at the output of the PD and $P_{late} = 1 - P_{early}$ is the probability of a late pulse. Clearly both P_{early} and P_{late} are functions of the sampling phase, τ. The gain or sensitivity of the bang-bang PD can be expressed as,

$$K_{pd_{BB}} = \frac{dE[I_{out}(\tau)]}{d\tau}|_{\tau=\tau_{lock}} = -2I\frac{dP_{early}}{d\tau}|_{\tau=\tau_{lock}} \tag{2.7}$$

Substituting Eq. (2.7) in Eq. (2.5),

$$f_{-3dB_{BB}} = -[\frac{\theta_{bb}f_{clk}}{\pi}][\frac{dP_{early}}{d\tau}|_{\tau=\tau_{lock}}] \tag{2.8}$$

Eq. (2.8) computes the loop bandwidth by linearizing the bang-bang PD and is valid as long as the bang-bang phase update,($= \theta_{bb}$) is small enough to keep the phase detector operating within the range of constant $K_{pd_{BB}}$ or approximately constant slope of the P_{early} and P_{late} versus τ curves shown in Fig. 2.3. Note that ISI and noise effect the

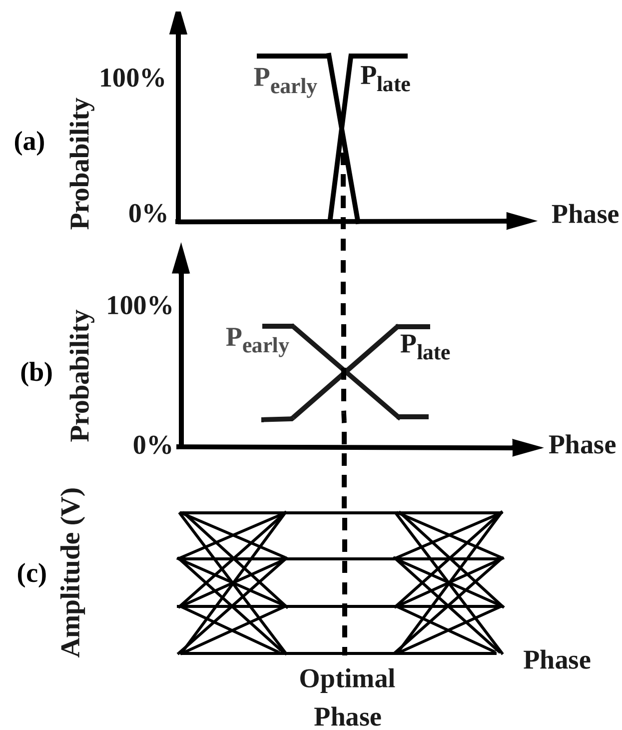


Figure 2.3: Effect of ISI and noise on PD characteristics. (a) Ideal bang-bang PD. (b) Bang-bang PD in ISI and noise. (c) 4-PAM Received eye diagram.

slope of the P_{early} and P_{late} curves shown in Fig. 2.3(a) & (b) and hence the gain of the PD. The statistical properties of the PD (i.e. the P_{early} and P_{late} curves) can be estimated if the probability density function (PDF) at the input to the CDR is known. This is dealt with in the next section. Furthermore, once the PD gain is known, the RMS jitter in the recovered clock (neglecting sources of noise and jitter within the loop) can be estimated following the linearized analysis in [26]. The resulting RMS jitter (in radians) can therefore be expressed as [1],

$$\sigma_{RMS} = \sqrt{\frac{\theta_{bb}}{4(-2\frac{dP_{early}}{d\tau}|_{\tau=\tau_{lock}})}} = \sqrt{I\frac{\theta_{bb}}{4K_{pd_{BB}}}} \tag{2.9}$$

Substituting Eq. (2.5) in (2.9) we get,

$$\sigma_{RMS} = \frac{\sqrt{2\pi}}{-4\frac{dP_{early}}{d\tau}|_{\tau=\tau_{lock}}}\sqrt{\frac{f_{-3dB_{BB}}}{f_{clk}}} \tag{2.10}$$

Eq. (2.10) relates the loop bandwidth and the statistical properties of the PD to the RMS jitter of the recovered clock. Note that for a fixed loop bandwidth, a CDR's recovered clock jitter is inversely proportional to the slope of its P_{early} vs. phase curves in the vicinity of the lock point. If the recovered clock jitter is high, the clock phase, τ will wander over a range for which the slope $dP_{early}/d\tau$ is no longer constant making it difficult to apply Eq. (2.10). This variation in $dP_{early}/d\tau$ can be taken into account by using a random walk model or Markov chain [16]. In this work, both the linear model in Eq. (2.10) and the Markov chain will be used to predict the RMS jitter of the CDR.

2.3 Stochastic Modeling of CDR input

The purpose of this section is to obtain an expression for the probability density function (PDF) of the input signal to the CDR (which is labeled as Y in Fig. 2.1) as a function of sampling phase, τ, from a knowledge of the channel response, the receiver front-end, and the additive noise. This expression can then be used to evaluate the P_{early} and P_{late} curves for the bang-bang CDR and eventually the gain of the PD.

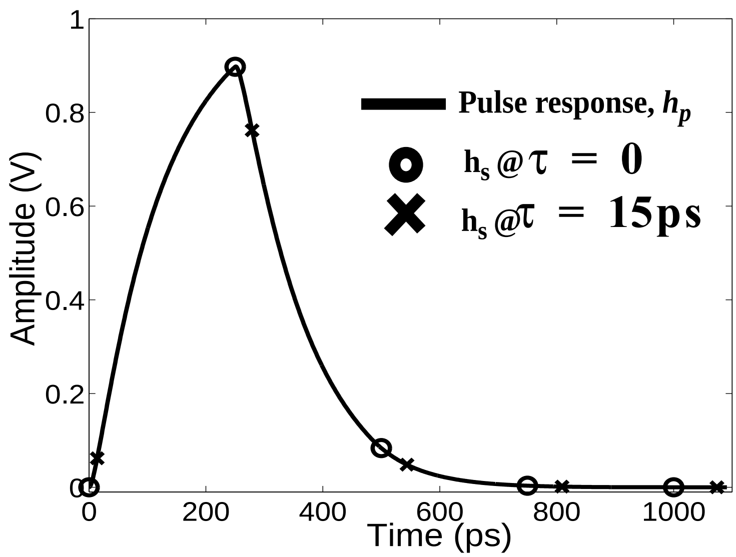


Figure 2.4: Pulse response, h_p of a typical serial link that consists of a 3 meter coaxial cable channel model and 4 GHz first order receive filter @ 4 Gb/s.

2.3.1 Effect of channel response

The analysis assumes that the pulse response of the channel is known. Fig. 2.4 shows a typical pulse response, $h_p(t)$, of the entire path from transmitter to the CDR input. Included in $h_p(t)$ is a coaxial cable model used as the channel and a receiver front end modeled as a first order low pass filter:

$$H_{LPF}(s) = \frac{1}{1 + sT_c} \tag{2.11}$$

The input to the CDR can be expressed as,

$$Y(t) = \sum_{k=-\infty}^{\infty} U(k)h_p(t - kT_b) \tag{2.12}$$

Here U is the random data input to the channel and Y is the receiver front end output. Fig. 2.5 illustrates how previous symbols interfere with the current bit to produce the sampled voltage at any particular sampling phase. Fig. 2.5(a) shows a sequence of transmitted symbols. Neglecting the channel delay, the channel outputs a sequence of pulses, each pulse being weighted by the corresponding transmitted symbol. This is shown in Fig. 2.5(b). The received signal is a sum of these pulses. Thus, at time $t = 2T_b + \tau$ the receiver sampled voltage $Y(2)$ can be expressed as a sum of points A, B and C in Fig. 2.5(b)

[1]The RMS jitter is computed on the recovered clock of the CDR

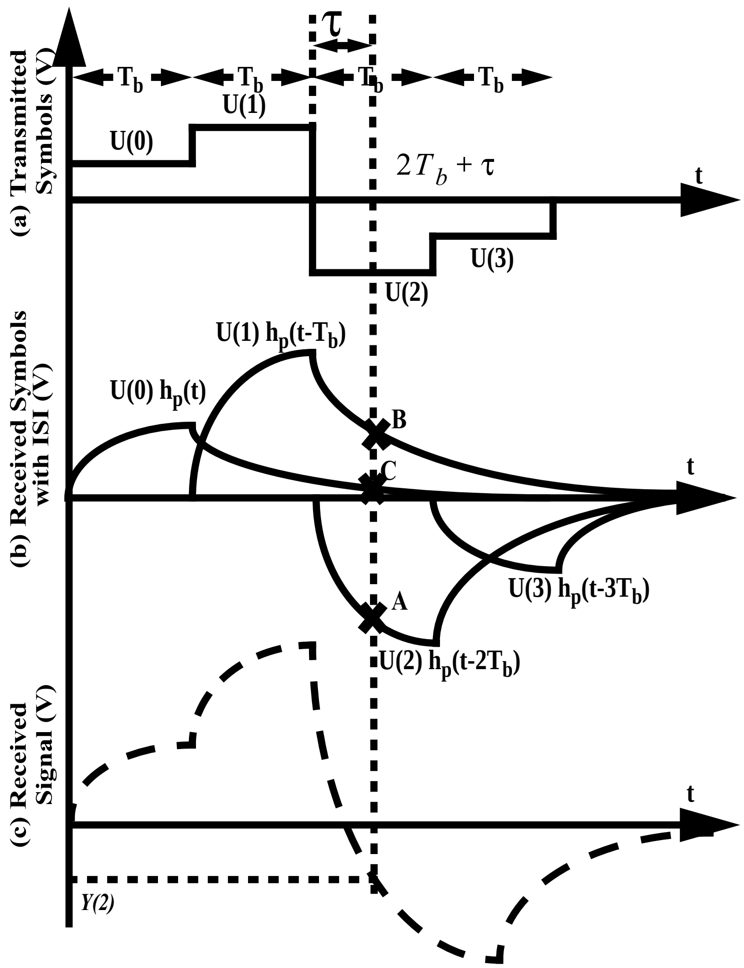


Figure 2.5: Example of superposition of pulse responses: (a) transmitted symbols, (b) received pulses (with ISI), (c) received signal.

where A is the sample of the current symbol and B, C are samples of previous symbols. Let h_s be the baud rate samples of h_p for a particular sampling phase τ. For instance, Fig. 2.4 plots h_s for two different sampling phases: $\tau = 0$ and $\tau = 15ps$. Thus h_s can be expressed as,

$$h_s(k) = h_p(kT_b + \tau) \tag{2.13}$$

Substituting Eq. (2.13) in Eq. (2.12) we get,

$$Y(lT_b + \tau) = \sum_{k=-\infty}^{\infty} U(k)h_s(l-k) \tag{2.14}$$

The infinite sum in Eq. (2.14) can be made finite by neglecting the negligible tails of $h_s(k)$ outside the range $0 \leq k \leq m$:

$$Y(l) = \sum_{k=0}^{m} U(k)h_s(l-k) \tag{2.15}$$

For a finite h_s of length $m+1$, there are L^{m+1} possible sequences of transmitted L-PAM data: $U(0), U(1), ...U(m)$. Let $\mathbf{A}$ be a $L^{m+1} \times (m+1)$ matrix whose rows are all of the possible transmitted L-PAM data patterns of length $m+1$ and $\mathbf{A}$(q,r) be the element of A in row q and column r. Hence, the channel output corresponding to the data pattern in row q of $\mathbf{A}$ is:

$$c_Y(q) = \sum_{r=1}^{m+1} \mathbf{A}(q,r)h_s(m+1-r) \tag{2.16}$$

Thus, (in the absence of noise) for a particular sampling phase there are L^{m+1} possible values of the CDR input, Y, given by Eq. (2.16), each corresponding to a row of the data matrix $\mathbf{A}$. Assuming random uncorrelated data, each sequence will occur with probability $1/L^{m+1}$. Thus the probability density function (PDF) for the signal Y (assuming no random noise) for a particular sampling phase can be expressed as,

$$f_Y(x) = \frac{1}{L^{m+1}} \sum_{q=1}^{L^{m+1}} \delta(x - c_Y(q)) \tag{2.17}$$

Note that the data matrix $\mathbf{A}$ can be generalized for line coding by weighting each term of the summation in Eq. (2.17) by the probability of the corresponding data pattern. Some PDs are inactive for certain received data patterns, in which case the corresponding terms in Eq. (2.16) must be omitted.

Table 2.1: Parameters for the system in Fig. 2.1

Signaling scheme	4-PAM with levels of -1.5 -0.5 0.5 1.5
Data rate	4 Gsymbol/s=8Gb/s
SNR	43 dB @ input to CDR
Channel	3m coaxial cable (-3dB BW=13.8 GHz)
Receiver front-end bandwidth	4 GHz

2.3.2 Additive Noise

Noise in the channel and receiver front end is modeled as a single additive noise source referred to the CDR input. If the PDF of the additive noise is $f_N(x)$, then the PDF of the signal Y including noise (Fig. 2.1) at the input to the CDR for any sampling phase can be obtained by simply convolving f_N and the noiseless PDF in Eq. (2.17)

$$f_Y(x) = \frac{1}{L^{m+1}} \sum_{q=1}^{L^{m+1}} f_N(x - c_Y(q)). \tag{2.18}$$

For the special case of Gaussian noise, with zero mean and variance σ^2,

$$f_N(x) = \frac{e^{-x^2/2\sigma^2}}{\sqrt{2\pi\sigma^2}}. \tag{2.19}$$

Substituting Eq. (2.19) in Eq. (2.18),

$$f_Y(x) = \frac{1}{L^{m+1}\sqrt{2\pi\sigma^2}} \sum_{q=1}^{L^{m+1}} e^{-(x-c_Y(q))^2/(2\sigma^2)}. \tag{2.20}$$

In essence, the PDF is a sum of Gaussian distributions. The constants $c_Y(q)$ define the means of the Gaussians in terms of the sampled pulse response h_s (deterministic jitter). Each Gaussian has a variance of σ^2 (random jitter). Note that for evaluating c_Y in Eq. (2.20), the entire pulse response from transmitter to the CDR input has to be considered.

2.3.3 System Level Parameters

System level parameters used for behavioral simulations are shown in Table 2.1. The input random data sequence is assumed to be a 4-PAM system with equiprobable values at +1.5, +0.5, -0.5 and -1.5. A 4-PAM system is chosen instead of a 2-PAM system in order to

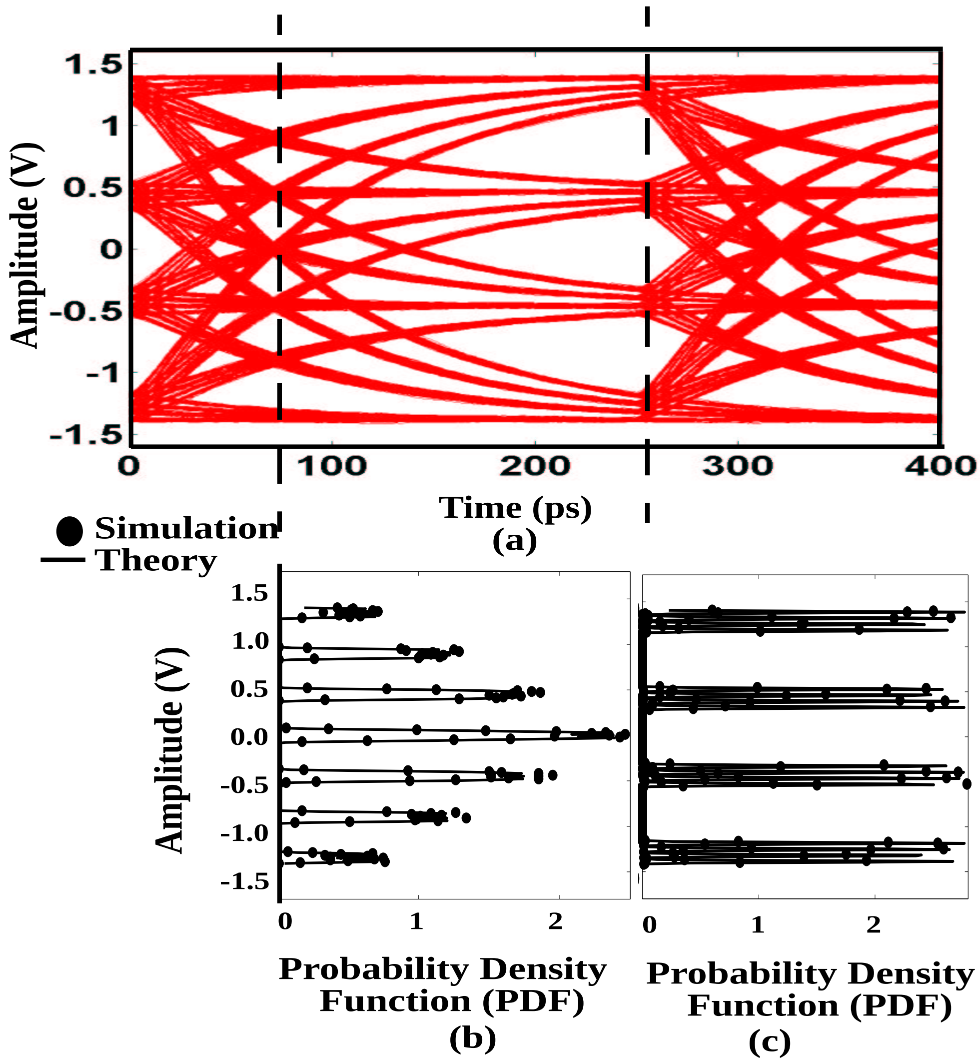


Figure 2.6: Probability density functions (PDF) at two different sampling phases of a given data eye. (a) Eye diagram. (b) PDF at data transition. (c) PDF at maximum data eye opening.

present a generic model for CDR analysis. Using Eq. (2.20) and the parameters in Table 2.1, the PDF at the input to the CDR is calculated for two different sampling phases (Fig. 2.6). Good agreement with time domain simulations in Simulink is also observed. The SNR and the channel length will be varied in subsequent sections to observe the effect of these parameters on CDR performance.

2.4 Multilevel CDR architectures

In this section an Alexander PD and a modified Sign-Sign Minimum Mean Squared Error (SSMMSE) PD-based CDR architectures for multilevel signals are modeled using the stochastic analysis in the previous section.

2.4.1 Alexander PD-based CDR

In the presence of data transitions, the Alexander PD [6] generates an early or late pulse depending on whether the clock leads or lags the data. A possible implementation of an Alexander PD modified for 4-PAM signals is shown in Fig. 2.7 [31]-[33][2]. The input data is sampled at the rising and falling edges of a full-rate clock. The input being a 4-PAM signal, the sampled values are sent to a bank of clocked comparators to detect the correct signal level. The choice of the comparator thresholds depends on the input data eye amplitude, but is normalized to +1,0 and -1 for the present discussion. The usual Alexander PD logic is authenticated by a transition detector which filters out undesired transitions such as +1.5 to -0.5 and vice versa [3]. Thus the desired transition types are those whose mid-point coincides with a threshold level [32],[33]: 1) Symmetric crossings i.e. transitions from +1.5 to -1.5 and vice versa; +0.5 to -0.5 and vice versa; 2) +1.5 to +0.5 and vice versa; 3) -1.5 to -0.5 and vice versa. The phase detector logic is enabled through a control signal whenever any one of these transitions are detected. For example, if a transition from -1.5 to +1.5 is detected then the early/late pulses can be generated through logic gates as:

$$Early = D_1 \oplus E_1 z^{-1}; Late = D_1 z^{-1} \oplus E_1 z^{-1} \tag{2.21}$$

[2]To date, 4-PAM CDRs have been implemented using an edge-sampled phase detector that relies on a bang-bang control loop[31]-[33]. One exception is [30] which uses edge samples in a linear control loop.

[3]Although [31] uses asymmetric transitions such as +1.5 to -0.5, it has been shown in [32] that asymmetric transitions lead to undesirable phase offsets.

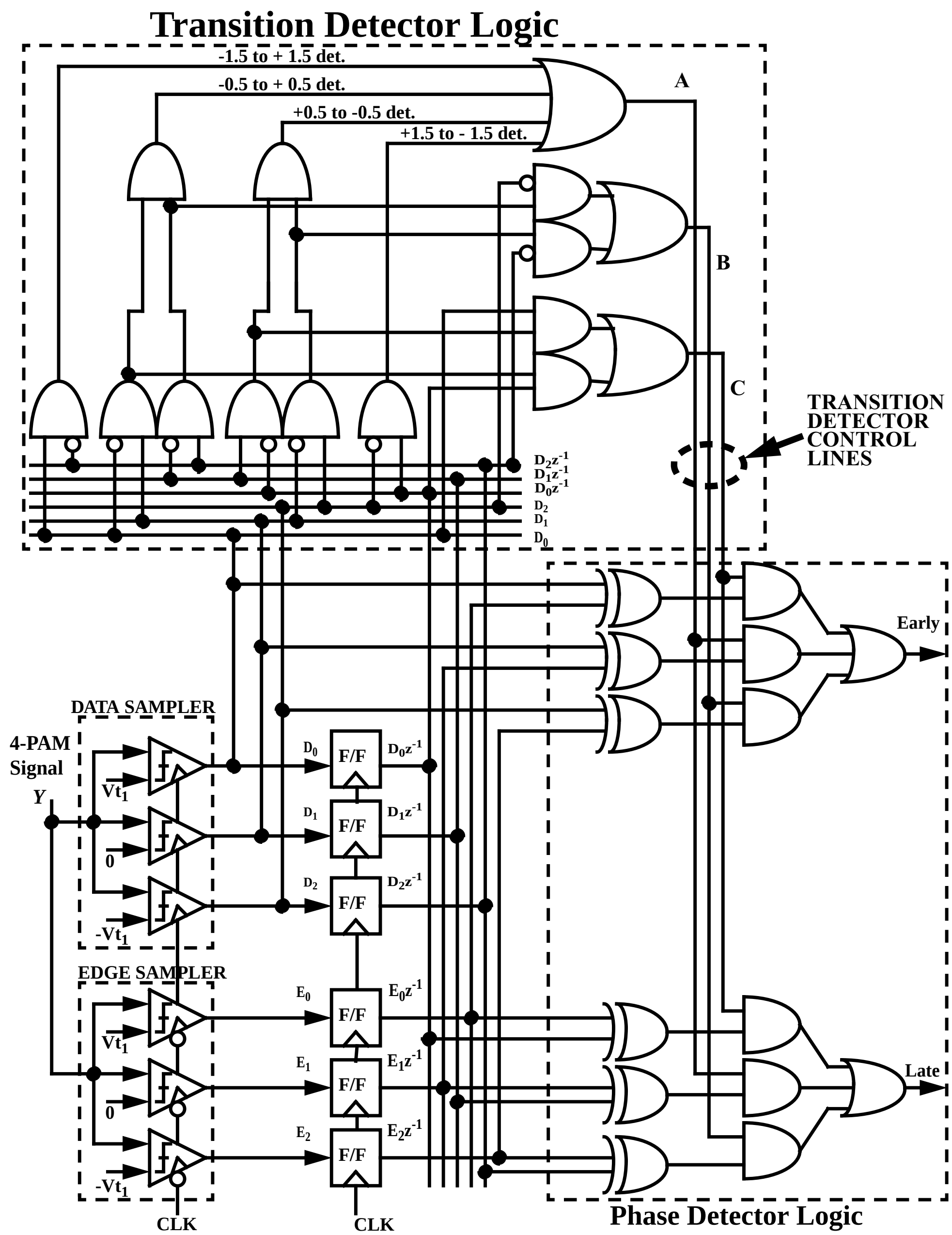


Figure 2.7: Block diagram of 4-PAM Alexander PD. Line A is enabled whenever a symmetric transition is detected; line B is enabled whenever a transition from -0.5 to -1.5 or -1.5 to -0.5 is detected and line C is enabled whenever a transition from +0.5 to +1.5 or +1.5 to +0.5 is detected.

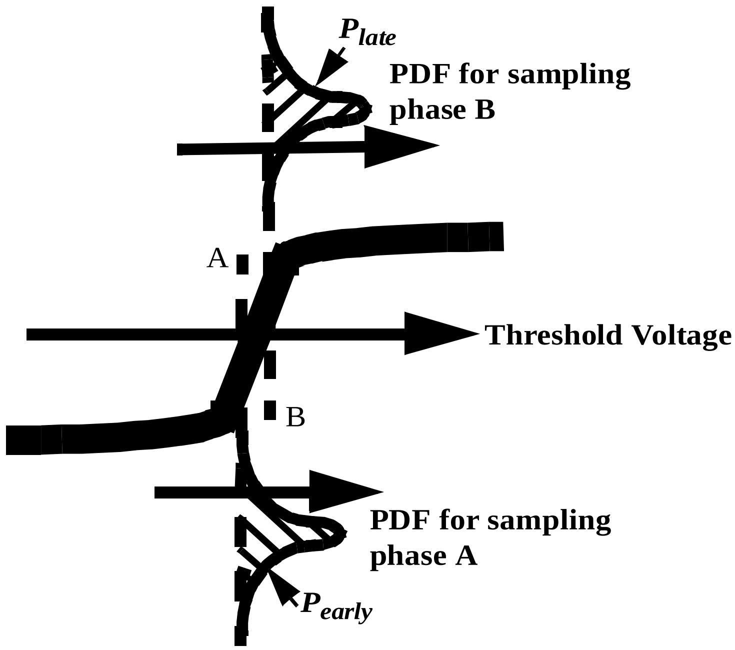


Figure 2.8: Example of calculating P_{early} and P_{late} for two different transition edge samples using PDFs.

where D_1 is the current data sample output of the zero threshold clocked comparator (Fig. 2.7), E_1 is the corresponding edge sample and D_1z^{-1} is the data sample from the previous period. To determine the P_{early} and P_{late} vs. sampling phase curves for this PD, the statistics of the received waveform at data transitions are required. Hence to model the CDR in lock, the PDF of the transition edge samples is needed.

Fig. 2.8 shows one of the data transitions of a 4-PAM signal and two PDFs corresponding to different transition edge sampling phases A and B. Sampling phase A leads the zero crossing while sampling phase B lags. For a leading sampling phase, we expect $P_{early} > P_{late}$ and vice versa for a lagging sampling phase. Note that an early pulse will be generated by the PD whenever the sampled value at the rising data transition edge is below the threshold. Thus for sampling phase A or B, the probability of an early pulse when the data transitions from -1.5 to +1.5 ($= P_{early,Y_{[-1.5\Rightarrow+1.5]}}$) can be expressed as,

$$P_{early,Y_{[-1.5\Rightarrow+1.5]}} = \int_{-\infty}^{0} f_{Y_{[-1.5\Rightarrow+1.5]}}(x)\,dx \tag{2.22}$$

where $f_{Y_{[-1.5\Rightarrow+1.5]}}(x)$ denotes the PDF corresponding to a transition from -1.5 to +1.5 in the 4-PAM signal Y. This PDF can be derived from the PDF in Eq. (2.20) by modifying the data matrix $\mathbf{A}$ to include only rows whose m-th and $(m+1)$-th columns are -1.5 and

+1.5 respectively. Consequently the modified 4-PAM data matrix will have dimensions $4^{m-1} \times (m+1)$. For example, if m=2 the modified data matrix $\mathbf{A}$ can be expressed as,

$$\mathbf{A}_{[-1.5 \Rightarrow +1.5]} = \begin{pmatrix} -1.5 & -1.5 & 1.5 \\ -0.5 & -1.5 & 1.5 \\ 0.5 & -1.5 & 1.5 \\ 1.5 & -1.5 & 1.5 \end{pmatrix} \tag{2.23}$$

Thus $f_{Y_{[-1.5 \Rightarrow +1.5]}}(x)$ can be expressed as,

$$f_{Y_{[-1.5 \Rightarrow +1.5]}}(x) = \frac{1}{4^{m-1}\sqrt{2\pi\sigma^2}} \sum_{q=1}^{4^{m-1}} e^{-\frac{(x - c_{Y_{[-1.5 \Rightarrow +1.5]}}(q))^2}{2\sigma^2}} \tag{2.24}$$

and

$$c_{Y_{[-1.5 \Rightarrow +1.5]}}(q) = \sum_{r=1}^{m+1} \mathbf{A}_{[-1.5 \Rightarrow +1.5]}(q, r) h_s(m + 1 - r) \tag{2.25}$$

Evaluating Eq. (2.22),

$$P_{early, Y_{[-1.5 \Rightarrow +1.5]}} = \frac{0.5}{4^{m-1}} \sum_{q=1}^{4^{m-1}} erfc(\frac{c_{Y_{[-1.5 \Rightarrow +1.5]}}(q)}{\sqrt{2\sigma^2}}) \tag{2.26}$$

where $erfc(x) = \frac{2}{\sqrt{\pi}} \int_x^\infty e^{-t^2} dt$ denotes the complementary error function. Similarly, the probability of a late pulse when the data transitions from -1.5 to +1.5 ($= P_{late, Y_{[-1.5 \Rightarrow +1.5]}}$) can be expressed as,

$$P_{late, Y_{[-1.5 \Rightarrow +1.5]}} = \frac{0.5}{4^{m-1}} \sum_{q=1}^{4^{m-1}} erfc(\frac{-c_{Y_{[-1.5 \Rightarrow +1.5]}}(q)}{\sqrt{2\sigma^2}}) \tag{2.27}$$

Similar equations for P_{early} and P_{late} can be derived for other data transition types. Using this method the P_{early} and P_{late} for any sampling phase can be determined for the system shown in Fig. 2.1 with an Alexander PD in the CDR. Fig. 2.9 shows plots of P_{early} and P_{late} for different sampling phases. Note that the recovered clock will lock to the sampling phase corresponding to $P_{early} = P_{late}$ if the CDR is stable. After lock is achieved, the behavior of the clock phase can be modeled as a random walk. The bang-bang nature of the CDR will cause the clock sampling phase to be updated by a fixed amount denoted by θ_{bb}. Using Eq. (2.8) the bang-bang phase update θ_{bb} can be calculated for a particular loop bandwidth once the average slope, $(=-2\frac{dP_{early}}{d\tau})$ is approximated in the vicinity of the lock point from Fig. 2.9. Once θ_{bb} is known, the rest of the loop can be designed as in [29]

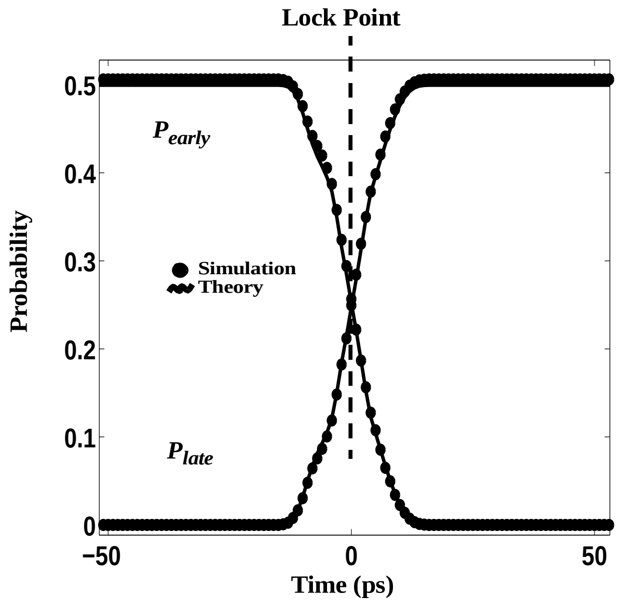


Figure 2.9: Plots of P_{early} and P_{late} values for Alexander PD for 13.8 GHz coaxial cable channel model, SNR=43 dB, 4Gsymbol/sec 4-PAM data and 4 GHz receiver front end.

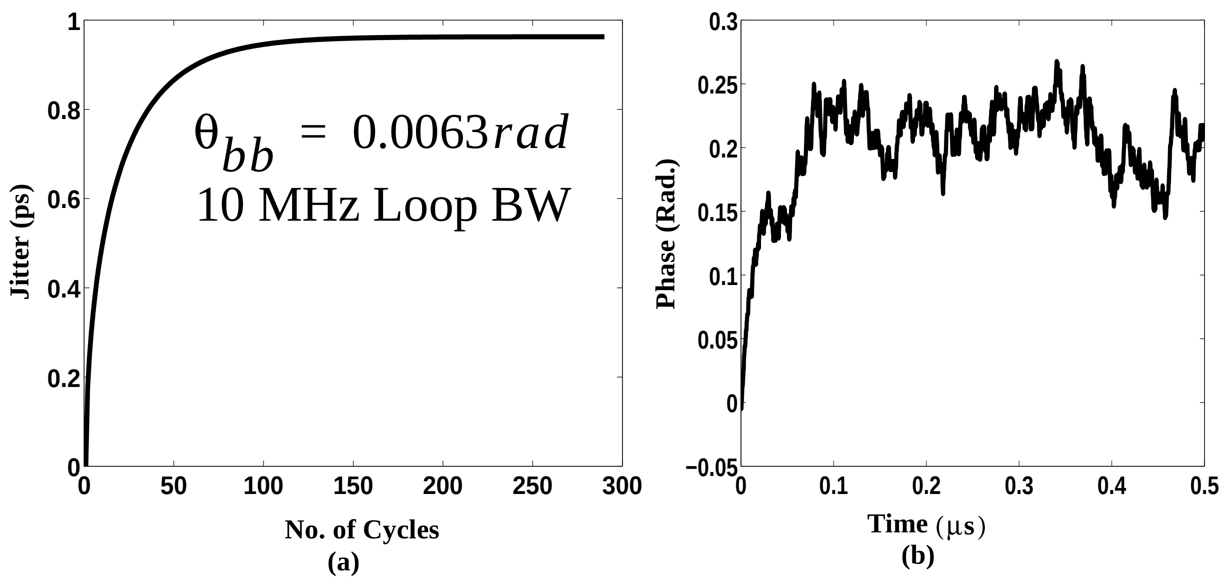


Figure 2.10: 10 MHz Alexander CDR characteristics for 13.8 GHz coaxial cable channel, SNR=43 dB and 4Gsymbol/sec 4-PAM data. (a) RMS Jitter buildup predicted by Markov model. (b) Simulated phase variation of 4-GHz clock recovered by Alexander PD-based CDR.

to provide $\zeta > 5$ for jitter peaking < 0.1 dB. Note that this also satisfies the condition of large stability factor which ensures a dominant proportional path in the bang-bang loop [26]. Thus the design methodology for the CDR is described as follows (assuming the VCO gain, K_{VCO} is known):

1) The probability curves, $P_{early}(\tau)$ and $P_{late}(\tau)$ are calculated for a particular channel, receiver front end bandwidth and input noise level.

2) The slope of these curves near the lock point can be used to calculate the charge pump current using Eq. (2.7) for a target phase detector gain, $K_{pd_{BB}}$. In this work, the target $K_{pd_{BB}}$ is set to 100 μA/rad for all CDRs.

3) The bang-bang phase update, θ_{bb} can be determined using Eq. (2.8) for a particular loop bandwidth, f_{-3dB}. In this work, the target loop bandwidth is set to 10 MHz for all CDRs. The choice of the loop bandwidth depends on the desired jitter tolerance of the CDR and also on the low frequency VCO phase noise that the CDR loop needs to filter out. A large loop bandwidth generally improves the jitter tolerance of the CDR and also filters out a significant amount of low frequency VCO noise. However, this also worsens the RMS jitter of the bang-bang CDR. In this work, the VCO was noiseless and therfore any loop bandwidth could have been used. The important point here is that for an apple-to-apple comparison of two or more CDRs, they have to be designed for the same loop bandwidth.

4) The loop resistor can be calculated using Eq. (2.4). In this work R=500 Ω.

5) The loop damping factor can be expressed as,

$$\zeta = \frac{1}{2}\sqrt{RC\omega_{-3dB}} \tag{2.28}$$

To achieve jitter peaking < 0.1dB, ζ needs to be larger than 5 [29]. Thus Eq. (2.28) places a lower limit on the loop filter capacitance. In this work, C=5nF and $\zeta = 6.26$. If it is required to maintain constant loop bandwidth for a variety of ISI and noise conditions it is necessary to ensure a wide range of charge pump currents on-chip. Variation of charge pump current to control the loop bandwidth has been reported in [44].

Once the loop is designed, the jitter in the recovered clock can be estimated using the linear model in Eq. (2.10). Alternately, a random walk model or Markov chain [16] can be utilized to predict the RMS jitter corresponding to a particular θ_{bb}. The jitter buildup in the recovered clock vs. the number of clock cycles is depicted in Fig. 2.10(a) for phase

Table 2.2: Parameters for 10 MHz Alexander PD-based CDR.

Loop bandwidth (MHz)	10
Charge Pump Current, (μA)	40
VCO gain (MHz/V)	200
θ_{bb}=Bang-bang phase update (rad.)	0.0063
Average PD slope near lock $=-2\frac{dP_{early}}{d\tau}\|_{\tau=\tau_{lock}}$ (/rad)	2.5
PD gain=$K_{pd_{BB}}$ (μA/rad)	100
R (Ω)	500
C (nF)	5
RMS jitter using linearized model i.e. Eq. (2.10) (ps)	0.9939
RMS jitter using Markov model (ps)	0.9627
RMS jitter from simulation (ps)	0.9962
Peak-to-peak jitter from simulation (ps)	6

updates corresponding to a 10 MHz loop bandwidth.

In summary, the CDR loop parameters are chosen to provide a certain loop bandwidth, phase detector gain and jitter peaking. Table 2.2 shows the parameters for a 10 MHz Alexander CDR. Peak-to-peak jitter of the CDR is simulated for a sequence of 4000 symbols. The VCO phase variation corresponding to this sequence is simulated and the maximum deviation from the mean phase is used to estimate the peak-to-peak jitter of the recovered clock. The RMS jitter was also simulated using this sequence. 4000 symbols was a large enough sequence to obtain jitter numbers that were well in agreement with that predicted by the Markov and linear jitter models. Sequence lengths larger than 4000 resulted in no significant change in the simulated RMS jitter. Simulated phase of the recovered clock is shown in Fig. 2.10(b).

In Fig. 2.10(a), the jitter buildup predicted by the Markov model is based on the probability curves of the phase detector. The Markov model shows how the RMS jitter of the recovered clock increases with the number of clock cycles and then eventually reaches a steady-state value. This is similar to the behavior of the long term jitter in a phase locked oscillator. The long term jitter (or absolute jitter) is the standard deviation of the phase of the VCO which is defined as,

$$\phi(t) = \int_0^t K_{VCO} V_c(t)\, dt \tag{2.29}$$

Fig. 2.10(b) plots $\phi(t)$. Thus the standard deviation of $\phi(t)$ once it reaches steady-state is the long term jitter of the loop and theoretically should equal the steady-state jitter predicted by the Markov model.

2.4.2 SSMMSE PD-based CDR

The following Sign-Sign (SSMMSE) rule [22] was introduced in Chapter 1:

$$\tau_{k+1} = \tau_k + \theta_{bb}\mathrm{sgn}(e_k)\mathrm{sgn}\left(\frac{\delta y(kT+\tau_k)}{\delta\tau_k}\right) \tag{2.30}$$

Here $y(t)$ is the received waveform,A_k the kth data bit, T_b the symbol period, τ_k the sampling phase for the kth data bit, and $e_k = A_k - y(kT_b + \tau_k)$. This resulted in the following logic (Chapter 1, Eq. (1.11))

$$Early = D(e \odot s); Late = D(e \oplus s) \tag{2.31}$$

The algorithm may be simplified by eliminating the error signal altogether. Suppose the PD is monitoring a +1.5 level. Thus the error signal $e = sgn[1.5 - y(t)]$ where $y(t)$ is the received signal. Note that e will be 1 most of the time since in the absence of overshoot it is highly unlikely that the signal will rise above 1.5. This can be easily seen in the 4-PAM eye diagram of Fig. 2.6(a). Setting e to 1 in Eq. (2.31) results in the following logic when the PD is monitoring a +1.5 level:

$$Early = D_0 s; Late = D_0\bar{s} \tag{2.32}$$

where D_0 is high when a +1.5 level is detected. A similar modification can be made when monitoring the -1.5 level. The only difference will be that the error signal in this case will be $e = sgn[-1.5 - y(t)]$. Therefore the error will be 0 most of the time when the PD is monitoring a -1.5 level. Setting e to 0 in Eq. (2.31) results in the following logic when the PD is monitoring a -1.5 level:

$$Early = \bar{D}_2\bar{s}; Late = \bar{D}_2 s \tag{2.33}$$

where D_2 is low when a -1.5 level is detected. Besides reduced hardware complexity, another advantage of monitoring only the maximum and minimum signal levels is lower jitter in the recovered clock [22].

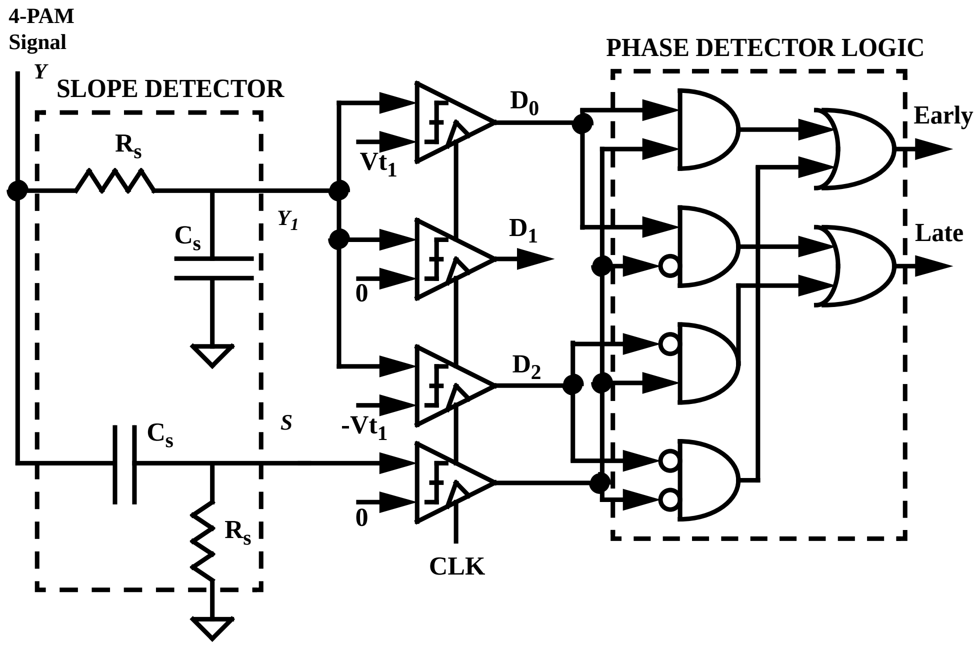


Figure 2.11: Multilevel PAM timing recovery using an SSMMSE PD with a full rate clock (+1.5 and -1.5 levels are being monitored).

The main challenge in the design of the PD is implementing a high frequency slope detector. One possibility is to use passive RC-CR sections as shown in Fig. 2.11. The relative phase shift between the data, Y_1 and slope, S will be 90° over a broad bandwidth. The low pass and high pass filters can be realized using on chip passive components. The choice of the filter time constant is a trade-off between bandwidth of the receiver front end and sensitivity of the slope detector. For this work, $(R_s C_s)^{-1} = 2\pi 10$ GRad/sec. As proposed in [40], an active filter may also be used. This will be discussed in chapter 4.

Note that in Fig. 2.11, the early/late decisions of the phase detector depend on both the signal (Y_1) and the time derivative (S) of the signal. Each of these signals will have their own c vectors (i.e. c_{Y_1} and c_S)[4] corresponding to each possible data pattern (Eq. 2.16). In order to model the combined effect of the data signal Y_1 and slope signal S, a joint PDF [34] needs to be constructed.

Note that in the absence of noise, only certain combinations of values may be observed for signals Y_1 and S at any time since these two signals evolve from the same pattern. These combinations of possible values are given by $(c_{Y_1}(q), c_S(q))$. Since there are 4^{m+1}

[4] c_{Y_1} and c_S can be computed by using Eq. (2.16) provided that the slope detector response is included in the channel model

Table 2.3: Parameters for 10 MHz SSMMSE PD-based CDR.

Loop bandwidth (MHz)	10
Charge Pump Current, (μA)	46
VCO gain (MHz/V)	200
θ_{bb}=Bang-bang phase update (rad.)	0.0072
Average PD slope near lock $=-2\frac{dP_{early}}{d\tau}\|_{\tau=\tau_{lock}}$ (/rad)	2.175
PD gain=$K_{pd_{BB}}$ (μA/rad)	100
R (Ω)	500
C (nF)	5
RMS jitter using linearized model i.e. Eq. (2.10) (ps)	1.146
RMS jitter using Markov model (ps)	1.187
RMS jitter from simulation (ps)	1.186
Peak-to-peak jitter from simulation (ps)	6.02

equiprobable data patterns for a pulse of length m+1, and each input data pattern produces voltages in the data and slope path simultaneously, hence the joint probability density function (assuming no noise) for a particular sampling phase can be expressed as,

$$f_{Y_1S}(x,z) = \frac{1}{4^{m+1}} \sum_{q=1}^{4^{m+1}} \delta(x - c_{Y_1}(q))\delta(z - c_S(q)) \tag{2.34}$$

The effect of noise can be introduced by convolving the noise distribution with the distribution in Eq. (2.34)[5]. For the special case of Gaussian noise, the joint PDF at a particular sampling phase can be expressed as,

$$f_{Y_1S}(x,z) = \frac{1}{4^{m+1}(2\pi\sigma_{Y_1}\sigma_S)} \sum_{q=1}^{4^{m+1}} e^{-\frac{1}{2}[(\frac{x-c_{Y_1}(q)}{\sigma_{Y_1}})^2+(\frac{z-c_S(q)}{\sigma_S})^2]} \tag{2.35}$$

Note that the noise variance of the slope signal (σ_S^2), is influenced by the pulse response in the slope path and hence is different from the noise variance of the data signal ($\sigma_{Y_1}^2$). A more detailed derivation is given in Appendix A. When the SSMMSE PD is monitoring +1.5 level, the probability that an early pulse will be generated for a particular sampling phase can be expressed as,

$$P_{early,[Y_1 \Rightarrow +1.5]} = \int_{V_{t_1}}^{1.5} \int_0^{\infty} f_{Y_1S}(x,z)\, dz\, dx \tag{2.36}$$

[5]refer to section 2.3.2

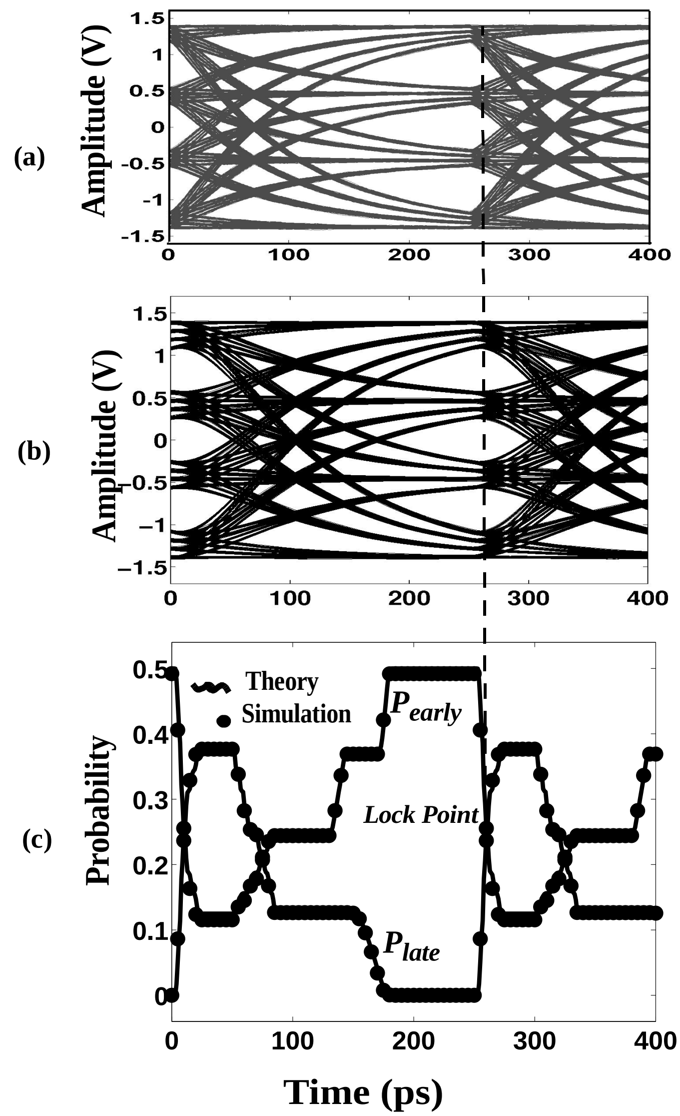


Figure 2.12: SSMMSEPD characteristics for coaxial cable channel model with 13.8 GHz -3dB bandwidth, SNR =43 dB, 4 Gsymbol/sec 4-PAM data and passive slope detector with 10 GHz cut-off frequency. (a) Eye diagram of CDR input (i.e. signal Y in Fig. 2.1). (b) Eye diagram of passive filter data output (i.e. signal Y_1 in Fig. 2.11. (c) Simulated and theoretical P_{early} and P_{late} for SSMMSEPD.

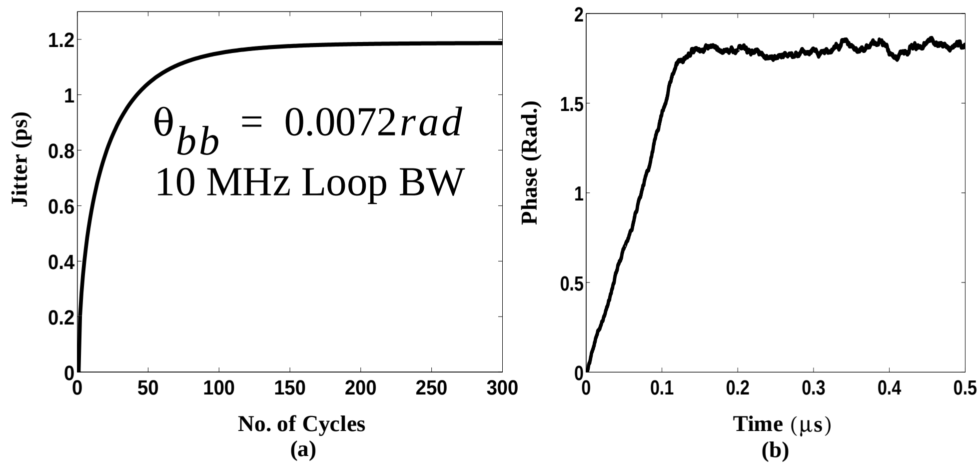


Figure 2.13: 10 MHz SSMMSE PD based CDR characteristics for coaxial cable channel model with 13.8 GHz bandwidth, SNR =43 dB, 4 Gsymbol/sec 4-PAM data and passive slope detector with 10 GHz cut-off frequency. (a) Jitter buildup predicted by Markov model. (b) Simulated excess phase variation of 4 GHz clock recovered by SSMMSE PD based CDR.

where V_{t_1}[6] represents the threshold voltage of the data comparator (Fig. 2.11). Evaluating the integrals in Eq. (2.36),

$$\begin{aligned} P_{early,[Y_1 \Rightarrow +1.5]} = K_1 \sum_{q=1}^{4^{m+1}} erfc(\frac{-c_S(q)}{\sigma_S\sqrt{2}}) erf[\frac{1.5 - c_{Y_1}(q)}{\sigma_{Y_1}\sqrt{2}}] \\ -K_1 \sum_{q=1}^{4^{m+1}} erfc(\frac{-c_S(q)}{\sigma_S\sqrt{2}}) erf[\frac{V_{t_1} - c_{Y_1}(q)}{\sigma_{Y_1}\sqrt{2}}] \end{aligned} \tag{2.37}$$

where $erf(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt$ denotes the error function and $K_1 = \frac{0.25}{4^{m+1}}$. The probability of obtaining a late pulse (when monitoring +1.5 level) can be expressed as,

$$P_{late,[Y_1 \Rightarrow +1.5]} = \int_{V_{t_1}}^{1.5} \int_{-\infty}^{0} f_{Y_1 S}(x,z)\, dz\, dx \tag{2.38}$$

Similar equations can be derived for early and late pulses when monitoring -1.5 level. Using these equations, the P_{early} and P_{late} for each sampling phase can be determined for the system shown in Fig. 2.1 with an SSMMSE PD in the CDR. Fig. 2.12 shows plots of P_{early} and P_{late} for all sampling phases along with the eye diagram of the received data. The RMS jitter can now be estimated using Eq. (2.10) or a random walk model (Markov

[6] If the maximum signal level is +1.5, the threshold, V_{t_1} will be +1.

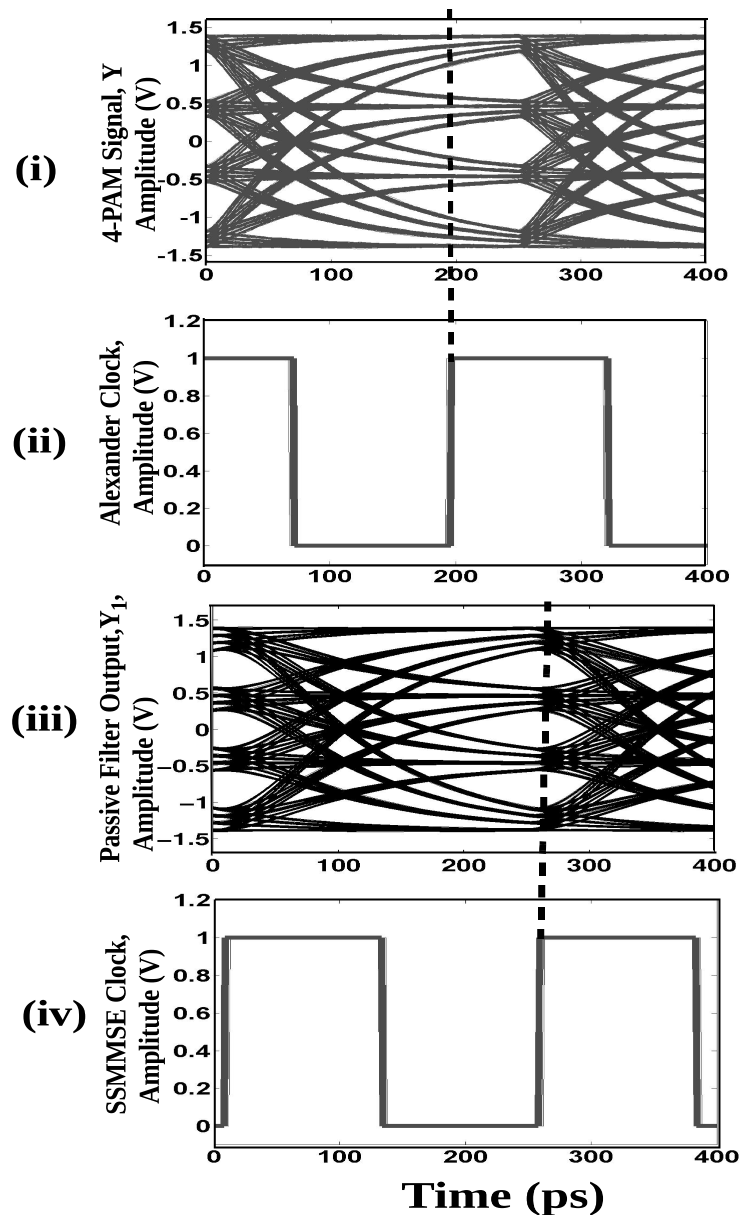


Figure 2.14: Eye diagrams. (i) 4-PAM input to CDR at 4GSymbol/sec with 13.8 GHz bandwidth channel, 4GHz receiver front-end and SNR=43dB. (ii) Alexander PD based CDR clock. (iii) Passive filter output. (iv) SSMMSE PD based CDR clock. For both CDRs, the loop bandwidth=10 MHz, R=0.5 kΩ , C=5nF, VCO gain=200 MHz/V, $K_{pd_{BB}}$=100 μA/rad. A coaxial cable channel model was used in all simulations.

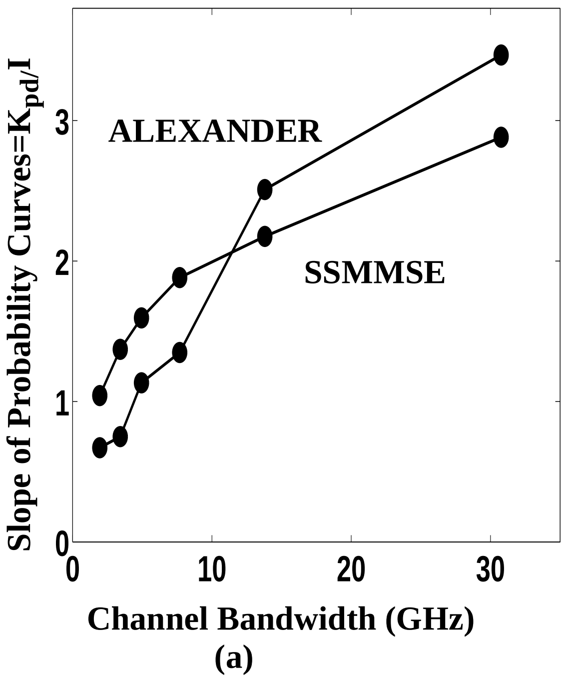
chain) for a particular loop bandwidth. Using the design methodology described for the Alexander PD-based CDR, the SSMMSE CDR is designed for 10 MHz loop bandwidth. Table 2.3 shows the parameter values of the designed CDR. Peak-to-peak jitter of the CDR is simulated for a sequence of 4000 symbols. The VCO phase variation corresponding to this sequence is simulated and the maximum deviation from the mean phase is used to estimate the peak-to-peak jitter of the recovered clock. The jitter buildup predicted by a Markov model is depicted in Fig. 2.13(a) for phase updates corresponding to a 10 MHz loop bandwidth. Simulated excess phase of the recovered clock is shown in Fig. 2.13(b). Fig. 2.14 depicts simulated eye diagrams of the data input to the CDR and the recovered clocks for Alexander PD and SSMMSE PD at 10 MHz loop bandwidth. Note that the lock point for the SSMMSE CDR corresponds to the maximum data eye opening, not the mid-point between data transitions as in the Alexander PD.

2.5 Effect of system non-idealities

In this section, the effect of different non-idealities on the CDR performance will be investigated.

2.5.1 Effect of channel bandwidth

Increasing the channel length reduces the bandwidth of the channel and leads to greater ISI. This decreases the slope of the P_{early} and P_{late} probability curves (Fig. 2.3) and if the charge pump current is increased to maintain the same loop bandwidth, results in larger RMS jitter (Eq. (2.10)). Fig. 2.15 plots the slope of the probability curves and RMS jitter of Alexander and SSMMSE PD-based CDR as a function of channel bandwidth. All Table 4.1 parameters for the 4-PAM system depicted in Fig. 2.1 were kept intact except the channel length. Both simulations and calculations predict that at large channel bandwidths, Alexander performs better than SSMMSE. However, at lower channel bandwidths, when ISI becomes large, SSMMSE is superior to Alexander PD-based CDR.



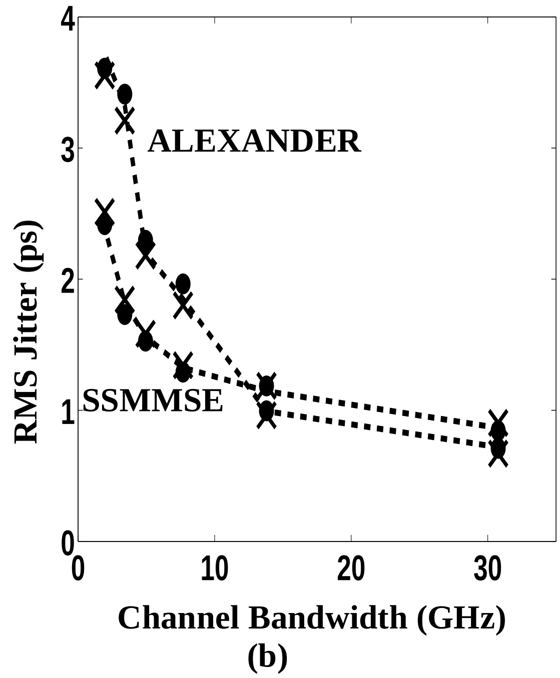


Figure 2.15: Effect of channel bandwidth on the slope of probability curves and RMS jitter of Alexander and SSMMSE PD-based CDR. For all CDRs, the loop bandwidth=10 MHz, R=0.5 kΩ , C=5nF, VCO gain=200 MHz/V, $K_{pd_{BB}}$=100 μA/rad. A coaxial cable channel model was used in all simulations. All other parameters were taken from Table 2.1. (a) Slope of probability curves vs. channel bandwidth. (b) RMS jitter vs. channel bandwidth (dashed line=linear jitter model (Eq. 2.10); cross=markov jitter model; dots = simulation).

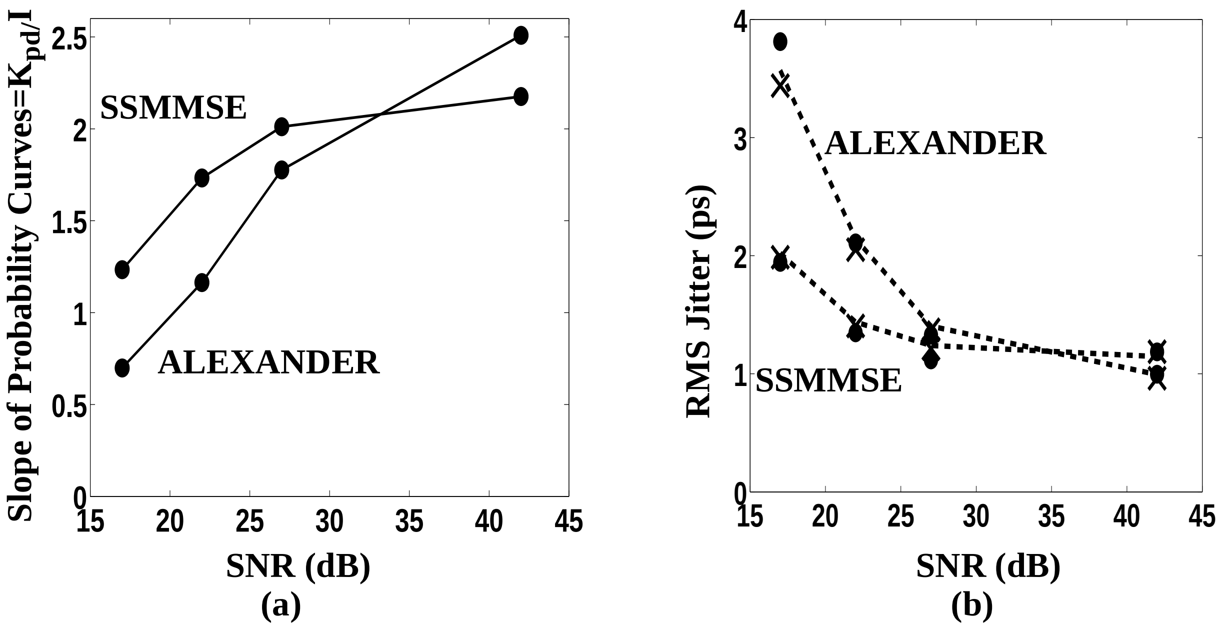


Figure 2.16: Effect of SNR on the slope of probability curves and RMS jitter of Alexander and SSMMSE PD-based CDR. For all CDRs, the loop bandwidth=10 MHz, R=0.5 kΩ , C=5nF, VCO gain=200 MHz/V, $K_{pd_{BB}}$=100 μA/rad. A coaxial cable channel model was used in all simulations. The channel bandwidth, 4-PAM data rate and receiver front end bandwidth were set to 13.8 GHz, 4 Gsymbol/sec and 4 GHz respectively. (a) Slope of probability curves vs. channel bandwidth. (b) RMS jitter vs. channel bandwidth (dashed line=linear jitter model (Eq. 2.10); cross=markov jitter model; dots = simulation).

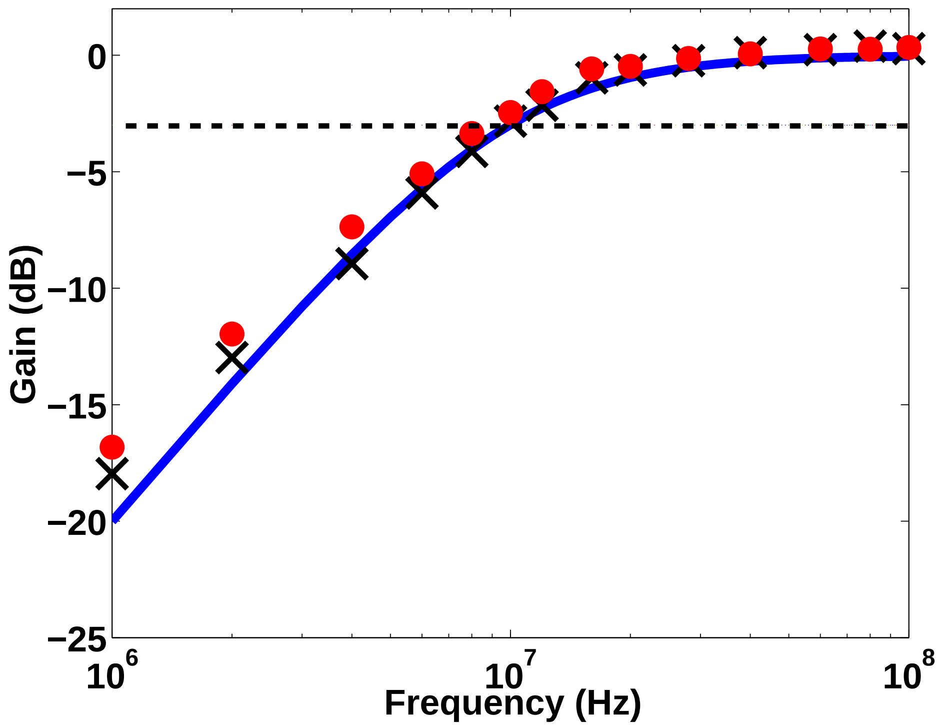


Figure 2.17: CDR transfer characteristics with 13.8 GHz coaxial cable channel, SNR=43 dB, 4 Gsymbol/sec 4-PAM data and 4 GHz receiver front end (solid line, linearized analysis; dots, simulation results for SSMMSE PD based CDR; cross, simulation results for Alexander PD-based CDR. For all CDRs, the loop bandwidth=10 MHz, R=0.5 kΩ , C=5nF, VCO gain=200 MHz/V, $K_{pd_{BB}}$=100 μA/rad.

2.5.2 Effect of SNR

As the noise power at the input to the CDR is increased, the signal-to-noise ratio (SNR) degrades, the slope of the probability curves is lowered and RMS jitter of both the Alexander and SSMMSE PD-based CDR increases. Fig. 2.16 plots the slope of the probability curves and RMS jitter of Alexander and SSMMSE PD-based CDR as a function of SNR. All Table 4.1 parameters for the 4-PAM system depicted in Fig. 2.1 were kept intact except the SNR. Both simulations and calculations predict that at large SNRs, Alexander performs better than SSMMSE. However, at lower SNRs, SSMMSE is superior to Alexander PD-based CDR.

2.5.3 Effect of VCO Jitter

To simulate the effect of VCO noise and verify the loop bandwidth, sinusoidal noise was introduced at the input to the VCO and the transfer functions from the VCO input to the output phase of the VCO were plotted along with the transfer functions for a linearized model in Fig. 2.17. Note that the peak-to-peak VCO phase change has to be kept small enough to keep the CDR within its approximately linear region of operation [27].

Thus the effect of VCO jitter is the same for either CDR since both are designed for the same loop bandwidth. Similarly noise in the loop filter and charge pump will have similar effect in either CDR. Hence, although these noise sources are not included in results of Figs 2.15 and 2.16, the comparison there is correct.

2.5.4 Effect of Transmitter Jitter

Sinusoidal jitter with varying amplitude was introduced at frequencies from 50 kHz to 100 MHz at the transmitter. At each jitter frequency, the jitter amplitude was gradually increased until bit errors occurred. Fig. 2.18 plots the jitter tolerance for the two CDRs at two different SNRs. At large SNRs (i.e. SNR=43 dB) Alexander is more jitter tolerant than SSMMSE CDR. However, at low SNRs (i.e. SNR=28 dB) the Alexander PD fails the jitter tolerance test even with no transmitter jitter. Hence, at low SNRs, the SSMMSE method has the potential to tolerate more jitter compared to the Alexander PD-based CDR for the given channel and noise conditions. This effect can be explained from the input eye diagrams shown in Fig. 2.19 for two different SNRs. At low SNRs, the data transitions are very blurred by noise, but the peak in the eye opening remains clearly discernible. Since the SSMMSE technique tracks the maximum data eye opening instead of the data transitions, it has better jitter tolerance compared to the Alexander PD based CDR at low SNRs.

2.6 Conclusion

The analysis and design of multilevel bang-bang CDRs were presented. A sampling-phase-dependent PDF is derived and utilized to model two different bang-bang CDRs: Alexander and SSMMSE. The CDRs are modeled by calculating the slope of the P_{early} and P_{late} vs. sampling phase curves in the vicinity of the lock point. The loop bandwidth of

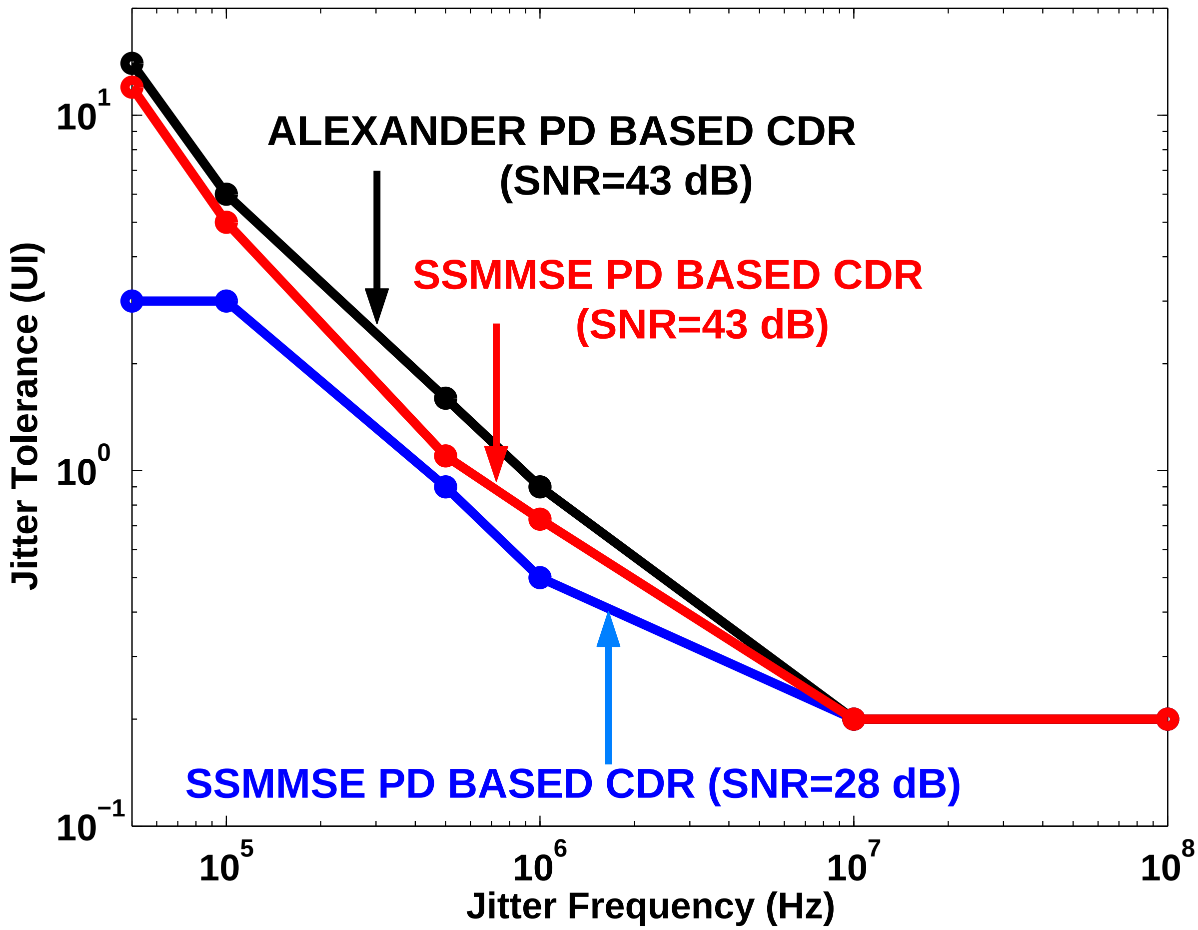
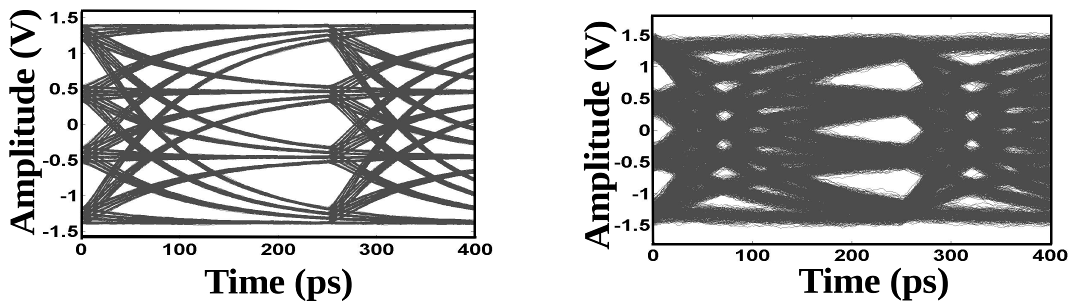


Figure 2.18: CDR jitter tolerance simulation results with 13.8 GHz bandwidth coaxial cable channel, 4 Gsymbol/sec and 4 GHz receiver front end. For all CDRs, the loop bandwidth=10 MHz, R=0.5 kΩ , C=5nF, VCO gain=200 MHz/V, $K_{pd_{BB}}$=100 μA/rad. Note that at SNR=28 dB Alexander PD based CDR fails the jitter tolerance test even without any transmitter jitter.



(a) (b)

Figure 2.19: Eye diagram of 4 Gsymbol/sec, 4-PAM data with 13.8 GHz coaxial cable channel and 4-GHz receiver front-end bandwidth. (a) SNR=43 dB (b) SNR=28 dB.

the CDR is directly proportional to the slope of the P_{early} and P_{late} curves in the vicinity of the lock point. A CDR whose PD has a lower slope in the P_{early} and P_{late} curves will require a larger charge pump current and a larger bang-bang phase step to meet a target loop bandwidth. Therefore, the slope of the P_{early} and P_{late} curves is an important performance metric for any bang-bang CDR. A steeper slope implies lower RMS jitter and higher jitter tolerance. Since the CDR input statistics effect the PD gain the choice of the best PD will in general depend on the channel ISI and noise. The analysis presented here is particularly well suited to multilevel systems where ISI and noise become important due to the degradation in voltage margin as a result of the increased number of levels.

Both analysis and behavioral simulations showed that for a coaxial cable channel and additive white Gaussian noise conditions assumed, the SSMMSE PD performed better than the Alexander PD at large ISI and low SNRs since the SSMMSE PD maintained a higher slope of the P_{early} and P_{late} curves. Qualitatively the effects of large ISI and noise is more deleterious at the data transitions than at the maximum data eye opening, thus causing the SSMMSE PD to perform better than the Alexander PD based CDR under these conditions.

A comparison of the hardware requirements of the two CDRs is given in Table 2.4. The modified SSMMSE method presented in this work is hardware efficient compared to an Alexander PD-based CDR. A particularly important feature of the modified SS-MMSE method is that it requires half the number of clock sampling phases as that of the Alexander PD. For example, to retime the data with a quarter rate clock, an Alexander

Table 2.4: Comparison of the hardware requirements of Alexander PD and SSMMSE PD.

Phase Detector	High-speed clocked comparators	Clock phases (per symbol period)	PD Logic	Other hardware
Modified SSMMSE	4	1	4 ANDs; 2 ORs.	Slope detector.
Alexander	6	2	6 XORs; 6 ANDs; 2 ORs	Transition detector. (12 ANDs, 3 ORs including one 4-input OR gate)

PD would require eight clock phases separated in phase by 45° but the SSMMSE method requires only four clock phases separated in phase by 90°. Thus the modified SSMMSE method would also require a simpler and lower power VCO.

Chapter 3

A Passive Filter Aided Timing Recovery Scheme

3.1 Introduction

This chapter focuses on the practical aspects of high-speed modified SSMMSE timing recovery. As discussed previously, modified SSMMSE algorithm simplifies the conventional SSMMSE algorithm for NRZ data such that only the slope information is required. In order to generate the slope information, a high-speed passive filter front-end is presented in this chapter. The filter provides simultaneous lowpass and highpass transfer characteristics to generate the data and its slope respectively. Slope detection is demonstrated at 10-Gb/s. As a proof of concept, the filter was used to extract a 2-GHz clock from a 2-Gb/s 2^{31}-1 random data sequence based on a modified sign-sign minimum mean squared error (SSMMSE) criterion. The circuit is fabricated in a 0.18 μm CMOS process and consumes 21.6 mW from a 1.8V supply. A half-rate modified SSMMSE PD based CDR architecture using the passive slope detector is proposed and compared with a conventional edge-sample CDR using identical circuit blocks. Simulations predict improved jitter performance for the proposed technique and similar power consumptions for the two techniques.

3.2 Background

Based on the analyses in chapters 1 and 2, the SSMMSE TR equation can be simplified to exclude the error signal e_k [40]:

$$\tau_{k+1} = \tau_k + 2\mu \text{sgn}(y(kT + \tau_k)\text{sgn}\left(\frac{\delta y(kT + \tau_k)}{\delta \tau_k}\right) \tag{3.1}$$

Note that implementation of this equation requires two latches for timing recovery; one latch for the data path and the other for the slope path. The number of latches can be reduced by directly multiplying the data signal $y(t)$ with its corresponding slope signal, $dy(t)/dt$ and then retiming the output with a single latch:

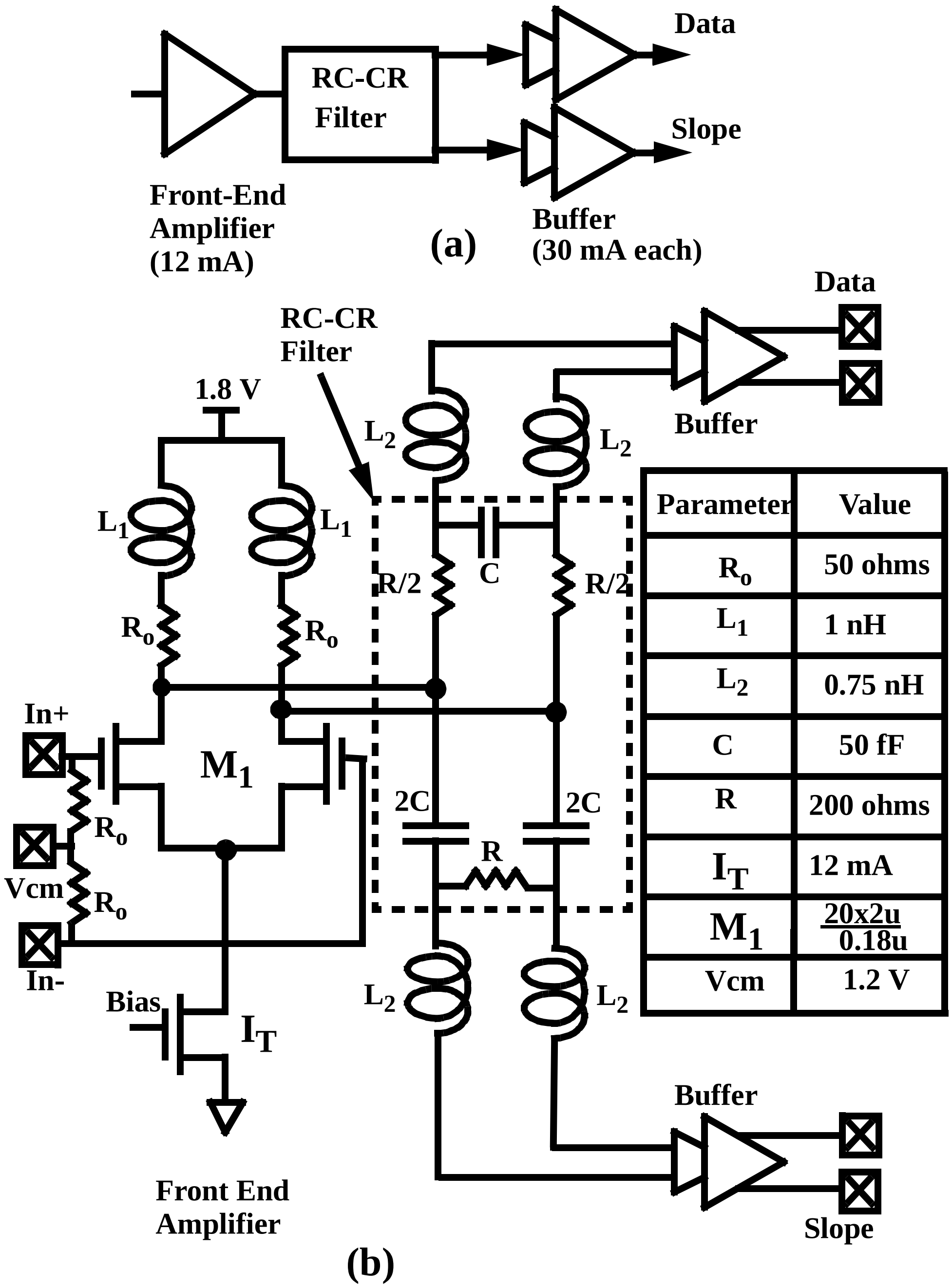
$$\tau_{k+1} = \tau_k + 2\mu \text{sgn}\left(y(kT + \tau_k)\frac{\delta y(kT + \tau_k)}{\delta \tau_k}\right) \tag{3.2}$$

Note that the timing function in Eq. (3.2) requires a continuous-time slope detector. This chapter deals with the implementation of the passive filter based continuous-time slope detector introduced in chapter 2.

3.3 Design and Implementation of Passive Filter

3.3.1 Topology

Fig. 3.1 shows the complete schematic of the passive filter. It consists of a front-end amplifier, an RC-CR section and two sets of output buffers. The lowpass RC section is called the “data path” and the high pass CR section is the “slope path”. To ensure a 90 degree relative phase shift between the data and slope paths, identical elements were used in both paths. The cut-off frequency of the passive filter is a critical parameter in the design. Decreasing the RC time constant ensures wide bandwidth in the data path, but reduces the gain in the slope path proportionately. The effect of variation in RC time constant on the loop performance can be evaluated using the simulation set-up shown in Fig 3.2. Table 3.1 summarizes the loop performance corresponding to three different RC time constants of the passive filter with a 6-GHz bandwidth front-end amplifier and 10-Gb/s input random data sequence. Note that at RC=8ps, the loop suffers from larger jitter due to a wide-open eye resulting in the “zero-slope condition”.As the RC time constant is increased from 8ps to 10ps, the slope of the probability curves increases,



Parameter	Value
R_o	50 ohms
L_1	1 nH
L_2	0.75 nH
C	50 fF
R	200 ohms
I_T	12 mA
M_1	$\frac{20x2u}{0.18u}$
Vcm	1.2 V

Figure 3.1: Passive Filter. (a) Block diagram. (b) Schematic.

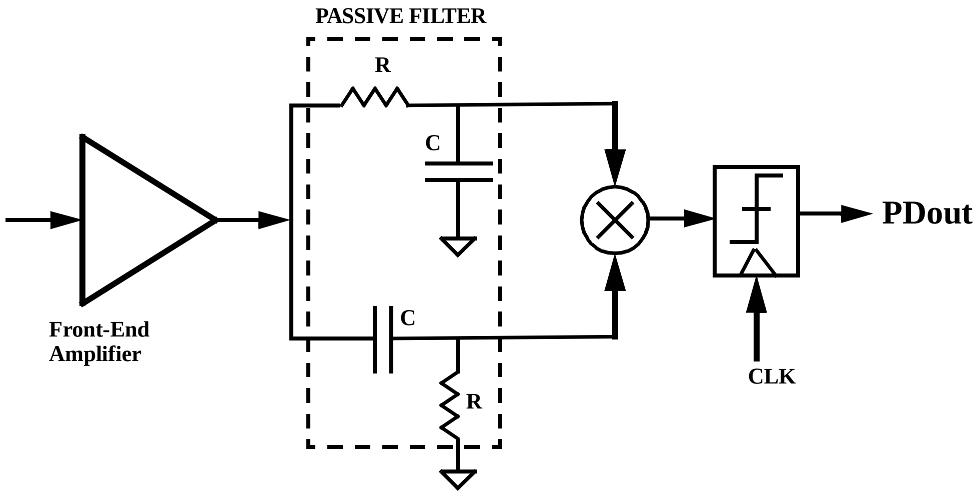


Figure 3.2: Simulation test set-up for evaluating the variation of RC time constant on the loop performance (the front-end amplifier was modeled as a first order filter with 6-GHz bandwidth).

resulting in lower jitter and larger gain in the slope path. However, the loop performance is somewhat diminished as the RC time constant is increased from 10ps to 12 ps. This is mainly due to the increase in ISI in the data path. To summarize, the RC time constant of the passive filter needs to be set to 10ps for 10-Gb/s operation. C was set to 50fF and R was set to 200 ohms.

Table 3.1 also shows the effect of RC time constant on the relative gain of the data and slope paths at a particular frequency. As the RC time constant is decreased, the gain in the slope path diminshes with respect to the gain in the data path. As a result, lower RC time constants reduce the swing of the slope signal output of the passive filter and this may degrade the gain of the phase detector.

At any two frequencies ω_1 and ω_2 the relative gains in the data an slope paths are given by : $A_1\omega_1 = A_2\omega_2$ where A_1 and A_2 are the relative gains at ω_1 and ω_2 respectively. Thus given the the relative gain at 8-GHz, the relative gain at another frequency can be computed.

From the half circuit of the RC-CR filter section shown in Fig. 3.1 (b), each path has an impedance equal to $\frac{R}{2} + \frac{1}{2j\omega C}$. Since the data path and slope paths are in parallel, the input impedance of the RC-CR section can be expressed as:

$$Z_{in} = \frac{R}{4} + \frac{1}{4j\omega C} \tag{3.3}$$

Table 3.1: Effect of passive filter RC time constant on loop performance (a 6-GHz bandwidth front-end amplifier and 10-Gb/s input random data sequence is assumed.

	RC=8 ps	RC=10 ps	RC=12 ps
Slope of Probability Curves (/Rad)	0.889	1.587	1.33
RMS Jitter in ps (using Eq. (2.8) with $f_{clk} = 10GHz; f_{3dB_{BB}} = 10MHz$)	0.709	0.397	0.473
Relative gains between data and slope path $= \frac{v_d}{v_s}(j\omega) = \frac{1}{j\omega RC}$ at 8-GHz	2.5	1.98	1.66

Hence, at low frequencies, Z_{in} is not matched to the 50 Ω system impedance. Therefore, in order to provide a broadband input match, a 50 Ω passive termination and a front-end amplifier were needed as shown in Fig. 3.1. Inductors L_1 and L_2 were used to improve the amplifier's bandwidth[1]. For a 600mV swing and 50 ohm output impedance, the tail current was chosen to be 12mA. The width of the diff pair transistors was set to 40μm in order to bias them at half peak f_T [45].

Output buffers were provided in both the data and slope paths, each comprised of two inductively peaked differential pairs (Fig. 3.3). The total current consumption was 72mA from a 1.8V power supply. Of this total, 12mA was consumed in the front-end amplifier and 30mA in each of the output buffers. Excluding the output buffers, the power consumption was 21.6 mW.

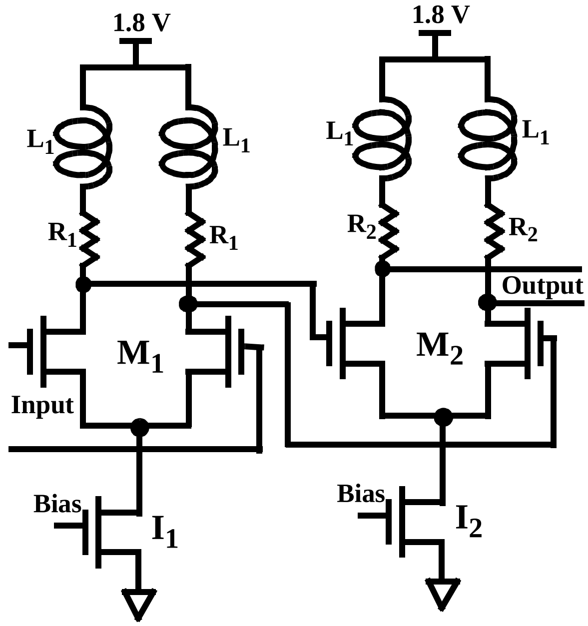
3.3.2 Modeling and Analysis

Fig. 3.4 (a) shows the small signal circuit of the passive filter. C_p denotes the parasitic capacitance at the input to the buffer. To simplify the analysis, the RCL-CRL sections are replaced by their equivalent Δ network by using a Y-Δ transformation (Fig. 3.4 (b)). The impedances in the Δ network can be expressed as,

$$Z_{1LPF}(j\omega) = Z_{3HPF}(j\omega) = j\omega(L_2 - \frac{1}{2\omega^2 C}) + \frac{L_2}{RC} = \frac{1}{Y_{1LPF}} \tag{3.4}$$

$$Z_{2LPF}(j\omega) = Z_{2HPF}(j\omega) = \frac{j\omega \frac{R}{2}(L_2 - \frac{1}{2\omega^2 C}) + \frac{L_2}{2C}}{j\omega L_2} = \frac{1}{Y_{2LPF}} \tag{3.5}$$

[1] ASITIC models for inductors are provided in Appendix B.



Parameter	Value
R_1	100 ohms
R_2	50 ohms
L_1	1 nH
I_1	10 mA
I_2	20 mA
M_1	$\frac{20x2u}{0.18u}$
M_2	$\frac{40x2u}{0.18u}$

Figure 3.3: Schematic of two-stage buffer.

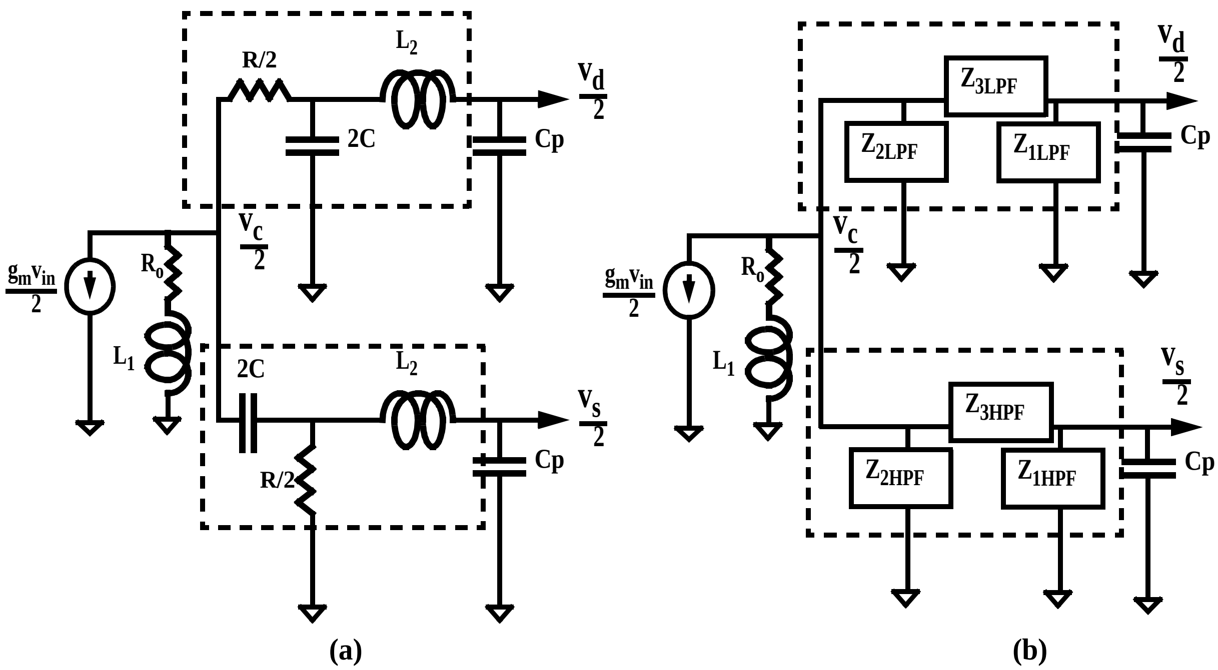


Figure 3.4: Small signal model of passive filter. (a) Small signal half-circuit. (b) Small signal half-circuit with RCL-CRL sections replaced by equivalent Δ sections.

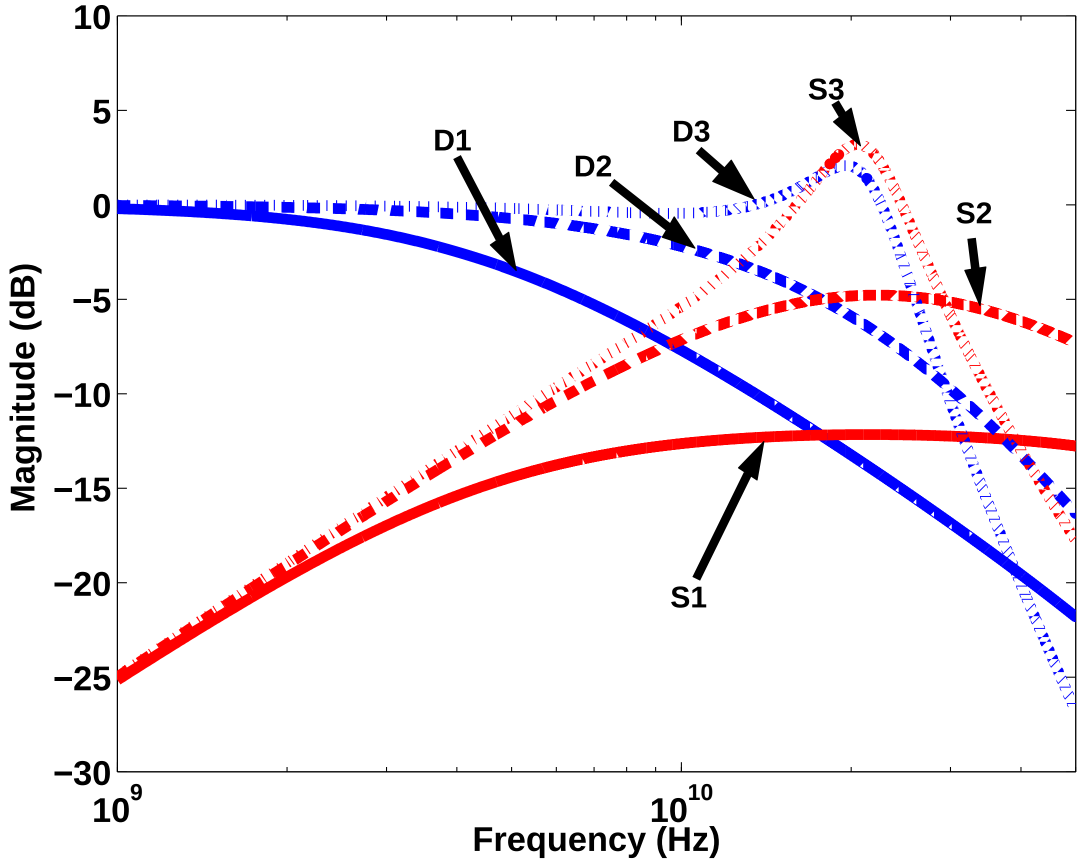


Figure 3.5: Data and slope path frequency responses. D1 and S1 respectively denote the data and slope path transfer functions without inductors L_1, L_2; D2 and S2 respectively denote the data and slope path transfer functions with inductor L_1 only and D3 and S3 respectively denote the data and slope path transfer functions without both inductors L_1, L_2. For these simulations, $g_m = 20mA/V, C_p = 110fF$ and all other parameters were taken from the table in Fig. 3.1.

$$Z_{3LPF}(j\omega) = Z_{1HPF}(j\omega) = -\omega^2 RC(L_2 - \frac{1}{2\omega^2 C}) + j\omega L_2 = \frac{1}{Y_{3LPF}} \tag{3.6}$$

The gain in the data path can be expressed as:

$$\frac{v_d}{v_{in}}(j\omega) = \frac{A_1(j\omega)Z_{1LPF}}{Z_{1LPF} + Z_{3LPF} + j\omega C_p Z_{1LPF} Z_{3LPF}} = A_1(j\omega)K_L(j\omega) \tag{3.7}$$

The gain in the slope path can be expressed as:

$$\frac{v_s}{v_{in}}(s) = \frac{A_1(j\omega)Z_{3LPF}}{Z_{1LPF} + Z_{3LPF} + j\omega C_p Z_{1LPF} Z_{3LPF}} = A_1(j\omega)K_H(j\omega) \tag{3.8}$$

where $A_1(j\omega)$ is the gain from $v_c/2$ to $v_{in}/2$ and can be expressed as:

$$A_1(j\omega) = \frac{-g_m}{Y_o + 2Y_{2LPF} + (1 - K_L(j\omega))Y_{3LPF} + (1 - K_H(j\omega))Y_{1LPF}} \tag{3.9}$$

Thus the ratio of the gains in the data and slope paths can be expressed as:

$$\frac{v_d}{v_s}(s) = \frac{Z_{1LPF}}{Z_{3LPF}} = \frac{1}{j\omega RC} \tag{3.10}$$

Eq. (3.10) shows that inductors L_1 and L_2 do not hamper the slope detection action of the passive filter. Fig. 3.5 plots the transfer functions in the data and slope paths with and without inductors L_1 and L_2. The plots reveal that inductors L_1 and L_2 improve the bandwidth and gain in both paths.

Note that since L_1 and L_2 are peaking inductors hence their Q is not important. Hence, lower-Q stacked inductors can be used to save area.

3.3.3 Measurement Results

The passive filter was fabricated in a 0.18-μm CMOS technology and occupied an area of 1.1 mm^2. The die photo is shown in Fig. 3.6. A network analyzer was used to measure the frequency response (Fig. 3.7) of the filter on wafer. The measured -3dB bandwidth in the data path was 6 GHz. In the slope path, the magnitude of S_{21} increased at a rate of 20dB/dec. The relative phase shift between the data and slope paths is plotted in Fig. 3.8(a). The phase shift is near 90 degrees over a broad bandwidth. The input impedance of the filter is shown in Fig. 3.8(b). A Centellax PRBS board was connected to the passive filter to test its functionality. Eye diagrams of data and slope outputs captured by an Agilent 86100B scope for a 10-Gb/s 2^{31}-1 PRBS sequence are shown in Fig. 3.9. Note that the slope output exhibits peaks aligned with transitions in the data waveform. At

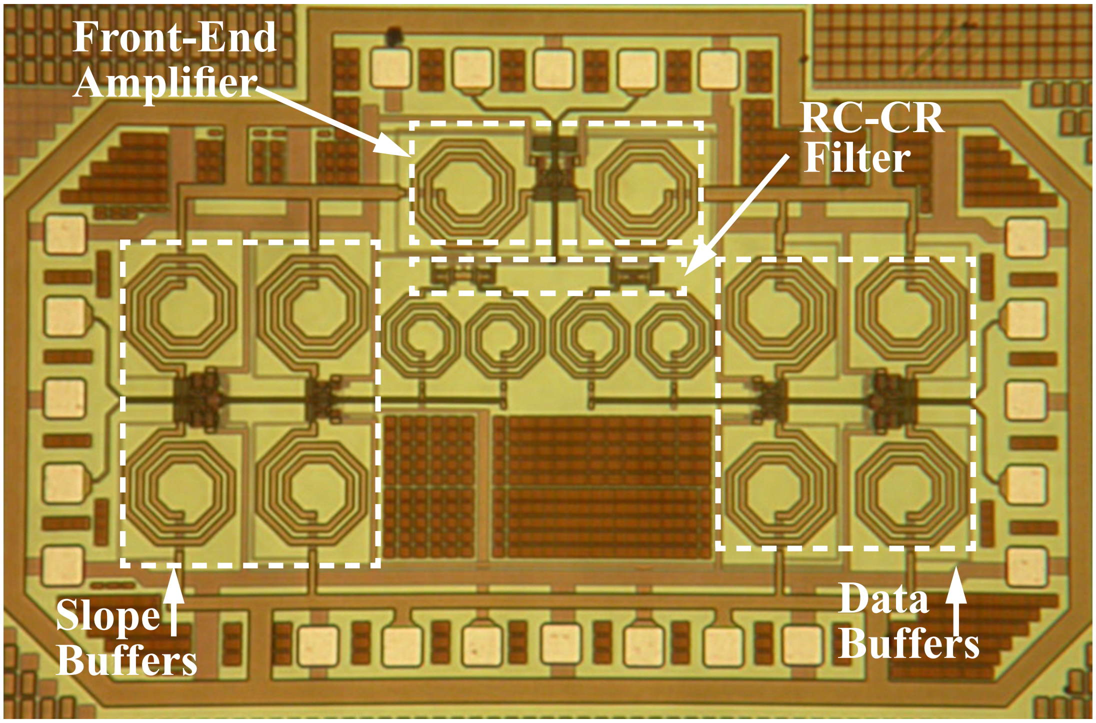


Figure 3.6: Die Photo of Passive Filter

high speeds, capturing the data and slope signal that are precisely aligned is challenging due to the mismatches in cables. To offset this issue, the data signal was captured first and then the same cable was connected to the slope path to capture the slope. The scope time delay settings were kept fixed during this measurement as shown in the time delay slots of the eye diagrams in Fig. 3.9.

3.4 Design and implementation of external timing recovery loop

The passive filter was combined with external components to demonstrate the proposed TR scheme as shown in (Fig. 3.10). The mixer, latch, VCO and loop filter were implemented on a separate board using commercial components. The mixer takes the product of the slope and data signals, as required by Eq. (3.2), and the latch performs the *sgn* operation. Table 3.2 summarizes the main features of the building blocks in the external TR loop. Since the output stage of the latch is open collector, a pull-up resistor R_c is needed at the output of the latch. The latch being differential and the VCO being single

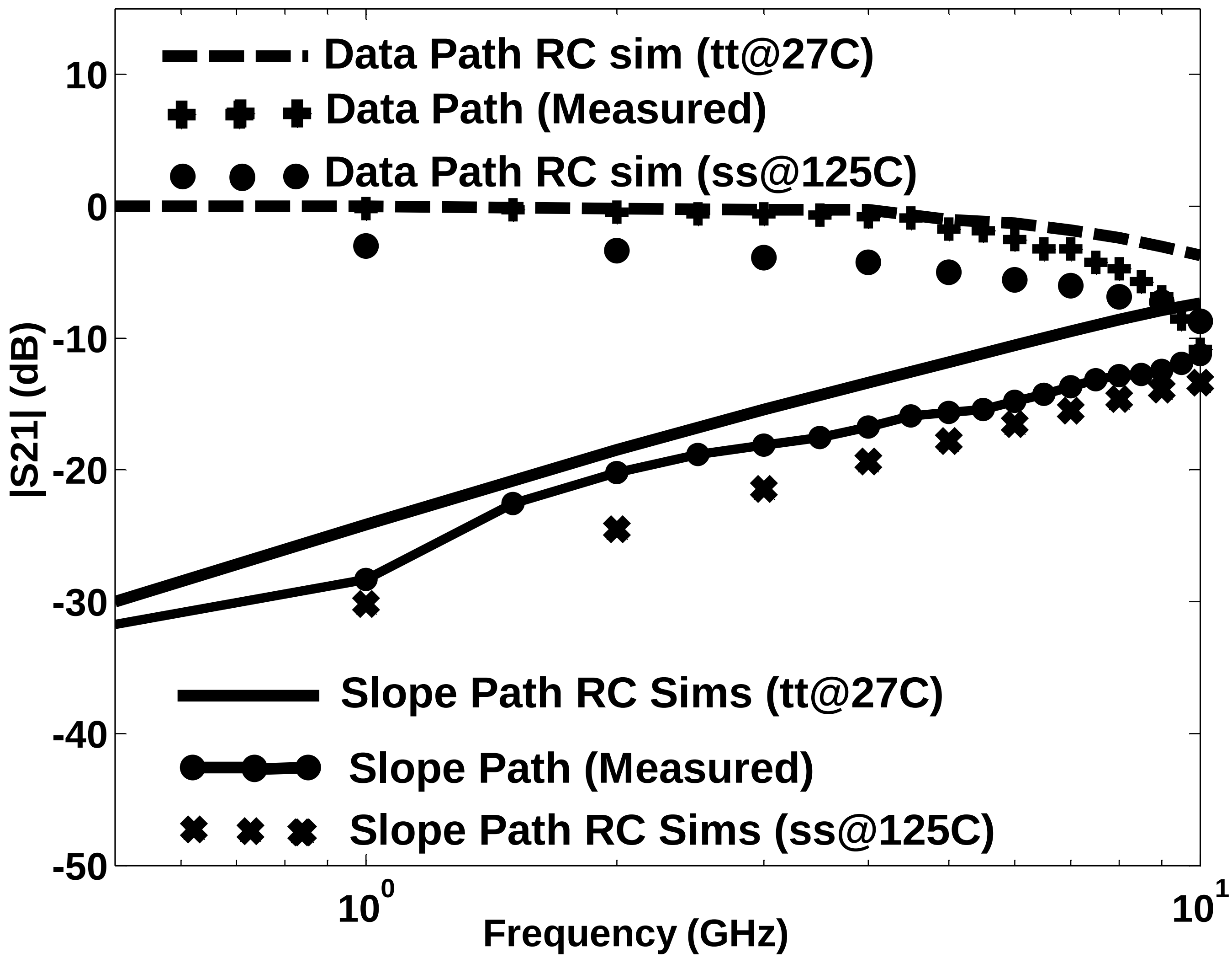
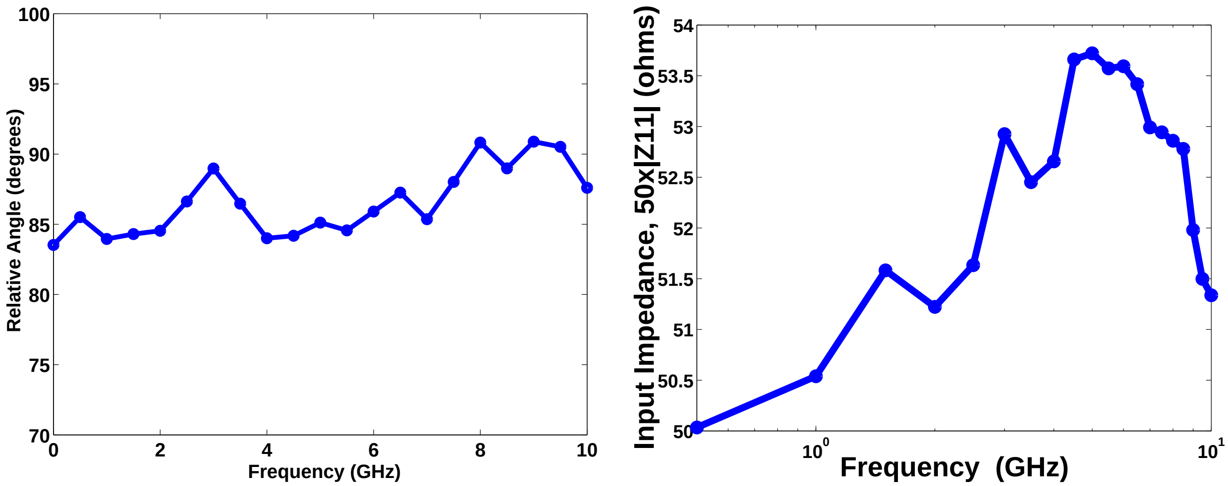


Figure 3.7: Measured and simulated S21 in the data and slope paths.



(a) (b)

Figure 3.8: Network analyzer measurements. (a) Relative angle between the data and slope paths.(b) Input impedance of the passive filter.

ended, only one side of the latch output was used. A coupling capacitor C_c was used to isolate the latch common mode voltage from the VCO control voltage. A coarse control voltage was applied through a resistor R_{coarse} to make the VCO oscillate near the desired center frequency. R_{coarse} is chosen large enough (=1kΩ) so that it produces no effect on the loop dynamics. Now the average latch output can be expressed as,

$$V_{Latch} = -V_{bb}P_{early}(\tau) + V_{bb}P_{late(\tau)} \tag{3.11}$$

where V_{bb} is the peak voltage per side of the latch(=200mV). Consequently the gain may be expressed as,

$$K_{pd_{BB}} = \frac{dV_{Latch}}{d(\tau)} = -2V_{bb}\frac{dP_{early}(\tau)}{d\tau} \tag{3.12}$$

Once $K_{pd_{BB}}$ is evaluated, loop equations can be derived using the linearized model in Fig. 3.11. Assuming K_{vco} is the VCO gain, the control voltage can be expressed as (Fig. 3.11),

$$v_{cont}(s) = \frac{1 + s\tau_1}{1 + s(\tau_1 + \tau_2)}(\theta_{in} - \theta_{out})K_{pd_{BB}} \tag{3.13}$$

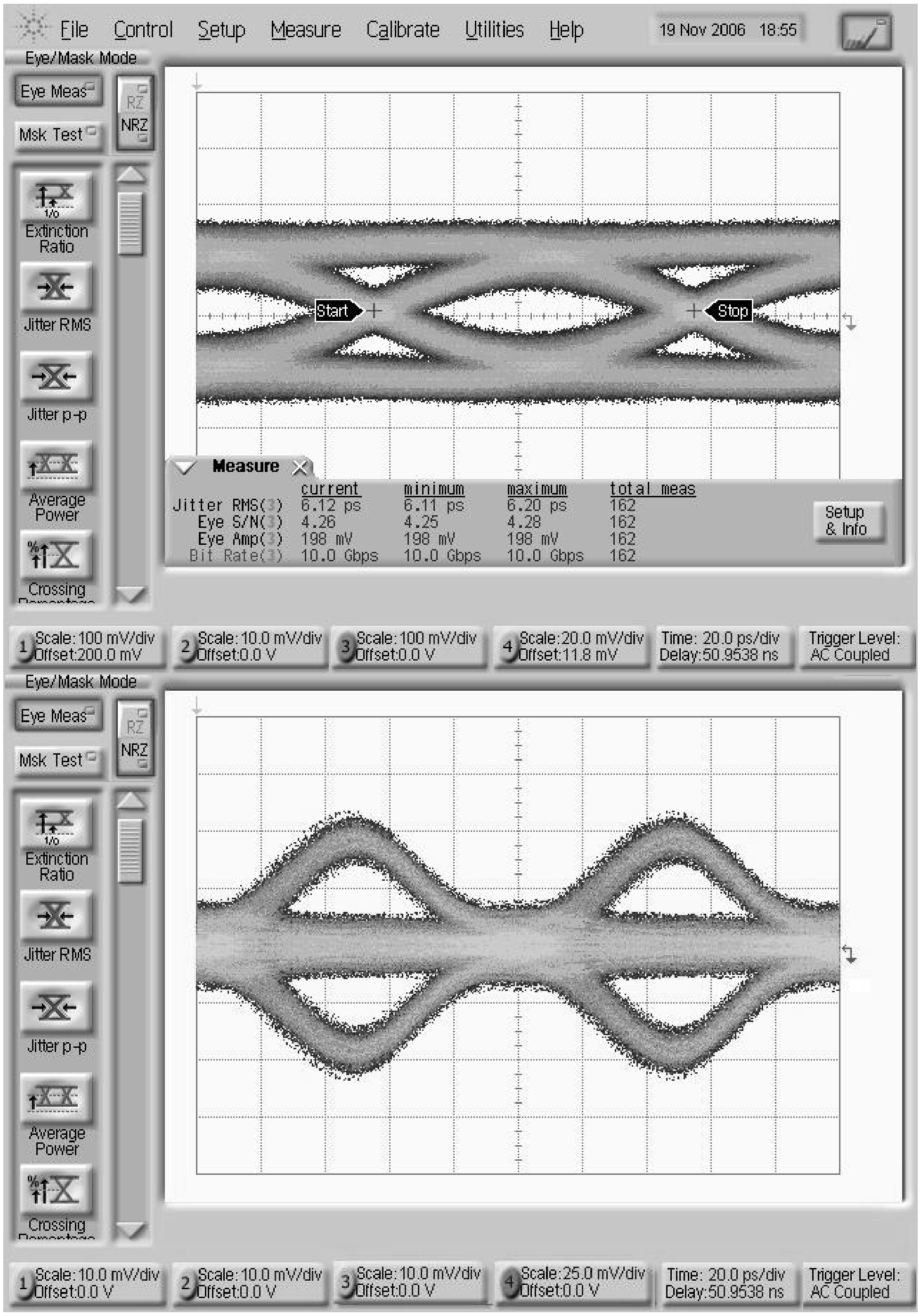


Figure 3.9: Data (top eye) and slope (bottom eye) outputs of passive filter at 10-Gb/s (Vertical scale (top eye)=100mV/div; Vertical scale (bottom eye)=25mV/div ; Horizontal scale=20ps/div).

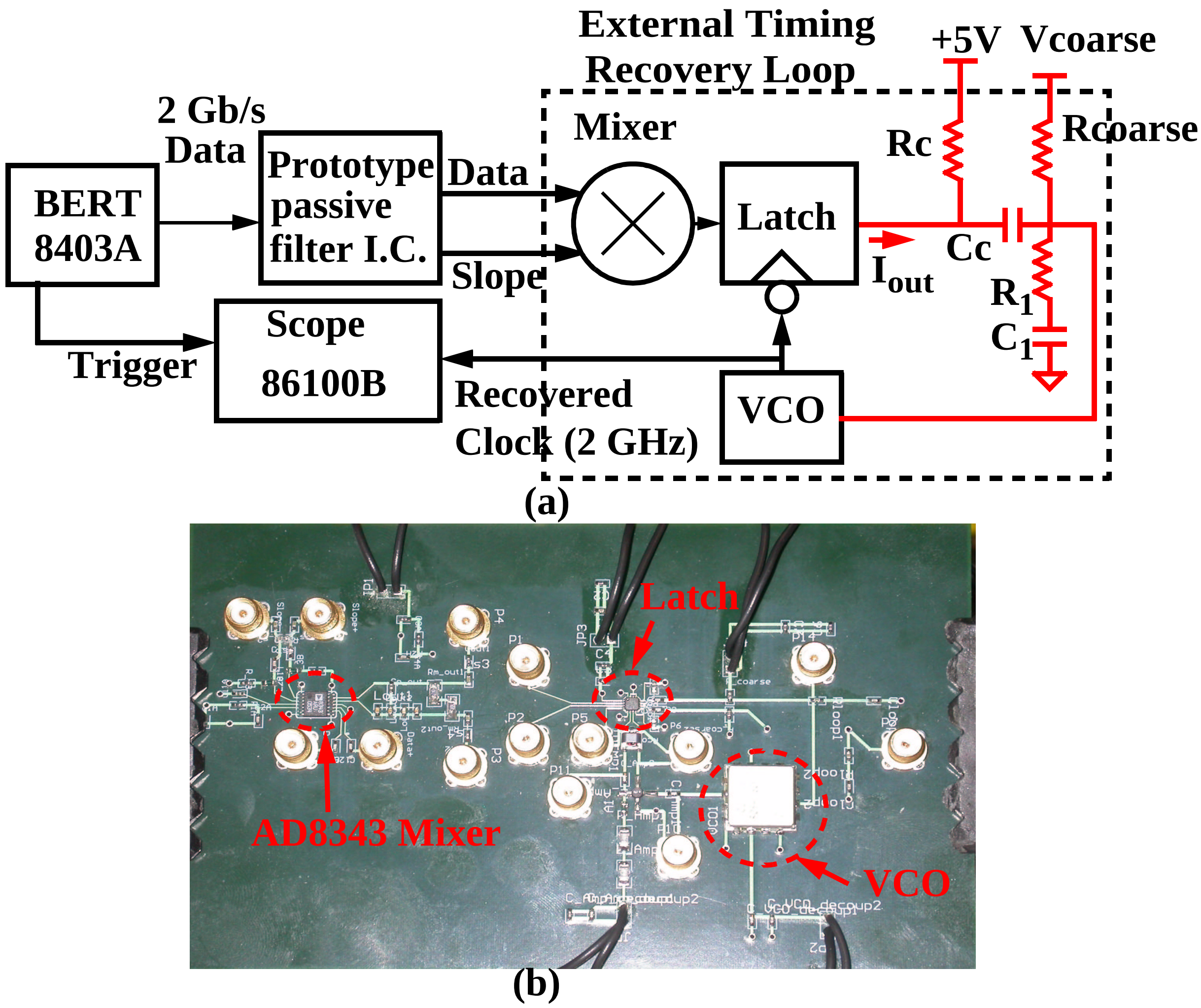


Figure 3.10: Passive filter aided external TR loop. (a) Test set up. (b) Photo of external TR loop.

Table 3.2: Description of components in external CDR loop

Block	Model	Features
Mixer	AD8343 Analog Devices	2.5-GHz bandwidth on RF, LO and IF ports. Noise Figure=14 dB
Latch	ADCMP572 Analog Devices	Ultrafast SiGe Latch
VCO	ROS-2150VW Mini-Circuits	Tuning Range=970-2150 MHz VCO Gain 70 MHz/V

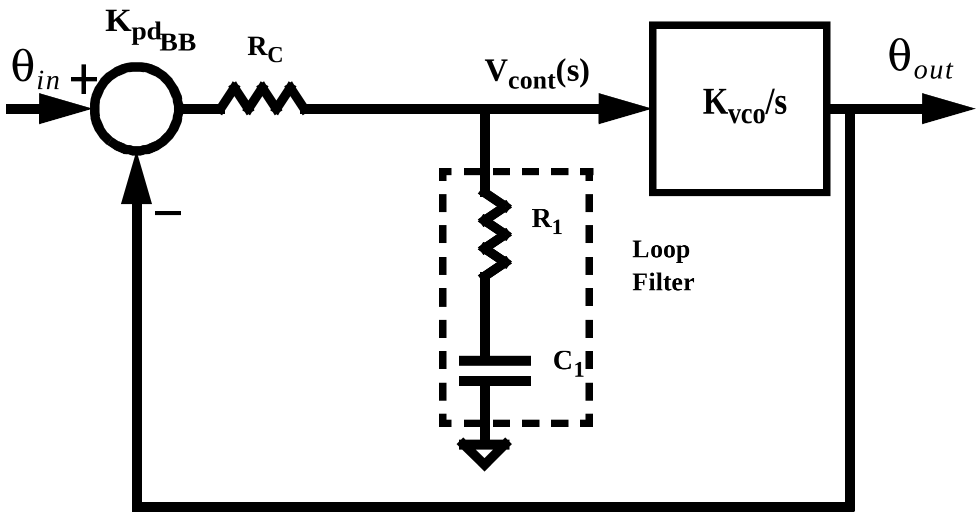


Figure 3.11: Linearized model of external TR loop.

where $\tau_1 = R_1C_1$ and $\tau_2 = R_cC_1$. The transfer function of the entire loop can be expressed as,

$$\frac{\theta_{out}}{\theta_{in}}(s) = \frac{\frac{K_{vco}K_{pd_{BB}}}{\tau_1+\tau_2} + s\tau_1\frac{K_{vco}K_{pd_{BB}}}{\tau_1+\tau_2}}{s^2 + s\frac{K_{vco}K_{pd_{BB}}\tau_1+1}{\tau_1+\tau_2} + \frac{K_{vco}K_{pd_{BB}}}{\tau_1+\tau_2}} \tag{3.14}$$

Since $K_{vco}K_{pd_{BB}}\tau_1 \gg 1$, the transfer function can be expressed as,

$$\frac{\theta_{out}}{\theta_{in}}(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.15}$$

where $\omega_n = \sqrt{K_{vco}K_{pd_{BB}}/(\tau_1 + \tau_2)}$ and $\zeta = 0.5\tau_1\omega_n$. As discussed in chapter 2, the loop bandwidth (for large damping factor ζ) can be approximated as:

$$\omega_{-3dB} \approx 2\zeta\omega_n \tag{3.16}$$

Substituting $\omega_n = 2\zeta/\tau_1$ in Eq. (3.16):

$$\tau_1 = 4\zeta^2/\omega_{-3dB} \tag{3.17}$$

Thus the design procedure for a target loop bandwidth (assuming K_{vco} and $K_{pd_{BB}}$ are known) can be outlined as follows:

(1) τ_1 can be computed using Eq. (3.17) for a target bandwidth and damping factor.

(2) ω_n can be computed using Eq. (3.16) for a target bandwidth and damping factor.

(3) Since $\omega_n = \sqrt{K_{vco}K_{pd_{BB}}/(\tau_1 + \tau_2)}$, τ_2 can be computed as:

$$\tau_2 = -\tau_1 + K_{vco}K_{pd_{BB}}/\omega_n^2 \tag{3.18}$$

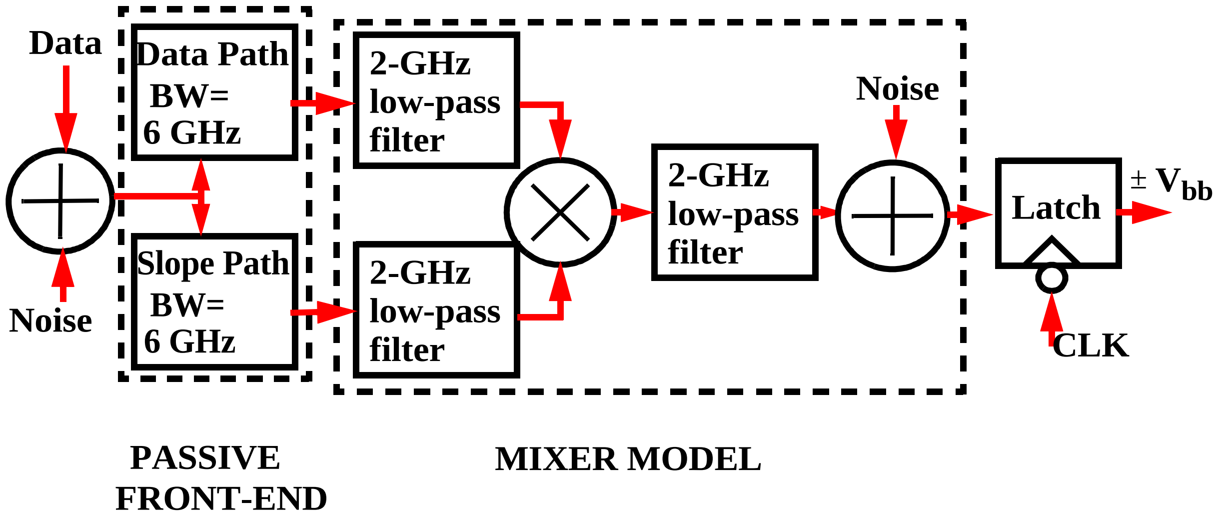


Figure 3.12: Simulink model for passive filter aided phase detector.

(4) Since $\tau_1 = R_1C_1; \tau_2 = R_cC_1$, with τ_1 and τ_2 known from steps (1)-(3), the loop filter parameters(i.e. C_1 and R_1) can be determined if R_c is known. Based on the spec. sheet for the ADCMP572 latch, R_c was set to 50 Ω. Thus $C_1 = \tau_2/R_c$ and $R_1 = \tau_1/C_1$.
(5) C_c has to be chosen large enough so that the transfer function with and without C_c remain the same.

The bang-bang PD gain,$K_{pd_{BB}}$ for the external timing recovery loop was estimated using the simulink model shown in Fig. 3.12. The passive filter was modeled using a first order low pass and high pass transfer function with a 6 GHz bandwidth[2]. The mixer was modeled as a multiplier block with first order filters at its inputs and output. According to the spec. sheet, the inputs and output bandwidth of the mixer is 2.5GHz. In the simulink model, the bandwidth was set to 2-GHz to maintain a safety margin. As discussed in chapter 2, $K_{pd_{BB}}$ is strongly influenced by noise. The noise level at the input to the model was chosen such that the SNR at the output of the passive filter agreed with measurements[3]. Noise was also injected at the output of the mixer to realize a 14 dB noise figure[4]. Under these conditions, the phase detector (which is comprised of the mixer and latch), was characterized in Simulink by simulating the P_{early} and P_{late} curves. Fig. 3.13 plots the eye diagram in the data path and the corresponding probability curves.

[2]A 6-GHz front-end bandwidth was chosen to be consistent with measured results.
[3]The SNR from measurements was 12.9. Refer to section 3.4.1, Fig. 3.14
[4]Based on the AD8343 spec. sheet, the mixer noise figure was 14dB.

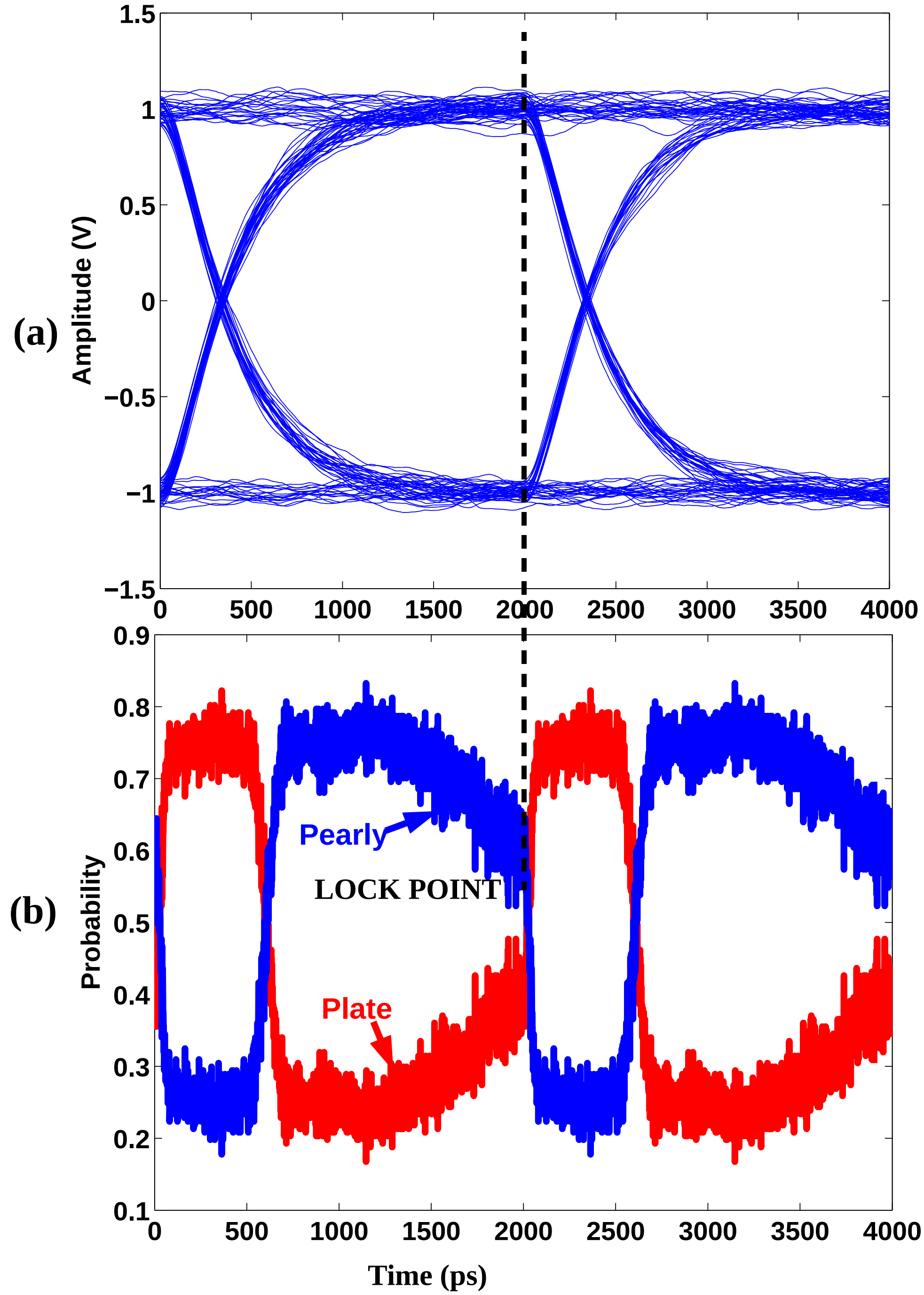


Figure 3.13: Passive filter aided phase detector characteristics. (a) Eye diagram at mixer input. (b) Probability curves at mixer output.

Table 3.3: Loop Parameters for the external CDR

Parameter	Value
Loop Bandwidth	16 MHz
Damping Factor, ζ	8
Average Slope (near lock point) $= -2\frac{dP_{early}}{d\tau}\|_{\tau=\tau_{lock}}$	2.3 /rad
$K_{pd_{BB}}$	0.46 V/rad
C_1	50 nF
$R_1 = R_c$	50 Ω
R_{coarse}	1 kΩ
C_c	10 nF
K_{vco}	2πx70 MRad/V-s

The average slope in the vicinity of the lock point is 2.3/rad. Thus $K_{pd_{BB}}$ is 0.46 V/rad (=0.2x2.3).

The choice of the loop bandwidth is a critical parameter in the design. The loop bandwidth was set to a high value (=16 MHz) to filter out VCO noise. The damping factor was set to 8 to ensure stability of the loop under stringent operating conditions. Thus following steps (1)-(5) the loop parameters can be computed for a particular bandwidth and damping factor. The loop parameters are tabulated in Table 3.3

3.4.1 Measurement Results

The mixer matching network was designed using the manufacturer's spec. sheet (Appendix C). The loop was tested with a 2-Gb/s 2^{31}-1 PRBS data pattern generated from a BERT. Fig. 3.14(a) shows data and slope outputs of the passive front-end at 2-Gb/s. Note the measured SNR for the data-eye is 12.8. Fig. 3.14(b) shows the mixer output corresponding to the 2-Gb/s passive filter output. As expected, a baud-rate timing tone is visible at the output of the mixer. Fig. 3.14(c) shows the recovered clock at 2-GHz. The resulting RMS jitter was 6.1 ps for a 2-GHz recovered clock.

The RMS jitter can be calculated using the linear jitter model presented in chapter 2

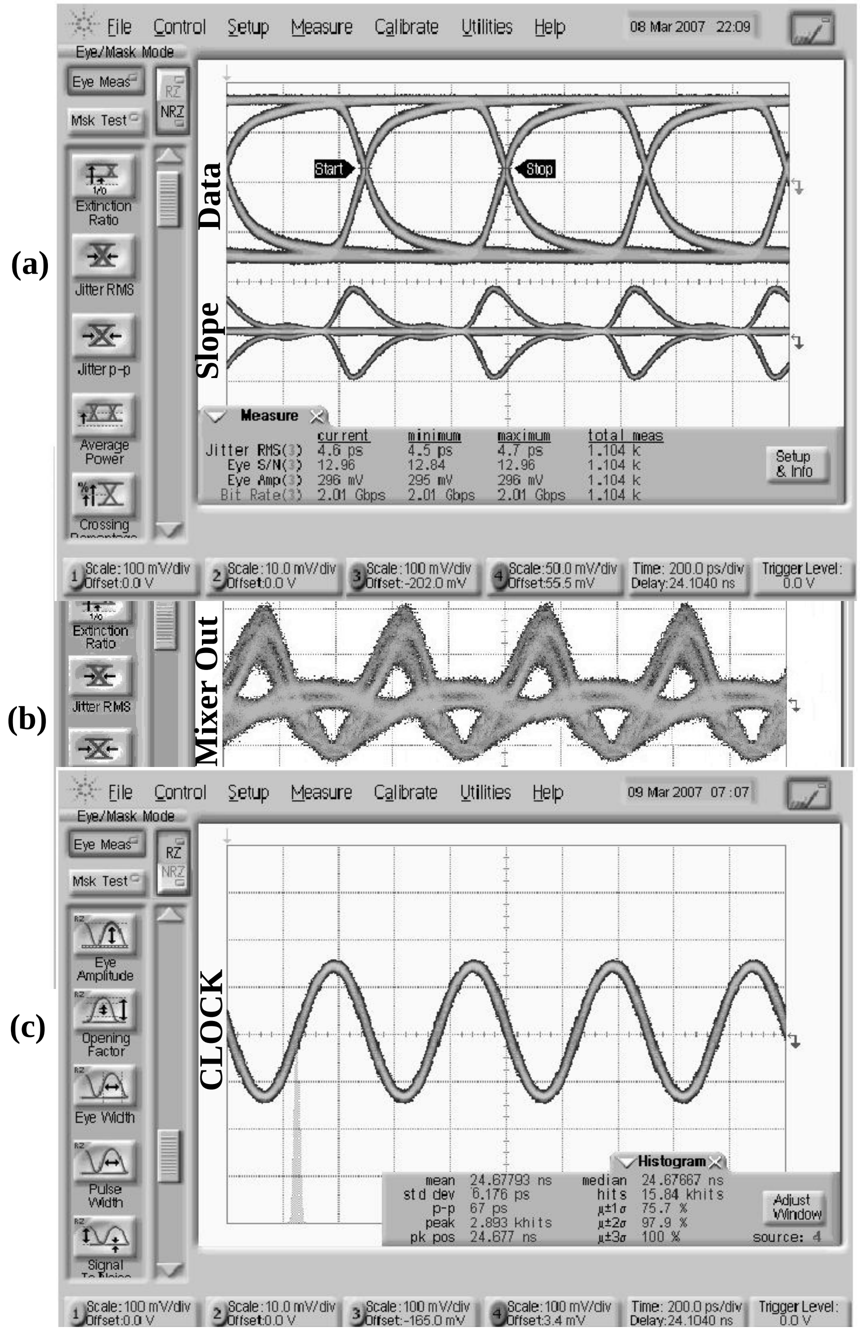


Figure 3.14: Waveforms at different points of the TR loop. (a) Data (top eye) and slope (bottom eye) outputs of passive filter at 2-Gb/s.(Vertical scale (top eye)=100mV/div; Vertical scale (bottom eye)=50mV/div ; Horizontal scale=200ps/div) (b) Mixer output corresponding to a 2-Gb/s random data sequence (Vertical scale= 50mV/div; Horizontal scale=200ps/div). (c) Recovered 2-GHz clock (Vertical scale= 100mV/div; Horizontal scale=200ps/div).

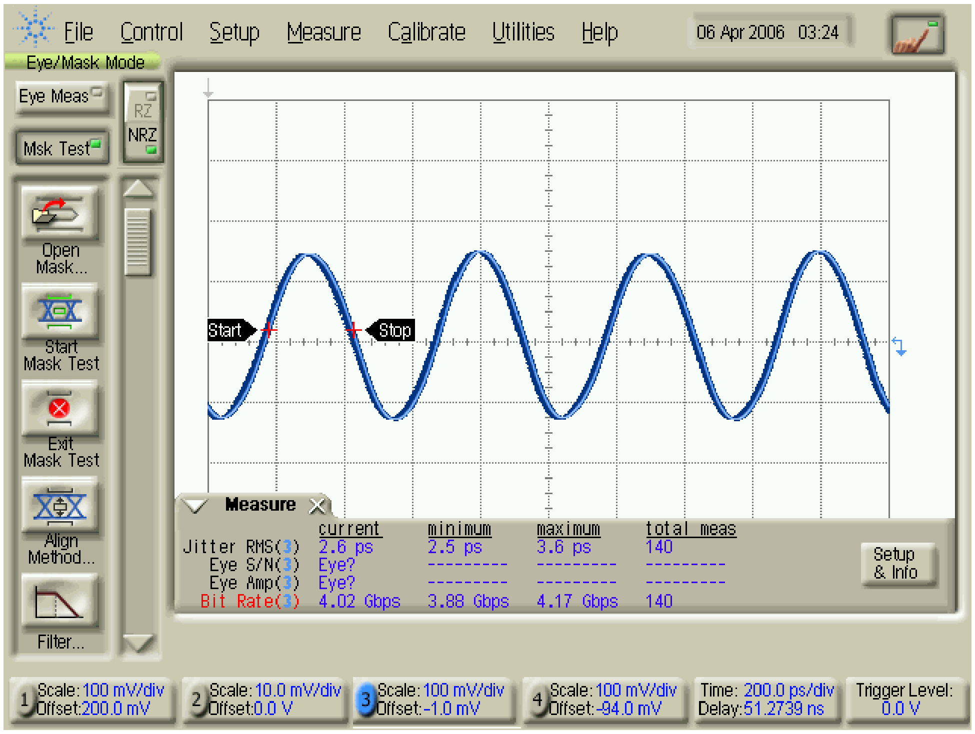


Figure 3.15: Recovered 2-GHz clock locked to a 2-GHz alternating pattern.

which is reproduced here for completeness:

$$\sigma_{RMS} = \sqrt{\frac{\theta_{bb}}{4(-2\frac{dP_{early}}{d\tau}|_{\tau=\tau_{lock}})}} \tag{3.19}$$

where θ_{bb} is the bang-bang phase update (in radians) which is given as:

$$\theta_{bb} = \frac{V_{bb} * K_{vco}}{f_{clk}} = \frac{0.2 * 2 * \pi * 70e6}{2e9} = 0.044 \tag{3.20}$$

Substituting values, the RMS jitter is computed to be 5.5 ps. Note that the linear jitter model does not account for noise sources within the loop such as VCO and power supply noise. To account for these factors, a 2-GHz alternating pattern was applied to the external timing recovery loop and the RMS jitter was measured with the loop locked to the alternating pattern. As shown in Fig. 3.15, the resulting RMS jitter on the recovered clock was 2.6 ps. This jitter is due to random noise sources within the loop and it does not include the data-dependent component. This random component can be added to the predicted jitter in an RMS fashion:

$$\sigma_{TOTAL} = \sqrt{\sigma_D^2 + \sigma_{Random}^2} = \sqrt{5.5^2 + 2.6^2} = 6.08ps \tag{3.21}$$

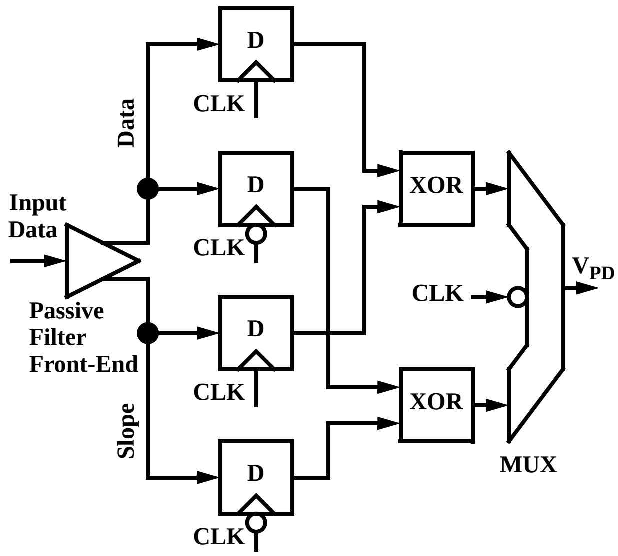


Figure 3.16: Block diagram of the half-rate modified SSMMSE PD.

Thus the measured jitter of 6.17ps is in agreement with that predicted by theory in Eq. 3.21.

3.5 Half-Rate Modified SSMMSE PD based CDR

The purpose of this section is to investigate the potential hardware advantages of a half-rate modified SSMMSE PD based CDR over a half-rate conventional edge-sample based CDR.

3.5.1 Proposed Half-Rate PD architecture

Fig. 3.16 shows the block diagram of a half-rate SSMMSE PD. The D-flip flops perform the *sgn* operations and the XOR gates take the product of the slope and data signals. The MUX combines the two parallel paths to generate the bang-bang phase detector output voltage, V_{PD}. Fig. 3.17 shows the block diagram of a typical half-rate edge-sample PD [9]. Comparison of the two phase detectors shows that modified SSMMSE PD requires fewer logic gates than a typical half-rate PD. However, SSMMSE PD based CDR requires a front end passive section to detect the slope of the incoming bit stream.

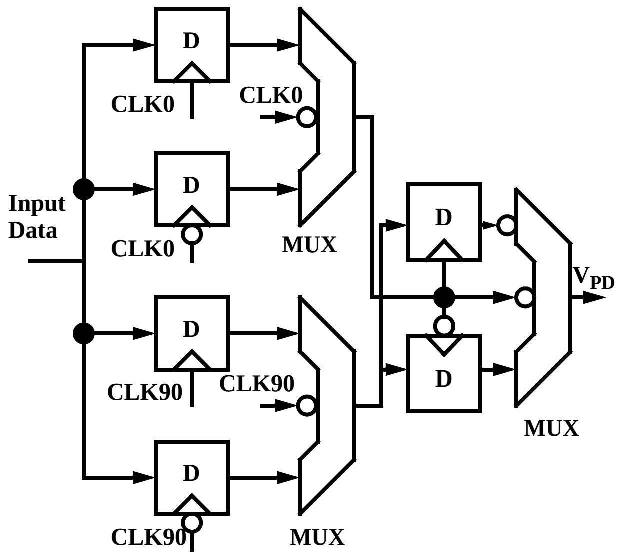
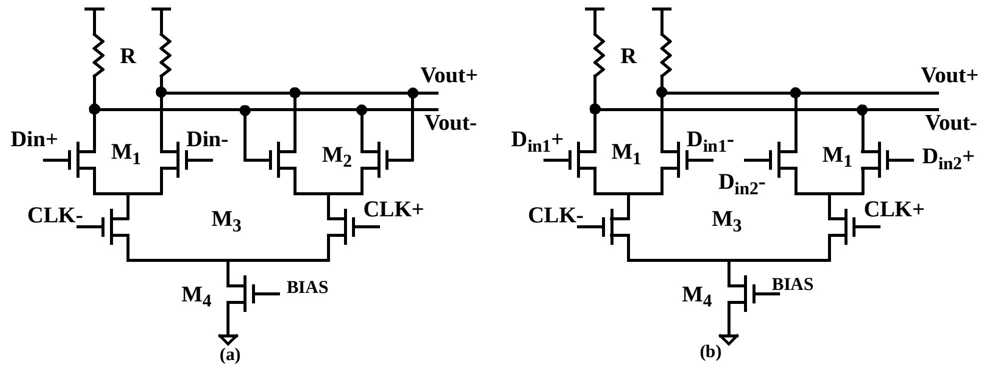


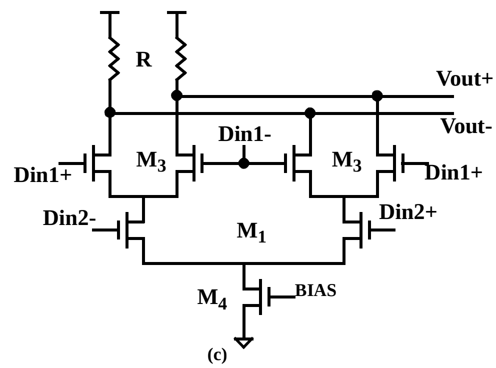
Figure 3.17: Block diagram of a typical half-rate edge-sample PD [9].

3.5.2 Simulation Results

The CDRs were simulated in a 0.18 μm CMOS process. The flip flops were identical to those reported in [35]. The logic gates were similarly sized as the flip-flops. Schematics of the flip-flops, MUX and XOR logic gates are shown in Fig. 3.18. Fig. 3.19 shows the simulation test setup for both CDRs. An I/O bandwidth of 6-GHz was assumed to model the effect of on-chip parasitics. For the modified SSMMSE PD, a cross-coupled differential LC VCO topology was used the power consumption of which was 8.1mW. This is similar to the power consumption reported for VCOs implemented in a 0.18 μm CMOS technology at similar speeds[36]. For the half-rate edge sampled PD based CDR, a typical [38],[39] two stage quadrature LC VCO (Q-VCO) is required to generate the in-phase and quadrature signals whereas the SSMMSE PD based CDR requires a single stage differential VCO. Fig. 3.20 shows the two topologies. Fig. 3.21 and Fig. 3.22 show the VCO outputs of the differential and Q-VCO. Note the deterioration in oscillation amplitude in the quadrature VCO; this is mainly caused by the reduction of the effective Q of the tanks due to the coupling between oscilltors [37].

Note that in Fig. 3.16, the clock phase is driving five loads and in Fig. 3.17 each clock phase is driving three loads. Thus the VCO in the SSMMSE PD is driving 5/3=1.7 times the load than each phase of the VCO in the edge-sample PD. Nevertheless, each





Parameter	Value
M_1	10/0.18
M_2	8/0.18
M_3	5/0.18
M_4	10/0.18
R	650
Power	1.6 mW

(d)

Figure 3.18: Latches and logic gates used in simulations. (a) Latch (b) MUX (c) XOR gate (d) Parameter Values.

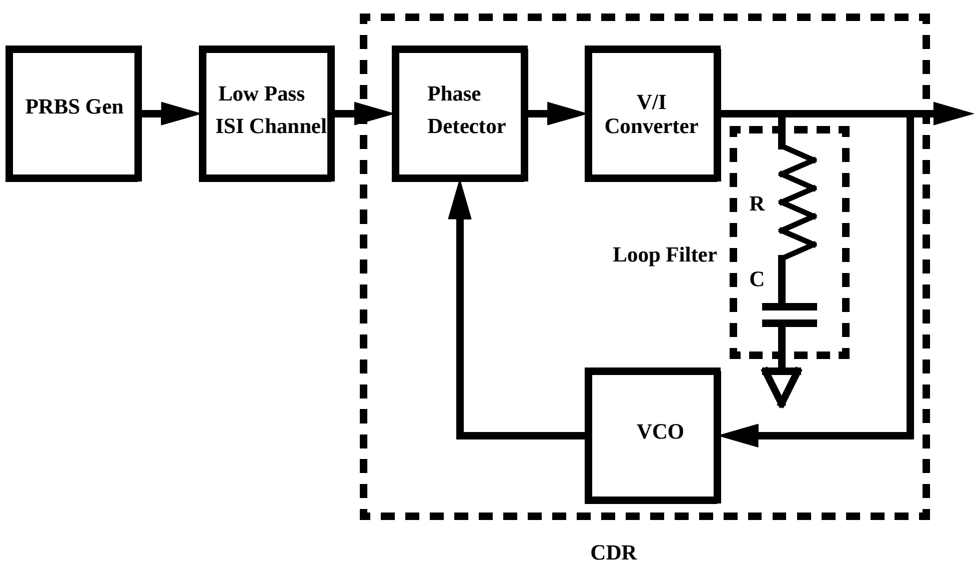


Figure 3.19: Simulation test setup.

Parameter	Value
M_1	70u/0.18u
M_2	23u/0.18u
M_3	47u/0.18u
M_4	15u/1u
L_1	650pH
C	1.2pF
I_{tail}	4.5 mA
Q_{tank}	10

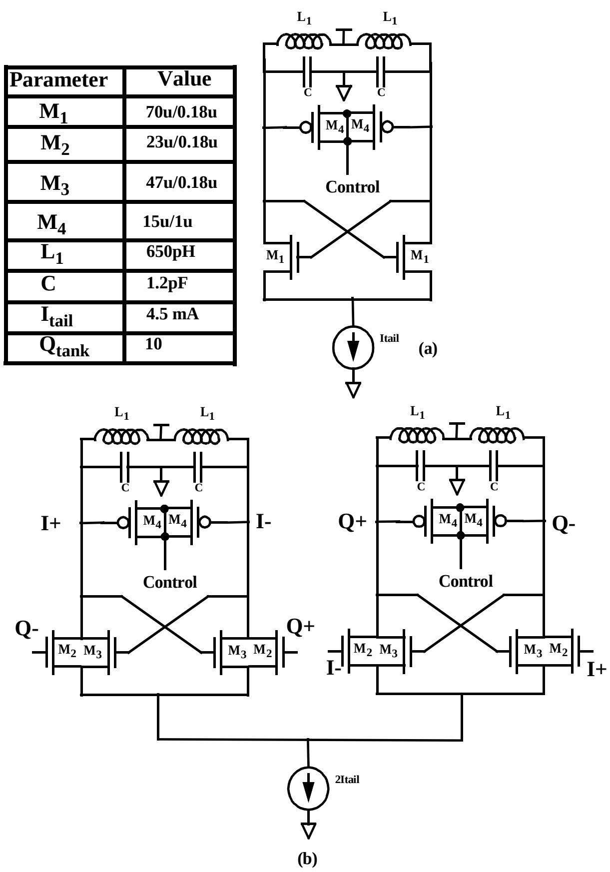


Figure 3.20: VCO topologies. (a) Single stage differential VCO. (b) Two stage quadrature VCO.

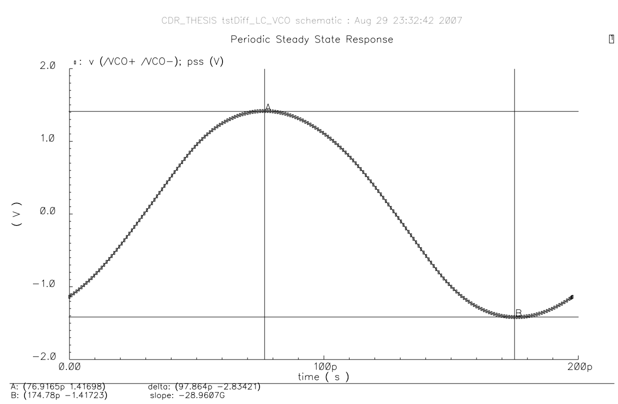


Figure 3.21: LC VCO differential output.

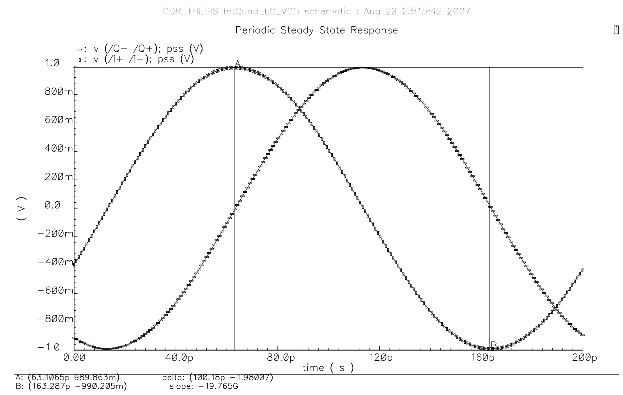


Figure 3.22: In phase and quadrature output of the quadrature VCO.

Table 3.4: CDR loop parameters used in simulations

Parameter	Value	Unit
Average PD Slope (near lock point)	2	/radian
K VCO	300	MHz/V
PD gain (near lock point)	100	$\mu A/Rad$
Charge Pump Current	50	μA
Loop Bandwidth	10	MHz
Loop Filter	R=0.33 C=6.9	kΩ nF

VCO buffer in the Alexander PD based CDR requires the same current as the buffer in the SSMMSE CDR since the output swing is lower in a Q-VCO.

A PRBS $2^{31}-1$ input pattern was used in simulations. The peak-to-peak input voltage per side was 300mV. The average PD output voltage vs. the sampling phase is plotted in Fig. 3.23. It can be seen that both PDs have approximately the same gain near the lock point. This could be due to the fact that both PDs are operating in the metastable region near the lock point. Table 3.4 lists the CDR loop parameters used in simulations. Figs 3.24 and 3.25 show eye diagrams at different points of the CDR loop for the modified SSMMSE and edge-sample CDR.

A summary of power dissipation of the two CDRs is given in Table 3.5. Note that although both CDRs have comparable power consumption (i.e. 54.5mW vs. 54.6 mW),

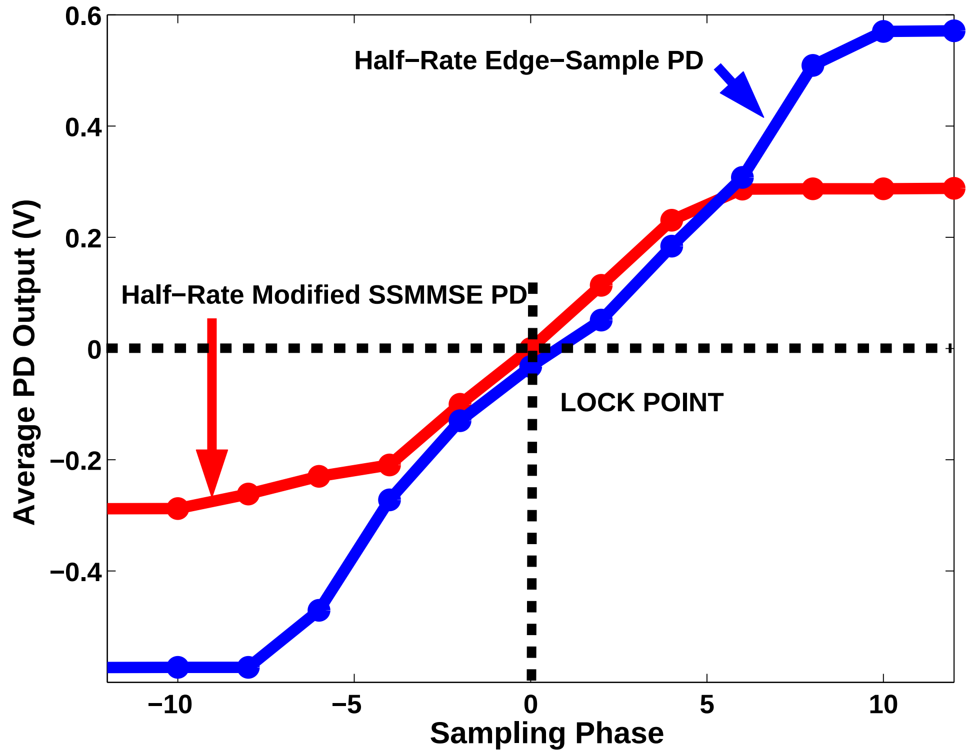


Figure 3.23: Phase detector characteristics for edge-sample and modified SSMMSE PD.

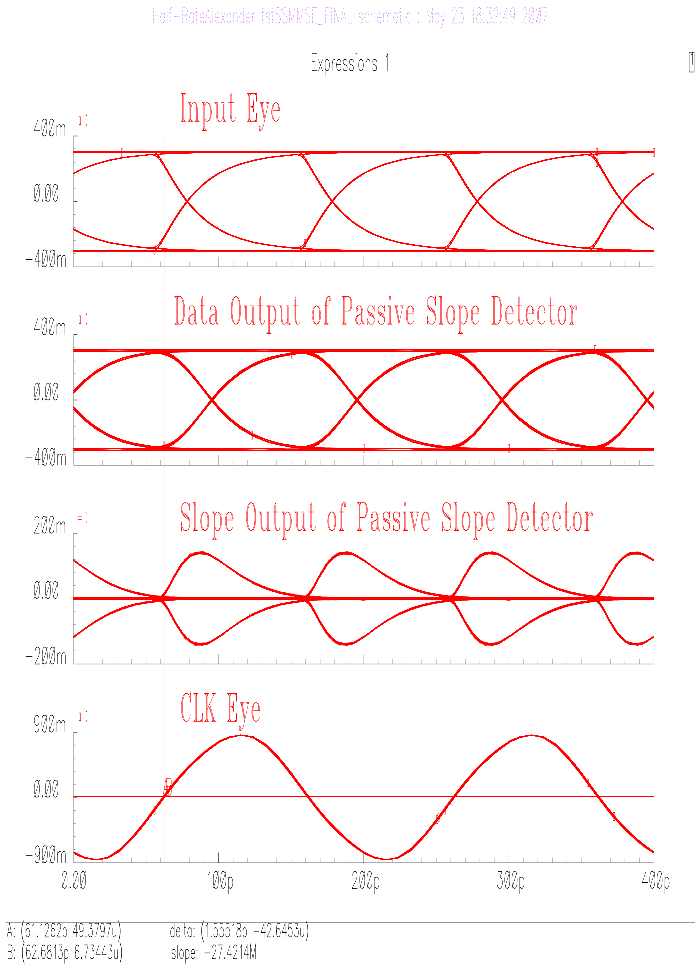


Figure 3.24: Eye diagrams for half-rate modified SSMMSE PD based CDR.

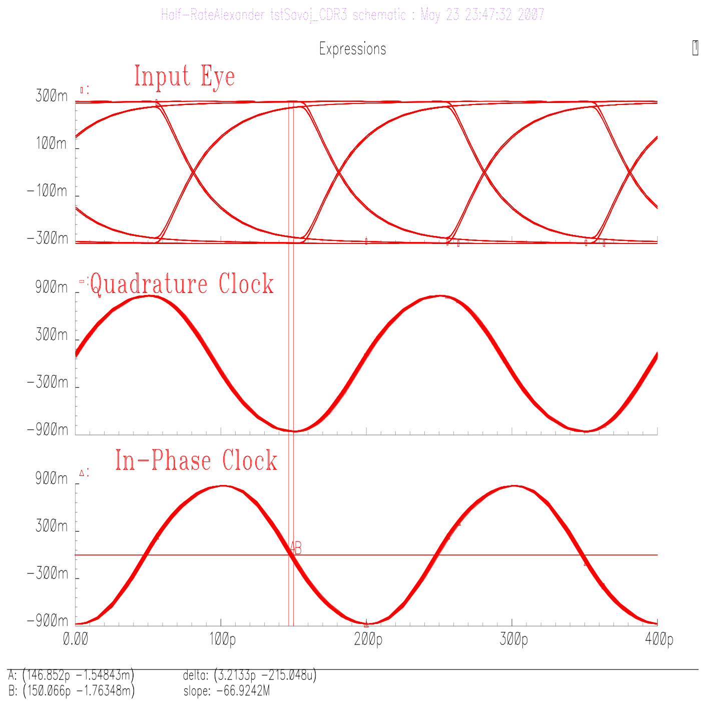


Figure 3.25: Eye diagrams for half rate edge-sample PD based CDR.

the modified SSMMSE technique consumes lower power in the VCO, the VCO buffer and the phase detector. Note also that in a practical implementation the edge-sample PD based CDR will typically consume more power than the power reported here since a front-end amplifier is normally used in these systems to drive the CDR with fast rise and fall times [1] but none was simulated here.

The recovered clock jitter of the two CDRs is depicted in Table 3.6. The edge-sample PD based CDR exhibits larger jitter because in the absence of data transitions, the PD holds on to its previous state and the clock phase drifts [9]. In contrast, the SSMMSE PD based CDRs are metastable during no data transition intervals, and consequently the mean PD output is zero during long strings of 1's and 0's.

3.6 Conclusion

This chapter presented a passive filter that is used to generate timing information from a random data waveform. This filter provides simultaneous lowpass and highpass transfer characteristics over a broad bandwidth. The high-pass transfer characteristic is utilized to provide the slope information unto 10-Gb/s. The data and slope signals can be used

Table 3.5: Simulated Power Breakdown of 10-Gb/s CDRs in 0.18 μm CMOS

Block	Modified SSMMSE PD based CDR	Edge-sample PD based CDR
Front-End	12mAx1.8v=21.6 mW	0
Phase Detector	9.8mAx1.8v=17.6 mW	13.3mAx1.8v=24mW
VCO	4.5mAx1.8v=8.1mW	2x4.5mAx1.8v=16.2mW
VCO Buffer	4mAx1.8v=7.2 mW	2x4mAx1.8v=14.4 mW
Total	54.5mW	54.6mW

Table 3.6: Period Jitter and Peak-to-Peak Jitter for simulated CDRs

CDR	Period Jitter,ps	Peak-to-peak Jitter, ps (400 clock cycles)
Modified SSMMSE PD based	0.74	1.55
Edge-sample PD based	0.78	3.2

to recover a clock based on the modified SSMMSE criterion. To demonstrate the timing recovery concept, the prototype passive filter was used with external components to recover a 2-GHz clock from a 2-Gb/s 2^{31}-1 random data sequence. A 10 Gb/s half-rate modified SSMMSE PD based CDR architecture is proposed and compared with a conventional edge-sample PD based CDR using identical circuit blocks in 0.18μm CMOS. Simulations predict similar power consumptions for the two techniques and lower jitter for the proposed technique. It has already been shown that modified SSMMSE timing recovery can improve the performance compared to edge-sample CDRs particularly in the presence of high levels of noise or interference [25]. Hence modified SSMMSE CDRs are a potentially useful alternative to conventional edge-sample PD based CDRs for high-speed applications.

Chapter 4

Dual-Function Analog Filter Aided Timing Recovery

4.1 Overview

This chapter presents a baud-rate timing recovery scheme that is aided by signals generated from a dual-function analog filter. The analog filter functions as a simultaneous lowpass and bandpass filter to generate the data and its slope respectively. Peaking is introduced in the lowpass data path to equalize a lossy channel. The timing recovery loop utilizes the equalized data and slope signals obtained from the dual-function analog filter to recover a clock based on a modified minimum mean squared error (MMSE) criterion. As a proof of concept, a prototype dual-function analog filter was fabricated in a 0.18-μm CMOS process and used to recover a 2-GHz clock from a 2-Gb/s 2^{31}-1 PRBS sequence.

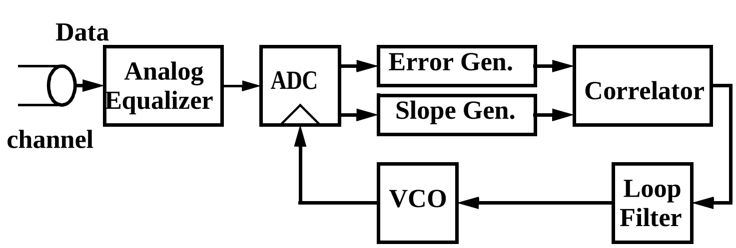


Figure 4.1: Conventional MMSE TR scheme with an analog (linear) equalizer [18].

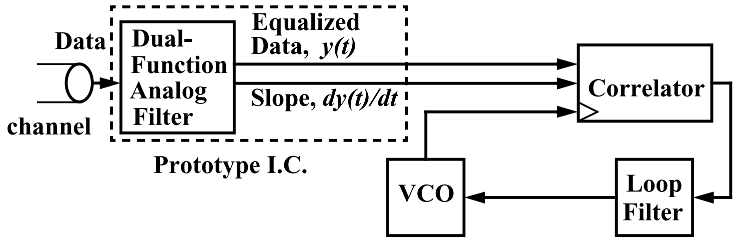


Figure 4.2: Proposed MMSE TR scheme with a dual-function analog filter.

4.2 Background

Fig. 4.1 shows the block diagram of a conventional MMSE scheme that uses an analog equalizer [18][1], [19], [20]. Slope detection in the conventional MMSE architecture is usually performed by using a two-tap FIR filter. This chapter proposes an active filter based slope detection scheme for MMSE TR. Fig. 4.2 shows the proposed scheme. Two important architectural differences are observed when compared to the conventional MMSE architecture. Firstly, an analog filter is used to perform both linear equalization and slope detection. The design and implementation of this dual-function analog filter is discussed in this chapter. Secondly, no error signal is required by the correlator. The correlator basically implements the error-signal free modified SSMMSE timing function introduced in Eq. (1.15):

$$\tau_{k+1} = \tau_k + \theta_{bb}\text{sgn}\left(y(kT+\tau_k)\frac{\delta y(kT+\tau_k)}{\delta\tau_k}\right) \tag{4.1}$$

Thus the correlator can be implemented as a Gilbert cell mixer in the analog domain. Note that if there is peaking in the data eye, the assumptions[2] about the sign of the error upon which Eq. (4.1) is based are no longer true. Nevertheless the nonlinearity in Eq. (4.1) generates a timing tone in the presence of peaking in the data eye which the TR loop can lock to. This is experimentally verified in section 4.4.

4.3 Dual-Function Analog Filter

This section attempts to describe the architecture of the dual-function analog filter block of Fig. 4.1. This block aids the TR loop by generating the slope and also performs linear

[1]This is a variation of the conventional MMSE scheme where the timing recovery is done prior to the ADC.

[2]Refer to Eq. (1.14) in chapter 1.

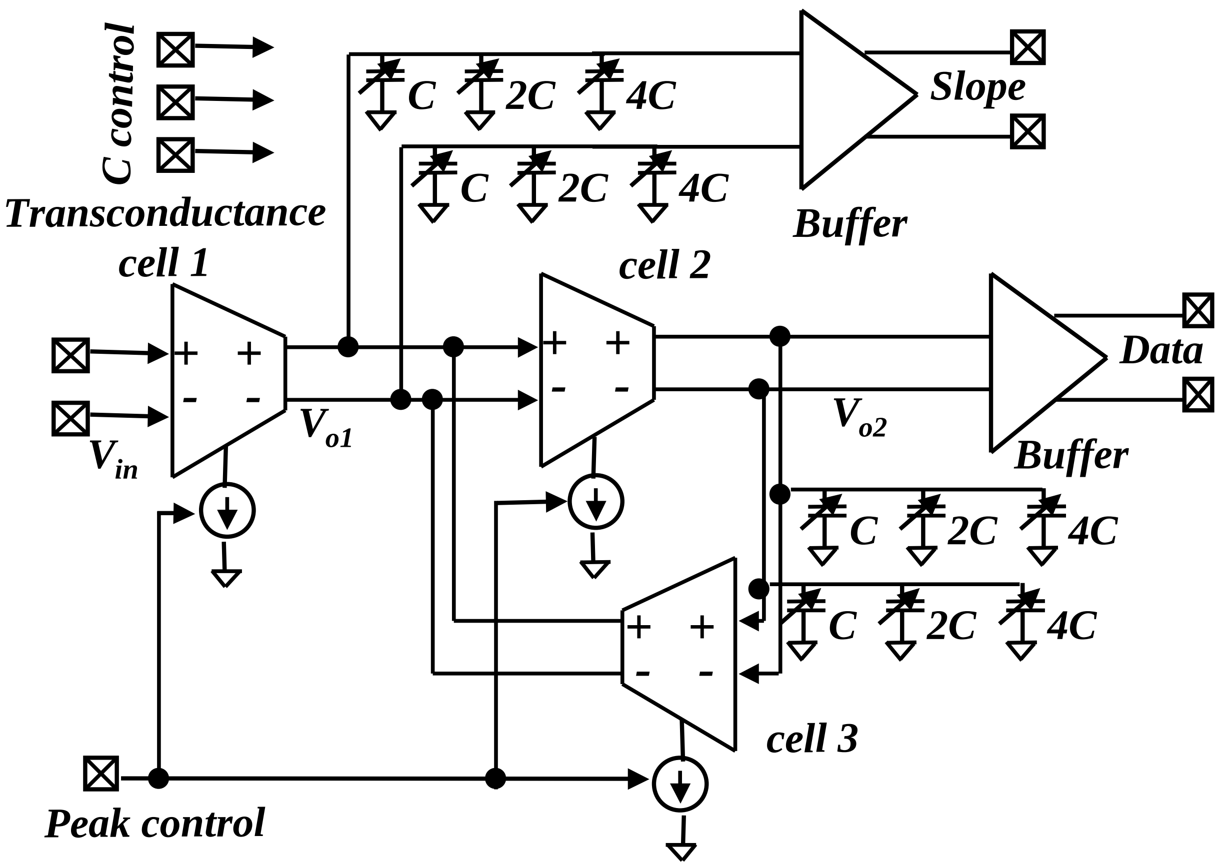


Figure 4.3: Dual-function analog filter topology.

equalization. Fig. 4.3 shows the architecture of the circuit. Note that this circuit can be derived from the block diagram in Fig. 1.16 (c) by replacing the integrator in the slope path by two integrators before the summing block. One integrator is placed at input and the other in the feedback path.

Note that the circuit in Fig. 4.3 has two outputs: data and slope and it consists of three identical transconductance cells arranged in negative feedback to realize a second order transfer function. The output impedance, R_o of each transconductance cell provides sufficient damping to ensure stability and avoid oscillations. Assuming g_m is the transconductance of each cell, C_{p1} the parasitic capacitance at V_{o1}, C_{p2} the parasitic capacitance at V_{o2}, C_{ext} the capacitance of a programmable on chip capacitor bank, $Z_{o1} = \frac{R_o}{2}||\frac{1}{sC_1}$ the impedance at node V_{o1}, $Z_{o2} = R_o||\frac{1}{sC_2}$ the impedance at node V_{o2}, $C_1 = C_{p1} + C_{ext}$ and $C_2 = C_{p2} + C_{ext}$, the transfer function in the data path can be expressed as,

$$\frac{V_{o2}}{V_{in}} = \frac{g_m^2 Z_{o1} Z_{o2}}{1 + g_m^2 Z_{o1} Z_{o2}} \tag{4.2}$$

The transfer function in the slope path can be expressed as:

$$\frac{V_{o1}}{V_{in}} = \frac{g_m Z_{o1}}{1 + g_m^2 Z_{o1} Z_{o2}} \tag{4.3}$$

Combining Eq. (4.2) and (4.4):

$$V_{o1} = \frac{1}{g_m Z_{o2}} V_{o2} \tag{4.4}$$

Since Z_{o2} approaches $\frac{1}{sC_2}$ at frequencies $\omega \gg 1/(R_o C_2)$, V_{o1} and V_{o2} are related as follows,

$$V_{o1} \approx s\frac{C_2}{g_m} V_{o2} \tag{4.5}$$

To achieve linear equalization along the data path, some peaking has to be introduced into the transfer function in Eq. (4.2). The frequency for peaking is obtained by substituting $s = j\omega$ in Eq. (4.2):

$$\frac{V_{o2}}{V_{in}}(\omega) = \frac{\omega_o^2}{-\omega^2 + j\omega(\omega_1 + \omega_2) + \omega_o^2 + \omega_1\omega_2} = H_2(\omega) \tag{4.6}$$

where $\omega_o = \frac{g_m}{\sqrt{C_1 C_2}}$, $\omega_1 = \frac{2}{R_o C_1}$, $\omega_2 = \frac{1}{R_o C_2}$. The magnitude response is

$$|H_2(\omega)| = \frac{\omega_o^2}{\sqrt{(\omega_o^2 + \omega_1\omega_2 - \omega^2)^2 + \omega^2(\omega_1 + \omega_2)^2}} \tag{4.7}$$

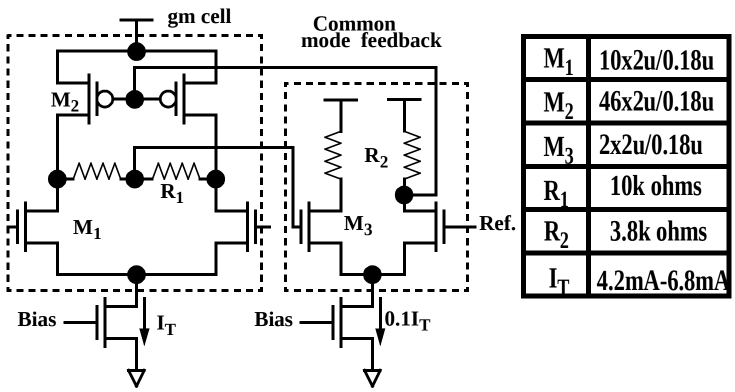


Figure 4.4: Transconductance cell of the dual-function analog filter.

Equating the derivative of Eq. (4.7) with respect to ω to zero allows solving for the peaking frequency, ω_{peak}:

$$\omega_{peak} = \sqrt{\omega_o^2 - \frac{1}{2}(\omega_1^2 + \omega_2^2)} \tag{4.8}$$

If $\omega_o < \sqrt{(\omega_1^2 + \omega_2^2)/2}$ then there is no peaking. When $\omega_o \gg \sqrt{(\omega_1^2 + \omega_2^2)/2}$, the peaking frequency can be approximated as,

$$\omega_{peak} \approx \frac{g_m}{\sqrt{C_1 C_2}} = \omega_o \tag{4.9}$$

Substituting Eq. (4.9) in Eq. (4.2) we get,

$$|H_2(\omega_{peak})| \approx \frac{\omega_{peak}^2}{\sqrt{(\omega_1^2\omega_2^2 + \omega_{peak}^2(\omega_1 + \omega_2)^2}} \tag{4.10}$$

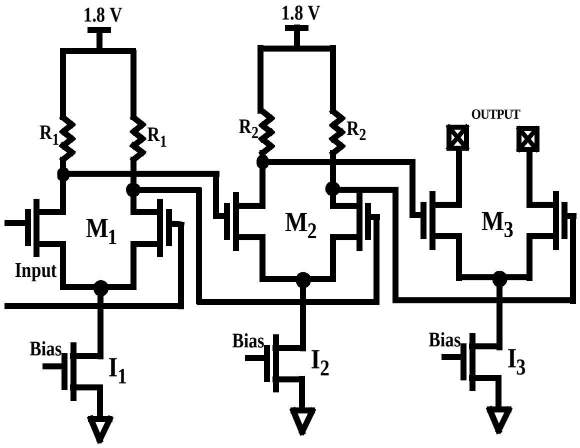
Since $\omega_{peak}^2(\omega_1 + \omega_2)^2 \gg \omega_1^2\omega_2^2$, Eq. (4.10) can be approximated as,

$$|H_2(\omega_{peak})| \approx \frac{\omega_{peak}}{(\omega_1 + \omega_2)} \tag{4.11}$$

Substituting expressions for ω_{peak}, ω_1 and ω_2 we get:

$$|H_2(\omega = \omega_{peak})| \approx \frac{g_m R_o}{\sqrt{\frac{C_1}{C_2}} + 2\sqrt{\frac{C_2}{C_1}}} \tag{4.12}$$

The amount of peaking in the magnitude response given by Eq. (4.6) is proportional to the product $g_m R_o$. The transconductance g_m is proportional to I_T^α where $\alpha < \frac{1}{2}$ due to mobility degradation and velocity saturation effects. The output resistance, R_o is dominated by the drain source resistance of MOSFETs and hence is inversely proportional



Parameter	Value
R_1	550 ohms
R_2	185 ohms
I_1	1 mA
I_2	3 mA
I_3	10 mA
M_1	$\frac{5x1u}{0.18u}$
M_2	$\frac{15x1u}{0.18u}$
M_3	$\frac{50x1u}{0.18u}$

Figure 4.5: Output buffers used in the dual-function analog filter.

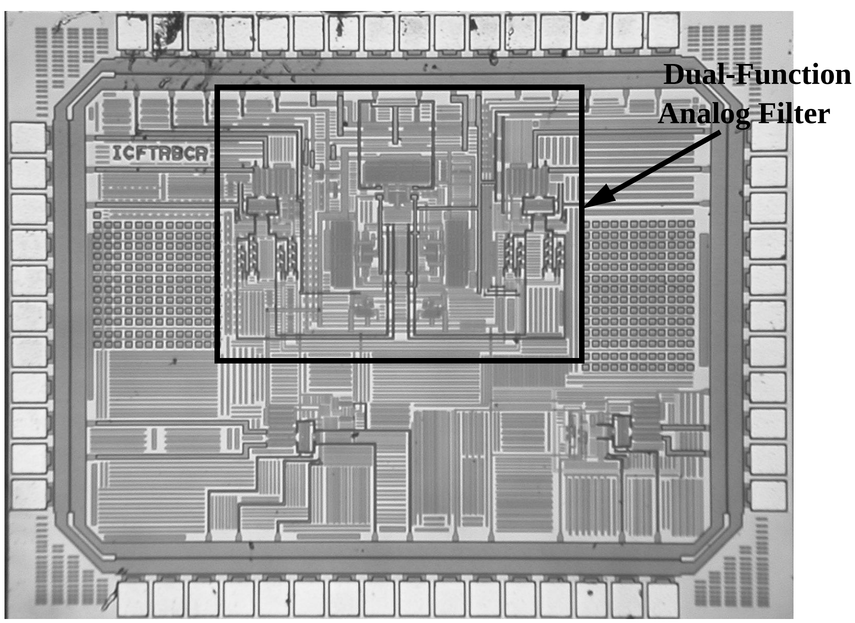


Figure 4.6: Die photo of dual-function analog filter.

Table 4.1: Measured Results for Dual-Function Analog Filter

Technology	0.18μm CMOS
Core Area	0.4 mm^2
Max. Peaking Freq.	2 GHz (for both data and slope path)
Max. Peak Gain	10 dB (for data path); 9 dB (for slope path)
Maximum Quality factor	3.8 (for both data and slope paths)
1 dB Compression point (Input at 2GHz)	-11 dBm (for both data and slope paths)
IIP3 (Inputs: 2000.5 MHz 1999.5 MHz)	1.3 dBm (Data path) 3.8 dBm (Slope Path)

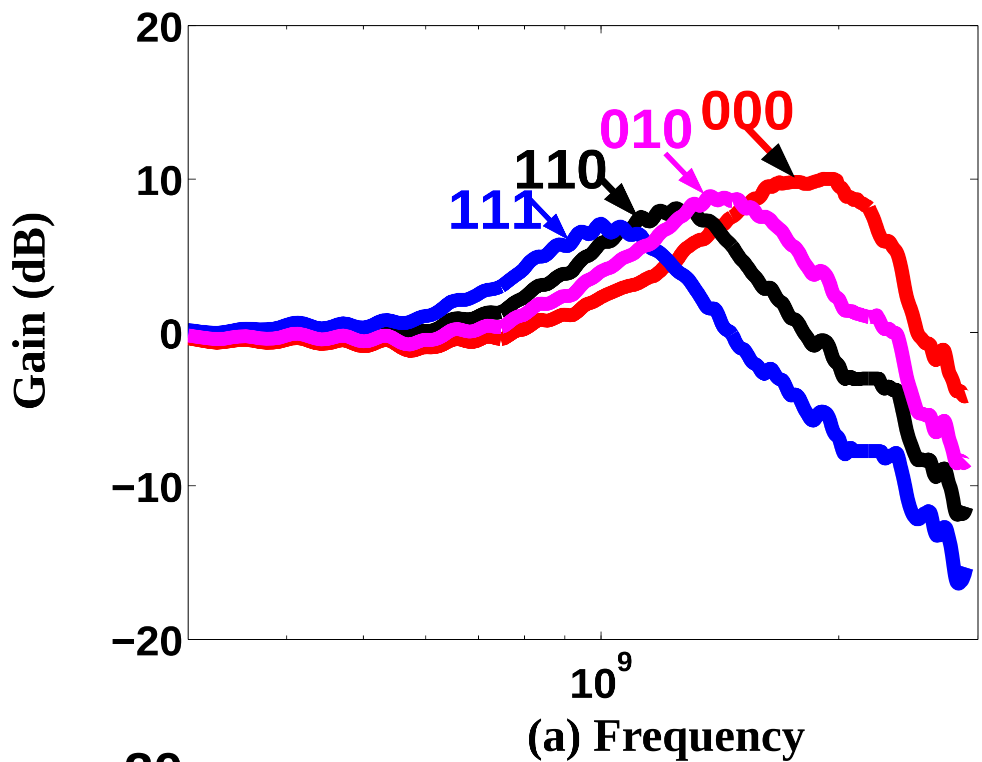
to I_T. Therefore, as I_T is increased, the amount of peaking is expected to decrease. Binary weighted capacitor banks and off-chip tail current control of the transconductance cells allowed programmable peaking frequencies and peaking amplitude variation respectively. Note that variation of tail current will cause the output common mode voltages of the transconductance cells to drift. To avoid these undesirable drifts, common-mode feedback (CMFB) was used.

Fig. 4.4(a) shows the schematic of the basic transconductance cell along with its common mode feedback (CMFB). Since cell 1 and cell 3 shared the same output nodes, a single CMFB circuit was used for both cells. Both the CMFB bias and the transconductance cell bias currents, I_T were controlled off chip.

Fig. 4.5 shows the schematic of the CML buffer used in the data and slope paths of the dual-function analog filter [35].

4.4 Measurement Results

The dual-function analog filter was fabricated in a 0.18-μm CMOS technology and occupied a core area of 0.4 mm^2. The die photo is shown in Fig. 4.6.



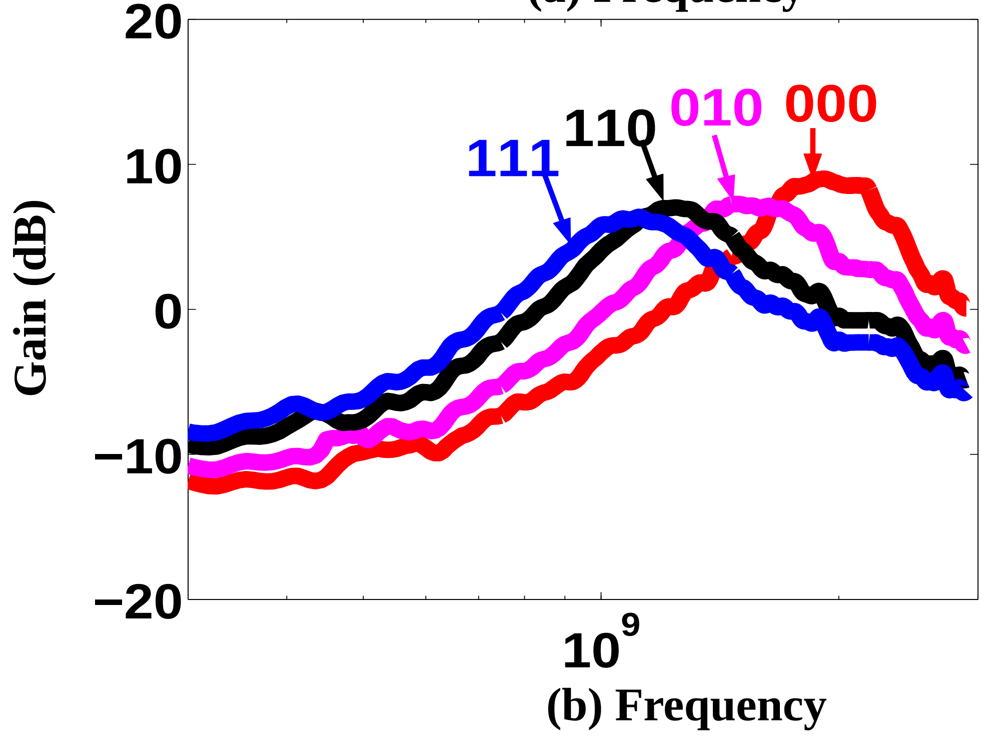


Figure 4.7: Measured frequency response for four different digital control word inputs to the binary weighted capacitor bank of the dual-function analog filter. (a) Data path. (b) Slope path.

4.4.1 Frequency Response

An HP 8595E spectrum analyzer was used to measure the frequency response (Fig. 4.7) of the filter. With all the switches in the capacitor bank turned off (digital control word input=000), the transfer function in both the data and slope path peak at 2 GHz with a peak gain of 10 dB and 9 dB respectively. Turning all the switches on (digital control word input=111) shifts the peaking frequency to 1 GHz. Since discontinuities in measured transfer functions occur at the same frequency for all transfer functions, hence these are primarily due to reflections. Reflections occur due to poor matching in the PCB traces, SMA connectors, cables and pads. Also, in Fig. 4.7(a) and 4.7(b), the slight degradation in peaking amplitude with changing peaking frequency can be explained using Eq. 4.12. As more capacitors are switched on the ratio C_1/C_2 decreases towards one. Consequently, the loss compensation capacity of the filter is degraded at lower frequencies. Table 4.1 summarizes the performance of the filter.

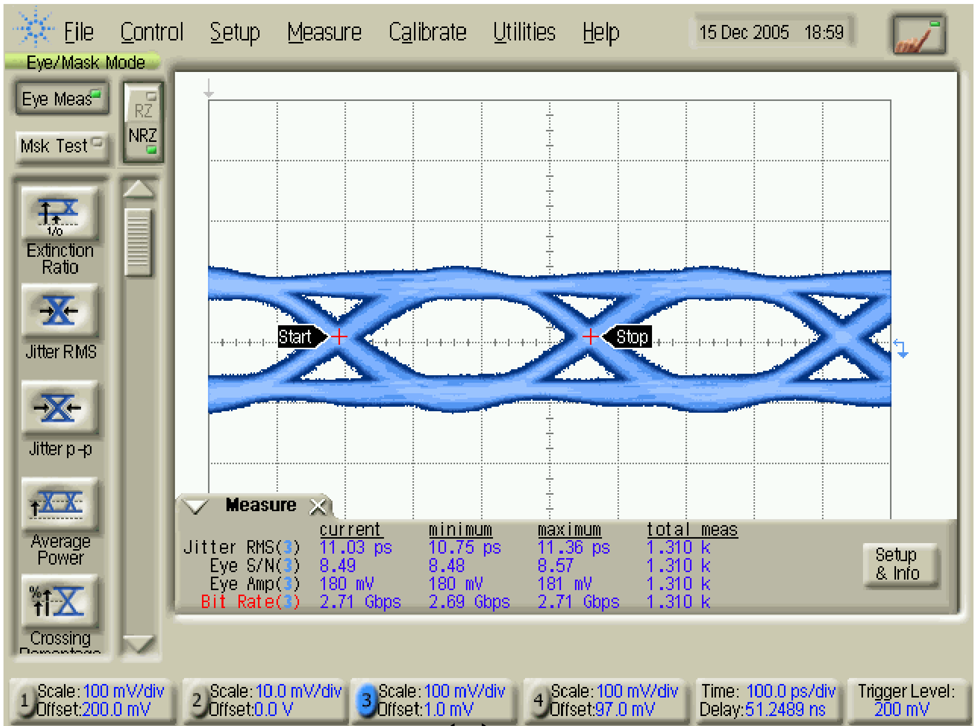
4.4.2 Slope Detection

An Agilent 8403A BERT was connected to the dual-function analog filter to test its functionality. Eye diagrams of the input and output eyes captured by an Agilent 86100B scope for a 2.7-Gb/s 2^{31}-1 PRBS sequence are shown in Fig. 4.8. The jitter at the input and output eyes are 11 ps and 12.6 ps respectively. The SNR at the input and output eyes are 8.49 and 6.43 respectively. Eye outputs of dual-function analog filter at 3.4 Gb/s are shown in Fig. 4.9.

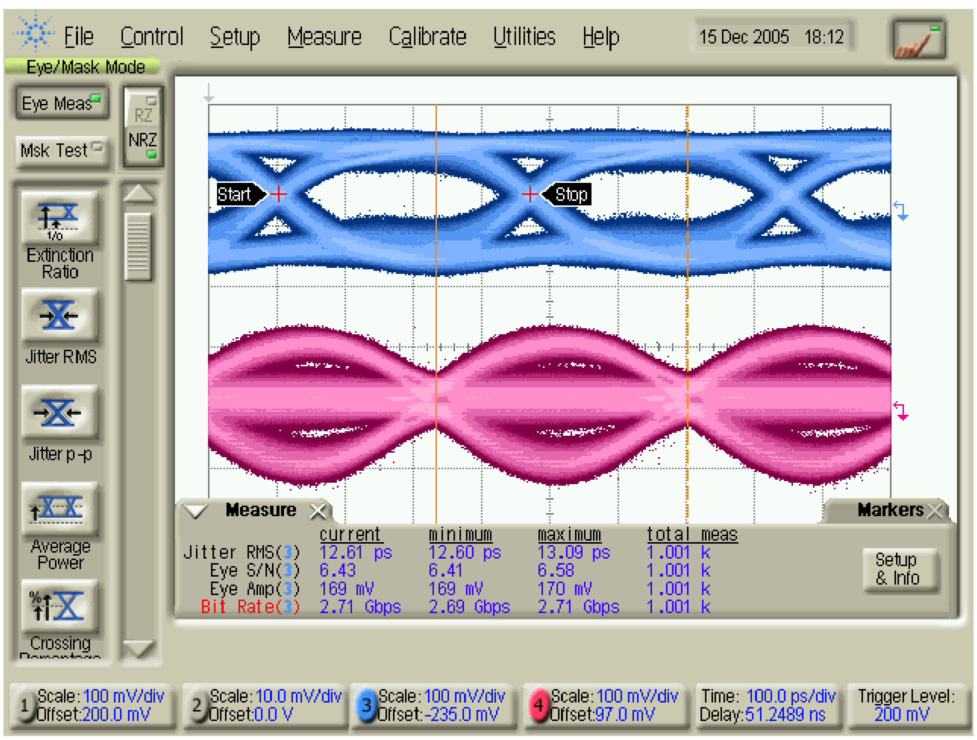
4.4.3 Noise Figure Measurement

Fig. 4.10 plots simulated and measured noise figure vs. frequency curves for the dual-function analog filter with peaking turned off and capacitor bank switched off. The discreapncy in the simulated and measured noise figures is possibly due to the inaccuracy of the noise models used by Spectre simulator. Note that the slope noise figure curves exhibit a minima at around 2-GHz. Since the slope path displays a band-pass response, low and high frequency signals that are not within the passband are attenuated, thus leading to a larger noise figure at those frequencies.

Transferring the noise figure in the data path to input referred noise and integrating from 100-MHz to 4-GHz, results in a noise voltage of 74.7 uV. Thus for a BER of 10e-12,



(a)



(b)

Figure 4.8: Dual-function analog filter input and output eyes at 2.7-Gb/s. (a) Input eye at 2.7 Gb/s. (Vertical scale=100mV/div; Horizontal scale=100ps/div). (b) Data (top eye) and slope (bottom eye) outputs at 2.7 Gb/s (Vertical scale=100 mV/div (top eye) and 100 mV/div (bottom eye); Horizontal scale=100ps/div).

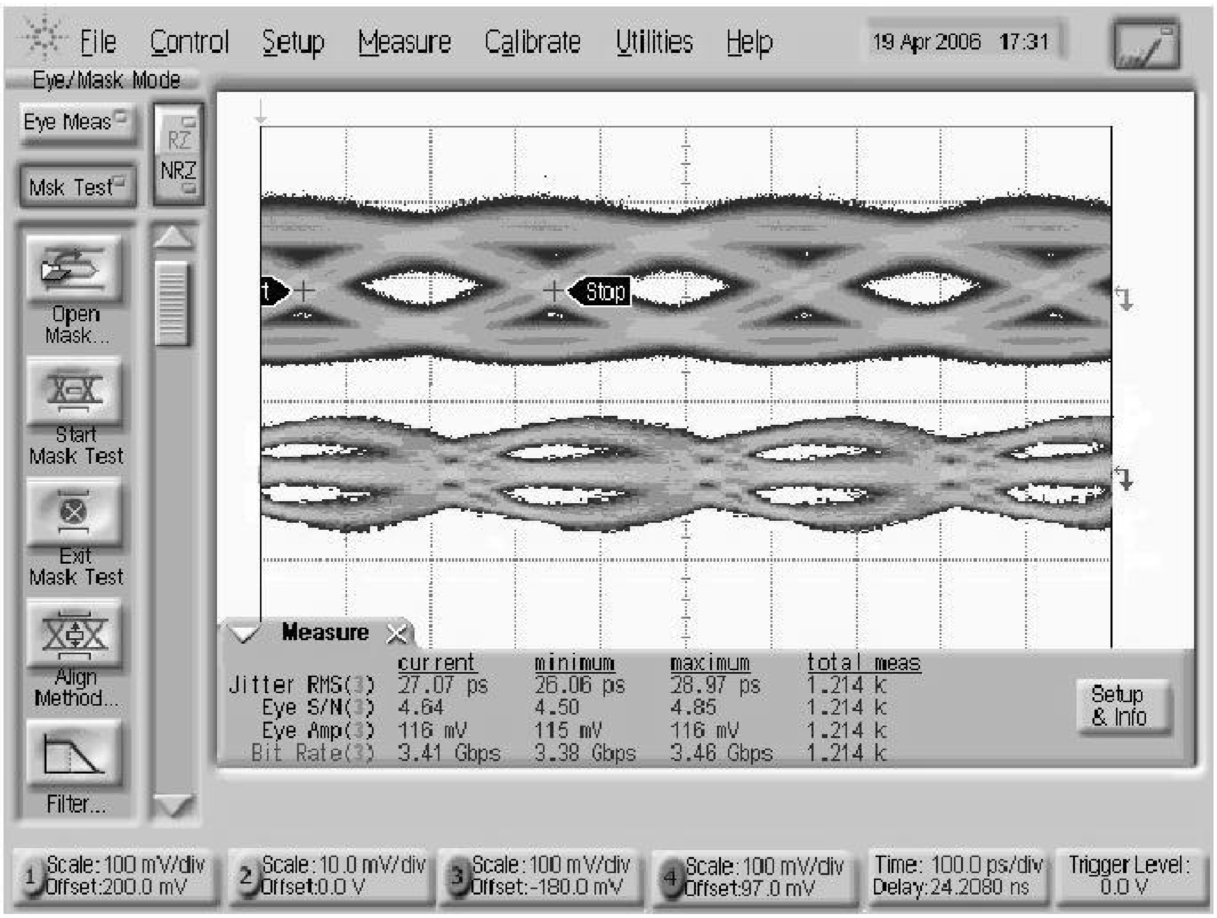


Figure 4.9: Data (top eye) and slope (bottom eye) outputs of dual-function analog filter at 3.4 Gb/s (Vertical scale=100 mV/div (top eye) and 100 mV/div (bottom eye); Horizontal scale=100ps/div).

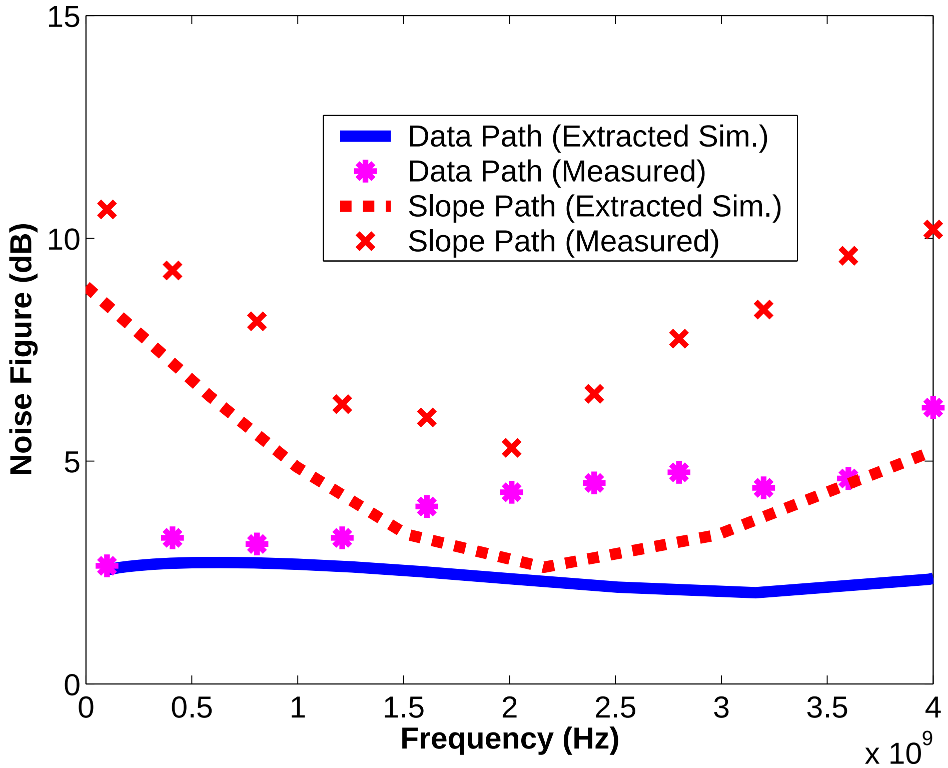


Figure 4.10: Simulated and measured noise figure vs. frequency for the dual-function ananlog filter with peaking turned off and capacitor bank switched off.

Table 4.2: Linear Equalizer Performance Comparison

Reference	Data Rate	Technology	Features	Power
This work	2 Gb/s	0.18μm CMOS	Analog filter with negative feedback	24.12mW (For Max Peaking)
[41]	3.5 Gb/s	0.18μm CMOS	Analog filter with source degeneration (adaptation included)	80 mW
[42]	2.5-3.5 Gb/s	0.25μm CMOS	FIR filter (adaptation included)	95mW

the sensitivity of the dual-function analog filter is 1mV (p-p) differential.

4.4.4 Linear Equalization

The peaking in the filter response can be used to equalize a lossy channel. As shown in Fig. 4.11, variation in peaking can be obtained by varying the filter current. Eye diagrams showing filter outputs with and without peaking are shown in Fig. 4.12. To test the loss compensation capacity of the filter, a 20 cm board to board channel including several coaxial cable sections was characterized as shown in Fig. 4.13. The channel was inserted between the BERT and the dual-function analog filter. The channel had a 12 dB loss at 1GHz. The relative loss of the channel at 1GHz is 7 dB since the loss at dc is 5 dB. For a 2-Gb/s 2^{31}-1 random data sequence, the eye at the channel output was barely open (Fig. 4.14(a). The eye jitter improves by more than 60% (i.e. 47.9 ps vs. 15.8 ps) at the analog filter output (Fig. 4.14(b)). The filter consumed 39.6 mW from a 1.8-V supply (for the case of no peaking). As shown in Table 4.2, this is comparable to published designs in standard CMOS technologies although direct comparisons are difficult since each design accommodates different features and data rates.

4.4.5 Timing Recovery

An external loop was used to demonstrate the proposed TR scheme (Fig. 4.15). The design of this off-chip loop was explained in chapter 3. Two tests were conducted with

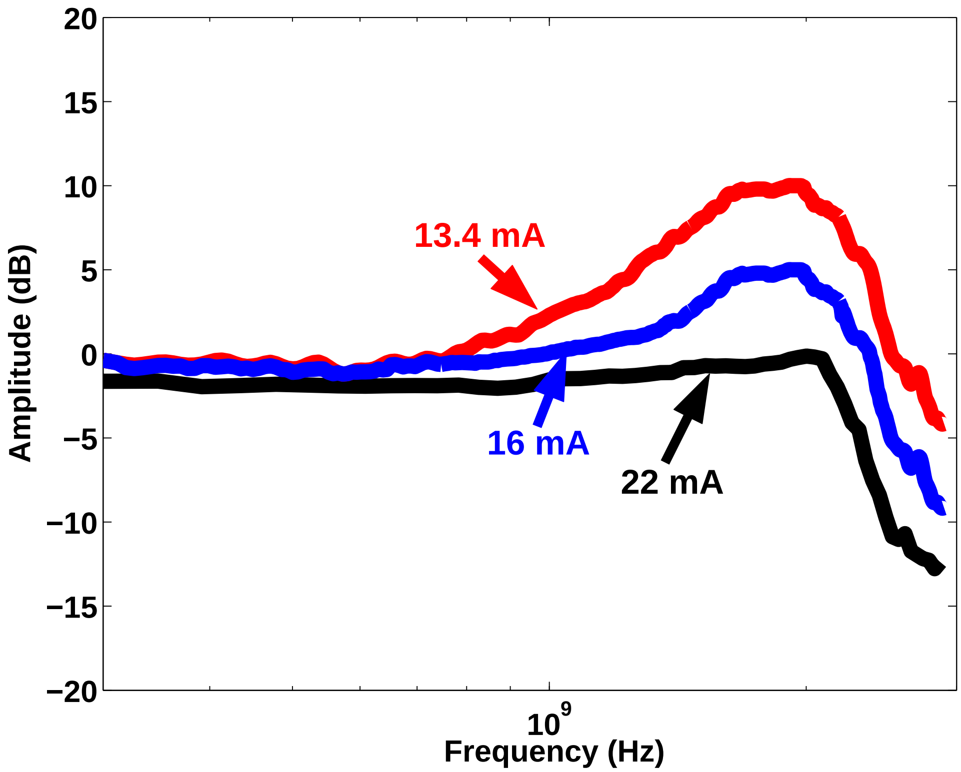


Figure 4.11: Peaking variation due to change in current in the dual-function analog filter.

a)

b)

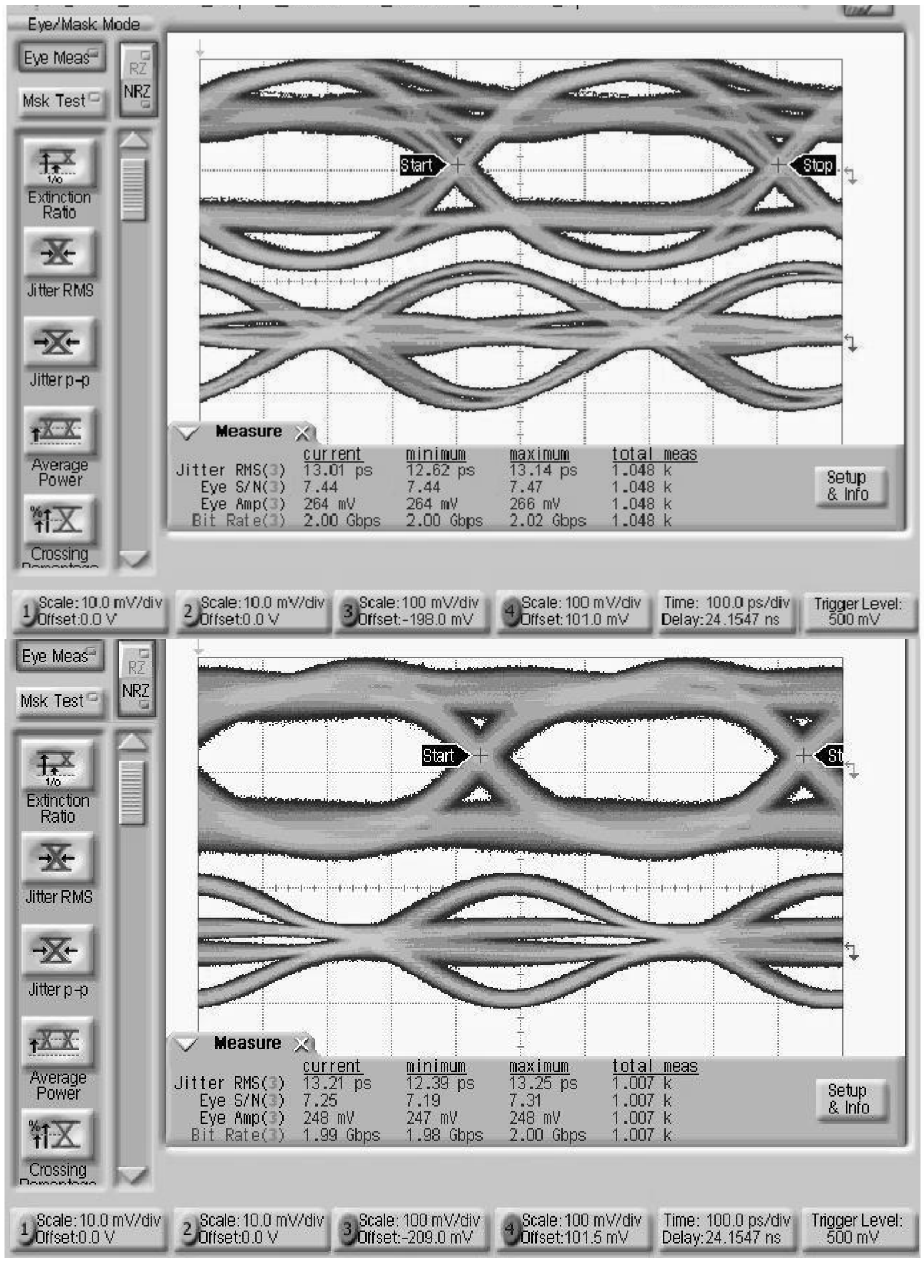


Figure 4.12: Effect of varying the current of the dual-function analog filter. (a) Data (top eye) and slope (bottom eye) outputs at 2-Gb/s (Vertical scale=100mV/div; Horizontal scale=100ps/div) for 13.4 mA current. (b) Data (top eye) and slope (bottom eye) outputs at 2-Gb/s (Vertical scale=100mV/div; Horizontal scale=100ps/div) for 22 mA current.

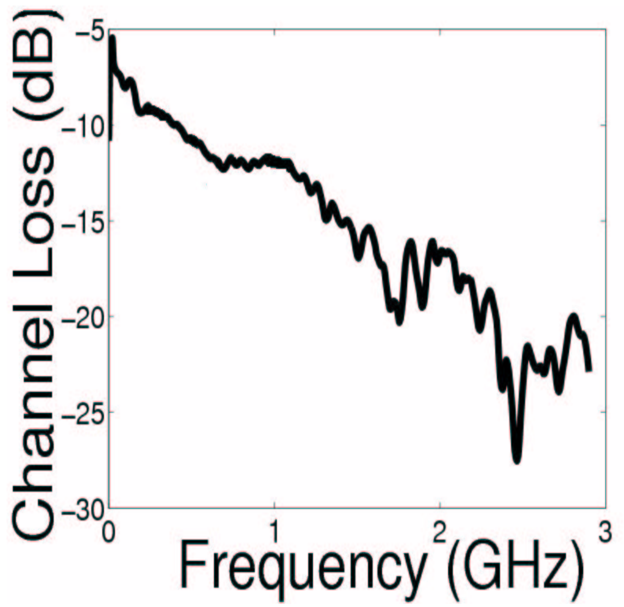


Figure 4.13: Frequency response of lossy channel.

the dual-function analog filter connected to the external timing recovery loop:
1) A PRBS $2^{31}-1$ was sent through a low loss coaxial cable and the filter current was adjusted to introduce peaking in the data eye output of the filter. This test was performed to verify that the proposed modified SSMMSE technique works for eyes that have peaking. Eye diagrams at different points of the TR loop are shown in Fig. 4.16. Fig. 4.16(a) shows the data and slope outputs with peaking in the data eye. Fig. 4.16(b) shows the mixer output which exhibits a baud-rate tone. Fig. 4.16(c) shows the recovered clock at 2 GHz with an RMS jitter of 6.5 ps.
2) A PRBS $2^{31}-1$ was sent through a lossy coaxial cable and the filter current was adjusted to equalize the lossy channel. This test was performed to show that the dual-function analog filter aided timing recovery scheme is capable of extracting a clock from a closed eye. Eye diagrams at different points of the TR loop are shown in Fig. 4.17. Fig. 4.17(a) shows the data input to the filter. Fig. 4.16(b) shows the data (top eye) and slope (bottom eye) output of the filter. Fig. 4.16(c) shows the recovered clock at 2 GHz with an RMS jitter of 9.7 ps.
Table 4.3 summarizes the performance of the TR scheme.

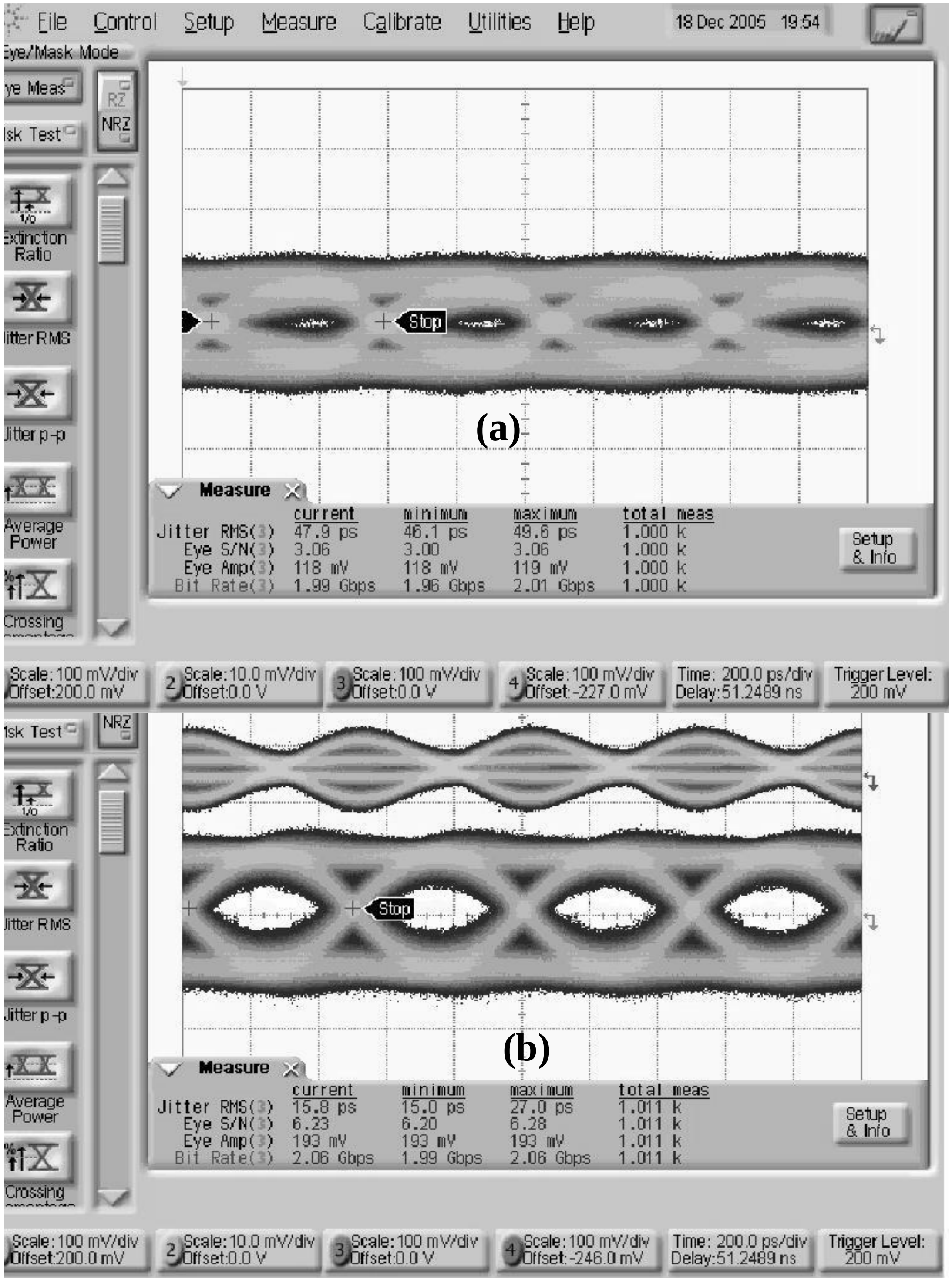


Figure 4.14: Linear equalization using the dual-function analog filter. (a) Output of lossy channel at 2-Gb/s (Vertical scale=100mV/div; Horizontal scale=200ps/div). (b) Data (bottom eye) and slope (top eye) outputs of dual-function analog filter at 2-Gb/s (Vertical scale=100mV/div; Horizontal scale=200ps/div)

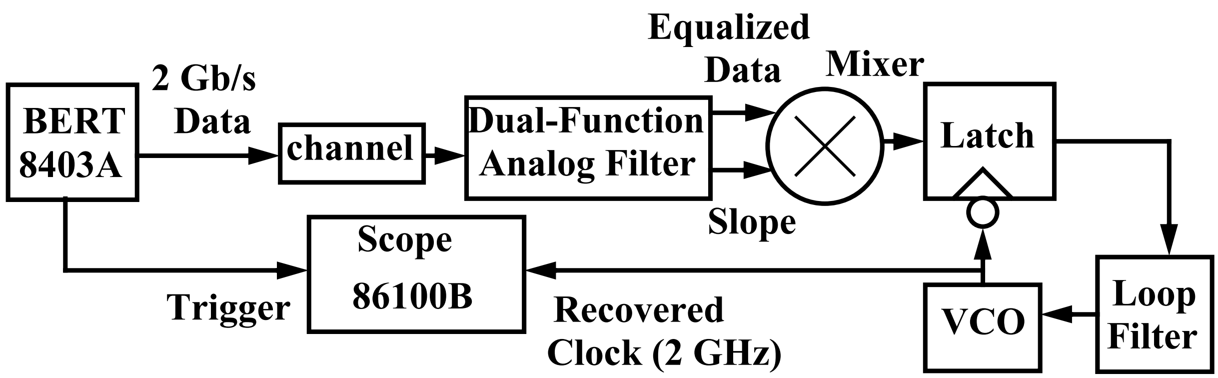


Figure 4.15: Test set up for external TR loop using the dual-function analog filter.

Table 4.3: Performance Summary & Comparison Table

Reference	Data Rate	Clock Freq.	Conditions	RMS Jitter
This work (Baud-rate)	2 Gb/s	2 GHz	Alternating data	2.6 ps
			2^{31}-1 PRBS; lossless channel	6.5 ps
			2^{31}-1 PRBS; lossy channel	9.7 ps
[13] (Baud-rate)	5 Gb/s	1 GHz	Random data; lossless channel	4.8 ps
[43] (Edge-sampled)	2.5 Gb/s	2.5 GHz	2^{23}-1 PRBS; lossless channel	17.4 ps

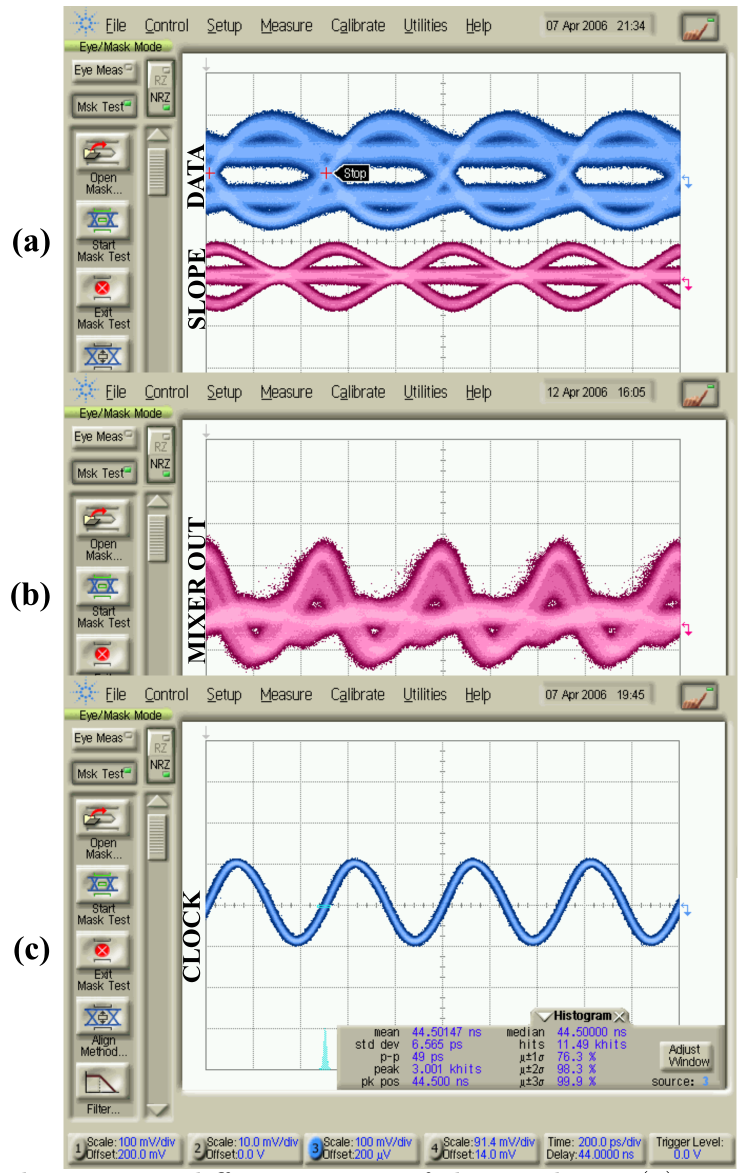


Figure 4.16: Eye diagrams at different points of the TR loop. (a) Data (top) and slope (bottom) outputs of dual-function analog filter at 2-Gb/s (Vertical scale=100mV/div; Horizontal scale=200ps/div), (b) Mixer output (Vertical scale=25mV/div; Horizontal scale=200ps/div), and (c) Recovered clock at 2-GHz (Vertical scale=100mV/div; Horizontal scale=200ps/div).

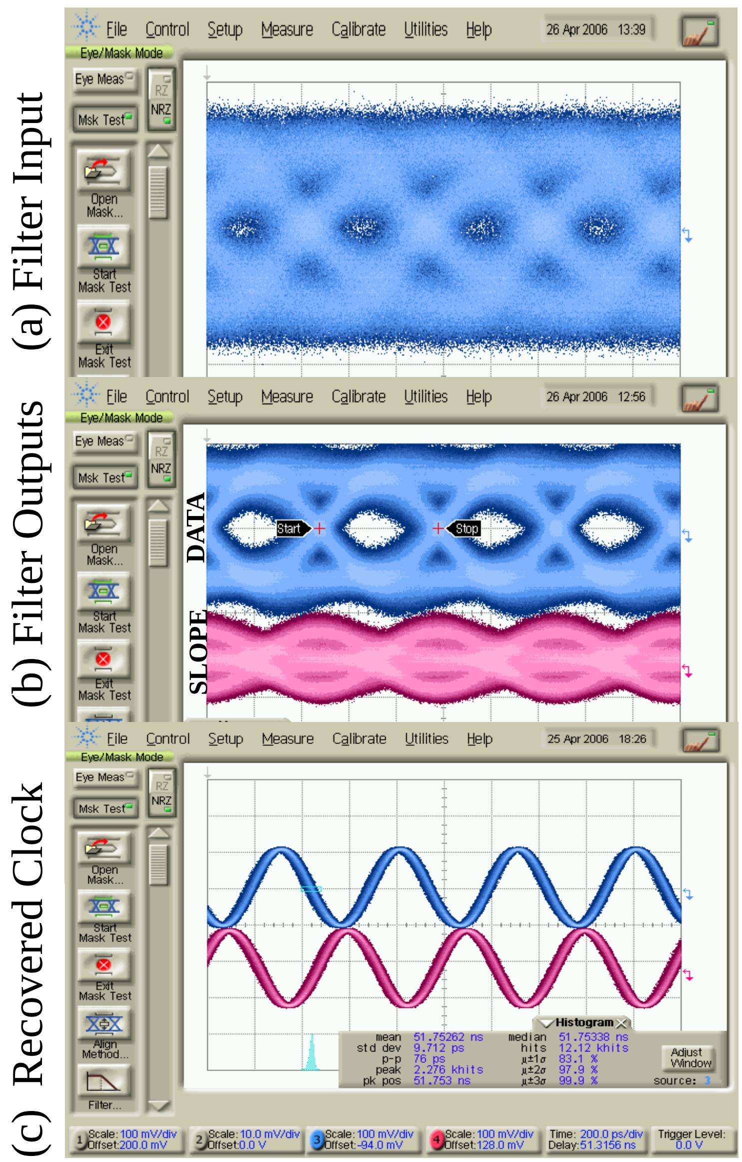


Figure 4.17: Eye diagrams at different points of the TR loop. (a) Channel output/filter input at 2-Gb/s (Vertical scale=25mV/div; Horizontal scale=200ps/div), (b) Equalized data (top) and slope (bottom) outputs of dual-function analog filter at 2-Gb/s (Vertical scale=25mV/div; Horizontal scale=200ps/div), and (c) Recovered clock at 2-GHz (Vertical scale=100mV/div; Horizontal scale=200ps/div).

4.5 Conclusion

This chapter presented a prototype dual-function analog filter that is capable of providing simultaneous lowpass and bandpass transfer characteristics. The bandpass transfer characteristic is utilized to provide the slope information and peaking in the lowpass path is introduced to perform linear equalization. To demonstrate the timing recovery concept, the prototype dual-function analog filter was used to recover a 2-GHz clock from a 2-Gb/s 2^{31}-1 random data sequence based on the modified MMSE criterion.

As a stand alone equalizer, the filter's performance is comparable to published prior art in 0.18μm CMOS. By recognizing that this filter architecture can also be used to perform the slope detection required for MMSE timing recovery, it can permit significant power savings in the TR loop.

Chapter 5

Conclusion

5.1 Summary and Future Work

High-speed baud-rate clock recovery techniques were studied in this thesis. Among the numerous clock recovery methods, edge-sampled CDRs are widely used in integrated circuits. Clock recovery without edge-samples or baud-rate clock recovery has the advantage of recovering the clock without sampling the edges of the incoming data and therefore, is hardware efficient and is an attractive alternative to edge-sampled CDRs.

Different baud-rate techniques were studied in chapter 1. In general, baud-rate techniques extract timing information (1) by monitoring specific input data patterns with an integrating front-end receiver (2) by comparing estimates of the pulse response (Mueller-Muller) or (3) by monitoring the error and slope information of the incoming data (MMSE). The first technique relies on specific patterns for extracting timing information whereas the second technique requires independent random data. MMSE timing recovery does not suffer from these issues and hence is an attractive candidate for competing with edge-sampled CDRs. However, the basic MMSE algorithm requires computation of the error signal as well as the slope, and this is performed in the digital domain by using a high-power ADC/DSP in magnetic-storage applications.

This work investigates possible solutions to the problems posed by MMSE CR when used in a high-speed serial link environment and thus develops a baud-rate scheme that is not constrained by the properties of the input data and also that does not require a power-hungry ADC/DSP. Called modified sign-sign MMSE (SSMMSE), the novel algorithm proposes the following changes to conventional MMSE: Firstly, it is shown that MMSE timing recovery can be performed for 2-PAM and 4-PAM without monitoring the error signal. Secondly, a continuous time approach to slope detection is proposed. Typically slope detection is done by using a two-tap FIR filter in magnetic-storage applications. But since the two tap FIR filter is only an approximation to the actual slope information, it leads to larger jitter in the recovered clock. Three slope detection architectures were briefly discussed in chapter 1: (1) Integrate and dump front-end based slope detector. (2) Passive filter based slope detector. (3) Active filter based slope detector.

Chapter 2 deals with the modeling and design of bang-bang CDRs. A sampling phase dependent probability density function (PDF) that is used to estimate the effect of intersymbol interference (ISI) and additive white noise on the characteristics of the phase detector (PD) in the CDR is developed. The PDF is modified to model an Alexander PD based CDR and a modified SSMMSE PD based CDR. Both analytical calculations and behavioral simulations predict that at equal loop bandwidths, the modified SSMMSE PD based CDR is superior to the Alexander PD based CDR at low channel bandwidths and low SNRs.

Chapter 3 presents a high-speed passive filter front-end for modified SSMMSE timing recovery. The filter provides simultaneous lowpass and highpass transfer characteristics to generate the data and its slope respectively. Slope detection is demonstrated at 10-Gb/s. The circuit is fabricated in a 0.18 μm CMOS process and consumes 21.6 mW from a 1.8V supply. As a proof of concept, the filter was used to extract a 2-GHz clock from a 2-Gb/s 2^{31}-1 random data sequence by using an external timing recovery loop. A half-rate modified SSMMSE PD based CDR architecture using the passive slope detector is proposed and compared with a conventional edge-sample CDR using identical circuit blocks. Simulations predict improved jitter performance for the proposed technique and similar power consumptions for the two techniques.

Chapter 4 presents a prototype dual-function analog filter that provides simultaneous lowpass and bandpass characteristics to generate the data and its slope respectively. Peaking is introduced in the lowpass data path to equalize a lossy channel. The timing recovery loop utilizes the equalized data and slope signals obtained from the dual-function analog filter to recover a clock based on a modified minimum mean squared error (MMSE) criterion. The filter was implemented in a 0.18-μm CMOS process and the maximum power consumption was 40 mW from a 1.8V power supply.

A comparison of the passive and active filters is given in Table 5.1.In general, PVT

Table 5.1: Comparison of passive and active filter based slope detectors

	Passive Filter	Active Filter
Power (1.8V Supply)	21.6 mW	24.12 mW (For Maximum Peaking) 40 mW (For No Peaking)
Speed (0.18 um CMOS)	Slope detection upto 10-Gb/s	Slope detection upto 3.4-Gb/s
Core Area	1.1 mm^2	0.4 mm^2
Other	-	Performs as a linear equalizer
Eye Quality	SNR=4.26 @ 10-Gb/s SNR=12.96 @ 2-Gb/s	SNR=4.64 @ 3.4-Gb/s SNR=7.25 @ 2-Gb/s

variations will degrade the gain and bandwidths in the data and slope paths of the passive filter.For the active filter, PVT variations will degrade the peaking frequency and peaking amplitude in the data and slope paths.

In short, the thesis demonstrates the use of passive and active filter front-ends to aid timing recovery. Power and area savings can be achieved (notably in the PD and VCO) by utilizing slope information from front-end filters without compromising the performance of the CDR.

Future work includes:

(1) Implementing a fully-integrated baud-rate CDR that utilizes the modified SSMMSE algorithm.

(2) Hardware demonstration using an integrate and dump front-end to aid the timing recovery loop.

Note that the major challenge in implementing a baud-rate CDR that utilizes the SSMMSE algorithm is the design of a high-speed slope detector. All other circuit blocks are identical to those used in typical edge-sampled CDRs.

The thesis pursues two options that address this issue. The first option is a high-speed passive filter. By using matching elements in the data and slope paths, a 10-Gb/s slope detector was designed, implemented and tested in 0.18 μm CMOS.

For applications where a linear equalizer is necessary, the linear equalizer can be configured as a slope detector. This is the second option pursued in the thesis. To demonstrate this concept, a dual-function analog filter was designed, implemented and tested in 0.18 μm CMOS.

5.2 Contributions of this work

The contributions of this work are as follows:

(1) This work proposes MMSE timing recovery as a potential baud-rate clock recovery scheme in high-speed serial links. A purely bang-bang type version of the MMSE technique that requires only the sign of the slope and sign of the data is developed (SSMMSE).

(2) This work presents a novel model that includes the effect of ISI and random noise in SSMMSE and Alexander type CDRs and shows that at large ISI and low SNRs, SSMMSE performs better than Alexander typs CDRs.

(3) This work demonstrates how a high-speed passive filter can be used to aid the timing recovery loop.

(4) This work demonstrates how a novel high-speed linear equalizer can be used to aid the timing recovery loop.

(5) This work also demonstrates that SSMMSE can be easily extended to 4-PAM CDRs and requires significantly less hardware than conventional Alexander type 4-PAM CDRs.

5.3 Publications arising from this thesis

The following is a list of publications based on this work:

<u>JOURNAL</u>

. F. Musa and A. Chan Carusone,"Modeling and Design of Multilevel Bang-Bang CDRs in the Presence of ISI and Noise,"IEEE Transactions on Circuits and Systems I: Regular Papers, October 2007.

. F. Musa and A. Chan Carusone, "A Baud-Rate Timing Recovery Scheme with a Dual Function Analog Filter," IEEE Transactions on Circuits and Systems II: Express Briefs, December 2006.

<u>CONFERENCE</u>

. F. Musa and A. Chan Carusone, "Clock recovery in high-speed multilevel serial links," IEEE International Symposium on Circuits and Systems, May 2003.

. F. Musa and A. Chan Carusone, “High-speed baud-rate clock and data recovery.,” IEEE ASICON 2007 (Invited Paper).

Paper to be submitted

. F. Musa and A. Chan Carusone, “A passive filter aided timing recovery scheme,” IEEE International Symposium on Circuits and Systems.

Appendix A

Joint PDF for the SSMMSE PD

A complete derivation of the joint PDF for the SSMMSE PD (i.e. Chapter2, Eq. (2.35)) is described in this Appendix:

For a noise-free SSMMSE PD, the joint PDF can be expressed as Eq. (2.34),

$$f_{Y_1S}(x,z) = \frac{1}{4^{m+1}} \sum_{q=1}^{4^{m+1}} \delta(x - c_{Y_1}(q))\delta(z - c_S(q)) \tag{A.1}$$

To determine the effect of Gaussian noise only, assume no signal is being applied to the CDR. Now assuming Gaussian noise with zero-mean is introduced at the receiver front-end, the noise in the slope paths and data paths will also be Gaussian with zero-mean. However, the noise power (i.e. σ^2) in these two paths will be different from each other since the transfer function in these two paths are different. Denoting the noise power in the data path by $\sigma_{Y_1}^2$ and that in the slope path by σ_S^2, the joint pdf can be expresed as [34],

$$f_{Y_1S}(x,z) = \frac{e^{-\frac{1}{2(1-\rho_{Y_1S}^2)}[(\frac{x}{\sigma_{Y_1}})^2 - 2\rho_{Y_1S}(\frac{x}{\sigma_{Y_1}})(\frac{z}{\sigma_S}) + (\frac{z}{\sigma_S})^2]}}{2\pi\sigma_{Y_1}\sigma_S\sqrt{1-\rho_{Y_1S}^2}} \tag{A.2}$$

Here ρ_{Y_1S} is the correlation coefficient function which is given as [34],

$$\rho_{Y_1S} = \frac{E[Y_1S] - E[Y_1]E[S]}{\sigma_{Y_1}\sigma_S} \tag{A.3}$$

Since the mean value of the Gaussian at any sampling phase is zero, hence $E[Y_1] = E[S] = 0$. Also $E[Y_1S] = R_{Y_1S}(0)$, where $R_{Y_1S}(0)$ denotes the cross correlation between Y_1 and S for a lag (or delay) of zero. Therefore,

$$\rho_{Y_1S} = \frac{E[Y_1S]}{\sigma_S\sigma_{Y_1}} = \frac{R_{Y_1S}(0)}{\sigma_S\sigma_{Y_1}} \tag{A.4}$$

Now the Gaussian noise Y_1 is wide sense stationary since its mean is constant (i.e. equal to zero) for all sampling phases and its autocovariance function, $C_{Y_1}(t_1, t_2) = E[Y_1(t_1)Y_1(t_2)] = E[Y(t_1)]E[Y(t_1)] = 0$ when $t_1 \neq t_2$, and $C_{Y_1}(t_1, t_2) = \sigma_{Y_1}^2\delta(t_1 - t_2)$ (i.e. autocovariance function depends on the delay between samples). If Y_1 is a wide-sense stationary process then its cross-correlation with its slope S can be expressed as ([34],pg369)

$$R_{Y_1S}(t_d) = -\frac{dR_{Y_1}(t_d)}{dt_d} \tag{A.5}$$

where t_d is the delay (or lag) between the Gaussian noise Y_1 and its slope, S and $R_{Y_1S}(t_d)$ is the auto-correlation function for Gaussian noise Y_1 for a delay of t_d. Substituting Eq. (A.5) in Eq. (A.3),

$$\rho_{Y_1S} = -\frac{R_{Y_1S}(0)}{\sigma_S\sigma_{Y_1}} = \frac{-1}{\sigma_S\sigma_{Y_1}}\frac{dR_{Y_1}(t_d)}{dt_d}|_{t_d=0} \tag{A.6}$$

$R_{Y_1}(t_d)$ is expressed as [34]

$$R_{Y_1}(t_d) = \int_{-\infty}^{\infty}[PSD_{Y_1}(f)]e^{j2\pi f t_d}\, df \tag{A.7}$$

where $PSD_{Y_1}(f)$ denotes the power spectral density of Y_1. Substituting Eq. (A.7) in Eq. (A.6) and simplifying,

$$\begin{aligned}
\rho_{Y_1S} &= -\frac{1}{\sigma_S\sigma_{Y_1}}\int_{-\infty}^{\infty} j2\pi f[PSD_{Y_1}(f)]\, df \\
&= \frac{\int_{-\infty}^{0} j2\pi f[PSD_{Y_1}(f)]\, df + \int_{0}^{\infty} j2\pi f[PSD_{Y_1}(f)]\, df}{-\sigma_S\sigma_{Y_1}} \\
&= \frac{-\int_{0}^{\infty} j2\pi f[PSD_{Y_1}(f)]\, df + \int_{0}^{\infty} j2\pi f[PSD_{Y_1}(f)]\, df}{-\sigma_S\sigma_{Y_1}} \\
&= 0.
\end{aligned} \tag{A.8}$$

Consequently, the Gaussian noise in the data path, Y_1 is uncorrelated to its slope, S at each sampling phase. Substituting $\rho_{Y_1S} = 0$ in Eq. A.2 the joint pdf for Gaussian noise and its slope can be expressed as,

$$f_{Y_1S}(x, z) = \frac{e^{-\frac{1}{2}[(\frac{x}{\sigma_{Y_1}})^2 + (\frac{z}{\sigma_S})^2]}}{2\pi\sigma_{Y_1}\sigma_S} \tag{A.9}$$

To obtain the combined effect of deterministic and Gaussian noise, Eq. (A.9) has to be convolved with Eq. (A.1). The result is the joint PDF for the SSMMSE PD:

$$f_{Y_1S}(x, z) = \frac{1}{4^{m+1}(2\pi\sigma_{Y_1}\sigma_S)}\sum_{q=1}^{4^{m+1}} e^{-\frac{1}{2}[(\frac{x - c_{Y_1}(q)}{\sigma_{Y_1}})^2 + (\frac{z - c_S(q)}{\sigma_S})^2]} \tag{A.10}$$

For the joint PDF to be valid, it must satisfy the following conditions:
1)The area under the joint PDF must be unity:

$$\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} f_{Y_1S}(x,z)\,dx\,dz = 1. \tag{A.11}$$

2) Integrating the joint PDF with respect to one variable from $-\infty$ to $+\infty$, results in the PDF of the other variable:

$$\int_{-\infty}^{\infty} f_{Y_1S}(x,z)\,dz = f_{Y_1}(x) \tag{A.12}$$

$$\int_{-\infty}^{\infty} f_{Y_1S}(x,z)\,dx = f_S(z) \tag{A.13}$$

Substituting Eq. (A.10) into the left hand side of Eq. (A.11):

$$\begin{aligned}
\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} f_{Y_1S}(x,z)\,dx\,dz &= \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \frac{1}{4^{m+1}(2\pi\sigma_{Y_1}\sigma_S)}\sum_{q=1}^{4^{m+1}} e^{-\frac{1}{2}[(\frac{x-c_{Y_1}(q)}{\sigma_{Y_1}})^2+(\frac{z-c_S(q)}{\sigma_S})^2]}\,dx\,dz \\
&= \frac{1}{4^{m+1}(2\pi\sigma_{Y_1}\sigma_S)}\sum_{q=1}^{4^{m+1}} \int_{-\infty}^{\infty} e^{-(x-c_{Y_1}(q))^2/(2\sigma_{Y_1}^2)}\,dx \int_{-\infty}^{\infty} e^{-(z-c_S(q))^2/(2\sigma_S^2)}\,dz \\
&= \frac{1}{4^{m+1}(2\pi\sigma_{Y_1}\sigma_S)}\sum_{q=1}^{4^{m+1}} \sqrt{2\pi}\sigma_{Y_1}\sqrt{2\pi}\sigma_S = \frac{1}{4^{m+1}(2\pi\sigma_{Y_1}\sigma_S)}[4^{m+1}(2\pi\sigma_{Y_1}\sigma_S)] = 1.
\end{aligned} \tag{A.14}$$

where $\int_{-\infty}^{\infty} e^{-(x-c_{Y_1}(q))^2/(2\sigma_{Y_1}^2)}\,dx = \sqrt{2\pi}\sigma_{Y_1}$ and $\int_{-\infty}^{\infty} e^{-(z-c_S(q))^2/(2\sigma_S^2)}\,dz = \sqrt{2\pi}\sigma_S$ [34]. Substituting Eq. (A.10) into the left hand side of Eq. (A.12):

$$\begin{aligned}
\int_{-\infty}^{\infty} f_{Y_1S}(x,z)\,dz &= \int_{-\infty}^{\infty} \frac{1}{4^{m+1}(2\pi\sigma_{Y_1}\sigma_S)}\sum_{q=1}^{4^{m+1}} e^{-\frac{1}{2}[(\frac{x-c_{Y_1}(q)}{\sigma_{Y_1}})^2+(\frac{z-c_S(q)}{\sigma_S})^2]}\,dz \\
&= \frac{1}{4^{m+1}(2\pi\sigma_{Y_1}\sigma_S)}\sum_{q=1}^{4^{m+1}} e^{-(x-c_{Y_1}(q))^2/(2\sigma_{Y_1}^2)} \int_{-\infty}^{\infty} e^{-(z-c_S(q))^2/(2\sigma_S^2)}\,dz \\
&= \frac{1}{4^{m+1}(2\pi\sigma_{Y_1}\sigma_S)}\sum_{q=1}^{4^{m+1}} e^{-(x-c_{Y_1}(q))^2/(2\sigma_{Y_1}^2)}\sqrt{2\pi}\sigma_S \\
&= \frac{1}{4^{m+1}}\sum_{q=1}^{4^{m+1}} \frac{1}{\sqrt{2\pi\sigma_{Y_1}^2}} e^{-(x-c_{Y_1}(q))^2/(2\sigma_{Y_1}^2)} = f_{Y_1}(x)
\end{aligned} \tag{A.15}$$

where $\int_{-\infty}^{\infty} e^{-(z-c_S(q))^2/(2\sigma_S^2)}\,dz = \sqrt{2\pi}\sigma_S$ [34]. Eq. (A.13) can be proved in a similar fashion.

Appendix B

Inductor Models for passive filter

1nH and 0.75nH spiral inductors were used in the passive filter (Refer to Chapter 3, Fig. 3.1). Physical dimensions of the inductors are provided in Table B.1. Fig. B.1 shows the equivalent circuit for the inductor. Equivalent circuit parameters for the two inductors are given in Table B.2. Fig. B.2 plots L(f) and Q(f) for for both inductors.

Table B.1: Physical dimensions of inductors used in passive filter

Property	L_1 inductor in Fig. 3.1	L_2 inductor in Fig. 3.1
No. of sides	8	8
Metal width	6 um	6 um
Spacing	4 um	4 um
radius	70 um	60 um
Number of turns	2.7	2.7
metal layer	metal 6	metal 6

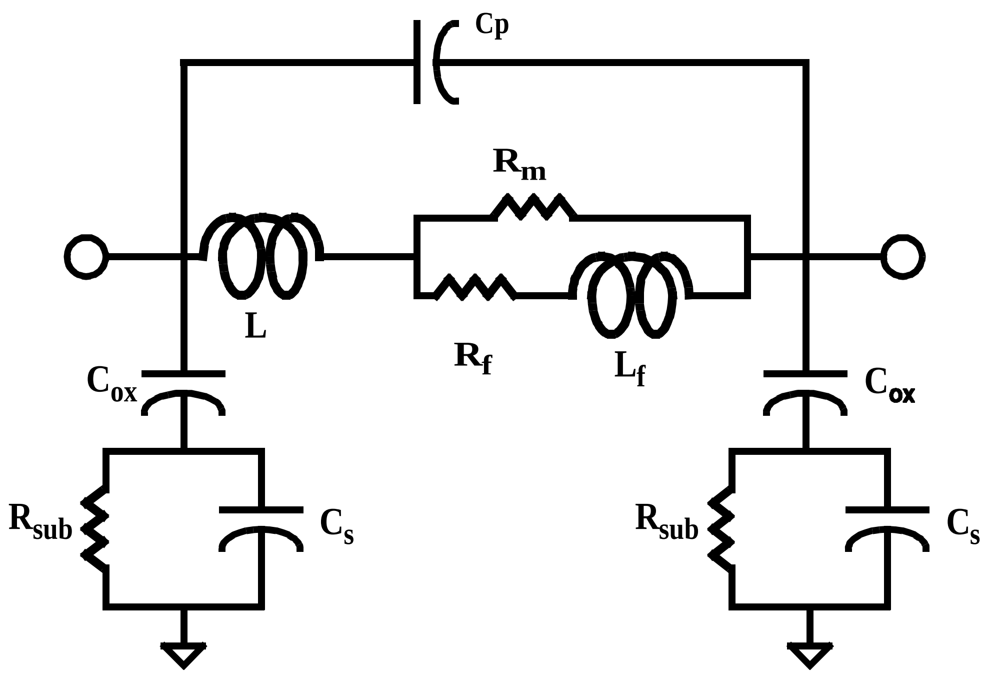


Figure B.1: Equivalent circuit for inductors used in the pasive filter.

Table B.2: Equivalent Circuit Parameters for 1nH and 0.75nH Inductors

Equivalent Circuit Parameter	L_1 inductor (Fig. 3.1)	L_2 inductor (Fig. 3.1)
L	0.97 nH	0.726 nH
R_m	6.38 Ω	5.17 Ω
L_f	10 pH	10 pH
R_f	153 Ω	124 Ω
C_{ox}	0.439 fF	0.356 fF
C_{s1}	1.19 pF	1.14 pF
C_p	10fF	10 fF
R_{sub}	884 Ω	917 Ω

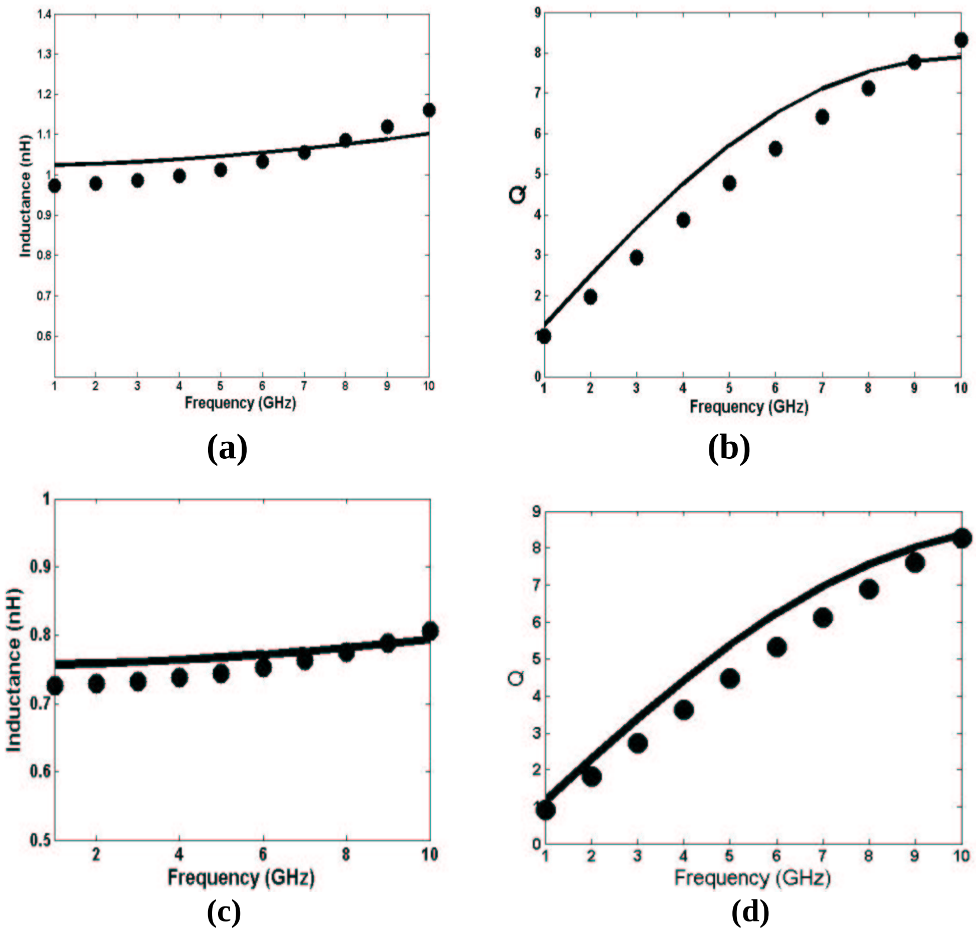


Figure B.2: PLots of L(f) and Q(f). (Dots=equivalent circuit model; line=ASITIC) (a) L(f) vs. frequency for L_1 (Fig. 3.1). (b) Q(f) vs. frequency for L_1 (Fig. 3.1). (c) L(f) vs. frequency for L_2 (Fig. 3.1). (d) Q(f) vs. frequency for L_2 (Fig. 3.1).

Appendix C

AD8343 Mixer Matching Network

Fig. C.1 shows the input output matching network and connection diagram for the AD8343 mixer that was used in the external CDR loop. The input and output matching networks were designed by uploading the S-parameter files from the ADI webpage into Cadence and then by following the procedure outlined in the AD8343 mixer spec. sheet. Fig. C.2 shows the S11 and S22 plots for the mixer.

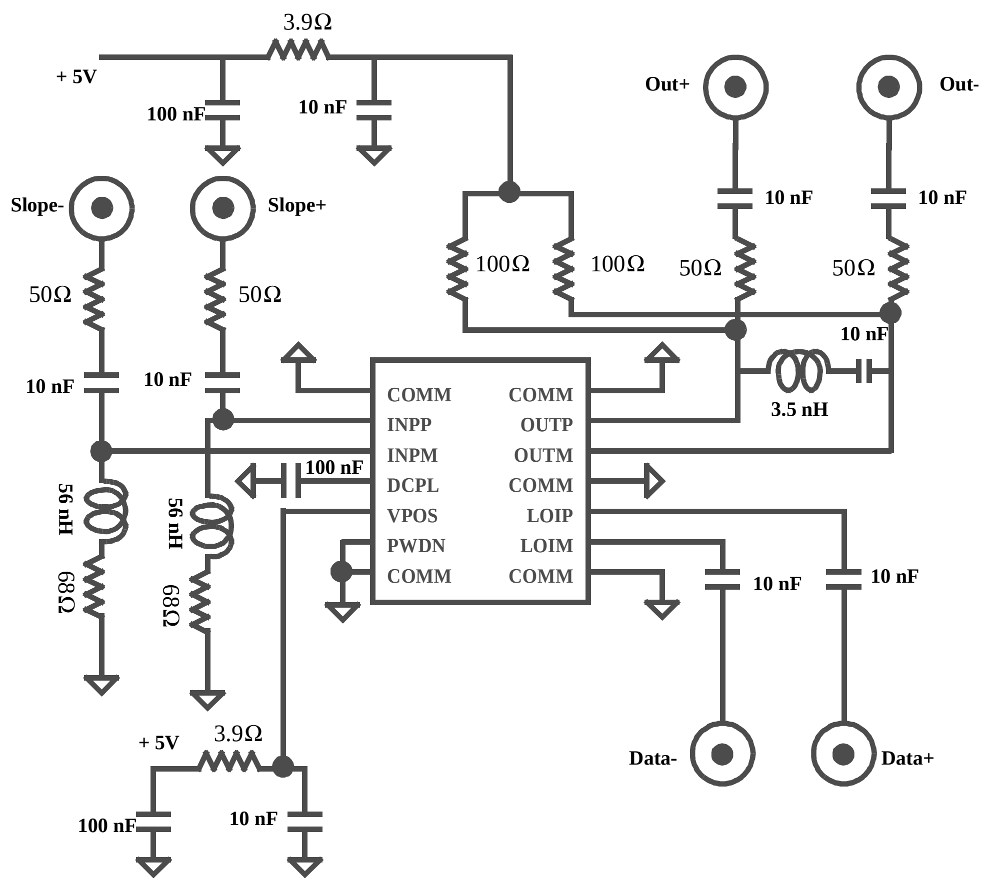


Figure C.1: AD8343 connection diagram.

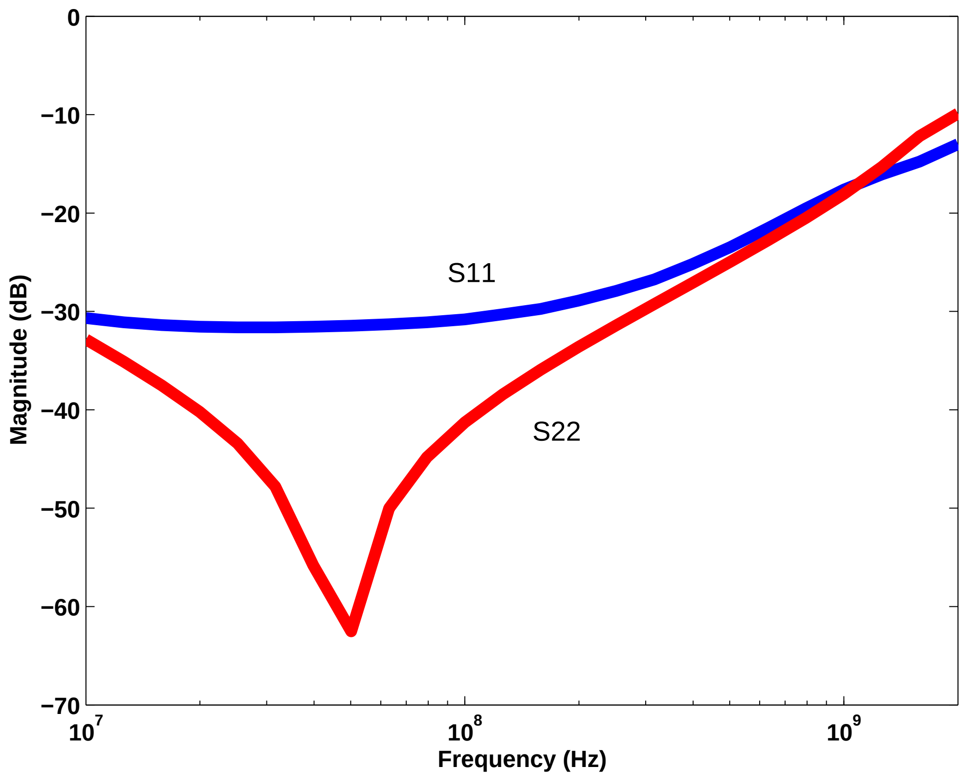


Figure C.2: Plots of S11 and S22 for the AD8343 with input and output matching networks.

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