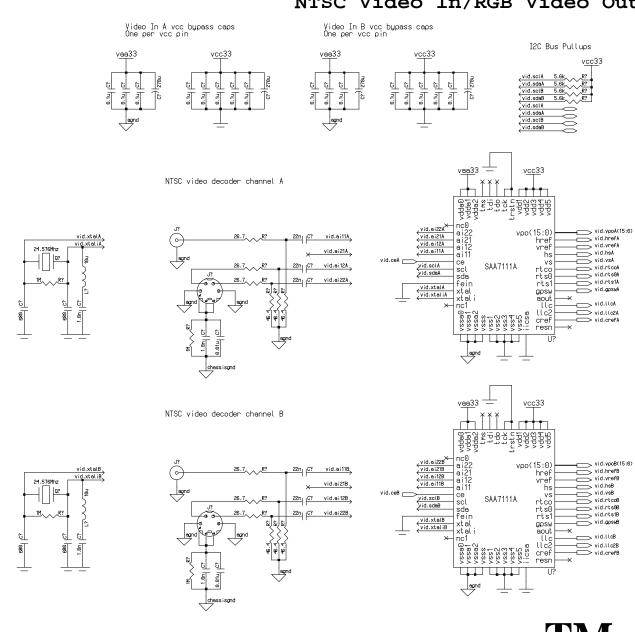
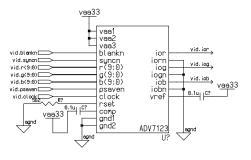
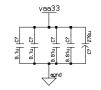
NTSC Video In/RGB Video Out

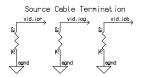


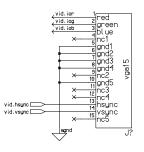
RGB Video Out Inputs Require 3.3v TTL Signals



Place Bypass Cap At Each Vaa

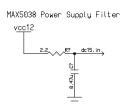


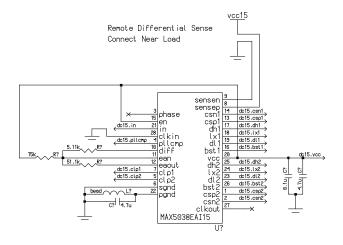


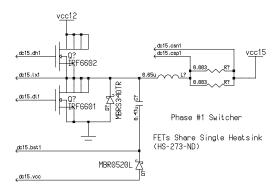


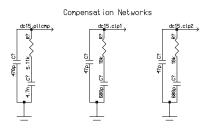
JESTEROE atod Toytenity

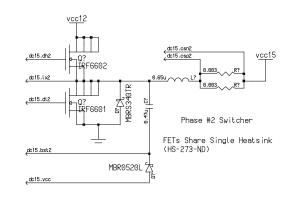
DC-DC Converter (1.5v 50A)

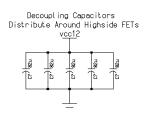


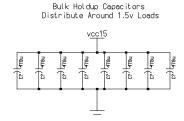








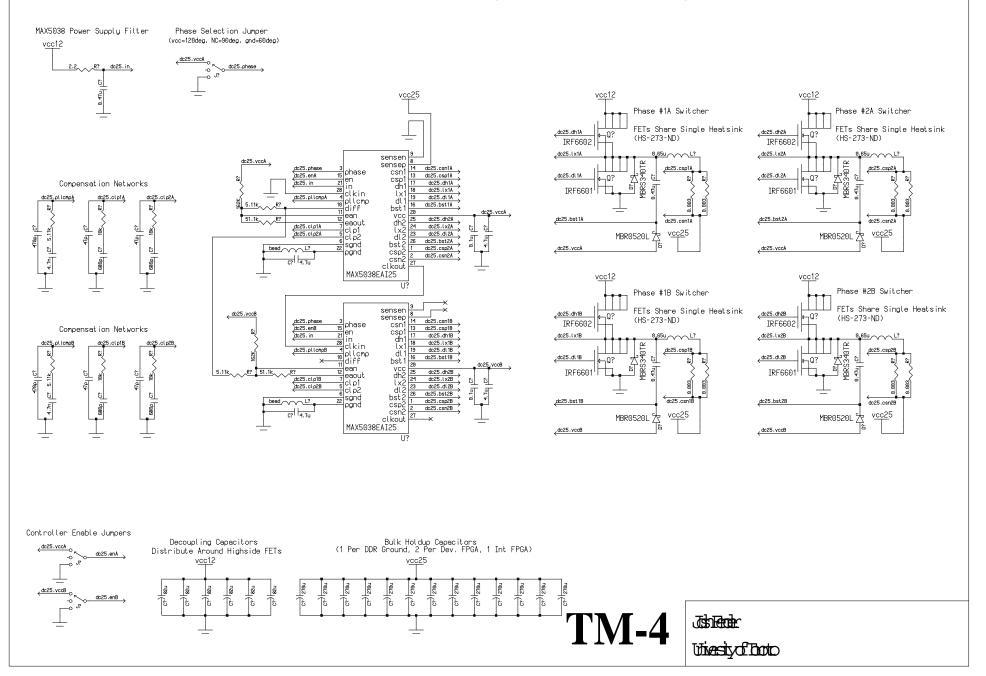


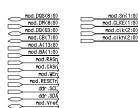


TM-4

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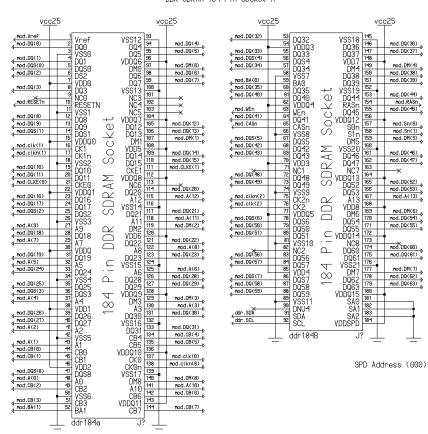
DC-DC Converter (2.5v 100A Peak)





DDR Module Sockets

DDR SDRAM 184 Pin Socket A



TM-4

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DDR Termination Regulator / Clock Buffer / Termination



mod.Sh(1:0)
mod.clk(2:0)
mod.clk(2:0)
mod.clk(2:0)
mod.clk(2:0)
mod.DM(8:0)
mod.M(13:0)
mod.RASh
mod.CASh
mod.CASh
mod.RESETh

Differential Clock Series Termination

_mod.clk(0)	18	R?	ddr.clk(0)
mod.clkn(0)	18,		ddr.clkn(0)
mod.clk(1)	18	, , R?	ddr.clk(1)
mod.clkn(1)	18		ddr.clkn(1)
mod.clk(2)	18,	, , R?	ddr.clk(2)
mod.clkn(2)	18	,	ddr.clkn(2)
•	_ 18_ ~	, , R?	,
	<u></u>	X R?	>
	~~	~ —	`

Termination Regulator

LP2995M

VSense

SPD Bypass Caps

AVin PVin

nc gnd

Vref Bypass Caps

SSTL-2 Series Termination

mod.DQ(0)	18	R?	ddr.DQ(0)	mod.DQS(0)	18,	√ <u>R</u> ?	ddr.DQS(0)
nod.DQ(1)	18,~	XR?	ddr.DQ(1)	nod DQS(1)	18,~	XR?	ddr.DQS(1)
nod DQ(2)	18,~	XR?	ddr.DQ(2)	nod DQS(2)	18,	XR?	ddr.DQS(2)
nod.DQ(3)	18,~,	XR?	ddr.DQ(3)	mod.DQS(3)	18,	X R?	ddr.DQS(3)
nod.DQ(4)	18,~	XR?	ddr.DQ(4)	nod DQS(4)	18,	XR?	ddr.DQS(4)
nod.DQ(5)	18,~,	×,R?	ddr.DQ(5)	mod.DQS(5)	18,	X.R?	ddr.DQS(5)
nod.DQ(6)	18,~,	X.R?	ddr.DQ(6)	mod.DQS(6)	18,	X.R?	ddr.DQS(6)
mod.DQ(7)	18,~	X R?	ddr.DQ(7)	mod.DQS(7)	18	XR?	ddr.DQS(7)
mod.DQ(8)	18,~	XR?	ddr.DQ(8)	mod.DQS(8)	18	R?	ddr.DQS(8)
nod DQ(9)	18,~	V.R?	ddr.DQ(9)	mod .DM(0)	18,	X.R?	ddr DM(0)
mod.DQ(10)	18,~		ddr.DQ(10)	mod .DM(1)	18.	R?	ddr.DM(1)
mod.DQ(11)	18	√.R?	ddr.DQ(11)	mod DM(2)	18	. `.R?	ddr DM(2)
mod.DQ(12)	18.~.		ddr.DQ(12)	mod.DM(3)	18.~	R?	ddr DM(3)
nod .DQ(13)	18.~	V.R?	ddr.DQ(13)	mod DM(4)	18.~		ddr DM(4)
nod.DQ(14)	18.	V.R?	ddr.DQ(14)	mod DM(5)	18.	V_R?	ddr DM(5)
mod.DQ(15)	18	V _{R?}	ddr .DQ(15)	mod.DM(6)	18.	\	ddr .DM(6)
mod.DQ(16)	18.	R?	ddr.DQ(16)	nod DM(7)	18.	√R?	ddr DM(7
nod .DQ(17)	18.	V.R?	ddr .DQ(17)	mod DM(8)	18,	√. <u>R?</u>	ddr .DM(8)
nod .DQ(18)	18.	V.R?	ddr DQ(18)	mod.CB(0)	18.	\ <u>R?</u>	ddr CB(0)
nod .DQ(19)	18.	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	ddr.DQ(19)	mod.CB(1)	18	\\ <u>R?</u>	ddr.CB(1
nod.DQ(20)	18.~	V.R?	ddr .DQ(20)	mod.CB(2)	18.	\\ <u>R?</u>	ddr CB(2)
mod.DQ(21)	18.	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	ddr .DQ(21)	mod.CB(3)	18.	\\ <u>R?</u>	ddr .CB(3)
mod.DQ(22)	18.	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	ddr.DQ(22)	mod.CB(4)	18,~	\\ <u>\\\</u> ?	ddr.CB(4)
mod.DQ(23)	18	V.R?	ddr.DQ(23)	mod.CB(5)	18.~	\^ <u>R?</u>	ddr (CB(5)
nod .DQ(24)	18	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	ddr .DQ(24)	mod.CB(6)	18	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	ddr.CB(6
mod.DQ(25)	-18.~	✓ <u>R?</u>	ddr.DQ(25)		-18.~	\R?	ddr CB(7
			ddr.DQ(26)	nod CB(7)		✓ <u>R?</u>	ddr.AK9
mod .DQ(26) mod .DQ(27)	- <u>18</u> ~	√ R? R?		mod.A(0)	- <u>18</u> ~	✓ <u>R?</u>	
nod.DQ(28)	-18 _~ ~	✓ <u>R?</u>	ddr.DQ(27)	mod.A(1)		V.R?	ddr.A(1
mod.DQ(29)		√ <u>R?</u>	ddr.DQ(29)	mod.A(3)	18_~	√ <u>R?</u> - R?	ddr.A(3
nod DQ(30)		VR?_	ddr.DQ(30)	mod.A(4)			ddr.A<4
nod DQ(31)		√ <u>k?</u>	ddr .DQ(31)	mod.A(5)		V. R?	ddr.A(5
nod.DQ(32)	18_~>	<u>~₽?</u>	ddr.DQ(32)	mod.A(6)	18_~~		ddr.A<6
mod .DQ(33)		√ <u>R?</u>	ddr.DQ(33)	mod.A(7)	18_~	V_R?_	ddr.A<7
nod .DQ(34)		V.R?_	ddr.DQ(34)	nod.A(8)	18_~>	V.R?	ddr.A(8
nod DQ(35)	18_~>	<u> </u>	ddr.DQ(35)	mod.A(9)	18_~~	V_R?_	ddr.A(9
mod DQ(36)	18_~	<u> </u>	ddr.D0(36)	mod A(10)	18	√ <u>R?</u>	ddr.A<10
mod.DQ(37)	18~~	Ÿ <u>₹?</u>	ddr.DQ(37)	mod.A(11)	18	√ <u>R?</u>	ddr.AK11
nod.DQ(38)	18_~>	Ÿ <u>₽?</u>	ddr.DQ(38)	mod.A(12)	18		ddr.A<12
nod.DQ(39)	18_~_	<u> </u>	ddr .DQ(39)	nod.A(13)	18		ddr.A<13
mod.DQ(40)	18	<u> </u>	ddr .DQ(40)	nod BA(0)	18	<u>√R?</u>	ddr BA(0
nod DQ(41)	18	VR?_	ddr DQ(41)	nod.BA(1)	18		ddr.BA(1
mod.DQ(42)	18		ddr .DQ(42)	nod RASn	18		ddr RAS
mod.DQ(43)	18		ddr.DQ(43)	nod.CASn	18	√ <u>R?</u>	ddr.CAS
mod.DQ(44)	18		ddr DQ(44)	nod WEn	18	√ <u>R?</u>	ddr.WE
mod.DQ(45)	18		ddr.DQ(45)	nod RESETn	18	√_ <u>R?</u> _	ddr .RESETi
mod.DQ(46)	18		ddr.DQ(46)	nod.Sn(0)	18	<u>√R?</u>	ddr.Sn(0
mod.DQ(47)	18		ddr.DQ(47)	mod.Sn(1)	18	√ <u>R?</u>	ddr.Sn(1
mod.DQ(48)	18		ddr.DQ(48)	mod.CLKE(0)	18	√ <u>R?</u>	ddr ، CLKE(0
mod.DQ(49)	18		ddr.DQ(49)	nod CLKE(1)	18	√ <u>R?</u>	ddr.CLKE(1
mod.DQ(50)	18		ddr.DQ(50)	•	<u>, 18</u> ~	~ <u>^</u> R?_	,
mod.DQ(51)	18,		ddr.DQ(51)		18,	<u> </u>	è
nod.DQ(52)	18,~	XR?	ddr.DQ(52)		<u>_ 18</u> _ ,	XR?	2
mod.DQ(53)	18	XR?	ddr.DQ(53)		18	XR?	,
mod.DQ(54)	18	XR?	ddr .DQ(54)		× 18 ×	XR?	
mod.DQ(55)	18	XR?	ddr.DQ(55)		718	V 27	,
mod.DQ(56)	18~	XR?	ddr.DQ(56)		×~	√ ¨	`
mod.DQ(57)	18~	V_R?	ddr .DQ(57)				
mod.DQ(58)	18~	XR?	ddr.DQ(58)				
mod DD(59)	-18 [~]	V 27	ddr .00(59)				

SSTL-2 Parallel Termination Place After Last Socket

		Place	After Last Socket	1 1 61 2 161111
Ð Ð	←ddi	vtt	← ddr.vtt	← ddr.vtt
Ð	mod.DQ(0)	47		0.1u ₁ [C
Þ	mod.DQ(1)	47\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	mod.DQS(1) 47 R?	0.1u C
Ð	mod.DQ(2)	47. R?	mod.DQS(2) 47 R?	0.1u C
Ð	mod.DQ(3)	47 R?	mod.DQS(3) 47 R?	0.1u C
Ð	mod .DQ(4)	47 R?	mod.DQS(4) 47, , ,R?	0.10 0
₽ ₽	mod.DQ(5)	47, R?	mod.DQS(5) 47 R?	0.1u C
ν Đ	mod.DQ(6)	47, R?	mod.DQS(6) 47 R?	0.1u C
v Þ	mod.DQ(7)	47 R?	mod.DQS(7) 47 R?	0.1u C
Đ	mod.DQ(8)	47 R?	mod.DQS(8) 47 R?	[0.1u C
b	mod.DQ(9)	47 R?	mod.DM(0) 47 R?	0.1u C
Þ	mod .DQ(10)		mod.DM(1) 47 R?	0.1u C
Þ	mod.DQ(11)		mod.DM(2) 47 R?	[0.1u C
Þ	mod.DQ(12)	47 × R?	mod.DM(3) 47 R?	0.1u C
Þ	mod .DQ(13)	47 R?	mod.DM(4) 47 R?	0.1u C
Ð	nod .DQ(15)	47~~~ R?	mod.DM(6) 47 R?	0.10 0
₽	mod .DQ(16)	47~~^\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	mod.DM(7) 47 R?	0.1u C
Ð	mod.DQ(17)	47. \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	mod.DM(8) 47, R?	0.1u C
Þ	mod.DQ(18)	47 R?	mod.CB(0) 47 R?	0.1u C
Ð	mod.DQ(19)	47 R?	mod.CB(1) 47 R?	0.1u C
Þ	mod.DQ(20)	47 R?	mod.CB(2) 47, R?	0.1u C
Đ Đ	mod .DQ(21)	47 R?	mod.CB(3) 47 R?	0.1u C
o D	mod.DQ(22)	47 R?	mod.CB(4) 47 R?	0.1u C
v D	mod.DQ(23)	47, R?	mod.CB(5) 47 R?	[0.1u C
b	mod.DQ(24)	47 R?	mod.CB(6) 47 R?	0.1u C
Þ	mod.DQ(25)	47 R?	mod.CB(7) 47 R?	[0.1u C
Þ	mod.DQ(26)	47 × R?	mod.A(0) 47 R?	I 0.1u C
Ď	mod.DQ(27)	47 V R?	mod.A(1) 47 R?	0.1u C
Þ	mod.DQ(28)	47 × R?	mod.A(2) 47 R?	0.1u C
Ð	mod.DQ(39)	47.00 R?	mod.A(4) 47 R?	0.1u C
₽	mod.DQ(31)	47~~~R?	mod.A(5) 47 R?	0.1u C
Þ	mod.DQ(32)	47\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	mod.A(6) 47 R?	0.1u C
Ð	mod.DQ(33)	47 R?	mod.A(7) 47 R?	0.1u C
Þ	mod.DQ(34)	47 R?	mod.A(8) 47, R?	0.1u C
Þ Þ	mod .DQ(35)	47 R?	mod.A(9) 47, AR?	0.1u C
D D	mod.DQ(36)	47 R?	mod.A(10) 47 R?	0.1u C
Þ	mod.DQ(37)	47 R?	mod.A(11) 47 R?	[0.1u C
b	mod.DQ(38)	47 × R?	mod.A(12) 47 R?	0.1u C
,	mod.DQ(39)	47 × R?	mod.A(13) 47 R?	0.1u C
•	mod .DQ(40)	47 × R?	mod.BA(0) 47 R?	0.1u C
•	mod .DQ(41)	47 R?	mod.BA(1) 47 R?	0.1u C
•	mod .DQ(42)	47 × R?	mod.RASn 47 R?	0.1u C
Þ	mod.DQ(44)	47	mod.WEn 47. R?	0.10
Þ	mod.DQ(45)	17\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	nod RESETN 47 R?	0.1u C
Ð	mod.DQ(46)	17\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	mod.Sn(0) 47 R?	0.1u C
Þ	mod .DQ(47)	47. R?	mod Sn(1) 47 R?	0.10 0
	mod .DQ(48)	47 R?	mod.CLKE(0) 47 R?	0.10 0
	mod .DQ(49)	47, R?	mod.CLKE(1) 47 R?	0.1u C
	mod .DQ(50)	47 × R?	417 V R?	0.1u C
	mod.DQ(51)	47 R?	√47 ∧ ∧ R?	[0.1u C
	mod.DQ(52)	47 × R?	<u>17</u> √√ R?	[0.1u C
	mod.DQ(53)	47 × R?	<u>^47</u>	0.1u C
	mod .DQ(54)	47 × R?	₹ 17 ₹ 7	0.1u C
	mod.DQ(55) mod.DQ(56)	47 R?	× 47 VVR?	0.1u C
	mod .DQ(57)	47. R?		0.1u C
	nod.DQ(58)	47.00 R?		0.10 0
	mod.DQ(59)	47 R?		0.1u C
	mod.DQ(60)	47\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\		+ 31104
	mod.DQ(61)	47. R?		
	mod .DQ(62)	47 R?		
	mod.DQ(63)	47 R?		
	·	-~~—		

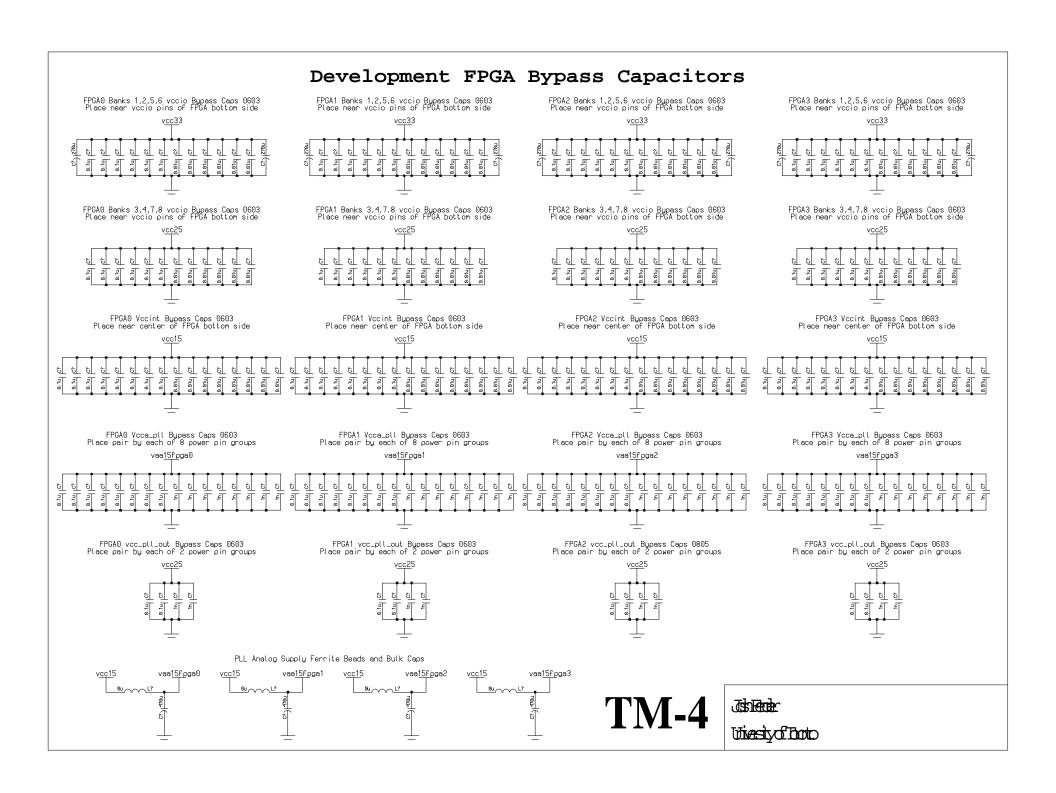
SSTL-2 Termination Bypass 1 Per 2 Termination Res

Тор	Leve	lΡ	orts
ddr	.clk(2:	3)	
ddr	.clkn(2	:0)	\equiv
, ddr	.Vref		=
ddr	SCL		=
ddr	SDA		=
ddr	.DQS(8:	θ)	\asymp
ddr	.DM(8:0		=
ddr	.DQ(63:	0) [
ddr	.CB<7:0		=
ddr	.A(13:0	, i	=
ddr	.BA<1:0	` `	=
ddr	.Sn(1:0)]	=
ddr	.CLKE(1	:0) ີ	
. ddr	.RASn		~
ddr	.CASn	_	
	WEn	_	\cong
ddr	RESETn	_	ightharpoons
		$\overline{}$	~

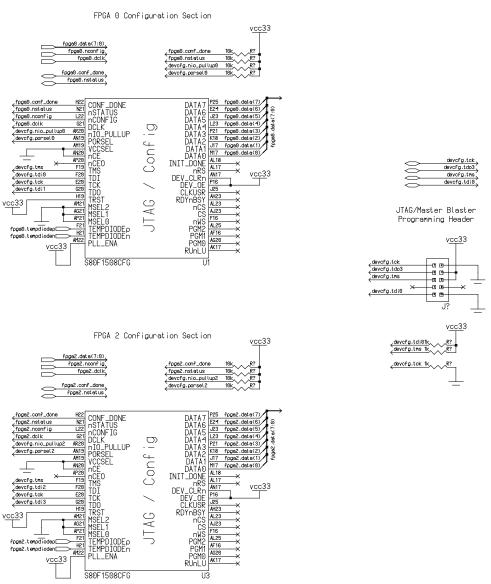
Termination Resistor's Values Are Placeholders Pending Board Level Simulation

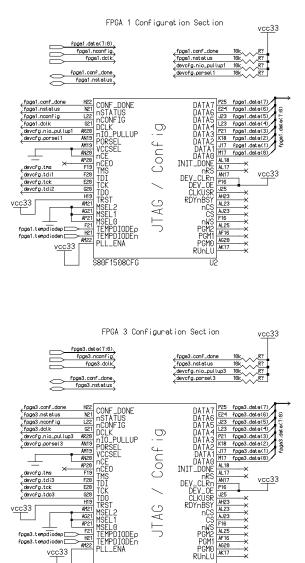
TM-4

Jastenier Vinasity of Tooto



Development FPGA Configuration



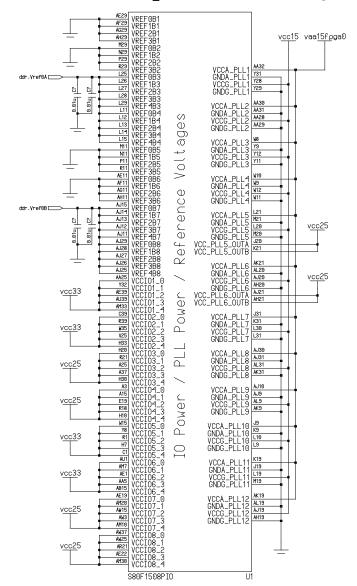


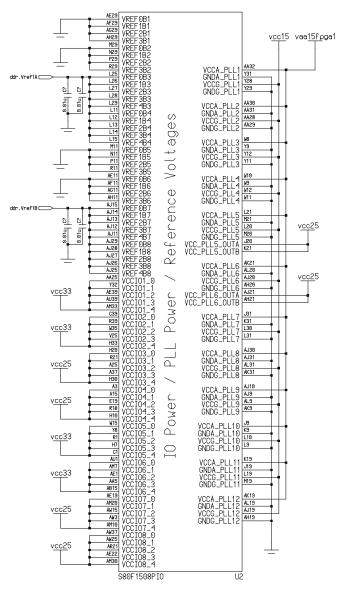
TM-4

Jahrenir Vivasiyof Tooto

S80F1508CFG

Development FPGAs 0, 1 IO/PLL Power & References

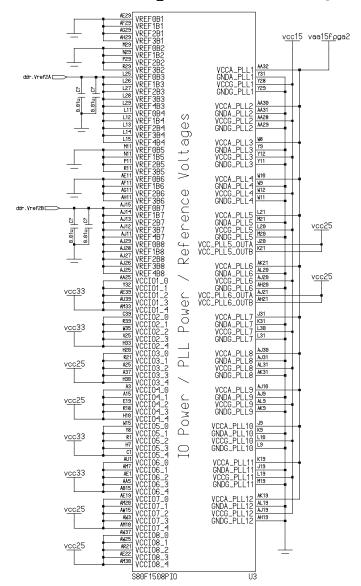


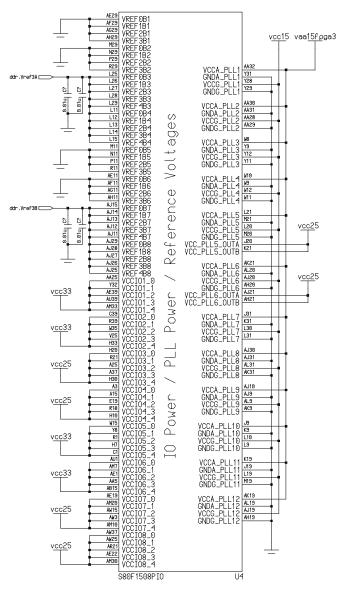


TM-4

Jishedir Vivasiyof Booto

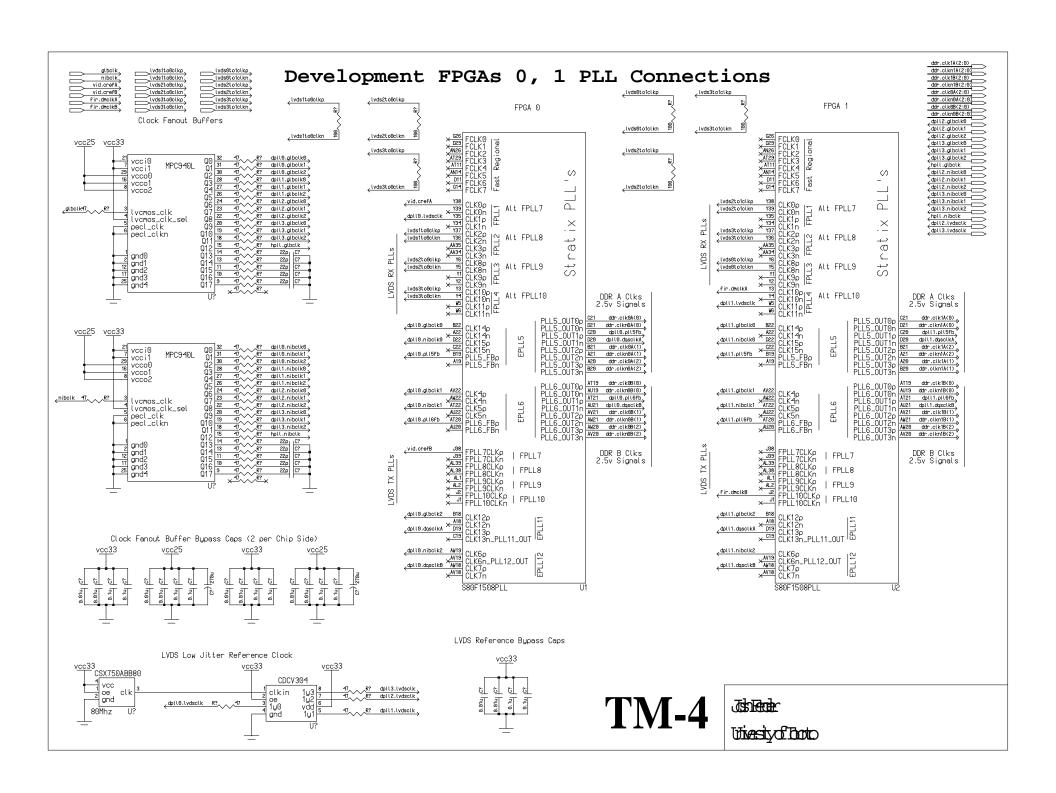
Development FPGAs 2, 3 IO/PLL Power & References

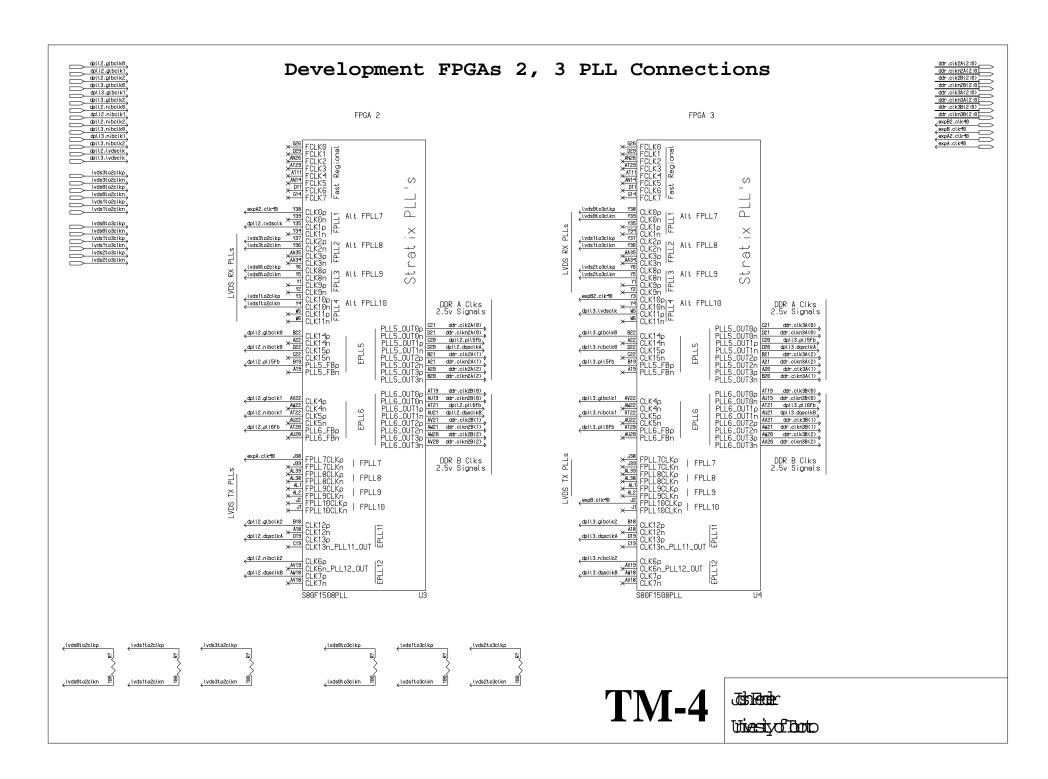


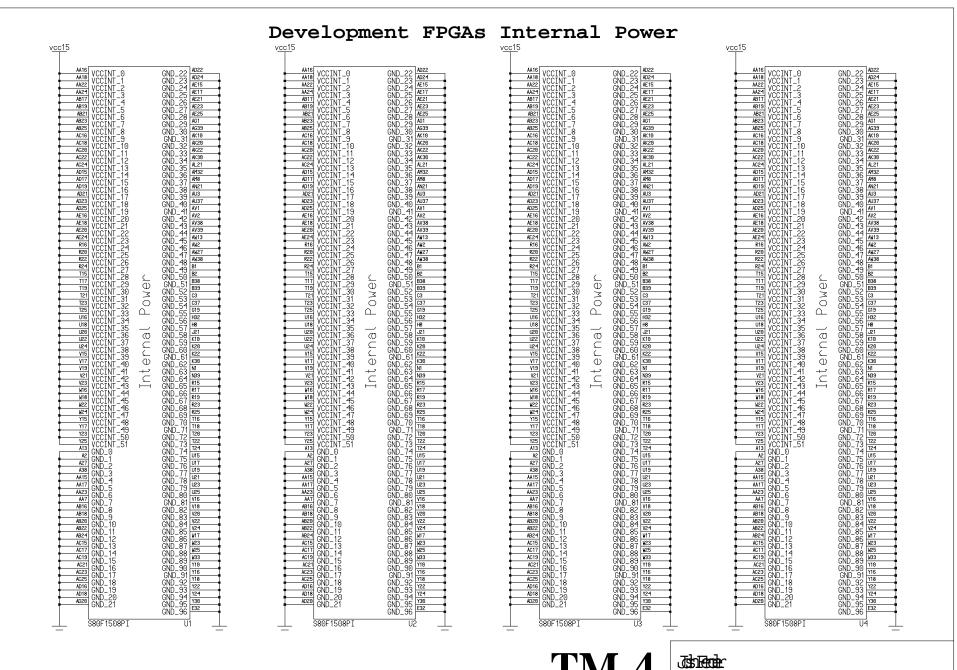


TM-4

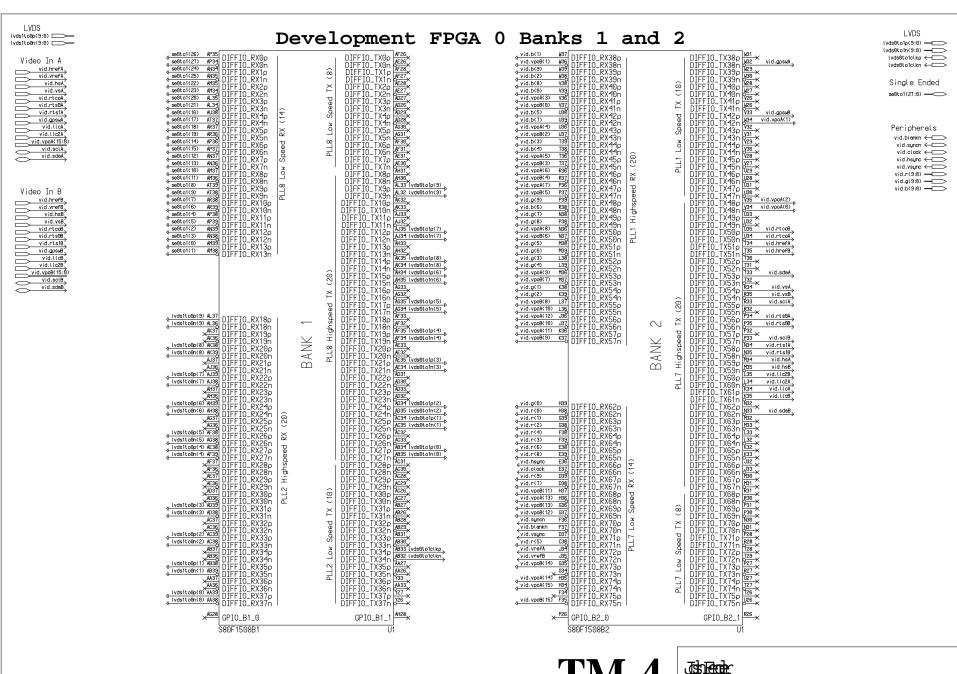
Jishedir Vivasiyo Tiboto







CHOOL TO VIEWILL



CHOOL DO TENATA

Development FPGA 0 Banks 3 and 4

GPI0_B3_67 75 2 debug0(1) → GPI0_B3_68 (2) → GPI0_B3_68 (2) → GPI0_B3_68 (2) → GPI0_B3_71 (2) → GPI0_B3_71

DQ5T0
DQ5T1
DQ5T2
DQ5T3
DQ5T3
DQ5T4
DQ5T4
DQ5T5
DQ5T5
DQ5T5
DQ5T6

DQ5T6 DQ5T7 DQ5T7 DQS5T DQS5T

DQGT0 B25 ddr.D08A(32) → DQGT1 D25 ddr.D08A(37) → DQGT2 D26 ddr.D08A(37) → DQGT3 DQGT3 DQGT4 C26 ddr.D09A(38) → DQGT4 D

DQ6T5 DQ6T6 DQ6T6 DQ6T6 DQ6T7 DQ6T7 DQS6T

B27 ddr.DQ9A(40)

| DQ7T0 | B27 | ddr. D08A(46) | DQ7T1 | C27 | ddr. D08A(46) | DQ7T2 | B27 | ddr. D08A(41) | DQ7T3 | B27 | ddr. D08A(41) | DQ7T3 | B27 | ddr. D08A(41) | DQ7T4 | A88 | ddr. D08A(42) | DQ7T6 | B28 | ddr. D08A(42) | DQ7T6 | B28 | ddr. D08A(47) | DQ7T7 | C28 | ddr. D08A(47) | DQ7T7 | C28 | ddr. D08S8A(5) |

DQ8T0 DQ8T1 DQ8T1 DQ8T2 DQ8T2 C29 ddr.DQ8A(53) DQ8T3 A30 ddr.DQ8A(52) DQ8T4 A31 ddr.DQ8A(52) A31 ddr.DQ0A(55) DQ8T5 DQ8T6 B31 ddr.DQ0A(51) DQ8T6 DQ8T7 B30 ddr.DQ0A(50)

| DOSTO | M32 | ddr. | D00A(68) | D03T1 | G32 | ddr. | D00A(67) | D03T2 | A32 | ddr. | D00A(75) | D03T2 | A34 | ddr. | D00A(63) | D03T4 | A33 | ddr. | D00A(63) | D03T4 | G33 | ddr. | D00A(63) | D03T6 | G34 | ddr. | D00A(63) | D03T6 | G34 | ddr. | D00A(53) | D03T7 | B33 | ddr. | D00SA(53) | D03T7 | B33 | ddr. | D00SA(57) | D0SST

RDN3 M24 ×

B30_ddr.DQS0A(6)

ddr.BA0A(1) E21 GPIO_B3_0
ddr.BA0A(1) 622 GPIO_B3_1
debugθ(2) J22
NP2 GPIO_B3_2

ddr.A0A(0) debug9(7) G23 ddr.A9A(10) F22 debug9(19) H23 ddr.DM0A(8) × F23 ddr.BA0A(0) × F24 debug9(13) G24 debug9(14) K24 debug@(15) H24 ddr .DM0A(4) F25

_ debug@(16) J24

debugg(17) G25 debug@(18) H25

_ddr.RASn0A × N25 debug9(19) 627

ddr.A0A(13) E29

ddr.CASn0A × F28 ddr.Sn0A(0) F29

debuge (22) D31 GP

debug@(23) J26 debug@(24) K26

debug9(32) G29 ddir .DMOA(7) D33

_ debug@(33) H29

debug@(34) G30 debug@(35) J28

| debug@(26.628 GPT0.B3.47 | debug@(27.032 GPT0.B3.48 | debug@(27.032 GPT0.B3.49 | debug@(28.027 GPT0.B3.50 | debug@(30.027 GPT0.B3.51 | debug@(30.027 GPT0.B3.52 | debug@(30.027 GPT0.B3.52 | debug@(30.027 GPT0.B3.53

debug@(36) K28 debug@(37) F31 GPIO_B3_62 GPIO_B3_63 GPIO_B3_63 ### GPIU_B3_63 ### GPIU_B3_64 ### GPIU_B3_65 ### GPIU_B3_65 ### GPIU_B3_65 ### GPIU_B3_66 ×P23 RUP3

S80F1508B3

debug@(20) K25 debug@(21) H26 , ddr.DM0A(6) D30 M25 N26 Addr. WEn8A F27

| 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000 | 000



Nibble Bus dev0.nib(49:0) ----

DDR SDRAM Bank A

ddr.WEn8A	ddr WEn
ddr.clk0A(2:0)	ddr.clk(2:0)
ddr.SDA9A	ddr.SDA
ddr.clkn0A(2:0)	ddr.clkn(2:0)
ddr.DM0A(8:0)	ddr.DM(8:0)
ddr.DQS8A(8:0)	ddr.DQS(8:0)
_ ddr.Vref0A	ddr.Vref
ddr .RASn0A	ddr RASn
ddr.CASn0A	ddr.CASn
ddr.Sn0A(1:0)	ddr Sn(1:0)
ddr.BA0A(1:0)	ddr.BA(1:0)
ddr.DQ0A(63:0)	ddr DQ(63:0)
ddr.A0A(13:0)	ddr.A(13:0)
ddr.CB0A(7:0)	ddr.CB(7:0)
ddr.CLKE0A(1:0)	ddr.CLKF(1:0)
_ ddr .RESETn0A	ddr.RESETn
ddr.SCL8A	ddr.SCI
`	ddi 100L

debug0(38:1)

Logic Analyzer Connector

	MIC	TOR	38	
, debug@(1)	1		^	debug9(2)
debug@(3)	17		5	debug9(4)
debug9(5)] 2		7	debug9(6) (
debug9(7)] 7		8	debug9(8)
debug@(9)] 6		10	debug@(10)
debug9(11)	3 5 7 9		24 68 D Z	debug@(12)
debug9(13)			14	debug0(14) (
debug9(15)	13 15		16	debug@(16)
debug8(17)	147		16 18	debug@(18) (
debug9(19)	19		20	debug0(20)
debug9(21)	0.4		20	debug0(22)
debug9(23)	55		54	debug0(24)
`debud9(25)	155		25	debug0(26)
debug@(27)	23 25 27 29 31 33 35 37		246862468 246862468	debug0(28) (
debug9(29)	154		20	debug0(30)
debug9(31)	51		22	debug0(32)
debug9(33)	32		24	debug0(34)
debug9(35)	135		36	debug0(36) (
debug9(37)	337		20	debug0(38)
`				
	11 gg gg	345 11	T gnd4	J?
	Ц	++		
		_		

down.nib(2)	(4) (2) (3) (3)
down.nibt2 DH CPTO_B4_1 CPTO_B4_12 CITX	(6) (4) (2) (3) (3)
	(4) (2) (3) (3)
	(4) (2) (3) (3)
GP10_B4_75 FFE	(2) b
GP10_B4_6	(2) b
GP10_B4_6 GP10_B4_7 GP10_B4_8 GP10	(2) b
49976-Intb(8) Fig. GP10_B4_7 GP10_B4_78 JIS 49076-Intb(8) Fig. GP10_B4_8 Fig. GP10_B4_8 Fig. GP10_B4_8 GP10_B4_8 Fig.	(2) b
	(2) →
GP10_B4_80 E16 GP10_B4_9	
GP10_B4_82 Mi8 × GP10_B4_11 GP10_B4_82 Mi8 × GP10_B4_81 Mi8 × M	ib(23).
GP10_B4_82 Mi8 × GP10_B4_11 GP10_B4_82 Mi8 × GP10_B4_83 Mi8 × GP10_B4_85 Mi8 × M	ib(23).
	ib(23).
GP10_B4_84 SIB	ib(23).
GP10_B4_85 M9 × M9	ib(23).
\$\frac{\text{dev6.nib(17)}}{\text{dev6.nib(18)}} = \frac{\text{GF10.B4.15}}{\text{GF10.B4.17}} \ \text{GF10.B4.85} \ \text{Fig. \text{Fig. SF10.B4.89}} \ \text{HI GF10.B4.18} \ \text{GP10.B4.88} \ \text{HI GF10.B4.89} \ \text{Viii GF10.B4.19} \ \text{dev6.nib(21)} \ \text{GF10.B4.19} \ \text{GP10.B4.29} \ \text{dev6.nib(21)} \ \text{BG GF10.B4.29} \ \text{GP10.B4.29} \ \text{Qev6.nib(21)} \ \text{BG GF10.B4.29} \ \text{Qev6.nib(22)} \ \text{BG GF10.B4.29} \ \text{Qev6.nib(23)} \ \text{BG GF10.B4.23} \ \text{DQ071 B6 Gev6.n} \ \text{Gev6.nib(24)} \ \text{BG GF10.B4.23} \ \text{DQ071 B6 Gev6.n} \ DQ071 B6 G	ib(23).
Age	ib(23).
GP10_B4_18 F20	ib(23).
GPIO_B4_90	ib(23).
dev0.nib(21) 55 GPIO_B4_21 dev0.nib(22) B4 GPIO_B4_22 D00T0 66 dev0.nib(24) 42 GPIO_B4_22 D00T0 66 dev0.nib(24) 42 GPIO_B4_23 D00T1 66 dev0.nib(24) 42 GPIO_B4_23 D00T1 67 GPIO_B4_23 D00T	ib(23).
dev0.nib(21) 55 GPIO_B4_21 dev0.nib(22) B4 GPIO_B4_22 D00T0 66 dev0.nib(24) 42 GPIO_B4_22 D00T0 66 dev0.nib(24) 42 GPIO_B4_23 D00T1 66 dev0.nib(24) 42 GPIO_B4_23 D00T1 67 GPIO_B4_23 D00T	ib(23).
GPIO_B4_27	ib(23).
deve.nib(24)	
K12 GPIO_B4_24 DQUT2 C7 deve.n	
ddc 404/11) ~ F10 UT 1U-U*1-4" UUU 41/2 doub c	ib(26)
	ib(27)
ddr.A9A(1) F10 GPT0_B4_25	
dev0.nib(30) H11 GPIO_B4_26 DQ0T4 A6 dev0.nib(32) G11 GPIO_B4_27 DQ0T5 A8 dev0.n	nib(31)
AGRICATION BA 28 I DON'T BE TO GET IN THE COLUMN BA 28	iib(33)
deve.nib(34) A4 GPIO_B4_29 ☐ DQ0T7 B8 deve.n	
K13 GPIO_B4_29 DQS0T B7 deve.n	ib(36)
dev0.nib(37)	
dev6.nib(38) J13 GPIO_B4_32	
2 2 2 2 2 2 2 2 2 2	
deve.nib(39) ↑ H12 GPIO_B4_34 ✓ DQ1T2 A9 ddr.DQ0A	
ddr.A0A(9) F11 GPIO_B4_35 DQ1T3 C11 ddr.D00A	
Web Color	(5)
4 de 191/12 519 GPIO_B4_37 DQ1T5 119 dd1.5000	
GPIO_B4_38 DQ1T6 Rt1 ddn DQ0A	
august 18 cal 6F10_B4_39	
	~~ >
	(9)
4 pva / o pad GPTU_B7_72	
dor.DMGA(9) L9 GPTO_B4_43 dev0.nib(43) GT3 GPTO_B4_44 DQCT1 L12 ddr.DMGA((8)
down.hb(43) 613 6710_B4_44 DQZT2 E12 6th-10080 ddr. 10080 ddr. 10080 ddr. 10080 ddr	
K14 GPIO_B1_13 GPIO_B4_46 DQ2T4 B12 ddr.D00A/	13)
ddr.DMoA(2) F13 GPIO_B4_47 DQ2T5 813 ddr.D00A(2) 445 DQ2T5 613 ddr.D00A(2)	11)
	14)
M13 GPIO_B1_10 D02T7 D13 ddr_D00A(15)
A GOT CLEEN (U) EII CDIO D4 EG DOCCI CIZ GOT DUSON	(1)
GPI0 B4 51	401
× 1 GPI0_B4_53 DQ3T1 1 DQ3T1	
40 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
	18)
	22)
1 DI 1 B4 5/ DI 1 S 5	23)
* M15 GPTO_B4_58	19)
ddr.A0A(7) G15 GPIO_B4_59 DQ3T7 DQS3T C15 ddr.DQS0A	
4 DQS3T DQS3T	
×P15 GP10_B4_61	24)
dev0.nib(48) × 16 GPT0_B4_62 DQ4T0 D16 ddr.D004X	29)
K16 CPTO B4 65 D04T3 B16 ddr.D00AK	28)
ddr.A0A(8) C16 GPIO_B4_66 DQ4T4 B17 ddr.DQ0A(1	26)
4 deve nib(49) Hi6 CDTO D4 C7 D04TE D1/ ddr.DUBAC	27)
N16 CDTO D4 CO DO4TE E17 ddr.DQ0AC	
P17 GPIO_B4_70 DQS4T C16 ddr.DQS9A	(3)
$\times \frac{\text{F15}}{\text{RUP4}}$ RUP4 RDN4 $\frac{\text{E16}}{\text{E16}} \times$	
S80F1508B4 U1	
2801 JARA UJ	

JEST HETCHE University of Thorto LVDS

\(\text{Vds2to0p(19:0)} \)
\(\text{Vds2to0p(19:0)} \)
\(\text{Vds3to0p(19:0)} \)
\(\text{Vds3to0p(19:0)} \)

Development FPGA 0 Banks 5 and 6

Self-03(9) Fig.	BANK 5 PLL10 Highspeed TX (28) PLL10	To Pi2
Vide31.09(0)		
S80F1508B5		U1

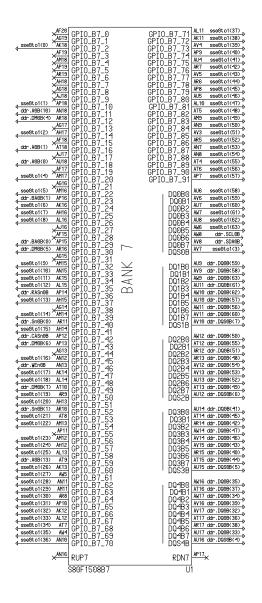
,	Daliv	.B	and	LO		
		DIFFIO_RX11 DIFFIO_RX11 DIFFIO_RX11 DIFFIO_RX11 DIFFIO_RX11 DIFFIO_RX11 DIFFIO_RX11	40		DIEETO TV1140	AA6 se0to2(40)
	[vds2to0n(13) AA2 [vds2to0p(18) AA3	DIFFIU_KAII	Z₽		DIFFIO_TX114p	AB7 se0to2(42)
		Kteetn-bûii	5".		DIFFIO_TX114n DIFFIO_TX115p	AA8 se0to2(60)
	lvds2to0n(18) AA4	DIFFID PX11	551		Interio TX1150	AA9 se0to2(26)
	[vds2to0p(12) AB2	DIFFIO RX11	Šn l	6	DIFFIO TX1160	AA10 se0to2(51)
	lvds2to0n(12) AB1	DIFFIO RX11	6n	(10)	DIFFIO TX116p	AA11 se0to2(34)
	lvds2to0p(17) AB3	DIFFIO RX11	70	~	DIFFIO TX1176	AA13 se0to2(44)
	lyds2to0n(17) AB4	DIFFIO_RX11	ŻĥΙ	₽	DIFFIO_TX117n	AA12 se0to2(53) AB9 se0to2(59)
	[vds2to0p(11) ACT	DIFFIO_RX11	80	D	DIFFIO_TX118p	AB9 se0to2(59) AB8 se0to2(58)
	[vds2to0n(11) AC2 [vds2to0p(16) AC3	DIFFIO_RX11	8n	Speed	DIFFIO_TX118n	AB8 se0to2(58) AB11 se0to2(56)
	lvds2to0n(16) AC4	DIFFIO_RX11	9ρ	δ	DIFFIO_TX119p	AB10 se0to2(49)
	Lyde2t oBo(1B) AD1	DIFFIO_RX11	9n	7	DIFFIO_TX119n	AB12 se0to2(61)
		D1FF10_RX12	[Qp]	Low	DTFFT0_TX150b	AB13 se0t o2(29)
	[vds2to0n(10) AD2 [vds2to0p(19) AD3	DIFF IO KX15	Un a		DTFFT0_1X150u	AB14 se0to2(36)
	[vds2to0n(19) AD4	DIFF IU_RX12	10 8	13	DIFF IO 1X1510	AC14 se0to2(46)
	[vds2to0n(19) AD4 [vds2to0p(15) AE3	DIELIO-KXIS	in .	చ	IDILL IN IXISIU	AC10 se0to2(50)
	lvds2to0n(15) AE4	DIELIO-KYIS	[2p] &		DIEE TO TX1220	AC9 se0to2(54)
	lvds2to0p(14) AF3	DIELIO-VVIS	5 D		DIELIO INICCII	AC12 se0to2(31)
	lvds2to0n(14) AF4	DIFFIO PY12	3p Pe 23n 3p 24p 8		DIFFIU TY123D	AC11 se0to2(30)
	lvds2to0p(8) AE2	NTFFTN PX12	3 A		.nteetn_tx1240	AB6 (vds0to2p(0)
	lvds2to0n(8) AF1	DIFFID PX12	ďη š		Interto TX1246	AB5 lyds0to2n(0)
	(vds2to0p(6) AF2	DIFFIO RX12	50 ≟		DIFFIO TX1250	AC8 lyds0to2p(1)
	(vds2to0n(6) AG2 (vds2to0p(9) AG3	DIFFIO RX12	50 -		DIFFIO TX125n	AC7 lyds@to2n(1)
		DIFFIO RX12	60 M		DIFFIO TX1260	AC6 (vds0to2p(2)
	(vds2to0n(9) AG4	DIFFIO_RX12	išni 🗟		DIFFIO_TX126n	AC5 (vds0to2n(2)
	[vds2to0p(3) AH2	DIFFIO_RX12	70		DIFFIO_TX127o	AD6 lvds0to2p(3)
	lvds2to0n(3) AH1	DIFFIO_RX12	7n		DIFFIO_TX127n	AD5 lyds0to2n(3) AD7 lyds0to2p(4)
	\left\{ \text{lvds2to0p(7) AH3} \\ \text{lvds2to0n(7) AH4} \end{array}	DIFFIO_RX12	!8p		DIFFIO_TX128p	AD7 lyds0to2p(4) AD8 lyds0to2p(4)
	(vds2to0p(2) AJ1	DIFFIO_RX12	!8n		DIFFI0_TX128n	AD9 (vds0to2p(5)
	Lude2t o0o(2) A I2	DIFFIO_RX12	!9p		DIFFIO_TX129p	AD10 lvds0to2n(5)
	1 vds2t n0n(5) 4.13	DIFFIO_RX12	!9n		DIFFIO_TX129n	AE5 lyds0to2p(6)
	(vds2to0p(5) AJ4	DIFFIO_RX13	Qp		DIFFIO_TX130p	AE6 lyds0to2n(6)
	[vds2to0n(5) AJ4 [vds2to0p(0) AK2	DIFF IO_EX13	ijn	6	DTFFT0_1X130u	AE7 lyds0to2p(7)
	(vds2to0n(0) AK1	DIFF IO-KX13]0	(50)	DTFF IO- 1X1310	AE8 lvds0to2n(7)
	Lyde2t oBo(4) AK3	DIFFIU_KXI3	in		DILLIO IXISIU	AF5 lvds0to2p(8)
	lvds2to0n(4) AK4	DIFF IU_KXI3	[SP] (o ×	DIFF 10_1X132D	AF6 lvds0to2n(8)
	[vds2to0p(1) AL3	DIFFIU_KXI3	20	TO	DIEETU TV132U	AF7 lvds0to2p(9)
	lvds2to0n(1) AL4	DIFFIO RXII	isbl /	DAINN Highspeed	DIFFIO TX115n DIFFIO TX115n DIFFIO TX115n DIFFIO TX115n DIFFIO TX115n DIFFIO TX115n DIFFIO TX117n DIFFIO TX117n DIFFIO TX117n DIFFIO TX120n DIFFIO TX130n	AF8 lvds0to2n(9)
	1	DILLIOTKVIS	3111 =	į į	DIFFID TV1340	AG5 lyds0to2o(10)
			_	- s	INTERTO TY134p	AG6 lvds0to2n(10)
			<	, <u>.</u>	Interto tx1350	AH6 (vds0to2p(11)
					DIFFID TX135p	AH5 lyds@to2n(11)
				LL9	DIFFID TX1360	AJ6 (vds0to2p(12)
				Ž	DIFFIO TX136n	AJ5 (vds0to2n(12)
				ш.	DIFFIO_TX1376	AK5 lvds0to2p(13) AK6 lvds0to2p(13)
	. se0to2(41) AM1				DIFFIO_TX137n	AKE (VdsUto2n(13)
	se0to2(41) AM1 se0to2(5) AM2	DIFFIO_RX13	l9pi		DIFFIO_TX138p	AG7 lvds0to2p(14)
	0001 02/42) MI	DIFFIO_RX13	8n		DIFFIO_TX138n	AG8 lvds0to2n(14) AH7 lvds0to2p(15)
		DIFFIO_RX13 DIFFIO_RX13 DIFFIO_RX13	19p		DIFFIO_TX139p	AH8 lyds0to2n(15)
	000102/E7) AP2				DIFFIO_TX139n	AJ8 (vds0to2p(16)
	soft 02(45) AP1	DIFFIO_RX12	[0p]		DIFFIO_TX140p	AJ7 lvds0to2n(16)
	se0t o2(16) AR1	DIFF IO-RX12	[0n]		DIFF 10_1X140n	AK8 lyds0to2p(17)
	se0to2(11) AR2	DIFFIO_RX13 DIFFIO_RX14 DIFFIO_RX14 DIFFIO_RX14	lib		DIFF IN IXIAID	AK7 lyds0to2n(17)
	se0to2(18) AT1	DILLIO-KYJ	1201 C		Interto tatas-	AL7 lvds0to2p(18)
	se0to2(19) AT2	DIELIO PAIZ	20 (DIEE TO TX1425	AL8 lvds0to2n(18)
		DIFFID_NAI	1301.1		DIFFIO TY1430	AH9 lvds0to2p(19)
	: se0to2(9) AM4	NTFFTN PX12	3p × 3n ∞		Intertorty1435	AH101vds0to2n(19)
	se0to2(13) AN3	NTFFTO RX12	14n v		DIFFIN TX1440	AD11 se0to2(28)
	se0to2(17) AN4	nterto RX1∠	14p Peeds 4n 9ds		Interto tx1446	AD12 se0to2(38)
		DIFFIO RX14	50 8	6	DIFFIO TX1450	AD13 se0to2(24)
	se0to2(8) AP3	DIFFIO_RX14	išni .	8	IDIFFIO_TX145h	AC13 se0to2(27)
	se0to2(2) AU2	DIFFIO RX14	P	\succeq	DIFFIO TX1460	AE10 se0to2(52)
	se0to2(14) AT3 se0to2(39) AR3	DIFFIO_RX14	i6n -	-	DIFFIO_TX146n	AE9 se0to2(48) AD14 se0to2(25)
	se0to2(39) AR3	DIFFIO_RX14	7p 9	- P	DIFFIO_TX147p	AE14 se0to2(21)
	se0to2(3) AR4 se0to2(35) AL5	DIFFIO_RX14	IZinl글	Speed	DIFFIO_TX147n	AE14 se0to2(21) AF9 se0to2(62)
	* cont o2(55) ALC	DIFFIO_RX14	8p L	Ş	DIFFIO_TX148p	AF10 se0to2(63)
	990t 02(12) AMS	DIFFIO_RX14	8n	.≥	DIFFIO_TX148n	AG9 lvds@to2clkp
	soft o2(10) AM6	DIFFIO.RXI	19p	Low	DIFFIO - 13339n DIFFIO - 13439n DIFFIO - 13440n DIFFIO - 13440n DIFFIO - 13441n DIFFIO - 13442n DIFFIO - 13442n DIFFIO - 13443n DIFFIO - 13443n DIFFIO - 13443n DIFFIO - 13443n DIFFIO - 13445n DIFFIO - 13450n	AG10 lyds0to2clkn
	soft o2(1) ANS	DIEFIO-RX12	iặυ	<u></u>	<u> U1FFI0_TX149</u> n	AE13 se0to2(22)
	se0to2(4) AN5	NTEL TO KX12	UP	ä	NTFF TO TX120b	AE12 se0t o2(23)
	se0to2(4) AN5 se0to2(0) AP5	NTELTO-KX15	ุบท ใ	굽	hittin-1X120u	AG12 se0to2(7)
	se0to2(33) AP6	NTELTO-KX15	10		DIFFIO_TX151p DIFFIO_TX151n	AF12 se0to2(6)
	1	DIFF IOTKX12	ini		.NTLLIOTIX12JU	β
	_se0to2(32) AF13	GPIO_B6_0			GPI0_B6_1	AF14 se0to2(20)
	•	GL 10_DO_0				v
		S80F1508B6			U	1

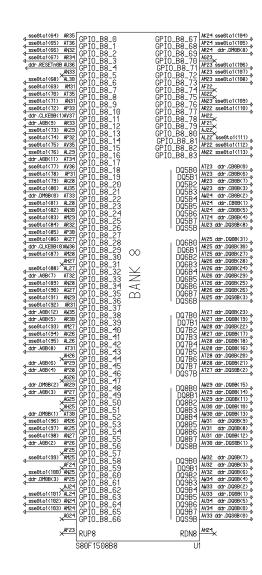
TM-4

JSHOOL VivesiyofTooto LVDS

Development FPGA 0 Banks 7 and 8







DDR SDRAM Bank B

ddr.WEn@B	ddr.WEn
ddr.clk0B(2:0)	ddr.clk(2:0)
ddr.SDA0B	ddr.SDA
ddr.clkn0B(2:0)	ddr.clkn(2:0)
ddr.DM0B(8:0)	ddr.DM(8:0)
ddr DQS0B(8:0)	ddr.DQS(8:0)
_ ddr.Vref0B	ddr.Vref
ddr RASneB	ddr.RASn
ddr .CASn8B	ddr CASn
ddr.Sn0B(1:0)	ddr.Sn(1:0)
ddr.BA0B(1:0)	ddr.BA(1:0)
ddr .DQ8B(63:0)	ddr.DQ(63:0)
ddr A0B(13:0)	ddr. A(13:0)
ddr.CB0B(7:0)	ddr.CB(7:0)
ddr .CLKE8B(1:0)	ddr.CLKF(1:0)
, ddr .RESETn0B	ddr.RESETn
ddr SCLOB	ddr.SCL
`	ddi 100L

TM-4

Jshedir Vivasiyof Borto

LVDS Development FPGA 1 Banks 1 and 2 lyds1to3p(19:0) — | New York (vds1to3n(19:0) — \[\frac{\text{\tik}}\text{\tik}\text{\tetx{\text{\tetx{\text{\text{\text{\text{\text{\text{\text{\texicr{\text{\text{\text{\text{\text{\text{\text{\texict{\text{\text{\texict{\text{\texicr{\texicr{\texicr{\text{\text{\text{\text{\text{\text{\tet DIFFIO_TX38p | W31 | selto2(52) | W32 | selto2(53) | W32 | selto2(53) | W29 | selto2(50) | W39 | selto2(51) lyds1to2p(19:0) — | | | FFIO_RX38n FFIO_RX39p lvds1to3clkp ← lyds2toin(1) W38 IO_RX39n IO_RX40p lvds1to3clkn ← lvds2to1p(2) V38 lvds1to2clko ← | lvds2to1n(2) V39 | lvds2to1p(3) V36 lvds1to2clkn ←□⊃ 10_RX41p 10_RX41n 10_RX42p Single Ended lvds2to1n(3) V37 lvds2to1p(4) U38 se1to2(63:0) lvds2to1p(5) U39 IO_RX42n se1to3(63:0) — DIFFIO_TX/n | M330 rvdstto3clkp | DIFFIO_TX5n | M331 rvdstto3clkn | DIFFIO_TX5n | M330 setto3c2t | DIFFIO_TX6n | M331 setto3c2t | DIFFIO_TX7n | M331 setto3c2t | DIFFIO_TX7n | M331 rvdstto3cl2 | DIFFIO_TX7n | M331 rvdstto3cl2 | DIFFIO_TX8n | DIFFIO_TX8 | AB3TU | AB3T ž IO_RX43p | DIFFIO TX45n | Vist to 2015 | Vist | Lvds2to1n(5) U37 | Lvds2to1p(6) T39 IO_RX43n IO_RX44p lvds2to1n(6) T38 lvds2to1p(7) T36 ΙΟ_RX45ρ ΙΟ_RX45η [vds2to1n(7) T37 DIFFIO_TX8p DIFFIO_TX8p DIFFIO_TX8n AL33Lvdsttc3p(18) lyds2to1p(8) R36 selto3(31) AT39 DIFFIO_RX8p selto3(31) AT39 DIFFIO_RX8n pelto3(45) 4730 DIFFIO_RX8n IO_RX46p IO_RX46n ž (lyds2to1n(8) R37 | MISSING | MISS lvds2to1p(9) P36 ΪΟ_RX47ρ ΙΟ_RX47n Highspeed se1to3(45) AT38 se1to3(53) AR38 (vds2to1n(9) P37 DIFFIO_RX9n DIFFIO_RX10o [vds2to1p(10) P39 ĬŎ_ŔX48p lvds2to1n(10) R38 RX48n [lvds2to1p(11) N38 IFFIO_RX49p IFFIO_RX49n lvds2to1n(11) P38 [vds2to1p(12) N36 selto3(15) AN39 DIFFIO_RX12p selto3(54) AN38 DIFFIO_RX12p selto3(58) AN39 DIFFIO_RX13p FIO_RX50p lvds2to1n(12) N37 FIO_RX50n FIO_RX51p lvds2to1p(13) M38 selto3(44) AM38 DIFFIO_RX13n lyds2to1n(13) M39 FIO_RX51n FIO_RX52p FIO_RX52n [vds2to1p(14) L38] (vds2to1n(14) L39 | Lvds2to1p(15) M36 IO_RX53p IO_RX53n IO_RX54p lvds2to1n(15) M37 lyds2to1p(16) K38 \succeq lvds2to1n(16) K39 FÍO_RX54n DIFFIO_TX17p
DIFFIO_TX17n
AG34lvds1to3n(13)
AF33 lvds1to3p(7)
AF34 lvds1to3p(7) | (vds2to1p(17) L37 IFFIO_RX55p IFFIO_RX55n lvds2to1n(17) L36 DIFFIO TX17n A334(vdslto3n(13))
DIFFIO TX18 A732 (vdslto3n(13))
DIFFIO TX18 A732 (vdslto3n(17))
DIFFIO TX180 A732 (vdslto3n(17))
DIFFIO TX190 A732 (vdslto3n(19))
DIFFIO TX190 A332 (vdslto3n(19))
DIFFIO TX200 A332 (vdslto3n(15))
DIFFIO TX200 A332 (vdslto3n(15))
DIFFIO TX210 A332 (vdslto3n(15))
DIFFIO TX210 A332 (vdslto3n(15))
DIFFIO TX210 A332 (vdslto3n(15))
DIFFIO TX220 A332 (vdslto3n(15)) lvds2to1p(18) J36 FFIO_RX56p FFIO_RX56n lvds2to1n(18) J37 \sim lvds2to1p(19) K36 peedsyb (vds2to1p(19) K36 (vds2to1n(19) K37 DIFFIO_RX57p Lvds3to1p(15)AK36 Lvds3to1p(19)AK38 BANK | Lvds3to1n(11)AJ36| DIFFID_RX210 | Lvds3to1p(17)AJ38| DIFFID_RX22p | Lvds3to1n(17)AJ38| DIFFID_RX22p | Lvds3to1p(12)AH37| DIFFID_RX22n | IFFIO_TX2Pn | GSS tVds tcdstr3, | IFFIO_TX2Pn | GSS tVds tcdstr3, | IFFIO_TX2Pn | AG3 tVds tcdstr3, | IFFIO_TX2Pn | AG3 tVds tcdstr3, | IFFIO_TX2Pn | AG3 tVds tcdstr6, | IFFIO_TX2Pn | AG3 tVds tcdstr2, | IFFIO_TX2Pn | AG3 tvds tcdstr2, | IFFIO_TX2Pn | AG3 test tcdstr2, | IFFI OIFFIO_RX23p OIFFIO_RX23n OIFFIO_RX24p lvds3to1n(12)AH36 lvds3to1p(16)AH39 se1to2(26) H39 se1to2(27) H38 se1to2(24) G39 DIFFIO_RX62p lyds3to1n(16)AH38 lyds3to1p(10)AG37 DIFFIO_RX24n DIFFIO_RX25p DIFFIO_RX25n DIFFIO_RX62n DIFFIO_RX63p DIFFIO_RX63n selto2(25) G38 selto2(22) F38 Lvds3to1n(10)AG36 Lvds3to1o(13)AF38 DIFFIO_RX26p FIO_RX64p selto2(23) F39 selto2(20) E38 Lvds3to1n(13)AG38 Lvds3to1p(11)AE38 DIFFIO_RX26n DIFFIO_RX27p DIFFIO_RX27n FFIO_RX64n FFIO_RX65p se1to2(21) E39 se1to2(10) E36 RX65n IO_RX66p IO_RX66n selto2(11) E37 selto2(19) D39 IO_RX67p IO_RX67n se1to2(18) D38 se1to2(17) H37 selto2(17) 10_RX68p 10_RX68n lyds3to1n(0) AD36 lyds3to1p(9) AD39 se1to2(16) H36 se1to2(15) G36 IFFIO_RX30n vds3to1p(3) AC31 Vds3to1p(3) AC31 DIFFIO_RX31p IO_RX69p IO_RX69n se1to2(12) F36 DIFFIO_RX32p DIFFIO_RX32n DIFFIO_RX33p 10_RX70p 10_RX70n 10_RX71p lvds3to1n(3) AC36 lvds3to1p(7) AC39 se1to2(13) F37 se1to2(8) D37 se1to2(8) Lvds3to1p(2) AB37 DIFFIO_RX33n DIFFIO_RX34p se1to2(9) IO_RX71n se1to2(6) se1to2(7) 10_RX72p 10_RX72n lvds3to1p(4) AB38 IFFIO_RX34n se1to2(3) | Uds3tolp(1) M33| | DIFFIO_RX35n | Uds3tolp(1) M37| | DIFFIO_RX36n | Uds3tolp(1) M37| | DIFFIO_RX36n | Uds3tolp(6) M33| | DIFFIO_RX36n | DIFFIO_RX36n | DIFFIO_RX37p | DIFFIO_RX36p | DIF IO_RX73p se1to2(2) DIFFIO_RX73n DIFFIO_RX74p se1to2(4) se1to2(5) H34 F34 DIFFIO_RX74n F34 DIFFIO_RX75p F35 DIFFIO_RX75n se1to2(8) (vds3to1n(6) AA38 DIFFIO_RX37n se1to2(1) se1to3(19) AG28 GPIO_B1_0 GPIO_B2_1 4 selto2(62) P26 GPIO_B2_0 AH28 se1to3(5) GPIO_B1_1 S80F1508B1 S80F1508B2 JESTEROER TM-4

Winesity of Boots

LVDS

lvds3to1p(19:0) ____

lvds3to1n(19:0)

lvds2to1o(19:0)

lyds2to1n(19:0)

Development FPGA 1 Banks 3 and 4

DQ6T0 DQ6T1 DQ6T1 D25 ddr.D01A(32) D25 ddr.D01A(37) D2612

A26 ddr.DQ1A(36)

| DOTTO | B27 | ddr.D014/49) | DOTTO |

DQS8T | B30 | ddr.DQS1A(6)

DQ9T0 A32 ddr.DQ1A(60)

DQ9T0 (32 ddr. D04K85) → DQ9T1 (32 ddr. D04K55) → DQ9T2 (32 ddr. D04K55) → DQ9T2 (33 ddr. D04K61) → DQ9T3 (33 ddr. D04K61) → DQ9T4 (33 ddr. D04K58) → DQ9T5 (34 ddr. D04K58) → DQ9T6 (34 ddr. D04K58) → DQ9T6 (35 ddr. D04K58) → DQ9T7 (35 ddr. D04K5

RDN3 M24

ddr.A1A(1) E21 GPIO_B3_0 ddr.BA1A(1) G22 GPIO_B3_1

GPIO_B3_10 GPIO_B3_11 GPIO_B3_12 GPIO_B3_13 GPIO_B3_14

GPIO_B3_24 GPIO_B3_25 GPIO_B3_25 GPIO_B3_26 GPIO_B3_27 GPIO_B3_28 GPIO_B3_29 GPIO_B3_30

GPIO_B3_30
GPIO_B3_31
GPIO_B3_32
GPIO_B3_33
GPIO_B3_34
GPIO_B3_35
GPIO_B3_36
GPIO_B3_36

ddr.A1A(0) ddr.A1A(10) F22 dev1.nib(11) × H23 dev1.nib(13) K23 4 dev1.nib(13) K23

ddr .DM1A(8) F23 dev1.nib(18) G24
dev1.nib(20) K24 dev1.nib(21) × N24 H24

ddr.DM1A(4) F25 dev1.nib(22) J24 dev1.nib(23) L24 dev1.nib(24) G25 dev1.nib(25) × H25

dev1.nib(26) G27 dev1.nib(27) K25 dev1.nib(28) H26

ddr.DM1A(6) D30

× M25 × N26 × N26 × F27

ddr.A1A(13) E29 ddr.CASn1A F28

ddr.Sn1A(0) F29

dev1.nib(29) XP27 dev1.nib(30) J26

dev1.nib(31) K26 dev1.nib(32) H27

ddr.DM1A(5) E30 ddr.SDA1A A35

ddr.Sn1A(1) F30

dev1.nib(36) × H28

dev1.nib(37) E31 dev1.nib(38) K27 dev1.nib(39) G29

ddr.DM1A(7) D33 dev1.nib(40) H29

dev1.nib(41) G30

B36 GPIO_B3_65 D34 GPIO_B3_65 GPIO_B3_66

S80F1508B3

×P23 RUP3

dev1.nib(42) dev1.nib(43) dev1.nib(44)

dev1.nib(45) dev1.nib(46) dev1.nib(47)

dev1.nib(48)

dev1.nib(35)



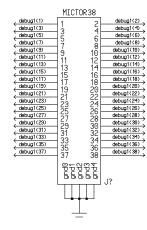
Nibble Bus dev1.nib(49:0) ----

4.2 CP	TO D4 73 [UB 00F.KIK(6)]
1-6	IO R4 74 617 ×
4_3 ĞP	
44 CP	TO R4 75 P18 X
1-1 85	±8−8 1−48 1u17 C
4_5 GP	
4_5 GP 4_6 GP	TO BA - 77 N17 C
1_0	10-D 1-70 D18
47 GP	
1_/	TO D4 79 F18 ddr.A1A(2)
4_8 GP	IU_B4_/9 =19 ddp 414/2)

DDR SDRAM Bank A

_ ddr.WEn1A	ddr.WEn
ddr.clk1A(2:0)	ddr.clk(2:0)
ddr.SDA1A	ddr.SDA
ddr.clkn1A(2:0)	ddr.clkn(2:0)
ddr.DM1A(8:0)	ddr.DM(8:0)
ddr.DQS1A(8:0)	ddr.DDS(8:0)
ddr.Vref1A	ddr.Vref
ddr.RASn1A	ddr.RASn
ddr.CASn1A	ddr,CASn
ddr.Sn1A(1:0)	ddr.Sn(1:0)
ddr.BA1A(1:0)	ddr.BA(1:0)
ddr .D01A(63:0)	ddr.DQ(63:0)
ddr.A1A(13:0)	ddr.A(13:0)
ddr.CB1A(7:0)	ddr.CB(7:0)
ddr.CLKE1A(1:0)	ddr.CLKE(1:0)
ddr.RESETn1A	ddr.RESETn
ddr.SCL1A	ddr.SCL
`	uui 100L

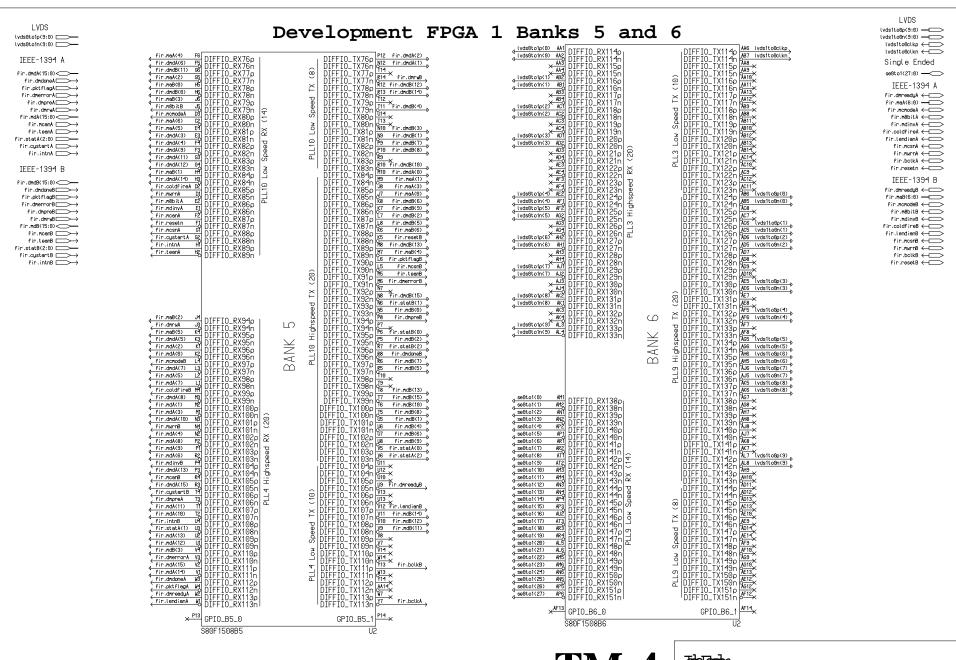
Logic Analyzer Connector



debug1(2) B3 debug1(7) D4	GPIO_B4_0 GPIO_B4_1 GPIO_B4_2		GPIO_B4_71 GPIO_B4_72 GPIO_B4_73	H17 debug1(30) K17 debug1(32) C18 ddr.A1A(6)
debug1(9) C4	GPIO_B4_3 GPIO_B4_4 GPIO_B4_5 GPIO_B4_6		GPIO_B4_74 GPIO_B4_75 GPIO_B4_76	917 P18 L17 N17
H9 × E6 × J10 debug1(15) D6	GPIO_B4_7 GPIO_B4_8 GPIO_B4_9		GPIO_B4_78 GPIO_B4_79 GPIO_B4_80	D18
x F8 F7 debug1(19) D7	GPIO_B4_10 GPIO_B4_11 GPIO_B4_12 GPIO_B4_13		GPIO_B4_81 GPIO_B4_82 GPIO_B4_83 GPIO_B4_84	M18 X M18 X G18 debug1(34)
debug1(11) D5 debug1(29) F9 debug1(13) C5	GPIO_B4_14 GPIO_B4_15 GPIO_B4_16		GPIO_B4_85 GPIO_B4_86 GPIO_B4_87	H18 debug1(38) J18 debug1(36) P19 N19
debug1(8) K11 J11 debug1(31) G10	GPIO_B4_18 GPIO_B4_19 GPIO_B4_20		ĞPİÖ_B4_88 GPIO_B4_89 GPIO_B4_90	P20 × N20 ×
debug1(6) B4 J12 debug1(12) K12	GPIO_B4_21 GPIO_B4_22 GPIO_B4_23 GPIO_B4_24		DQ0T0 DQ0T1 DQ0T2	06 debug1(17) B6 C7 debug1(21)
debug1(27) E8 debug1(33) G11	GPIO_B4_25 GPIO_B4_26 GPIO_B4_27		DQ0T2 DQ0T3 DQ0T4 DQ0T5 DQ0T6	A7 C8 debug1(25) A6 debug1(5) A8
debug1(4) A4 debug1(16) K13 debug1(1) A5	GPIO_B4_28 GPIO_B4_29 GPIO_B4_30 GPIO_B4_31 GPIO_B4_32	4	DQ0T7 DQS0T	B8 × B7 ×
debug1(18) H12	GPIO_B4_33 GPIO_B4_34	3ANK	DQ1T0 DQ1T1 DQ1T2 DQ1T3	C9 ddr.DQ1A(1) B9 ddr.DQ1A(4) A9 ddr.DQ1A(0) C11 ddr.DQ1A(3)
debug1(14) H13 debug1(23) D8 ddr.A1A(12) E10 , M13	GPIO_B4_36 GPIO_B4_37 GPIO_B4_38	ш	DQ1T4 DQ1T5 DQ1T6 DQ1T7	A10 ddr.DQ1A(5) C10 ddr.DQ1A(7) A11 ddr.DQ1A(2) B11 ddr.DQ1A(6)
ddr.CLKE1A(1) E9 ddr.RESETn1A D10 J14 ddr.DM1A(0) D9	GPIO_B4_40 GPIO_B4_41 GPIO_B4_42		DQS1T DQ2T0 DQ2T1	### B10 ddr.DQS1A(0) #### A12 ddr.DQ1A(9) ### D12 ddr.DQ1A(12)
debug1(37) G13 debug1(35) G12 debug1(20) K14	GPIO_B4_43 GPIO_B4_44 GPIO_B4_45 GPIO_B4_46		DQ212 DQ2T3	E12 ddr.DQ1A(8) E13 ddr.DQ1A(10) B12 ddr.DQ1A(13)
ddr.DM1A(2) F13 ddr.DM1A(1) F12 N13 ddr.CLKE1A(8) E11	GPIO_B4_47 GPIO_B4_48 GPIO_B4_49 GPIO_B4_50		DQ2T4 DQ2T5 DQ2T6 DQ2T7 DQS2T	B13 ddr.DQ1A(11) DC13 ddr.DQ1A(14) DD13 ddr.DQ1A(15) DC12 ddr.DQS1A(1)
debug1(18) H14 × M14 × N14 × M14 , ddr.A1A(5) F14	GPIO_B4_51 GPIO_B4_52 GPIO_B4_53		DQ3T0 DQ3T1	C14 ddr.DQ1A(16) D14 ddr.DQ1A(17) E14 ddr.DQ1A(20)
debug1(24) K15 debug1(22) H15	GPIO_B4_54 GPIO_B4_55 GPIO_B4_56 GPIO_B4_57		DQ3T2 DQ3T3 DQ3T4 DQ3T5	A14 ddr.DQ1A(21) B14 ddr.DQ1A(18) B15 ddr.DQ1A(22)
× M15 × N15 × N15 × G15 → P15	GPIO_B4_58 GPIO_B4_59 GPIO_B4_60 GPIO_B4_61		DQ3T6 DQ3T7 DQS3T	D15 ddr.DQ1A(19) C15 ddr.DQS1A(2)
2 L16 × J16 × M16 debug1(28) K16	GPIO_B4_62 GPIO_B4_63 GPIO_B4_64		DQ4T0 DQ4T1 DQ4T2 DQ4T3	A16 ddr.DQ1A(24) D16 ddr.DQ1A(29) A17 ddr.DQ1A(25) B16 ddr.DQ1A(28)
debug1(26) H16 debug1(26) H16 N16 ddr.DM1A(3) F17	GPIO_B4_65 GPIO_B4_66 GPIO_B4_67 GPIO_B4_68		DQ4T4 DQ4T5 DQ4T6	B17 ddr.DQ1A(26) b D17 ddr.DQ1A(27) b E17 ddr.DQ1A(31) b C17 ddr.DQ1A(30) b
× F15	GPIO_B4_69 GPIO_B4_70 RUP4		DQ4T7 DQS4T RDN4	C16 ddr.DQS1A(3)
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JEST HETCHE University of Toronto



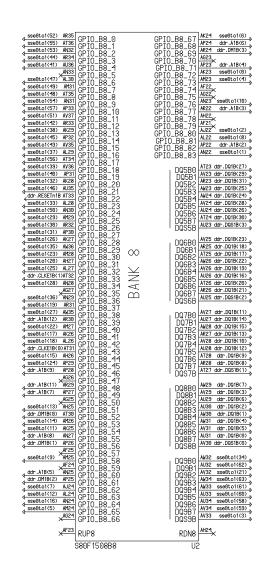
TM-4

Jishedir Vivesiyo Tooto

Development FPGA 1 Banks 7 and 8



AF20				AL11 sse0to1(76)
AG19	GPI0_B7_0		GPI0_B7_71	AK11 sse0to1(73)
01-1/1075 N/10	GPI0_B7_1		GPIO_B7_72 GPIO_B7_73	AV4 sse0to1(77)
Sse0to1(107) AK16 AF19 sse0to1(108) AM18 sse0to1(112) AP19	GPIO_B7_2 GPIO_B7_3		GPIO_B7_73	AP9 sse0to1(78)
00001 01/109 AM19	GPIO_B7_3 GPIO_B7_4 GPIO_B7_5		GPIN RT 14	AU4 ddr.SCL1B
9990t 01(112) AP19	ĞPİÖLB7L4		GPIO_B7_75	AR7 ddr.CASn1B
sse0to1(110) AR19	GPIO_B7_5 GPIO_B7_6		GPI0_B7_76	AV5 sse0to1(75)
4 3360001(1107 AK13	IGPIN B7 6		GPID R7 77	AR6 sse0to1(67)
XAG18	GP10_B / _ /		GB10_B1_18	AP8 sse0to1(74)
XAJ18	GPIO_B7_8		GPI0_B7_79	AU5 sse0to1(80)
XAP18	GPI0_B7_9		GPI0_B7_80	AL10 sse0to1(68)
sse0to1(113) AN18	GPI0_B7_10		GPI0_B7_81	AT5 sse0to1(70)
ddr.DM1B(8) AR18	GPI0_B7_11		GPIO_B7_82 GPIO_B7_83	AM9 sse0to1(66)
AG17	GPIO_B7_12 GPIO_B7_13		GP10_B7_83	AN9 sse0to1(91)
XAH17	GPI0_B7_13		GPI0_B7_84	AV3 ddr.SDA1B
XAF18	GPI0_B7_14		GPI0_B7_85	AR5 sse0to1(64)
XAT18	ĞPİÖ_B7_15		GPIO_B7_86	AN7 sse0to1(71)
XAJ17	GPIO_B7_16		GPIO_B7_87	AN8 sse0to1(82)
XAU18	GPI0_B7_17		GPIO_B7_88	AT4 sse0to1(65)
XAF17	GPIO_B7_18 GPIO_B7_19		GPIO_B7_89 GPIO_B7_90	AT6 ddr.Sn1B(0)
sse0to1(103) AM17	GPI0_B7_19		GPI0_B7_90	AP7 sse0to1(72)
4 3300001(100) AITT	GPI0_B7_20		GPI0_B7_91	
sse0to1(99) AM16	GPI0_B7_21			AU6 ddr.DQ1B(59)
sse0to1(106) AP16	GPIO_B7_22 GPIO_B7_23		l DQ0B0	AV6 ddr.DQ1B(58)
0000t 01/104) AV16	GPI0_B7_23		DQ0B1	AU7 ddr.DQ1B(63)
AH16	GPI0_B7_24		DQ0B2	AW7 ddr.DQ1B(57)
	GPI0_B7_25		DQ0B3	AU8 ddr.DQ1B(60)
AJ16 AE15	GPI0_B7_26		DQ0B4	AN6 ddr.DQ1B(62)
XAF15	GPIO_B7_25 GPIO_B7_27		DQ0B5	AW8 ddr.DQ1B(56)
sse0to1(105) AP15	16210 87 78		DQ0B6	AV8 ddr.DQ1B(61)
ddr.DM1B(4) AR16	GPI0_B7_29	\sim	DQ0B7	AV7 ddr.DQS1B(7)
AG15	GP10_B7_30		DQS0B	NY GOI IDGOID(17)
sse0to1(96) XM15	1 CDTO D7 21			AU9 ddr.DQ1B(51)
econt o1(109) AN15	GPIO_B7_32 GPIO_B7_33 GPIO_B7_34	\cong	DQ1B0	AV9 ddr.DQ1B(50)
sse0to1(97) AK15	GPI0_B7_33	\sim	DQ1B1	AW9 ddr.DQ1B(54)
sse0to1(101) AL15	GPI0_B7_34	$ \triangleleft$	DQ1B2	AU11 ddr.DQ1B(48)
ddr.A1B(1) AP14	GP10_B7_35	\sim	DQ1B3	AW10 ddr.DQ1B(53)
4 UUITANIBET) AFTH	GPI0_B7_36		DQ1B4	AU10 ddr .DQ1B(55)
sse0to1(90) XAG14	GPIO_B7_37		DQ1B5	AW11 ddr.DQ1B(49)
sse0to1(93) AM14	GPI0_B7_38		DQ1B6	AV11 ddr.DQ1B(52)
ddr.DM1B(5) AR11	IGPTO B7 39		DQ1B7	AV10 ddr.DQS1B(6)
AH14	GPI0_B7_40		DQS1B	MY TO GOI ID GO ID (G)
ddr.A1B(10) XAP12	GPI0_B7_41			AW12 ddr.DQ1B(46)
ddn 110/0\ 1012	GPI0_B7_42		ı DQ2B0	AT12 ddr.DQ1B(42)
4 UGIT A 15(6) AF 13	GPI0_B7_43		DQ2B1	AR12 ddr.DQ1B(44)
sse0to1(100) AN12	GPIO_B7_44 GPIO_B7_45		DQ2B2 DQ2B3	AR13 ddr.DQ1B(40)
sse0to1(102) AN13	GPI0_B7_45		DQ2B3	
sse0to1(94) AK14			DQ2B4	AV12 ddr.DQ1B(47)
sse0to1(95) AL14	GPI0_B7_47		DQ2B5	AU13 ddr .DQ1B(45)
ddr.DM1B(6) AT10	GPI0_B7_48		DQ2B6	AT13 ddr.DQ1B(41)
sse0to1(92) AR9	IGP10 B7 49		DQ2B3 DQ2B4 DQ2B5 DQ2B6 DQ2B7 DQS2B	AU12 ddr.DQS1B(5)
4 3360001(3E) AKS	GPI0_B7_50		DQS2B	NOTE dal i.bao ib(3)
ddr.BA1B(0) AR10	H;PHI R / 51			AU14 ddr.DQ1B(38)
ddr.WEn1B AT8	GP10_B7_52		l DQ3B0	AT14 ddr.DQ1B(39)
`sepAt o1(87) AM13	GPI0_B7_53		DQ3B1	AR14 ddr.DQ1B(36)
ddc RAIR(1) AP11	GPI0_B7_54		DQ3B2 DQ3B3	AW14 ddr.DQ1B(34)
00001 01/92\ AM12	GPI0_B7_55		DQ3B3	AV14 ddr.DQ1B(35)
4 SSECUTIOS/ MITE	GP10_B7_56		I DQ3B4	AV15 ddr.DQ1B(33)
00001 01/993 XII 12	GPI0_B7_57		DQ3B5	AR15 ddr.DQ1B(32)
ddr.RASn1B AT9	GPI0_B7_58		D0386	AT15 ddr.DQ1B(37)
sse0to1(86) AK13	GPI0_B7_59		DQ3B7 DQS3B	AU15 ddr.DQS1B(4)
ddr.Sn1B(1) AW5	GPI0_B7_60		' DQS3B	DIO GGI IDGO IDC 17
ssent o1(98) AN11	GPI0_B7_61			AW16 ddr.CB1B(3)
sse0to1(69) AM11	GPI0_B7_62		1 DQ4B0	AT16 ddr.CB1B(1)
esplit of (84) APR	GPI0_B7_63		DQ4B1	AW17 ddr.CB1B(2)
espet o1(85) AP19	GP10_B7_64		DQ4B2 DQ4B3	AV16 ddr.CB1B(7)
scott o1/79) AV12	GPI0_B7_65		DQ4B3	AV17 ddr.CB1B(6)
econt o1(81) Al 12	GPIO R7 66		DQ4B4	AT17 ddr.CB1B(5)
ddc DM1R(7) AT7	GPI0_B7_67		DQ4B5	AR17 ddr.CB1B(4) →
ddc 41R(13) AU4	GPI0_B7_68		DQ4B6	AU17 ddr.CB1B(0)
econt o1/89) ANIA	GPIO_B7_67 GPIO_B7_68 GPIO_B7_69		DQ4B7	AU16 ddr.DQS1B(8)
4 SSECTOT(83) ANTO	GPI0_B7_70		DQ4B4 DQ4B5 DQ4B6 DQ4B7 DQS4B	no io dai ibao ib(g)
Akite	l			AP17
×AN16	RUP7		RDN7	```` ×
	S80F1508B7		Už]
	0001 10000 /		Uz	-

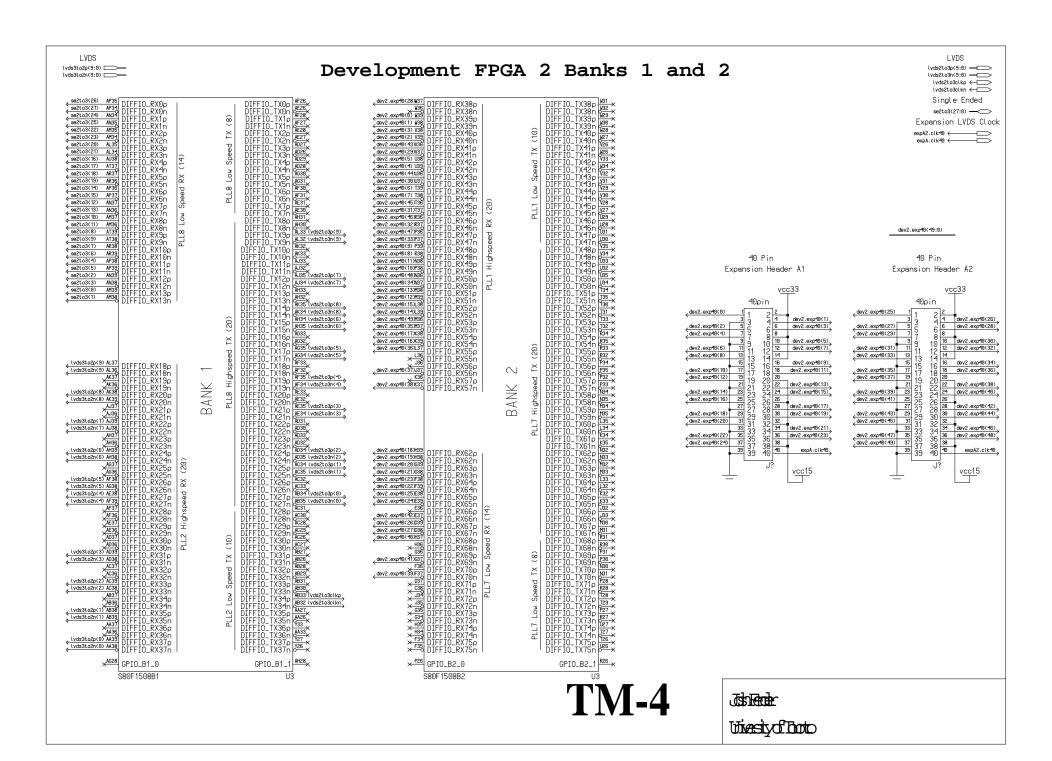


DDR SDRAM Bank B

ddr.WEn1B	ddr.WEn
ddr.clk1B(2:0)	ddr.clk(2:0)
ddr.SDA1B	ddr.SDA
ddr.clkn1B(2:0)	ddr.clkn(2:0)
ddr.DM1B(8:0)	ddr.DM(8:0)
ddr .DQS1B(8:0)	ddr.DQS(8:0)
, ddr.Vref1B	ddr.Vref
ddr .RASn1B	ddr.RASn
ddr.CASn1B	ddr.CASn
ddr.Sn1B(1:0)	ddr.Sn(1:0)
ddr.BA1B(1:0)	ddr.BA(1:0)
ddr .DQ1B(63:0)	ddr.DQ(63:0)
ddr.A1B(13:0)	ddr.A(13:0)
ddr.CB1B(7:0)	ddr.CB(7:0)
ddr.CLKE1B(1:0)	ddr.CLKE(1:0)
_ ddr .RESETn1B	ddr.RESETn
ddr .SCL1B	ddr.SCL
`	ddi 100L

TM-4

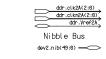
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Development FPGA 2 Banks 3 and 4

ddr.A2A(1) E21	GPI0_B3_0		GPI0_B3_67	A36 ddr.SCL2A
ddr.BA2A(1) G22 dev2.nib(0) J22	GPI0_B3_1		GPI0_B3_68	F32 K29
dev2.nib(2) N22	GPIO_B3_2 GPIO_B3_3		GPIO_B3_69 GPIO_B3_70	F33 ^
dev2.nib(3) M22	GPIO_B3_3 GPIO_B3_4		PDT0 D2 71	B37 ×
dev2.nib(4) P22	GPIO_B3_4 GPIO_B3_5 GPIO_B3_6		GPIO_B3_72 GPIO_B3_73 GPIO_B3_74 GPIO_B3_75	F33
ddr A2A(0) E22	GPIO_B3_6		GPT0 B3 73	G31 C
dev2.nib(5) G23	GPIO_B3_7		GPI0_B3_74	135
ddr.A2A(10) F22 dev2.nib(6) N23	IGPIO B3 8		GPI0_B3_75	H31 X
dev2.nib(7) H23	GPIO_B3_9 GPIO_B3_10		GPIO_B3_76 GPIO_B3_77	G33 ×
	GPI0_B3_10		GP10_B3_77	C36
ddr DM2A(8) F23	GPIO_B3_11 GPIO_B3_12		GPIO_B3_78	E34 ×
_dev2.nib(9) M23	GPIO_B3_12 GPIO_B3_13		GPIO_B3_79 GPIO_B3_80	G32 ×
	ICPIN R3 14		GPIO_B3_81	D36 V
dev2.nib(10) G24	LGPI0_B3_15		GPI0_B3_82	E35 ×
dev2.nib(11) K24 dev2.nib(12) N24	GPI0_B3_16			
dev2.nib(13) H24	GPI0_B3_17			B23 ddr.CB2A(1)
ddn DM2A(4) E25	GPI0_B3_18		DQ5T0	E23 ddr.CB2A(4)
dev2.nib(14) J24	GPIO_B3_19		DQ5T1	D23 ddr.CB2A(5)
dev2.nib(15) L24	GPIO_B3_20 GPIO_B3_21		DQ5T2 DQ5T3	A23 ddr.CB2A(0)
dev2.nib(16) G25	GPIO_B3_22		DQ5T4	A24 ddr.CB2A(2)
dev2.nib(17) P24	GPTO R3 23		Dasts	B24 ddr.CB2A(6)
dev2.nib(18) H25	GPI0_B3_24		l DQ5T6	C24 ddr.CB2A(3)
dev2.nib(19) N25 ,ddr.RASn2A F26	GPI0_B3_25		DQ5T7	D24 ddr.CB2A(7) C23 ddr.DQS2A(8)
dev2.nib(20) G27	GPI0_B3_26		DQS5T	OCO GGI IDGOERTO
dev2.nib(21) K25	GPIO_B3_27 GPIO_B3_28		DOCTO	B25 ddr.DQ2A(32)
dev2.nib(22) H26	GPIO_B3_28 GPIO_B3_29		DQ6T0 DQ6T1	E25 ddr.DQ2A(33)
ddr.DM2A(6) D30	CPTO RS SO	(^)	DQ6T2	D25 ddr .D02A(37)
dev2.nib(24) M25	GPIO_B3_31 GPIO_B3_32 GPIO_B3_33		DOSTS	A26 ddr.DQ2A(36)
dev2.nib(28) N26	GPIO_B3_31 GPIO_B3_32	\searrow	DQ6T3 DQ6T4	B26 ddr.DQ2A(34)
ddr.WEn2A F27	GPI0_B3_33	Z	DQ6T5	D26 ddr.DQ2A(38)
ddr.AZA(13) E29 dev2.nib(30) M26	GPI0_B3_34	\forall	DQ6T6	E26 ddr.DQ2A(35)
	GPI0_B3_31 GPI0_B3_32 GPI0_B3_33 GPI0_B3_34 GPI0_B3_35 GPI0_B3_36	$ \Delta $	DQ6T7	C25 ddr.DQS2A(4)
ddr.Sn2A(0) F29 dev2.nib(32) N27	GPIO_B3_36 GPIO_B3_37		1 DQS6T	
dev2.nib(32) N27	GPIO_B3_37 GPIO_B3_38		DQ7T0	B27 ddr.DQ2A(40)
4 dev2.nib(34) U31	GPI0_B3_39		DQ7T1	C27 ddr D02A(45)
dev2.nib(37) J26	GPI0_B3_40		DQ7T2	D27 ddr.DQ2A(44)
dev2.nib(38) K26 dev2.nib(39) H27	GPI0_B3_41		DQ7T3	E27 ddr.DQ2A(41) B28 ddr.DQ2A(43)
ddr.DM2A(5) E30	GPIO_B3_42 GPIO_B3_43 GPIO_B3_44 GPIO_B3_45		DQ7T4	A28 ddr.DQ2A(42)
ddr SDA2A A35	GPIO_B3_43 GPIO_B3_44		DQ7T5	D28 ddr.DQ2A(46)
ddr.Sn2A(1) F30	GPIO_B3_44 GPIO_B3_45		DQ7T6 DQ7T7	E28 ddr D02A(47)
dev2.nib(40) M27	GPIO_B3_46		DQS7f	C28 ddr.DQS2A(5)
dev2.nib(41) N28	GPIO_B3_46 GPIO_B3_47		Daori	l
dev2.nib(42) G28 dev2.nib(43) D32	GPI0_B3_48		, DQ8T0	A29 ddr.DQ2A(48) B29 ddr.DQ2A(49)
dev2.nib(43) D32 dev2.nib(44) J27	GPI0_B3_49		DQ8T1	C29 ddr.DQ2A(53)
dev2.nib(45) M28	GPI0_B3_50		DQ8T2 DQ8T3	C30 ddr.DQ2A(54)
dev2.nib(46) H28	GPIO_B3_51 GPIO_B3_52		DUS13	A30 ddr.DQ2A(52)
dev2.nib(47) E31			DQ8T4 DQ8T5	A31 ddr.DQ2A(55)
dev2.nib(48) K27	GPIO_B3_54		DQ8T6	B31 ddr.DQ2A(51)
dev2.nib(49) G29	GPI0_B3_55		DQ8T7	C31 ddr.DQ2A(50)
ddr.DM2A(7) D33 dev2.nib(1) H29	GPT0 B3 56		DQS8T	B30 ddr.DQS2A(6)
dev2.nib(23) G30	GPIO_B3_57 GPIO_B3_58			A32 ddr.DQ2A(60)
dev2.nib(25) J28	GPIO_B3_58 GPIO_B3_59		DQ9T0	C32 ddr.DQ2A(57)
dev2.nib(26) B35	GPIO_B3_59 GPIO_B3_60		DQ9T1	B32 ddr.DQ2A(56)
dev2.nib(27) C35	GPIO_B3_60 GPIO_B3_61		DQ9T2 DQ9T3	A34 ddr.DQ2A(63)
dev2.nib(29) K28	GPIO_B3_61 GPIO_B3_62		DQ9T4	A33 ddr .DQ2A(61)
dev2.nib(31) F31	IGPIO B3 63		DQ9T5	C33 ddr.DQ2A(62)
dev2.nib(33) B36 dev2.nib(35) D34	GPIO_B3_64		DQ9T6	C34 ddr.DQ2A(58) B34 ddr.DQ2A(59)
dev2.nib(35) D34 dev2.nib(36) J29	GPI0_B3_65		DQ917	B34 ddr.DQ2A(59) B33 ddr.DQS2A(7)
4 SOLEMINOON OF	GPI0_B3_66		' DQS9T	DOG GGI IDAOLIN II
× P23	DI IDO		DDNO	M24 ×
	RUP3		RDN3	
	S80F1508B3		U:	3

* 88 * 89 * 89 * 89 * 89 * 89 * 89 * 89	GP10.B4.10 GP10.B4.11 GP10.B4.13 GP10.B4.13 GP10.B4.15 GP10.B4.15 GP10.B4.16 GP10.B4.17 GP10.B4.19 GP10.B4.19 GP10.B4.11 GP10.B4.11 GP10.B4.11 GP10.B4.11 GP10.B4.11 GP10.B4.12 GP10.B4.15 GP10.B4.15 GP10.B4.16 GP10.B4.16 GP10.B4.17 GP10.B4.18 GP10.B4.18 GP10.B4.18 GP10.B4.18 GP10.B4.18 GP10.B4.18 GP10.B4.20	Λ.	GPIO_B4_71 GPIO_B4_72 GPIO_B4_72 GPIO_B4_74 GPIO_B4_75 GPIO_B4_75 GPIO_B4_76 GPIO_B4_77 GPIO_B4_87 GPIO_B4_87 GPIO_B4_88 GPIO_B4_88 GPIO_B4_88 GPIO_B4_89 GPIO_B4_89 GPIO_B4_89 GPIO_B4_80 GPIO_B4_80 GPIO_B4_80 GPIO_B4_80 GPIO_B4_80 GPIO_B4_80 GPIO_B4_80 GPIO_B4_80 GPIO_B4_80 GPIO_B4_80 GPIO_B4_80 GPIO_B4_80 GPIO_B4_80 GPIO_B4_80 GPIO_B4_80 GPIO_B4_90	H17 × K17 × Adr. A2A(6)
ddr.A2A(19) #113 #13 ddr.A2A(12) #16 ddr.A2A(12) #17 ddr.A2A(12) #18 ddr.A2A(12) #18 ddr.A2A(12) #18 ddr.A2A(12) #18 ddr.A2A(12) #18	GPIO_B4_32 GPIO_B4_33 GPIO_B4_34 GPIO_B4_35 GPIO_B4_36 GPIO_B4_37 GPIO_B4_38 GPIO_B4_39 GPIO_B4_40	BANK	DQ1T0 DQ1T1 DQ1T2 DQ1T3 DQ1T3 DQ1T4 DQ1T5 DQ1T6 DQ1T7 DQS1T	G9 ddr.D02A(1) B9 ddr.D02A(1) A9 ddr.D02A(3) C11 ddr.D02A(3) A10 ddr.D02A(5) C10 ddr.D02A(5) C11 ddr.D02A(5) C11 ddr.D02A(6) B10 ddr.D02A(6) B10 ddr.D02A(6)
ddr.DM2A(0) × J14 ddr.DM2A(0) × G13	GPIO_B4_41 GPIO_B4_42 GPIO_B4_44 GPIO_B4_44 GPIO_B4_45 GPIO_B4_46 GPIO_B4_47 GPIO_B4_48 GPIO_B4_49 GPIO_B4_50		DQ2T0 DQ2T1 DQ2T2 DQ2T3 DQ2T4 DQ2T5 DQ2T5 DQ2T6 DQ2T7 DQS2T	A12 ddn.DQ2A(9) D12 ddn.DQ2A(12) E12 ddn.DQ2A(18) E13 ddn.DQ2A(18) B12 ddn.DQ2A(13) B13 ddn.DQ2A(11) D13 ddn.DQ2A(11) D13 ddn.DQ2A(15) C12 ddn.DQ2A(15)
# M14 # M14 # M14 # M14 # M14 # M15 #	GPIO.B4.51 GPIO.B4.52 GPIO.B4.53 GPIO.B4.54 GPIO.B4.55 GPIO.B4.55 GPIO.B4.56 GPIO.B4.58 GPIO.B4.59 GPIO.B4.59		DQ3T0 DQ3T1 DQ3T2 DQ3T3 DQ3T4 DQ3T5 DQ3T5 DQ3T6 DQ3T7 DQS3T	C14 ddr.DQ2A(16) D14 ddr.DQ2A(17) E14 ddr.DQ2A(21) A14 ddr.DQ2A(21) B14 ddr.DQ2A(18) B15 ddr.DQ2A(22) E15 ddr.DQ2A(23) D15 ddr.DQ2A(23) C16 ddr.DQ2A(23)
ddr.A2A(8) / F17	GPIO_B4_61 GPIO_B4_62 GPIO_B4_62 GPIO_B4_64 GPIO_B4_65 GPIO_B4_65 GPIO_B4_66 GPIO_B4_68 GPIO_B4_68 GPIO_B4_69 GPIO_B4_70		DQ4T0 DQ4T1 DQ4T2 DQ4T3 DQ4T3 DQ4T4 DQ4T5 DQ4T6 DQ4T7 DQS4T	A16 ddr.DQ2A(24) D16 ddr.DQ2A(29) A17 ddr.DQ2A(28) B16 ddr.DQ2A(28) B17 ddr.DQ2A(28) D17 ddr.DQ2A(26) D17 ddr.DQ2A(30) C16 ddr.DQ2A(30) C16 ddr.DQS2A(3)
× F15	RUP4 S80F1508B4		RDN4 U3	E16 ×

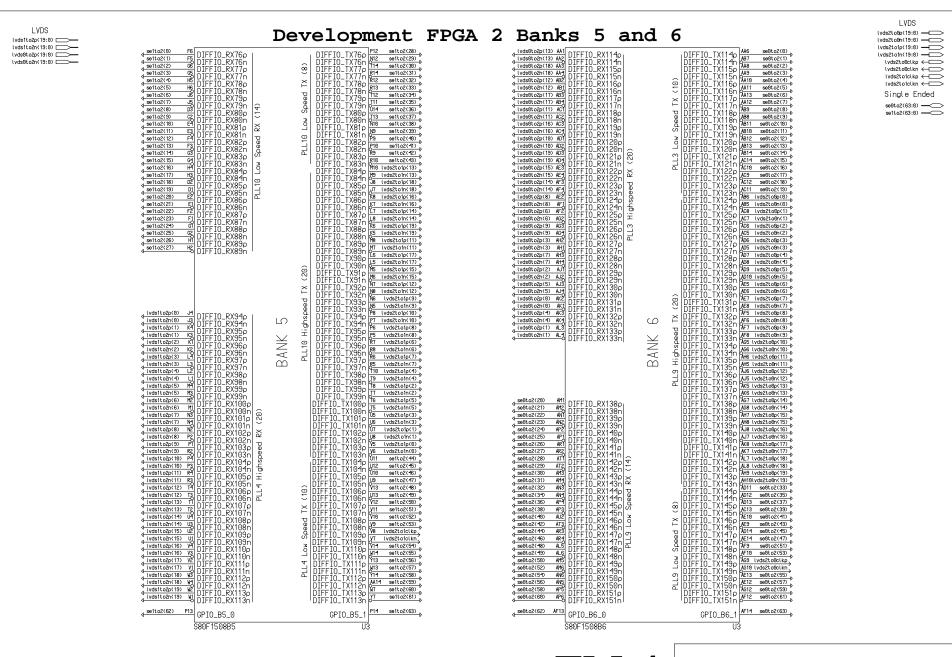


DDR SDRAM Bank A

, ddr.WEn2A	LI UE
ddr.clk2A(2:0)_	ddr.WEn
ddr.SDA2A	ddr.clk(2:0) ddr.SDA
ddr.clkn2A(2:0)	ddr.clkn(2:0)
ddr.DM2A(8:0)	ddr.DM(8:0)
ddr.DQS2A(8:0)	ddr.DQS(8:0)
ddr.Vref2A	ddr.Vref
ddr.RASn2A	ddr.RASn
ddr.CASn2A	ddr.CASn
ddr .Sn2A(1:0)	ddr.Sn(1:0)
ddr.BA2A(1:0)	ddr.BA(1:0)
ddr .DQ2A(63:0)	ddr.D0(63:0)
ddr.A2A(13:0)	ddr.A(13:0)
ddr.CB2A(7:0)	ddr.CR(7:0)
ddr.CLKE2A(1:0)	ddr.CLKE(1:0)
ddr .RESETn2A	ddr.RFSFTn
ddr.SCL2A	ddr.SCI
`	ddi 100L

TM-4

Jahrenic Vivesiyo Tooto



TM-4

Jahrenir Vivasiyof Tooto

Development FPGA 2 Banks 7 and 8

×AF20	GPI0_B7_0		GPIO_B7_71	AL11 sse2to3(37)
VAG 13	GPTO_B7_1		GPIO_B7_72	AK11 sse2to3(38)
sse2to3(0) ^AK18	GPIO_B7_2		GPT0 B7 73	AV4 sse2to3(39) AP9 sse2to3(40)
×AF19 AM18	GPI0_B7_3		GPI0_B7_74	AP9 sse2to3(40) AU4 sse2to3(41)
^AD19	GPI0_B7_4		GP10_B /_ /5	AR7 sse2to3(42)
XAR19	GPIO_B7_5		GPI0_B7_76	AV5 sse2to3(43)
AH18	GPI0_B7_6		GPIO_B7_77	AR6 sse2to3(44)
CAG18	GPIO_B7_7 GPIO_B7_8		GPIO_B7_78 GPIO_B7_79	AP8 sse2to3(45)
_AJ18	GPIO_B7_8 GPIO_B7_9 GPIO_B7_10 GPIO_B7_11 GPIO_B7_12		GPIO_B7_73	AU5 sse2to3(46)
sse2to3(1) ^AP18	GP10_B7_10		GPIN R7 81	AL10 sse2to3(47)
ddr.A2B(10) AN18	GPT0_B7_11			AT5 sse2to3(48)
ddr.DM2B(4) AR18 AG17	GPIO_B7_11 GPIO_B7_12 GPIO_B7_13		GPIO_B7_82 GPIO_B7_83	AM9 sse2to3(49) AN9 sse2to3(50)
eea2t o3(2) AH17	H3PHL R7 13		GPIN R7 84	AV3 sse2to3(51)
4 ddc_13P(1) ×AF18	GPIO_B7_14 GPIO_B7_15		GPIO_B7_85 GPIO_B7_86	AR5 sse2to3(52)
ddr.A2B(1) AT18	GPIO_B7_15		GPIO_B7_86	AN7 sse2to3(53)
_AJ17	GPIO_B7_16 GPIO_B7_17		GPIO_B7_87 GPIO_B7_88	AN8 sse2to3(54)
dar. AZB(U) AU18	GPIO_B7_18		GPIO_B7_89	AT4 sse2to3(55)
AF17	GPĪŎ_B7_19		GP10_B7_90	AT6 sse2to3(56)
sse2to3(4) AM1/	GPI0_B7_20		GPI0_B7_91	AP7 sse2to3(57)
sse2to3(5) ×AG16	GPIN R7 21			AU6 sse2to3(58)
	IGPIN R7 22		l DQOBO	AV6 eea2t o3(59)
eea2t o3(6) AK16	GP10_B7_23		DQ0B1	AU7 sse2to3(60)
00021 02(7) AU16	GPI0_B7_24		DQ0B2	AW7 sse2to3(61)
cco2t o3(8) Al 16	GPI0_B7_25		DQ0B3	AU8 sse2to3(62)
AU16	ĞPİÖ_B7_26		DQ0B4	AW6 sse2to3(63)
	GPIO_B7_27 GPIO_B7_28		DQ0B5	AN8 ddr.SCL2B
ddc RA2R(B) AP15	GPI0_B7_28		DQ0B6	AV8 ddr.SDA2B
ddr DM2B(5) AR16	GPIO_B7_29 GPIO_B7_30	_	DQ0B7 DQS0B	AV7 sse2to3(3)
AG15	GPIO_B7_25 GPIO_B7_26 GPIO_B7_27 GPIO_B7_29 GPIO_B7_29 GPIO_B7_30 GPIO_B7_31 GPIO_B7_32 GPIO_B7_33 GPIO_B7_33 GPIO_B7_33		, DASAR	•
sse2to3(9) XM15	GPIO_B7_31 GPIO_B7_32 GPIO_B7_33	\/	00100	AU9 ddr.DQ2B(59)
sse2to3(10) AN15	GPI0_B7_32	\Rightarrow	DQ1B0	AV9 ddr.DQ2B(58)
sse2to3(11) AK15	GPIO_B7_33 GPIO_B7_34	_	DQ1B1 DQ1B2	AW9 ddr.DQ2B(63)
sse2to3(12) AL15	GPIO_B7_34 GPIO_B7_35	<1	DQ1B3	AU11 ddr.DQ2B(61)
ddr.RASn2B AP14	GPIO_B7_35	ш	00103	AW10 ddr.DQ2B(62)
sse2to3(13) AH15	GPIO_B7_35 GPIO_B7_36 GPIO_B7_37		DQ1B4 DQ1B5	AU10 ddr.DQ2B(57)
. AG14	GPIO_B7_38		Daibs	AW11 ddr.DQ2B(56)
sse2to3(14)^AM14	GPIO_B7_38 GPIO_B7_39		DQ1B7	AV11 ddr.DQ2B(60)
ddr Sn2B(0) AR11	GPIO_B7_40		DQS1B	AV10 ddr.DQS2B(7)
sse2to3(15) AH14	GPTO_B7_41		DWOID	
", ddr ، CASn2B AP12	GPIO_B7_42		ı DQ2B0	AV12 ddr DQ2B(50)
ddr DM2B(6) AP13	GPIO_B7_43		D0204	AT12 ddr DQ2B(55)
×AG13	GP10_B7_44		DQ2B2 DQ2B3 DQ2B4 DQ2B4 DQ2B5 DQ2B6 DQ2B7 DQS2B	AR12 ddr.DQ2B(51)
sse2to3(16)^AN12	GPI0_B7_45		DQ2B3	AR13 ddr.DQ2B(48)
ddr.WEn2B AN13	GPI0_B7_46		DQ2B4	AV12 ddr .DQ2B(54)
sse2to3(17) AK14	IGPTO B7 47		DQ2B5	AV13 ddr .DQ2B(53)
sse2to3(18) AL14 ddr.DM2B(7) AT10	GPTO B7 48		DQ2B6	AU13 ddr .DQ2B(52)
sse2to3(19) AR9	GPIO_B7_49		DQ2B7	AT13 ddr.DQ2B(49) AU12 ddr.DQS2B(6)
sse2to3(20) AH13	IGPIN R7 50		DQS2B	MUTZ GGI DGOZB(6)
dde Sn2R(1) AP10	IGPIN R / 51			AU14 ddr.DQ2B(41)
sse2t.n3(21) AT8	10710-87-56		DQ3B0	AT14 ddr .DQ2B(45)
eep2t n3(22) AM13	GPI0_B7_53		DQ3B1	AR14 ddr .DQ2B(42)
AP11	GPI0_B7_54		DQ3B2	AN14 ddr.DQ2B(47)
eea2t n3(23) AM12	GPI0_B7_55		D03B3 D03B4	AV14 ddr.DQ2B(46)
sse2to3(24) AH12	GPI0_B7_56		D03B4	AV15 ddr.DQ2B(43)
	GPI0_B7_57		DQ3B5	AR15 ddr.DQ2B(40)
ddr.A2B(13) AT9	GPIO_B7_58 GPIO_B7_59		DQ3B6	AT15 ddr.DQ2B(44)
sse2to3(26) AK13	GP10_B7_60		DQ3B7 DQS3B	AU15 ddr.DQS2B(5)
sse2to3(27) AW5	GPIO_B7_61		, D#22B	ν
sse2to3(28) AN11	GPIO_B7_61 GPIO_B7_62		, DQ4B0	AW16 ddr DQ2B(35)
sse2to3(29) AM11	GPIO_B7_63		DQ4B1	AT16 ddr.DQ2B(37)
sse2to3(30) AR8	GPIO_B7_64		DQ4B2	AW17 ddr DQ2B(34)
sse2to3(31) AP10	GPIO_B7_65		DQ4B3	AV16 ddr DQ2B(39)
sse2to3(32) AK12	GPIO_B7_66		DQ4B4	AV17 ddr.DQ2B(32)
sse2to3(33) AL12	IGPIN R7 67		bq485	AT17 ddr.DQ2B(36)
sse2to3(34) AT7	GPIO_B7_67 GPIO_B7_68		DQ4B6	AR17 ddr.DQ2B(38)
sse2to3(35) AW4	GPIO_B7_69 GPIO_B7_69		no4R7	AU17 ddr DQ2B(33)
sse2to3(36) AN10	GPIO_B7_68 GPIO_B7_69 GPIO_B7_70		DQ4B7 DQS4B	AU16 ddr DQS2B(4)
41.40			240 10	1017
×AN16	RUP7		RDN7	AP17
				7
	S80F1508B7		U:	5

sse2to3(64) AR35	GPI0_B8_0		GPIO_B8_67	AK24 sse2to3(104)
sse2to3(65) AT36	GPIO_B8_0 GPIO_B8_1		GPIO_B8_67 GPIO_B8_68	AP24 sse2to3(105)
sse2to3(66) AN32	GPIO_B8_2		GPIO_B8_69	AR24 ddr.DM2B(8)
sse2to3(67) AR34	GPIO_B8_3		CDIO_DO_03	AG23
ddr .RESETn2B AU36	GPIO_B8_3 GPIO_B8_4		GPIO_B8_70 GPIO_B8_71	AP23 sse2t o3(106)
AN33	GD TO DO T		CDTO DO 70	AK23 sse2to3(107)
, sse2to3(68) AL30	GPIO_B8_5		GPIO_B8_72 GPIO_B8_73	AM22 0002+ 02/1001
sse2to3(69) AM31	GPI0_B8_6		GPI0_B8_73	AF22
eea2t n3(70) AT35	GPIO_B8_7		GPI0_B8_74	AG22
sse2t.n3(71) AN31	GPIO_B8_8		GPI0_B8_75	AN23 sse2t o3(109)
sse2to3(72) AP33	GPIO_B8_9		GPIO_B8_76	AR22 sse2to3(110)
ddr .CLKE2B(1)AV37	GPI0_B8_10		GPI0_B8_77	AH22
ddr .A2B(9) AR33	GPI0_B8_11		GPI0_B8_78	AF21.
sse2to3(73) AK29	GPIO_B8_12		GPI0_B8_79	AJ22
sse2to3(74) AP32	GPI0_B8_13		GPI0_B8_80	
	GPI0_B8_14		GPI0_B8_81	
sse2to3(75) AV35	GP10_B8_15		GPIO_B8_82	AP22 sse2to3(112)
sse2to3(76) AL29	GPI0_B8_16		GPI0_B8_83	AN22 sse2to3(113)
ddr.A2B(11) AT34	GPI0_B8_17			
sse2to3(77) AV36	GPI0_B8_18		DQ5B0	AT23 ddr.CB2B(0)
sse2to3(78) AP31	ĞPİÖ_B8_19		DQ5B1	AV23 ddr.CB2B(6)
sse2to3(79) AK28	GPI0_B8_20		D05B2	AR23 ddr.CB2B(7)
sse2to3(80) AU35	GPIO_B8_21		DUEDS	AW23 ddr.CB2B(3)
ddr.DM2B(0) AT33	GPIO_B8_21 GPIO_B8_22		DOEDA	AW24 ddr.CB2B(2)
sse2to3(81) AL28	GPIO_B8_22 GPIO_B8_23		DQ5B3 DQ5B4 DQ5B5	AV24 ddr.CB2B(1)
sse2to3(82) AN30	ODIO DO 24		DOEDO	AU24 ddr.CB2B(5)
sse2to3(83) AM29	GPIO_B8_24		DQ5B6	AT24 ddr.CB2B(4)
sse2to3(84) AR32	GPIO_B8_25 GPIO_B8_26		DQ5B7	AU23 ddr.DQS2B(8)
sse2to3(85) AP30	GPI0_B8_26		DQS5B	
sse2to3(86) AK27	GPI0_B8_27		00000	AV25 ddr.DQ2B(31)
ddr.CLKE2B(0)AW36	GPI0_B8_28		l DQ6B0	AR25 ddr.DQ2B(30)
sse2to3(87) AM28	GPI0_B8_29	∞	DQ6B1	AT25 ddr .DQ2B(27)
AH27	GPI0_B8_30		DQ6B2	AW26 ddr .DQ2B(28)
, sse2to3(88) AL27	GPI0_B8_31		DQ6B3	AV26 ddr .DQ2B(24)
ddr.A2B(7) AT32	GPIO_B8_32 GPIO_B8_33 GPIO_B8_34	\simeq	DQ6B4	AU26 ddr .DQ2B(29)
sse2to3(89) AN28	GPI0_B8_33	\sim	DQ6B5	AT26 ddr .DQ2B(25)
	GPI0_B8_34	<	DQ6B6	
sse2to3(90) AG27	GPIO_B8_35	\sim	DQ6B7	AR26 ddr.DQ2B(26)
sse2to3(91) AN29	CDIO DO OC		DQS6B	AU25 ddr.DQS2B(3)
sse2to3(92) AR31	GPIO_B8_37			l
ddr A2B(12) AW35	GPI0_B8_38		DQ7B0	AV27 ddr .D02B(23)
ddr.A2B(5) AR30	GPIO_B8_38 GPIO_B8_39		DQ7B1	AU27 ddr.DQ2B(19)
sse2to3(93) AM27	GPIO_B8_40		no782	AW28 ddr.DQ2B(22)
sse2to3(94) AK26	GP10_B8_41		DQ7B2 DQ7B3	AR27 ddr.DQ2B(17)
sse2to3(95) AL26	GPIO_B8_42		DQ7B4	AV28 ddr .DQ2B(18)
ddr.A2B(8) AT31	GPIO_B8_43		Dã7B5	AU28 ddr .DQ2B(16)
AH26	GPIO_B8_44		Da7B6	AT28 ddr.DQ2B(20)
ddr.A2B(6) ^AP29	GPI0_B8_45		batby	AR28 ddr.DQ2B(21)
ddr.A2B(4) AP28	GPIO_B8_46		DQS7B	AT27 ddr.DQS2B(2)
AG26	GPIO_B8_47		DQ37D	
ddr.DM2B(2) AR29	GPIO_B8_48		DQ8B0	AW29 ddr .DQ2B(15)
ddr.A2B(3) AP27	GPIO_B8_49			AV29 ddr.DQ2B(14)
_AG25			DQ8B1	AU29 ddr.DQ2B(11)
AH25	GPI0_B8_50		DQ8B2	AU39 ddr.DQ2B(10)
_ ddr .DM2B(1) AT30	GPI0_B8_51		DQ8B3	AW30 ddr.DQ2B(13)
sse2to3(96) AM26	GPI0_B8_52		DQ8B4	AW31 ddr.DQ2B(9)
9992t n3(97) AK25	GPI0_B8_53		DQ8B5	AV31 ddr.DQ2B(8)
9902t n3(98) AN27	GPI0_B8_54		D08B6	AU31 ddr.DQ2B(12)
ddn 120(2) 1020	GPIO_B8_55 GPIO_B8_56		DQ8B7	AV30 ddr.DQS2B(1)
4 ddi (AZB(Z) Al Z6 AF25 AM2E	GPI0_B8_56		DQS8B	ATOO GGI IDAOLDY IV
sse2to3(99) XM25	GPI0_B8_57			AW32 ddr.DQ2B(7)
AF24	GB10_B8_28		ı DQ9B0	AU32 ddr.DQ2B(3)
	GPI0_B8_59		DQ9B1	
sse2to3(100) AN25	GPI0_B8_60		DQ9B2	AV32 ddr.DQ2B(6)
ddr.DM2B(3) AP25	GPI0_B8_61		DQ9B3	AW34 ddr.DQ2B(4)
AJ24			l DQ9B4	AW33 ddr.DQ2B(2)
sse2to3(101) AL24	GPIO_B8_62 GPIO_B8_63		l bassis	AU33 ddr.DQ2B(1)
sse2to3(102) AN24	GPI0_B8_64		DQSB6	AU34 ddr.DQ2B(5)
sse2to3(103) AM24	GPIO_B8_65		DQSB7	AV34 ddr DQ2B(0)
×AG24	GPI0_B8_66		Dasab	AV33 ddr.DQS2B(0)
	5, 10_00_00		D@00D	l
×AF23	RUP8		RDN8	AH24
_	KUFO		VDINO	
	S80F1508B8		U] ^



DDR SDRAM Bank B

, ddr.WEn2B	ddr.WEn
ddr.clk28(2:0)	ddr.clk(2:0)
ddr.SDA2B	ddr.SDA
ddr.clkn2B(2:0)	ddr.clkn(2:0)
ddr.DM2B(8:0)	ddr.DM(8:0)
ddr.DQS2B(8:0)	ddr DQS(8:0)
. ddr.Vref2B	ddr.Vref
ddr.RASn2B	ddr RASn
ddr CASn2B	ddr CASn
ddr.Sn2B(1:0)	ddr.Sn(1:0)
ddr.BA2B(1:0)	ddr.BA(1:0)
ddr.DQ2B(63:0)	ddr DQ(63:0)
ddr.A2B(13:0)	ddr.A(13:0)
ddr.CB2B(7:0)	ddr.CB(7:0)
ddr.CLKE2B(1:0)	ddr.CLKE(1:0)
, ddr.RESETn2B	ddr.RESETn
ddr.SCL2B	ddr.SCL
	uui 100L

TM-4

Jahren Vivestyof Booto

LVDS Development FPGA 3 Banks 1 and 2 lyds3to1p(19:0) — lvds3to1n(19:0) — 4 selto3(0) AP35 DIFFIO_RX0p 4 selto3(2) AP34 DIFFIO_RX0n DIFFIO_RX1p DIFFIO_RX1p DIFFIO_RX1p DIFFIO_RX1p DIFFIO_RX1p DIFFIO_TX38p | W31 | seeto3(52) | W32 | seeto3(53) | W31 | seeto3(53) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | W32 | seeto3(50) | (vds@to3p(@) W37 | DIFFIO_RX38p | Lvds0to3n(0) | W36 | Lvds0to3p(1) | W39 DIFFIO_RX38n DIFFIO_RX39p lvds3to0clkp ← [vds0to3n(1) W38 lvds3to0clkn ← (vds0to3o(2) V38 IN RX40c lyds3to1clko ← lvds0to3n(2) V39 lvds3to1clkn ←□⊃ [vds0to3p(3) V36 IO_RX41p Single Ended lyds0to3n(3) V37 n RX41n lvds0to3p(4) U38 se0to3(63:0) lvds0to3p(5) U36 IO_RX42n se1to3(63:0) ----| DIFFIO_TX/n | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | Miss | | lvds0to3p(6) T39 IN RX43n IO_RX44p IO_RX44p lvds0to3n(6) T38 setto3(32) AN37 Setto3(32) AN36 Setto3(32) AN37 Setto3(32) AN37 | lvds0to3p(8) | R36 0_RX45n DIFFIO_TX8p DIFFIO_TX8n DIFFIO_TX8n Al33 (vds3to1p(1)) selto3(35) 4739 DIFFIO_RX8p selto3(34) 4739 DIFFIO_RX8n selto3(35) 4739 DIFFIO_RX8n IO_RX46p IO_RX46n (vds0to3n(8) R37 (vds0to3p(9) P36 0_RX47p se1to3(35) AT38 se1to3(36) AR38 (vds0to3n(9) P37 DIFFIO_RX9n DIFFIO_RX10o I0_RX47n | lvds0to3p(10) P39 DIFFIO TX480 V35 (vds3:06x(18)-DIFFIO TX48n (33 (vds3:06x(19)-DIFFIO TX49n (33 (vds3:06x(19)-DIFFIO TX49n (35 (vds3:06x(19)-DIFFIO TX59n (35 (vds3:06x(19)-DIFFIO TX59n (34 (vds3:06x(19)-DIFFIO TX59n (34 (vds3:06x(14)-DIFFIO TX51p (35 (vds3:06x(14)selto3(37) AR39 DIFFIO RX10p selto3(38) AP38 DIFFIO RX10p selto3(39) AP39 DIFFIO RX11p selto3(49) AN39 DIFFIO RX11p lvds0to3n(10) R38 IO_RX48n [vds0to3p(11) N38 IO_RX49p | lyds0to3n(11) P38 IFFIO_RX49n (lvds0to3p(12) N36 setto3(40) M39 DIFFIO_RX12p setto3(41) M38 DIFFIO_RX12p setto3(42) M39 DIFFIO_RX13p IO_RX50p [vds0to3n(12) N37 FFIO_RX50n FFIO_RX51p FFIO_RX51p FFIO_RX51n FFIO_RX52p FFIO_RX52n FFIO_RX53p FFIO_RX53n FFIO_RX54p lvds0to3p(13) M38 DIFF 10 TX5 | 0 T3 | Ves3 00 (14) |
DIFF 10 TX5 | 0 T35 | Ves3 00 (14) |
DIFF 10 TX5 | 0 T35 | Ves3 00 (14) |
DIFF 10 TX5 | 0 T30 | Ves3 00 (15) |
DIFF 10 TX5 | 0 T31 | Ves3 00 (15) |
DIFF 10 TX5 | 0 T31 | Ves3 00 (15) |
DIFF 10 TX5 | 0 T33 | Ves3 00 (17) |
DIFF 10 TX5 | 0 T33 | Ves3 00 (17) |
DIFF 10 TX5 | 0 T33 | Ves3 00 (12) |
DIFF 10 TX5 | 0 T33 | Ves3 00 (12) |
DIFF 10 TX5 | 0 T34 | Ves3 00 (13) |
DIFF 10 TX5 | 0 T34 | Ves3 00 (13) |
DIFF 10 TX5 | 0 T34 | Ves3 00 (13) |
DIFF 10 TX5 | 0 T34 | Ves3 00 (13) |
DIFF 10 TX5 | 0 T34 | Ves3 00 (13) |
DIFF 10 TX5 | 0 T34 | Ves3 00 (13) | selto3(43) AM38 DIFFIO_RX13n lvds0to3n(13) M39 [vds0to3p(14) L38 1vds0to3n(14) L39 [vds0to3p(15) M36] lvds0to3n(15) M37 1vds0to3p(16) K38 [vds0to3n(16) K39 DIFFIO_TX17p
DIFFIO_TX17n
DIFFIO_TX17n
A635 (vds3to1p(0))
A634 (vds3to1p(10))
AF33(vds3to1p(10))
AF33(vds3to1p(10))
AF33(vds3to1p(10)) lvds0to3p(17) L37)IFFIO_RX55p)IFFIO_RX55n lvds0to3n(17) L36 lvds0to3p(18) J36 DIFFIO TX17n A834 (vds8t6nfs)DIFFIO TX18 AF38 (vds8t6nfs)DIFFIO TX18 AF38 (vds8t6nfs)DIFFIO TX18 AF38 (vds8t6nfs)DIFFIO TX18 AF38 (vds8t6nfs)DIFFIO TX19 AF38 (vds8t6nfs)DIFFIO TX20 AF38 (vds8t6nfs)DIFFIO TX20 AF38 (vds8t6nfs)DIFFIO TX20 AF38 (vds8t6nfs)DIFFIO TX21 AF38 (vds8t6nfs)DIFFIO TX21 AF38 (vds8t6nfs)DIFFIO TX22 AF38 (vds8t6nfs)DIFFIO TX22 AF38 (vds8t6nfs)DIFFIO TX28 AF38 (vds8t6nfs)DIFFIO TX28 AF38 (vds8t6nfs)DIFFIO TX28 AF38 (vds8t6nfs)DIFFIO TX28 AF38 (vds8t6nfs)DIFFIO TX28 AF38 (vds8t6nfs)DIFFIO TX28 AF38 (vds8t6nfs)DIFFIO TX28 AF38 (vds8t6nfs)DIFFIO TX28 AF38 (vds8t6nfs)DIFFIO TX28 AF38 (vds8t6nfs)-IFFIO_RX56p IFFIO_RX56n lvds0to3p(18) J37 lvds0to3p(19) K36 \sim (vds0to3p(19) K36 (vds0to3p(19) K37 DIFFIO_RX57p | Lvds1to3n(1) AK36 | Lvds1to3p(2) AK38 BANK $\forall \mathbb{K}$ Uvdstto3p(2) M39 DIFFIO_RX20p Uvdsito3n(3) AJ36 Uvdsito3n(4) AJ39 Uvdsito3n(4) AJ39 Uvdsito3n(4) AJ39 Uvdsito3n(5) AJ37 Uvdsito3n(5) AJ37 Uvdsito3n(5) AJ37 Uvdsito3n(5) AJ37 Uvdsito3n(5) AJ37 Uvdsito3n(5) AJ37 Uvdsito3n(5) AJ37 Uvdsito3n(5) AJ37 Uvdsito3n(5) AJ37 Uvdsito3n(6) AJ37 Uvdsito3n(6) AJ37 Uvdsito3n(7) OIFFIO_RX23p OIFFIO_RX23n OIFFIO_RX24p lvds1to3n(5) AH36 lvds1to3p(6) AH39 se0to3(26) H39 se0to3(27) H38 se0to3(24) G39 se0to3(25) G38 se0to3(22) F38 lyds1to3n(6) AH38 lyds1to3p(7) AG37 DIFFIO_RX24n DIFFIO_RX25p DIFFIO_RX25n DIFFIO_RX62n DIFFIO_RX63p DIFFIO_RX63n DIFFIO_RX64p lvds1to3n(7) AG36 lvds1to3o(8) AF38 DIFFIO_RX26p lvds1to3p(9) AE38 se0to3(23) F39 E38 DIFFIO_RX26n DIFFIO_RX27p DIFFIO_RX27n I0_RX64n I0_RX65ρ se0to3(20) Udsitio3x(39) AF39 DIFFIO_RX27p
Udsitio3x(39) AF39 DIFFIO_RX27p
Udsitio3x(19)AF37 DIFFIO_RX28p
Udsitio3x(19)AF36 DIFFIO_RX28p
Udsitio3x(11)AE37 DIFFIO_RX28p se0to3(21) E39 se0to3(10) E36 I0_RX65n se0to3(10) IO_RX66p IO_RX66n se0to3(11) se0to3(19) se0t o3(17) se0t o3(17) se0t o3(16) ĬŎ_RX67n IO_RX68p se0to3(16) H36 se0to3(15) G36 se0to3(14) G37 se0to3(12) F36 lvds1to3n(12)AD36 lvds1to3p(13)AD39 IFFIO_RX30n I0_RX68n Lvds1to3p(14)AC37 Lvds1to3p(14)AC37 Lvds1to3p(14)AC37 DIFFIO_RX31n I0_RX69p I0_RX69n DIFFIO TX69n K99 self-03(41)
DIFFIO TX790 N89 self-03(38)
DIFFIO TX790 N81 self-03(38)
DIFFIO TX790 N81 self-03(38)
DIFFIO TX790 N81 self-03(38)
DIFFIO TX790 N82 self-03(38)
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DIFFIO TX790 N82 self-03(38)
DIFFIO TX790 N83 self-03(38)
DIFFIO TX790 N83 self-03(38)
DIFFIO TX790 N83 self-03(38) 10_RX70p 10_RX70p 10_RX70n 10_RX71p 10_RX71n DIFFIO_RX32p DIFFIO_RX32n DIFFIO_RX33p Lvds1to3n(14)AC36 Lvds1to3p(15)AC39 se0to3(13) se0to3(8) se0to3(9) se0to3(6) se0to3(7) se0to3(3) IO_RX72p IO_RX72n lvds1to3n(16)AB36 lvds1to3p(17)AB38 IFFIO_RX34n IO_RX73p \(\text{\text{Vds1to3n(17)AB39}}\) \(\text{DIFFIO_RX35c}\) \(\text{\text{Vds1to3n(18)AA37}}\) \(\text{DIFFIO_RX35c}\) se0to3(2) IFFIO_RX73n IFFIO_RX74p se0to3(4) se0to3(5) DIFFIO_RX35n DIFFIO_RX36p DIFFIO_RX36n DIFFIO_RX37p Lvds1to3n(18)AA36 Lvds1to3p(19)AA39 H34 F34 DIFFIO_RX74n DIFFIO_RX75p DIFFIO_RX75n se0to3(0) Lvds1to3n(19)AA38 DIFFIO_RX37n DIFF10_TX75n | U26 | se0t.03(55) se0to3(1) F35 selto3(62) AG28 GPIO_B1_0 4 se0to3(62) P26 GPI0_B2_0 AH28 se1to3(63) R26 se0to3(63) GPIO_B1_1 GPIO_B2_1 S80F1508B1 S80F1508B2 JESTEROER TM-4

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LVDS

lvds1to3p(19:0) ____

(vds1to3n(19:0)

lvds0to3o(19:0)

lyds0to3n(19:0)

Development FPGA 3 Banks 3 and 4

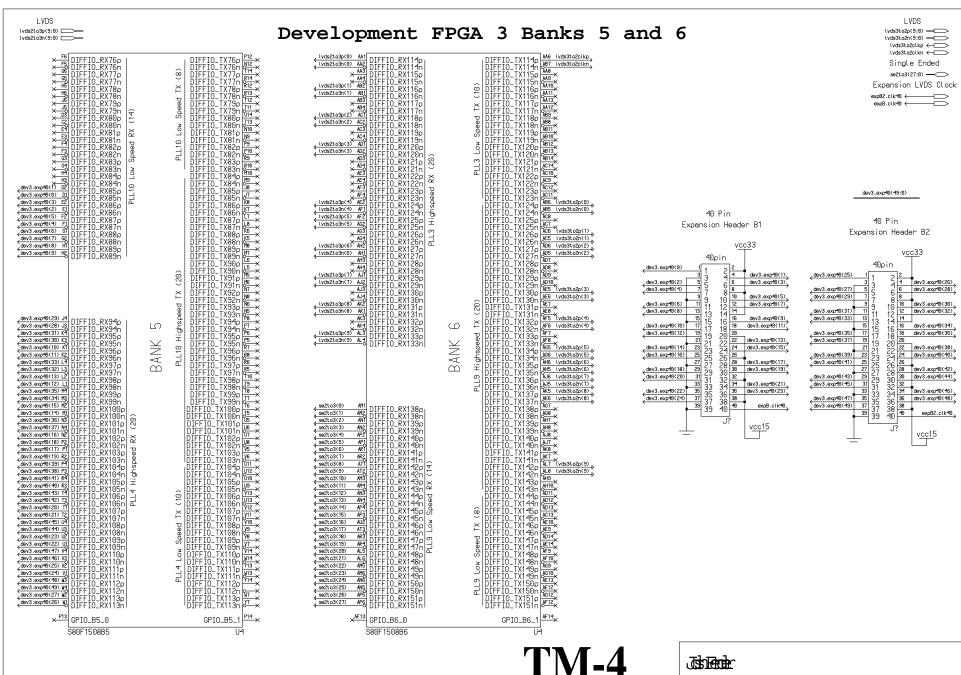
_ ddr.A3A(1) E21				A36 ddr.SCL3A
ddr.BA3A(1) G22	GPIO_B3_0 GPIO_B3_1		GPIO_B3_67 GPIO_B3_68	F32
× J22	GPTO B3 2		GPT0 R3 69	K29 💭
× M22	GPIO_B3_3		GPI0_B3_70	E33 × B37 ×
C P22	GPIO_B3_4 GPIO_B3_5		GPIO_B3_71	F33 ×
ddr.A3A(0) E22	GP1U_B3_6		GP10_B3_73	G31 × D35 ×
ddr.A3A(10) X F22	GPIO_B3_7 GPIO_B3_8		GPIO_B3_74	H31 X
, N23	GPIO_B3_8 GPIO_B3_9		GPIO_B3_75	J30 ×
€ H23 K23	GPI0_B3_10		GPĪO_B3_77	C36 ×
ddr.DM3A(8) F23	GPIO_B3_11 GPIO_B3_12		CPIO_B3_78	E34 🖔
. ddr.BA3A(0) × F24	GPI0_B3_13		GP10_B3_/1 GP10_B3_72 GP10_B3_73 GP10_B3_75 GP10_B3_75 GP10_B3_77 GP10_B3_79 GP10_B3_80 GP10_B3_80 GP10_B3_81	G32 × D36 ×
G24	GPI0_B3_14		GPIO_B3_81	E35 ×
× K24	GPIO_B3_15 GPIO_B3_16		GPIO_B3_82	
× N24 → H24	GPIO_B3_17			B23 ddr.CB3A(1)
ddr.DM3A(4) F25	GPIO_B3_18 GPIO_B3_19		DQ5T0 DQ5T1	E23 ddr.CB3A(4)
× J24			0.0512	D23 ddr.CB3A(5)
× L24	GPIO_B3_21		D0513	A23 ddr.CB3A(0) A24 ddr.CB3A(2)
X P24	GPIO_B3_22 GPIO_B3_23		DQ5T4 DQ5T5	B24 ddr.CB3A(6)
€ H25 N25	GPIO_B3_23 GPIO_B3_24 GPIO_B3_25		DQ5T6 DQ5T7	024 ddr.CB3A(3) → D24 ddr.CB3A(7)
_ddr.RASn3A F26	GPIO_B3_20 GPIO_B3_21 GPIO_B3_22 GPIO_B3_23 GPIO_B3_24 GPIO_B3_25 GPIO_B3_26		DQ5T7	C23 ddr.DQS3A(8)
` 627	GPIO_B3_27			205 11 20011001
€ K25 H26	GPTN R3 28		DQ6T0	B25 ddr.DQ3A(32) E25 ddr.DQ3A(33)
ddr.DM3A(6) D30	GPIO_B3_29 GPIO_B3_30	\sim	DQ6T0 DQ6T1 DQ6T2	D25 ddr.DQ3A(37)
× M25	GPIO_B3_31 GPIO_B3_32		רוטשען ן	A26 ddr.DQ3A(36) B26 ddr.DQ3A(34)
ddr. WEn3A × F27	GPIO_B3_31 GPIO_B3_32 GPIO_B3_33	\Rightarrow	DQ6T4	C26 ddr.DQ3A(38)
ddr.A3A(13) E29	HPH B3 34	\equiv	DQ6T5 DQ6T6	D26 ddr.DQ3A(39)
_ddr.CASn3A × M26	GPI0_B3_35	$\widetilde{\mathbf{a}}$	I DQ6T7	E26 ddr.DQ3A(35) C25 ddr.DQS3A(4)
_ddr.Sn3A(0) F29	GPIO_B3_36 GPIO_B3_37		1 DQS6T	, , , , , , , , , , , , , , , , , , ,
× N27	GPTN R3 38		, DQ7T0	B27 ddr.DQ3A(40) C27 ddr.DQ3A(45)
× 126	GPIO_B3_39 GPIO_B3_40		DQ7T1	D27 ddr.DQ3A(44)
Ç K26	GPIO_B3_40 GPIO_B3_41		DQ7T2 DQ7T3	E27 ddr.D03A(41)
_ ddr .DM3A(5) × E30	GPTO B3 42		DQ7T4	B28 ddr.DQ3A(43) A28 ddr.DQ3A(42)
ddr.SDA3A A35	GPIO_B3_43 GPIO_B3_44		DQ7T5 DQ7T6	D28 ddr.DQ3A(46)
ddr.Sn3A(1) F30	GPIN R3 45		DQ7T7 DQS7T	E28 ddr.DQ3A(47)
× M27	GPI0_B3_46		DQS7T	C28 ddr.DQS3A(5)
× G28	GPIO_B3_47 GPIO_B3_48		DQ8T0	A29 ddr.DQ3A(48)
∑ D32 327	GPI0_B3_49		DQ8T1	B29 ddr.DQ3A(49) C29 ddr.DQ3A(53)
× M28	GPIO_B3_50 GPIO_B3_51		DQ8T2 DQ8T3	C30 ddr.DQ3A(54)
∵ H28	GPI0_B3_52		DQ8T4	A30 ddr.DQ3A(52)
€ E31 K27	GPI0_B3_53		DQ8T5	A31 ddr.DQ3A(55) B31 ddr.DQ3A(51)
Ç G29	GPIO_B3_54 GPIO_B3_55		DQ8T6	C31 ddr.DQ3A(50)
ddr.DM3A(7) ^ D33	GPT0 B3 56		Daset	B30 ddr.DQS3A(6)
× 123	GPIO_B3_57 GPIO_B3_58		ı DQ9T0	A32 ddr.DQ3A(60)
× J28	GPIO_B3_59		D09T1	C32 ddr .DQ3A(57)
€ B35 C35	IGPIN R3 60		DQ9T2 DQ9T3 DQ9T4	B32 ddr.DQ3A(56) A34 ddr.DQ3A(63)
Ç K28	GPIO_B3_61 GPIO_B3_62		DU9[3 D09T4	A33 ddr.DQ3A(61)
∑ F31 B36	LCDIU B3 E3		I nngts	C33 ddr.DQ3A(62) C34 ddr.DQ3A(58)
× D34	GPIO_B3_64 GPIO_B3_65 GPIO_B3_66		DQ9T6 DQ9T7 DQS9T	B34 ddr.DQ3A(59)
× J29	GPI0_B3_66		DQS9T	B33 ddr.DQS3A(7)
× P23				M24
	RUP3		RDN3	^
:	S80F1508B3		U-	1

dev3.nib(0) B3 dev3.nib(2) D4 dev3.nib(3) G8 dev3.nib(4) G7 dev3.nib(5) E5	GPIO_B4_0 GPIO_B4_1 GPIO_B4_2 GPIO_B4_3		GPIO_B4_71 GPIO_B4_72 GPIO_B4_73 GPIO_B4_74	H17 dev3.nib(1) K17 C18 ddr.A3A(6) P18 ×
dev3.nib(6) C4 dev3.nib(7) G9 dev3.nib(8) H9 dev3.nib(10) E6 dev3.nib(10) J10 dev3.nib(11) D6	GPIO_B4_4 GPIO_B4_5 GPIO_B4_6 GPIO_B4_7 GPIO_B4_8 GPIO_B4_9		GPIO_B4_74 GPIO_B4_75 GPIO_B4_76 GPIO_B4_77 GPIO_B4_78 GPIO_B4_79 GPIO_B4_80	17 × http://dx.ddr.A3A(4) bts://dx.ddr.A3A(3)
dev3.nib(12) F8 dev3.nib(13) F7 dev3.nib(14) D7 dev3.nib(15) E7 dev3.nib(16) D5 dev3.nib(17) F9	GPIO_B4_10 GPIO_B4_11 GPIO_B4_12 GPIO_B4_13 GPIO_B4_14 GPIO_B4_15 GPIO_B4_16		GPIO_B4_81 GPIO_B4_82 GPIO_B4_83 GPIO_B4_84 GPIO_B4_85 GPIO_B4_86 GPIO_B4_87	N18 × M18 × G18 × H18 × J18 × P19 ×
dev3.nib(18) C5 dev3.nib(19)	GPIO_B4_17 GPIO_B4_18 GPIO_B4_19 GPIO_B4_20 GPIO_B4_21		GPIO_B4_88 GPIO_B4_89 GPIO_B4_90	N19 × P20 × N20 ×
dev3.nib(24) J12 ddr.A3A(11) F10 dev3.nib(28) E8 dev3.nib(30) H11 dev3.nib(32) G11 dev3.nib(32) A4	GPIO_B4_23 GPIO_B4_24 GPIO_B4_25 GPIO_B4_26 GPIO_B4_27 GPIO_B4_28		DQ0T1 DQ0T2 DQ0T3 DQ0T4 DQ0T5 DQ0T6	B6
dev3.nib(37)	GPIO_B4_30 GPIO_B4_31 GPIO_B4_32 GPIO_B4_33 GPIO_B4_34	SANK 4	DQ0T7 DQS0T DQ1T0 DQ1T1 DQ1T2 DQ1T3	B7 dev3.nib(36) C9 ddr.D03A(1) B9 ddr.D03A(4) A9 ddr.D03A(9) C11 ddr.D03A(5) A10 ddr.D03A(5)
dev3.nib(41) D8 dev3.nib(41) D8 ddr.A3A(12) E10 ddr.CLKE3A(1) E9 ddr.RESETn3A D10 dev3.nib(42) J14	GPIO_B4_36 GPIO_B4_37 GPIO_B4_38 GPIO_B4_39 GPIO_B4_40 GPIO_B4_41 GPIO_B4_41		DQ114 DQ1T5 DQ1T6 DQ1T7 DQS1T	C10 ddr.DQ3A(7) A11 ddr.DQ3A(2) B10 ddr.DQ3A(6) B10 ddr.DQ3A(0) A12 ddr.DQ3A(9)
dev3.nib(44) G12 dev3.nib(44) G12 dev3.nib(44) G12 ddr.DM3A(2) F13 ddr.DM3A(1) F12	GPĪO_B4_42 GPIO_B4_43 GPIO_B4_44 GPIO_B4_45 GPIO_B4_67 GPIO_B4_67 GPIO_B4_48 GPIO_B4_48 GPIO_B4_49		DQ2T0 DQ2T1 DQ2T2 DQ2T3 DQ2T4 DQ2T5 DQ2T6	D12 ddr.D03A(12) → E12 ddr.D03A(8) → E13 ddr.D03A(10) → B12 ddr.D03A(11) → B13 ddr.D03A(14) → C13 ddr.D03A(14) → D13 ddr.D03A(15) →
ddr.CLKE3A(6) E11 dev3.nib(45) H14	GPIO_B4_50 GPIO_B4_51 GPIO_B4_52 GPIO_B4_53 GPIO_B4_54 GPIO_B4_55		D02T7 D0S2T D03T0 D03T1 D03T2 D03T3	C14 ddr.DQ3A(16) C14 ddr.DQ3A(16) D14 ddr.DQ3A(17) E14 ddr.DQ3A(20) A14 ddr.DQ3A(21) B14 ddr.DQ3A(18)
dev3.nib(47)	GPIO_B1_57 GPIO_B4_58 GPIO_B4_59 GPIO_B4_60 GPIO_B4_61 GPIO_B4_61		D0314 D0315 D0315 D0376 D0377 D0S3T	B15 ddr.DQ3A(22) → E15 ddr.DQ3A(23) → D15 ddr.DQ3A(19) → C15 ddr.DQS3A(2) → A16 ddr.DQ3A(24) →
dev3.nib(48)	GPIO_B1_63 GPIO_B4_64 GPIO_B4_65 GPIO_B4_66 GPIO_B4_67 GPIO_B4_68		DQ4T1 DQ4T2 DQ4T3 DQ4T4 DQ4T5 DQ4T6	D16 ddr.DQ3A(29) → A17 ddr.DQ3A(25) → B16 ddr.DQ3A(28) → B17 ddr.DQ3A(26) → D17 ddr.DQ3A(27) → E17 ddr.DQ3A(31) →
√ ddr.DM3A(3) ^ F17 × P17 × F15	GPIO_B4_69 GPIO_B4_70 RUP4 S80F1508B4		DÕAT7 DQS4T RDN4 U4	C17 ddr.DQ3A(30) C16 ddr.DQS3A(3) E16 X



TM-4

Jahrenia Vinesiyof Dooto



CHOOL TO CHERALLY

Development FPGA 3 Banks 7 and 8

AF20 AG19 ASse2to3(187) AK18	GPIO_B7_0		GPIO_B7_71 GPIO_B7_72 GPIO_B7_73 GPIO_B7_74 GPIO_B7_75	AL11 sse2to3(76)
AG19	GPI0_B7_1		GPIO_B7_72 GPIO_B7_73	AK11 sse2to3(73) AV4 sse2to3(77)
AF19	IGPTO R7 2		GPI0_B7_73	
sse2to3(108) AM18	GPI0_B7_3		GPIO_B7_74 GPIO_B7_75	AP9 sse2to3(78) AU4 ddr.SCL38
eep2t n3(112) AP19	GPI0_B7_4		ĞPİÖ_B7_75	AR7 ddr.CASn3B
sep2t o3(110) AP19	GPIO_B7_5		GP10 B7 76	AV5 sse2to3(75)
AH18	GPI0_B7_6		GF 1U_D / _ / /	AR6 sse2to3(67)
^AG18	GPIO_B7_7		GPIO_B7_78 GPIO_B7_79	AP8 sse2to3(74)
XAJ18	GPIO_B7_8 GPIO_B7_9		GPIO_B7_79 GPIO_B7_80	AU5 sse2to3(80)
ÇAP18	GPIO_B7_9 GPIO_B7_10		GPIO_B7_80 GPIO_B7_81	AL10 sse2to3(68)
sse2to3(113) AN18	GPIO_B7_10		GPIO_B7_82	AT5 sse2to3(70)
_ddr.DM3B(8) AR18	GPT0_B7_12		GPIO_B7_82 GPIO_B7_83	AM9 sse2to3(66)
AG17	GPIO_B7_12 GPIO_B7_13		GPIO_B7_84	AN9 sse2to3(91)
AH17	GPIO_B7_14		GPIO_B7_85	AV3 ddr SDA3B
×AF18 ×AF18	GPI0_B7_15		CPIN R7 QC	AR5 sse2to3(64)
VALIO	GPI0_B7_16		GPI0_B7_87	AN7 sse2to3(71)
AJ17 AU18	IGPIO R7 17		GPI0_B7_88	AN8 sse2to3(82) AT4 sse2to3(65)
XAC17	GPIO_B7_18 GPIO_B7_19		GPIO_B7_89 GPIO_B7_90	AT4 sse2to3(65) AT6 ddr.Sn3B(0)
sse2to3(103) AM17	GPI0_B7_19		GPIO_B7_87 GPIO_B7_88 GPIO_B7_89 GPIO_B7_90	AP7 sse2to3(72)
4G16	GPI0_B7_20		GPI0_B7_91	A 7 GGCECGC(7E)
sse2to3(99) XM16	GPI0_B7_21		00000	AU6 ddr.DQ3B(59)
sse2to3(106) AP16	GPIO_B7_20 GPIO_B7_21 GPIO_B7_22 GPIO_B7_23 GPIO_B7_24		DQ0B0	AV6 ddr.DQ3B(58)
sse2to3(104) AK16	GPIO_B7_23 GPIO_B7_24		DQ0B1 DQ0B2	AU7 ddr.DQ3B(63)
AH16	GPIO_B7_25		DQ0B3	AN7 ddr.DQ3B(57)
sse2to3(111) AL16	GPIO_B7_25 GPIO_B7_26		DQ0B4	AU8 ddr.DQ3B(60)
AJ16 AF15	IGPIN R7 27		DQOB5	ANG ddr.DQ3B(62)
AF15	GPIO_B7_28 GPIO_B7_29 GPIO_B7_30		DQOB6	AW8 ddr.DQ3B(56)
A 2267 (02) W 12	GP10_B7_29	_	DQ0B7	AV8 ddr.DQ3B(61)
ddr.DM3B(4) AR16	GP10_B7_30	1 -	l Dasob	AV7 ddr.DQS3B(7)
sse2to3(96) AM15	GPIO_B7_31 GPIO_B7_32 GPIO_B7_33 GPIO_B7_34 GPIO_B7_35			AU9 ddr.DQ3B(51)
sse2to3(109) AN15	GPI0_B7_32	\cong	DQ1B0	AU9 ddr.DQ3B(51) AV9 ddr.DQ3B(50)
sse2to3(97) AK15	GPIO_B7_33 GPIO_B7_34	\geq	DQ1B1	AN9 ddr.DQ3B(54)
sse2t.o3(101) Al 15	GPIO_B7_33 GPIO_B7_34	$ \triangleleft$	DQ1B2	AU11 ddr .DQ3B(48)
ddc 43R(1) 4P14	GPI0_B7_35	$ \Delta $	DQ1B3	AW10 ddr .DQ3B(53)
AH15	GPIO_B7_36 GPIO_B7_37		DQ1B4 DQ1B5	AU10 ddr.DQ3B(55)
sse2to3(90)^AG14	GPIO_B7_38		DQ1B6	AW11 ddr.DQ3B(49)
sse2to3(93) AM14	GPIO_B7_39		DQ1B7	AV11 ddr.DQ3B(52)
ddr DM3B(5) AR11	GPIO_B7_40		DQS1B	AV10 ddr.DQS3B(6)
×AH14	ĞPİÖLB7LAĞ		DWOTD	
ddr.A3B(10) AP12	GPI0_B7_42		DQ2B0	AV12 ddr .DQ3B(46)
ddr.A3B(0) AP13	GPI0_B7_43		DOOD4	AT12 ddr .DQ3B(42)
AG13 . sse2to3(100) AN12	GPI0_B7_44		DQ2B1 DQ2B3 DQ2B4 DQ2B5 DQ2B5 DQ2B6 DQ2B7 DQS2B	AR12 ddr .DQ3B(44)
sse2to3(100) AN12 sse2to3(102) AN13	GPI0_B7_45		DQ2B3	AR13 ddr.DQ3B(40) AV12 ddr.DQ3B(47)
sse2to3(94) AK14	LCPTO R7 46		DQ2B4	AV13 ddr .DQ3B(43)
sse2to3(95) AL14	GP10_B / _ 4 /		DQ2B5	ALI13 ddr D03R(45)
ddr.DM3B(6) AT10	ĞPİÖ_B7_48 GPİO_B7_49		D0586	AT13_ddr_D038(41)
sse2to3(92) AR9	GPIO_B7_49 GPIO_B7_50		D0000	AU12 ddr.DQS38(5)
	GPIO_B7_50 GPIO_B7_51		. D#95B	ν
ddr.BA3B(0) AR10	CDIO DZ EG		DQ3B0	AU14 ddr.DQ3B(38)
ddr NEn38 AT8	CPTO R7 52		D03R1	AT14 ddr .DQ3B(39)
sse2to3(87) AM13	CPIO P7 54		ก็ก็สียื่	AR14 ddr .DQ3B(36)
ddr.BA3B(1) AP11			DQ3B2 DQ3B3 DQ3B4	AN14 ddr.DQ3B(34)
sse2to3(83) AM12	GP10_B7_56		ĎãšBă	AV14 ddr .DQ3B(35)
sse2to3(88) AL13	1 GP1U_B / _5 /		1 110385	AV15 ddr .DQ3B(33)
sse2to3(88)^AL13 ddr.RASn3B AT9	GPI0_B7_58		DQ3B6 DQ3B7 DQS3B	AR15 ddr.DQ3B(32) AT15 ddr.DQ3B(37)
cca2t a3(86) AV13	GPIO_B7_59		DQ3B7	AU15 ddr.DQS38(4)
dde Sp3R(1) AUS	GPIO_B7_60		' DQS3B	NOTO GGI (DEGODICT)
sse2to3(98) AN11	I GPIO_B7_61		50.45	AW16 ddr.CB3B(3)
eea2t n3(69) AM11	GPIO_B7_62 GPIO_B7_63		DQ4B0 DQ4B1	AT16 dde CR3R(1)
sse2to3(84) AR8	GPIO_B7_63		DQ4B2	AN17 ddr.CB3B(2)
sse2to3(85) AP10	GPIO_B7_64 GPIO_B7_65		DQ4B3	AV16 ddr.CB3B(7)
sse2to3(79) AK12	GPIO_B7_65 GPIO_B7_66		DQ4B4	AV17 ddr.CB3B(6)
sse2to3(81) AL12	GPIO_B7_67		DQ4B5	AT17 ddr.CB3B(5)
ddr.DM3B(7) AT7	IGPIN R7 69		DQ4B6	AR17 ddr.CB3B(4)
ddr A3B(13) AW4	GPIO_B7_68 GPIO_B7_69		DQ4B7	AU17 ddr.CB3B(0)
sse2to3(89) AN10	GPIO_B7_70		DOSAB	AU16 ddr .DQS3B(8)
4140				1017
×AN16	RUP7		RDN7	AP17
	S80F1508B7		U	1
	JOUR IDUOD /		U-	1

sse2to3(52) AR35	GPI0_B8_0		GPIO_B8_67	AK24 sse2to3(6)
sse2to3(55) AT36	GPI0_B8_1		GPIO_B8_68	AP24 ddr. A3B(6)
sse2to3(53) AN32	OLIO-DO-1			AR24 ddr.DM3B(3)
sse2to3(44) AR34	GPI0_B8_2		GPIO_B8_69	AG23
sse2to3(41) AU36	GPIO_B8_3		GPI0_B8_70	AP23 ddr . A3B(4)
, AN33	GPI0_B8_4		- GP10 88 71	AK23 sse2to3(0)
	GPI0_B8_5		GPIO_B8_72 GPIO_B8_73	
sse2to3(47)^AL30	GPI0_B8_6		GPI0_B8_73	AM23 sse2to3(4)
sse2to3(49) AM31	GPIO_B8_7		GPI0_B8_74	AF22
sse2to3(48) AT35	GPIO_B8_8		ĞPİÖ_B8_75	AG22 AG22
sse2to3(54) AN31	GPTO B8 9		ODTO DO 70	AN23 sse2t o3(10)
sse2to3(57) AP33			GPI0_B8_76	AR22 ddr.A3B(3)
sse2to3(51) AV37	GPI0_B8_10		GPIO_B8_77	AH22
	GPIO_B8_11		GPIO_B8_78 GPIO_B8_79	AF21.
sse2to3(42) AR33	GPI0_B8_12		GPI0_B8_79	MF21
sse2to3(38) AK29	GPI0_B8_13		GPI0_B8_80	AJ22 sse2to3(2)
sse2to3(45) AP32	GPIO_B8_14		GPI0_B8_81	AL22 sse2to3(8)
sse2to3(43) AV35	GP10_B8_15		GPIO_B8_82	AP22 ddr.A3B(2)
sse2to3(37) AL29			00 10 00 00	AN22 sse2to3(1)
sse2to3(56) AT34	GPIO_B8_16		GPI0_B8_83	
sse2to3(39) AV36	GPI0_B8_17			AT23 ddr.DQ3B(27)
	GPI0_B8_18		ı DQ5B0	
sse2to3(40) AP31	GPIO_B8_19		DQ5B1	AV23 ddr.DQ3B(29)
sse2to3(32) AK28	GPI0_B8_20		DQ5B2	AR23 ddr .DQ3B(31)
sse2to3(46) AU35	GPIO_B8_21			AW23 ddr.DQ3B(25)
ddr .RESETn3B AT33	GP10_B8_21		DQ5B3	AW24 ddr.DQ3B(24)
sse2to3(33) AL28	GPIO_B8_22 GPIO_B8_23		DQ5B4	AV24 ddr.DQ3B(28)
sse2to3(50) AN30	GPI0_B8_23		DQ5B5	AU24 ddr.DQ3B(26)
	GPI0_B8_24		DQ5B6	
sse2to3(29) AM29	GPIN R8 25		DQ5B7	AT24 ddr.DQ3B(30)
sse2to3(30) AR32	GP10_B8_26		DQ5B7 DQS5B	AU23 ddr .DQS3B(3)
sse2to3(31) AP30	GPIO_B8_27		DWOOD	
sse2to3(26) AK27			DOCDO	AV25 ddr.D03B(23)
sse2to3(35) AW36	GPI0_B8_28		DQ6B0	AR25 ddr.DQ3B(18)
sse2to3(23) AM28	GPIO_B8_29	∞	DQ6B1	AT25 ddr.DQ3B(17)
sse2to3(20) AH27	GP10_B8_30		DQ6B2	AW26 ddr .DQ3B(22)
	GPIO_B8_31		DQ6B3	
sse2to3(25) AL27	GPIN BR 32	\sim	DQ6B4	AV26 ddr DQ3B(19)
ddr.CLKE3B(1)AT32	GPIO_B8_33 GPIO_B8_34	$\overline{}$	DQ6B5	AU26 ddr .DQ3B(16)
sse2to3(28) AN28	GPIO_B8_34	\overline{A}	DÕEBE	AT26 ddr.DQ3B(20)
_AG27	ODIO DO 37			AR26 ddr.DQ3B(21)
_ sse2to3(36) AN29	GPI0_B8_35	\simeq	DQ6B7	AU25 ddr.DQS3B(2)
sse2to3(19) AR31	GPIO_B8_36		' DQS6B	THE GOT TO GOOD TEX
sse2to3(27) AW35	GB10_B8_31			AV27 ddr.DQ3B(11)
	GPI0_B8_38		ı DQ7B0	
ddr.A3B(12) AR30	GPI0_B8_39		DQ7B1	AU27 ddr .DQ3B(14)
sse2to3(22) AM27	GPIO_B8_40		D0782	AW28 ddr .DQ3B(15)
sse2to3(17) AK26	GPIO_B8_41		DQ7B2 DQ7B3	AR27 ddr.DQ3B(13)
sse2to3(18) AL26	OD TO DO 40		00704	AV28 ddr.DQ3B(10)
ddr.CLKE3B(0)AT31	GPI0_B8_42		DQ7B4	AU28 ddr DQ3B(12)
sse2to3(15) AH26	GPI0_B8_43		DQ7B5	AT28 ddr.DQ3B(9)
sse2to3(24) AP29	GPI0_B8_44		DQ7B6	AR28 ddr.DQ3B(8)
	GPIO_B8_45		DQ7B7 DQS7B	
ddr.A3B(9) AP28	GPI0_B8_46		D087B	AT27 ddr.DQS3B(1)
AG26	GPIO_B8_47		Daoid	
ddr.A3B(11) AR29			nnopn	AW29 ddr DQ3B(7)
ddr.A3B(7) AP27	GPIO_B8_48		DQ8B0	AV29 ddr.DQ3B(3)
	GPIO_B8_49		DQ8B1	AU29 ddr.DQ3B(6)
sse2to3(13) AH25	GPI0_B8_50		DQ8B2	AU30 ddr.DQ3B(2)
	GPI0_B8_51		DQ8B3	
	GP10_B8_52		DQ8B4	AW30 ddr .DQ3B(1)
sse2to3(14) AM26	GPI0_B8_53		DQ8B5	AW31 ddr DQ3B(4)
sse2to3(11) AK25	CPIN RQ 54		Dűébő	AV31 ddr DQ3B(5)
ddr.A3B(8) AN27	GPI0_B8_55			AU31 ddr.DQ3B(0)
ddr.DM3B(1) AP26	GL10-D9-22		DQ8B7	AV30 ddr.DQS3B(0)
AF25	GPI0_B8_56		¹ DQS8B	
sse2to3(9) AM25	GPIO_B8_57			AW32 sse2to3(34)
4504	GPIO_B8_58		ı DQ9B0	
100/E) XHIZT	GPIO_B8_59		DQ9B1	
ddr.A3B(5) XA725	GP10_B8_60		DQ9B2	AV32 sse2to3(21)
ddr.DM3B(2) AP25	GPIO_B8_61		l Dajaba	AW34 sse2to3(63)
sse2to3(7) AJ24			00004	AW33 sse2to3(61)
sse2to3(12) AL24	GPIO_B8_62 GPIO_B8_63		DQ9B4 DQ9B5	AU33 sse2to3(60)
sse2to3(16) AN24	GP10_B8_63		nnagg	AU34 sse2to3(58)
sse2to3(5) AM24	GPI0_B8_64		DQ9B6	AV34 sse2to3(59)
4 SOCIACO MILI	GPI0_B8_65		DQ9B7	AV33 sse2to3(3)
×AG24	GPI0_B8_66		DQS9B	MY33 SSBC103(3)
				L
× ^{AF23}	RUP8		RDN8	AH24
] ``
;	S80F1508B8		U-	4



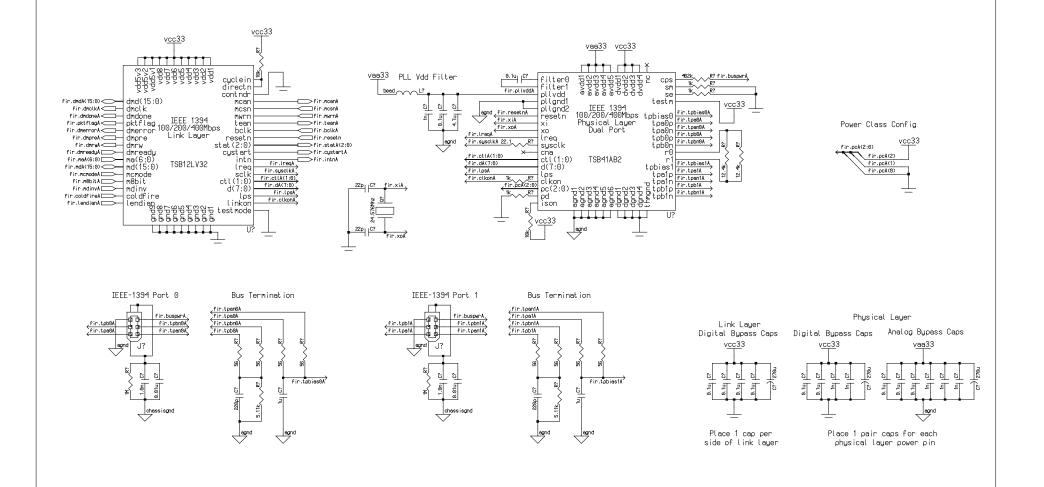
DDR SDRAM Bank B

, ddr.WEn3B	ddr.WEn
ddr.clk38(2:0)	ddr.clk(2:0)
ddr.SDA3B	ddr SDA
ddr.clkn3B(2:0)	ddr.clkn(2:0)
ddr.DM3B(8:0)	ddr.DM(8:0)
ddr.DQS3B(8:0)	ddr DQS(8:0)
. ddr.Vref3B	ddr.Vref
ddr.RASn3B	ddr RASn
ddr.CASn3B	ddr.CASn
ddr.Sn3B(1:0)	ddr Sn(1:0)
ddr.BA3B(1:0)	ddr.BA(1:0)
ddr.DQ3B(63:0)	ddr DQ(63:0)
ddr.A3B(13:0)	ddr.A(13:0)
ddr.CB3B(7:0)	ddr.CB(7:0)
ddr.CLKE3B(1:0)	ddr.CLKE(1:0)
, ddr.RESETn3B	ddr.RESETn
ddr.SCL3B	ddr.SCL
	uui 130L

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IEEE-1394 (Firewire) Channel A

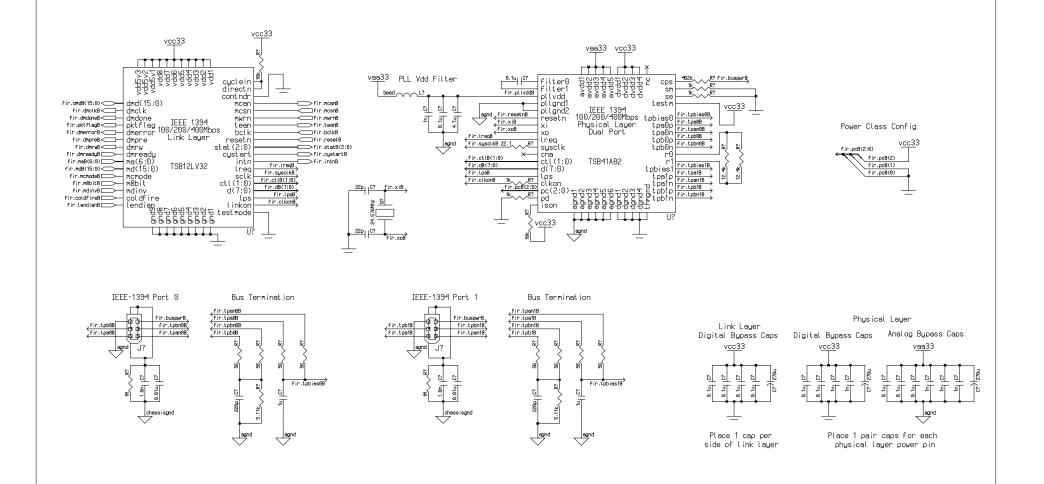




TM-4

Jastedar Vivasilyof Booto

IEEE-1394 (Firewire) Channel B

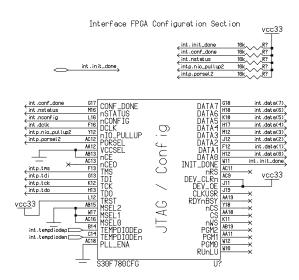




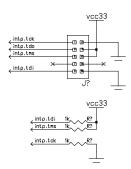
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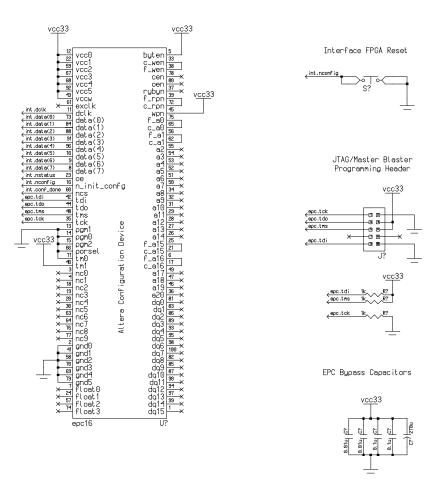
Interface FPGA Device Configuration



JTAG/Master Blaster Programming Header



Enhanced Configuration Device and JTAG Connector



TM-4

Jish Herder University of Torotto devcfg.tdk3
devcfg.tms
devcfg.tdi0

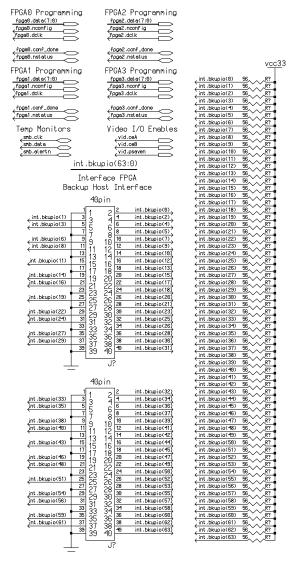
Interface FPGA IO Banks (PCI & Device Programming)

→ lpci.intbn → lpci.intdn → lpci.idsel | lpci.ed(63:0) | lpci.cben(7:0) → lpci.devseln → lpci.lockn → loci.perrn → lpci.serrn → lpci.m66en → lpci.stopn → lpci.per → loci,req64n → lpci.ack64n → lpci.per64 → loci pmen

	PCI Bu	18	
Lpci.ed(18) F22	GPIO_B3_0 GPIO_B3_1 GPIO_B3_1 GPIO_B3_2 GPIO_B3_3 GPIO_B3_4 GPIO_B3_6 GPIO_B3_6 GPIO_B3_6 GPIO_B3_8 GPIO_B3_9 GPIO_B3_10 GPIO_B3_11	DQ7T0 DQ7T1 DQ7T2 DQ7T3 DQ7T4 DQ7T5 DQ7T6 DQ7T7 DQ87T	R20
Lpci.cben(4) D16	D05T0	DQ8T0 DQ8T1 DQ8T2 DQ8T3 DQ8T4 DQ8T5 DQ8T6 DQ8T7 DQ8ST	B22 lpci.ed(21) A22 lpci.ed(22) C22 lpci.ed(28) D22 lpci.ed(35) A23 lpci.ed(25) C23 lpci.ed(23) E23 lpci.ed(23) E23 lpci.ed(24) D23 lpci.id(24)
tpci.ad(8)	D06T0 D06T1 D06T2 D06T3 D06T4 D06T5 D06T6 D06T6 D06T7 D0S6T	DQ9T0 DQ9T1 DQ9T2 DQ9T3 DQ9T4 DQ9T5 DQ9T6 DQ9T7 DQS9T	A24 lpci.ad(29) C25 lpci.ad(30) A25 lpci.inten D24 lpci.ad(28) B24 lpci.ad(28) B25 lpci.ad(31) A26 lpci.gntn B26 lpci.ad(27) C24 lpci.ad(27)
× ^{J18}	RUP3 S30F780B3	RDN3 U?	<u>к19</u> ×

(pci.edf4s)	GPIO.B4.0 GPIO.B4.1 GPIO.B4.2 GPIO.B4.2 GPIO.B4.3 GPIO.B4.4 GPIO.B4.5 GPIO.B4.7 GPIO.B4.7 GPIO.B4.9 GPIO.B4.10 GPIO.B4.11 GPIO.B4.12 GPIO.B4.13 GPIO.B4.13 GPIO.B4.13	D02T0 D8 × D02T1 B8 × D02T2 B9 vci.ed(31) D02T3 B9 vci.ed(32) D02T5 B8 dover0.td(8) D02T6 B8 dover0.td(8) D02T6 B8 dover0.td(8) D02T7 A9 (pci.ed(35)) D02T7 B9 (pci.ed(35))
Lpci.intdn	D0010 D0011 D00112 D0013 D0013 D0014 D0017 D0016 D0016 D0017 D0017	D03T0 E19 Loci acd(41)
## Smb.data	DQ1T0 DQ1T1 DQ1T2 DQ1T3 DQ1T3 DQ1T4 DQ1T5 DQ1T6 DQ1T7 DQ1T7	D04T0 B12
× H11	RUP4 S30F780B4	RDN4 G11 ×

Proged.com/ down	Foga2.noonfig. Foga2.cot(4) Foga2.cot(4) Foga2.cot(4) Foga2.cot(4) Foga2.cot(4) Foga2.dot(6) Foga2.dot(7) Foga2.dot(7) Foga2.dot(7) Foga2.dot(7) Foga2.dot(7) Foga2.dot(7) Foga2.dot(7) Foga2.dot(7) Foga2.dot(7) Foga2.dot(7) Foga2.dot(7) Foga2.dot(7)
int.blupio(49) 11	vid.ceB vid.pseven vid.pseven fpga3.nconf_ig fpga3.conf_done fpga3.dcik fpga3.conf_done fpga3.dcik fpga3.dcik
Int. blougio(5) Kg DIFFIO = XX65p DIFFIO = XX76p DIFFIO = XX65p DIFFIO = XX65p DIFFIO = XX65p DIFFIO = XX65p DIFFIO = XX65p DIFFIO = XX65p DIFFIO = XX65p	int. bkupio(28) int. bkupio(21) int. bkupio(21) int. bkupio(51) int. bkupio(51) int. bkupio(51) int. bkupio(53) int. bkupio(32) int. bkupio(32) int. bkupio(33) int. bkupio(33) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53) int. bkupio(53)



TM-4

Jish Redir University of Dicoto Dipswitches

Interface FPGA "Nibble" Bus IO

Panel LEDs
int.panLed(3:0) —

PCB LEDs
int.led(3:0) —

S30F780B1 U?	dev1.nib(17) #728	DIFFIO_RX4p DIFFIO_RX4p DIFFIO_RX5p DIFFIO_RX5p DIFFIO_RX5p DIFFIO_RX7p DIFFIO_RX7p DIFFIO_RX7p DIFFIO_RX1p	BANK 1	DIFFIO_TX3p DIFFIO_TX4p DIFFIO_TX4p DIFFIO_TX4p DIFFIO_TX5p DIFFIO_TX5p DIFFIO_TX6p DIFFIO_TX6p DIFFIO_TX6p DIFFIO_TX7p DIFFIO_TX7p DIFFIO_TX7p DIFFIO_TX9p DIFFIO_TX9p DIFFIO_TX9p DIFFIO_TX9p DIFFIO_TX9p DIFFIO_TX1p	715 dev1.nib(31) 720 dev1.nib(55) 721 dev1.nib(55) 722 dev1.nib(27) 725 dev1.nib(37) 727 dev1.nib(37) 728 dev1.nib(37) 729 dev1.nib(37) 729 dev1.nib(37) 729 dev1.nib(37) 729 dev1.nib(37) 729 dev1.nib(37) 729 dev1.nib(37)
		DIFFIO_RX19n		DIFFIO_TX19n	р ×

"Nibble" Bus for Dev FPGA 1

"Nibble" Bus for Dev FPGA 0

"Nibble" Bus for Dev FPGA 3 "Nibble" Bus for Dev FPGA 2 dev3.nib(28) AC24 dev3.nib(41) AC23 dev3.nib(41) AC23 GPI0_B8_0 GPI0_B8_1 dev3.nib(11) AB22 AH20 dev3.nib(22) dev3.nib(36) AE25 GPIO_B8_3 GPIO_B8_4 GPIO_B8_5 GPIO_B8_6 GPIO_B8_7 DQTBB | Ale28 dev3.nib(22)-DQTB1 | Ale28 dev3.nib(21)-DQTB2 | Ale28 dev3.nib(17)-DQTB3 | Ale28 dev3.nib(32)-DQTB3 | Ale21 dev3.nib(32)-DQTB5 | Ale21 dev3.nib(32)-DQTB5 | Ale21 dev3.nib(39)-DQTB5 | Ale21 dev3.nib(39)-DQTB7 | Ale28 dev3.nib(39)-DQTB7 | Ale28 dev3.nib(39)-DQTB7 | Ale28 dev3.nib(39)dev3.nib(26) AD24 dev3.nib(15) AB21 dev3.nib(0) AB20 dev3.nib(29) AC22 dev3.nib(14) AC20 A20 GPIO_B8_8

MA20 GPIO_B8_9

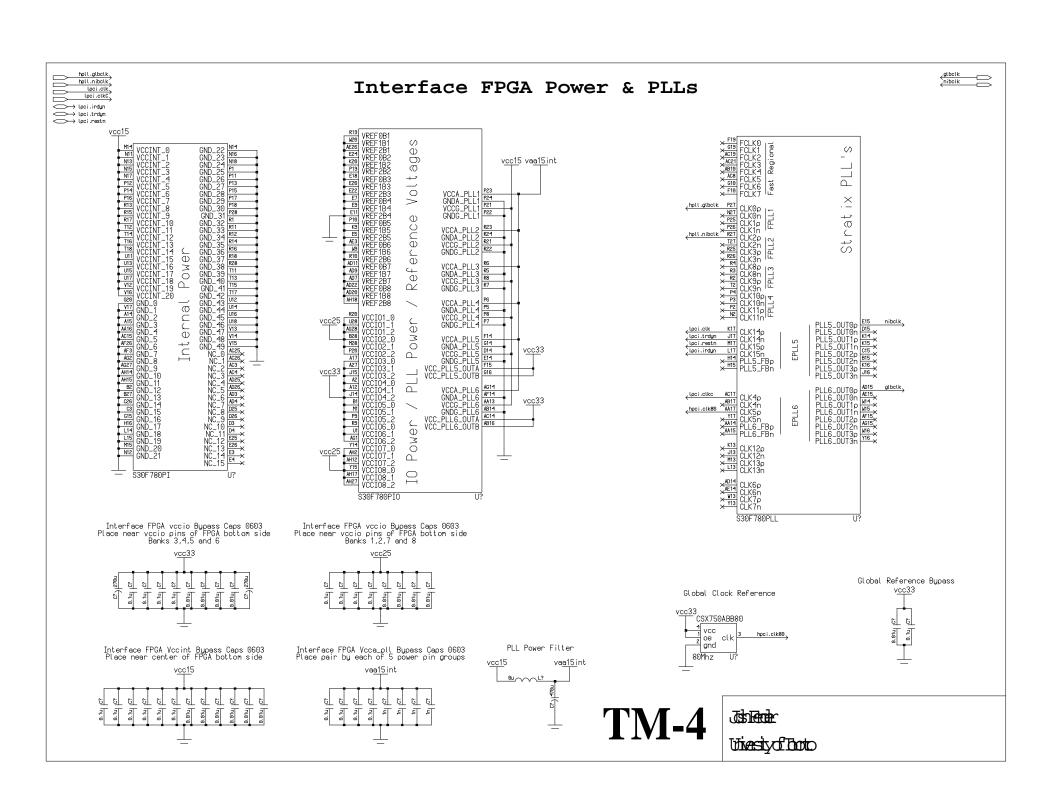
VI8 GPIO_B8_10

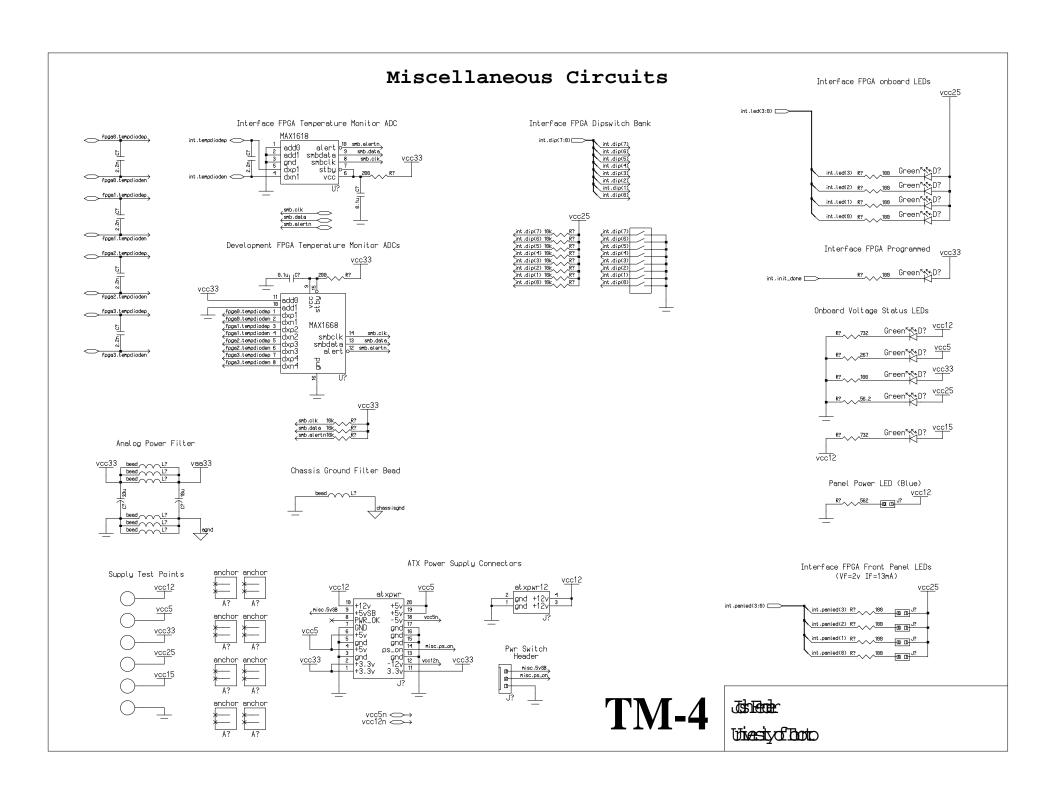
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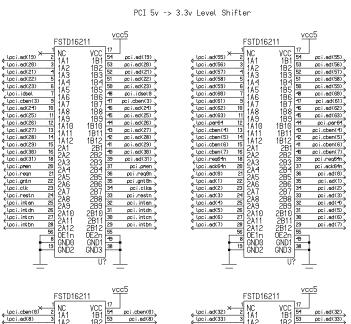
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PCI Expansion Slot and Interface FPGA Voltage Converters



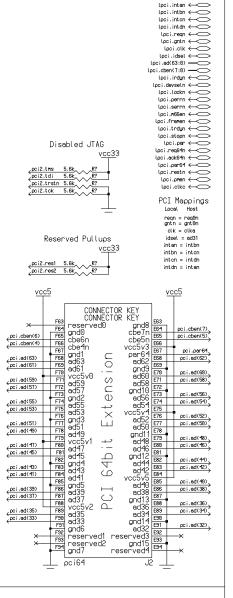
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Slot 0 PCI

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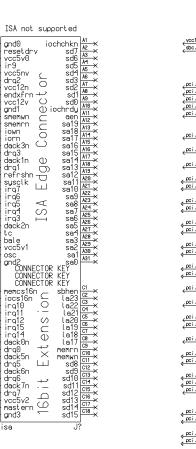
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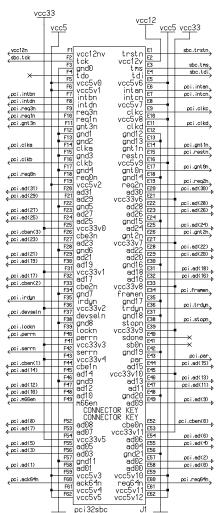
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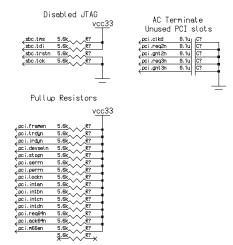
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Single Board Computer and PCI







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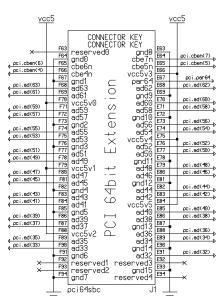
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