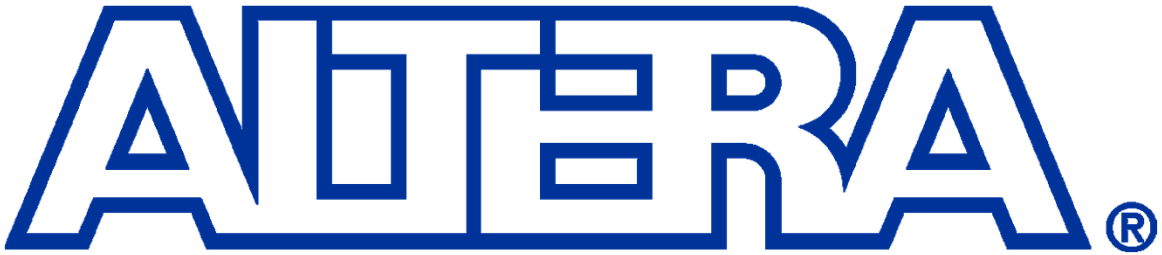

Learn to Design with Stratix III FPGAs' Programmable Power Technology and Selectable Core Voltage

Vaughn Betz and Sanjay Rajput

Agenda

- The power challenge
- Stratix® III power innovations
  - Programmable power
  - Selectable core voltage
  - Quartus® II power optimization
  - IO power: On-chip dynamic termination and DDR3
- Device selection and competitive overview
- Wrap up

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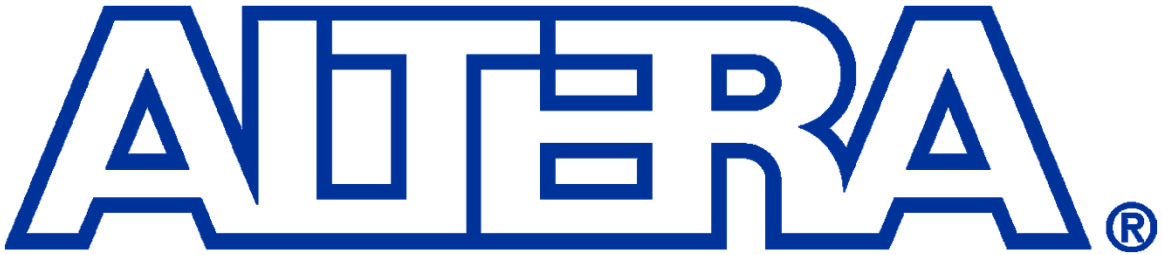


The Power Challenge

Altera's End Customers

Consumer Broadcast Automotive

Entertainment
Broadband
Audio/video
Video display

Broadcast
Studio
Satellite
Broadcasting

Automotive
Navigation
Entertainment

Test, Measurement and Medical

Instrumentation
Medical
Test equipment
Manufacturing

Communications

Wireless
Cellular
Basestations
Wireless LAN

Networking
Switches
Routers

Wireline
Optical
Metro
Access

Military and Industrial

Military
Secure comm.
Radar
Guidance and control

Security and Energy Management
Card readers
Control systems
ATM

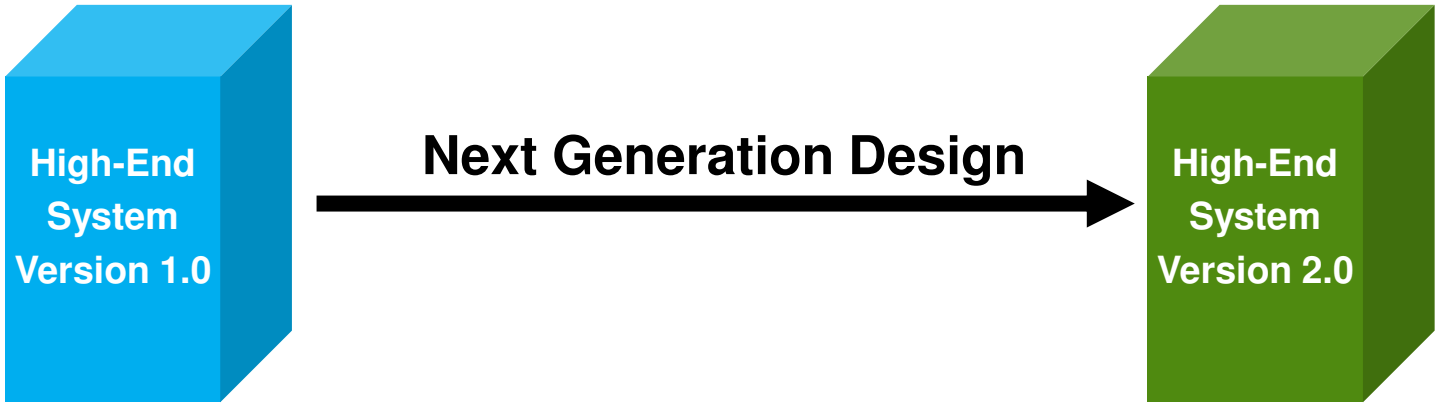
Computer and Storage

Computers
Servers
Mainframe

Storage
RAID
SAN

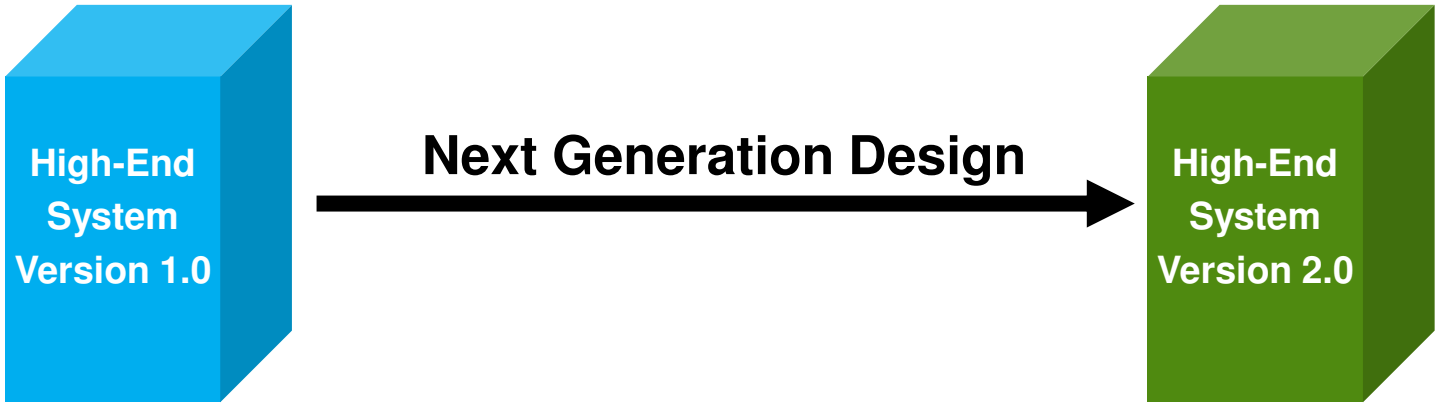
Office Automation
Copiers
Printers
MFP

The Challenge: System Design Trend



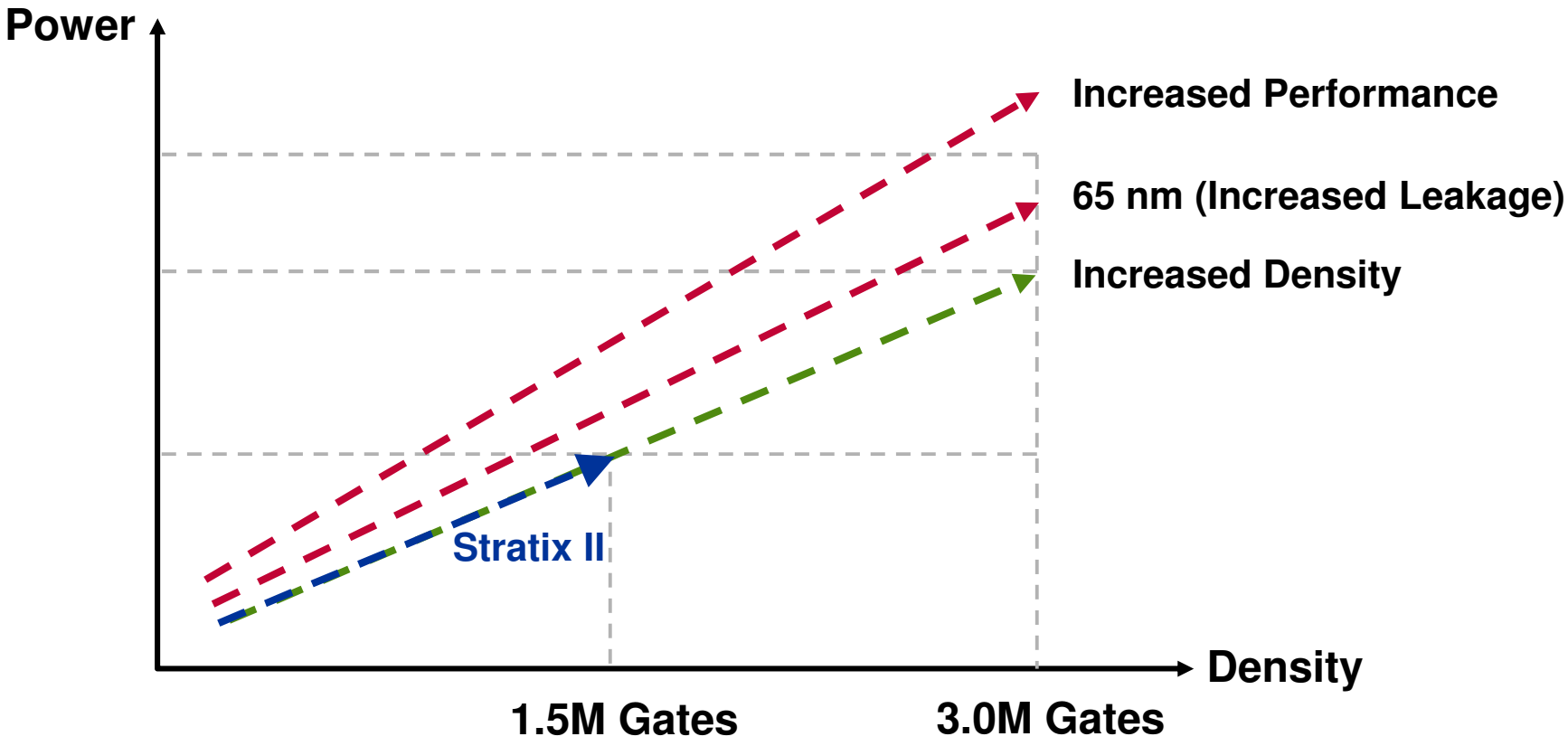
New System Requirements	Stratix III FPGAs
Higher processing performance	✓
Customizable capabilities	✓
Integration of more functions	✓
Re-programmability	✓
Similar physical constraints	✓

The Challenge: System Design Trend

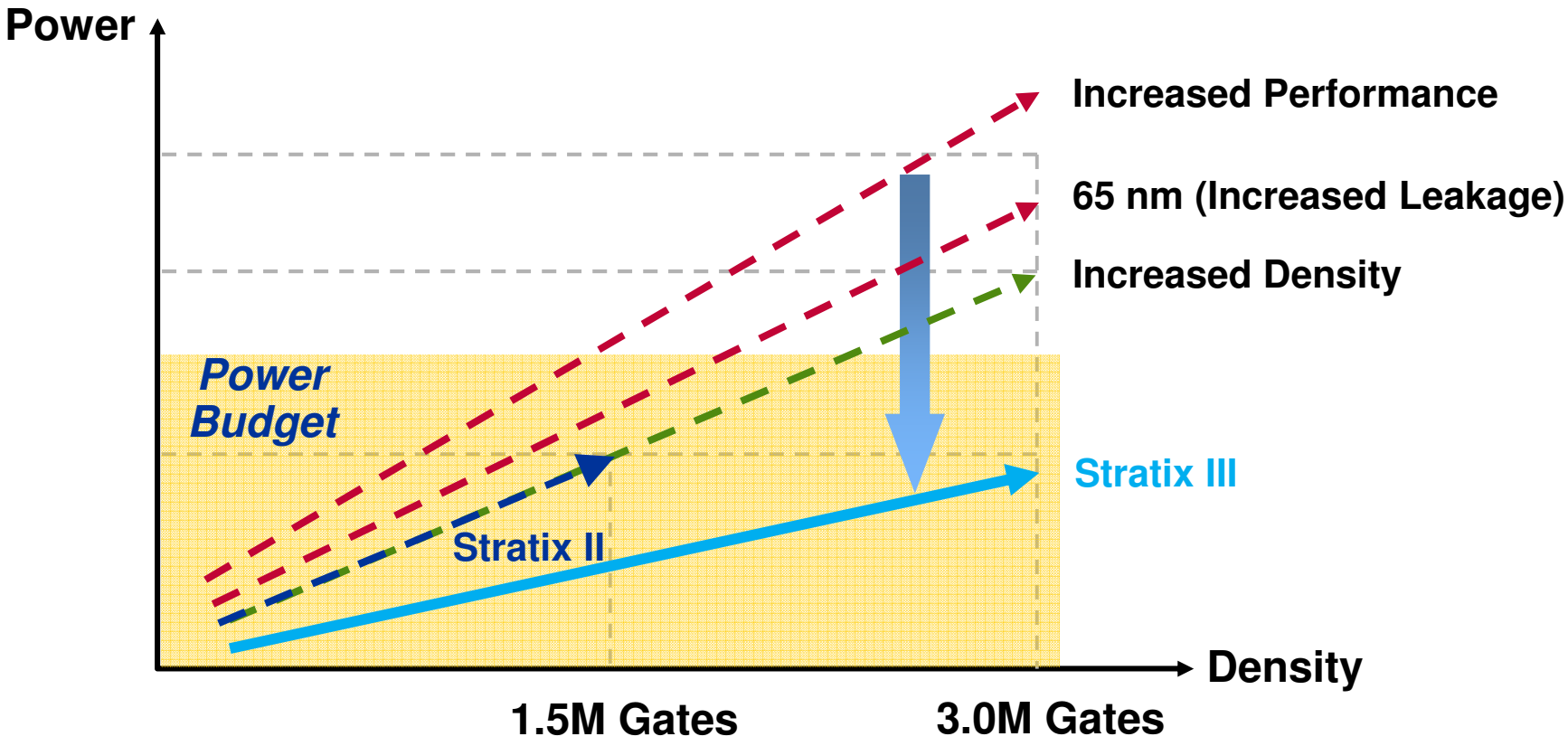


New System Requirements	Stratix III FPGAs
Higher processing performance	✓
Customizable capabilities	✓
Integration of functions	✓
Re-programmability	✓
Similar physical constraints	✓
Same or Lower Power Budget	✓

Meeting the Power Challenge



Meeting the Power Challenge



Stratix III FPGAs cut power by 50% vs. 90 nm

Benefits of Lower Power

- Stay within a fixed power budget
  - Chassis limits (heat, space, current)
  - Outside power budget → not an option
- Reduce system cost
  - Fewer/smaller heat sinks and fans
  - Smaller power supplies
- Increase reliability
  - No fans → no moving parts
  - Lower system temperature
- Reduce design time and effort to meet power and thermal constraints

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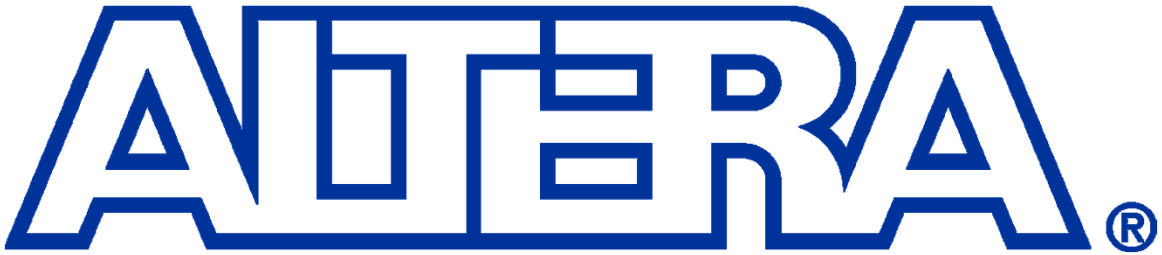

Stratix III FPGAs: Lower Power, Higher Performance

Industry-Leading Low-Power Technology

Stratix III FPGA Power Reduction Technique	Lower Static Power	Lower Dynamic Power
Silicon Process Optimizations	✓	✓
Programmable Power Technology	✓	✓
Selectable Core Voltage (0.9 V or 1.1 V)	✓	✓
Power Optimized DDR Memory Interface	✓	✓
Quartus II Software PowerPlay Power Analysis and Optimization	✓	✓

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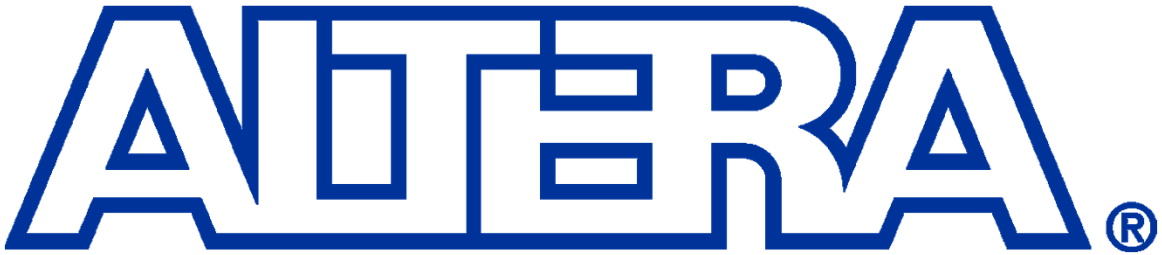
Leading Edge Process Technology

Increased Performance, Reduced Power

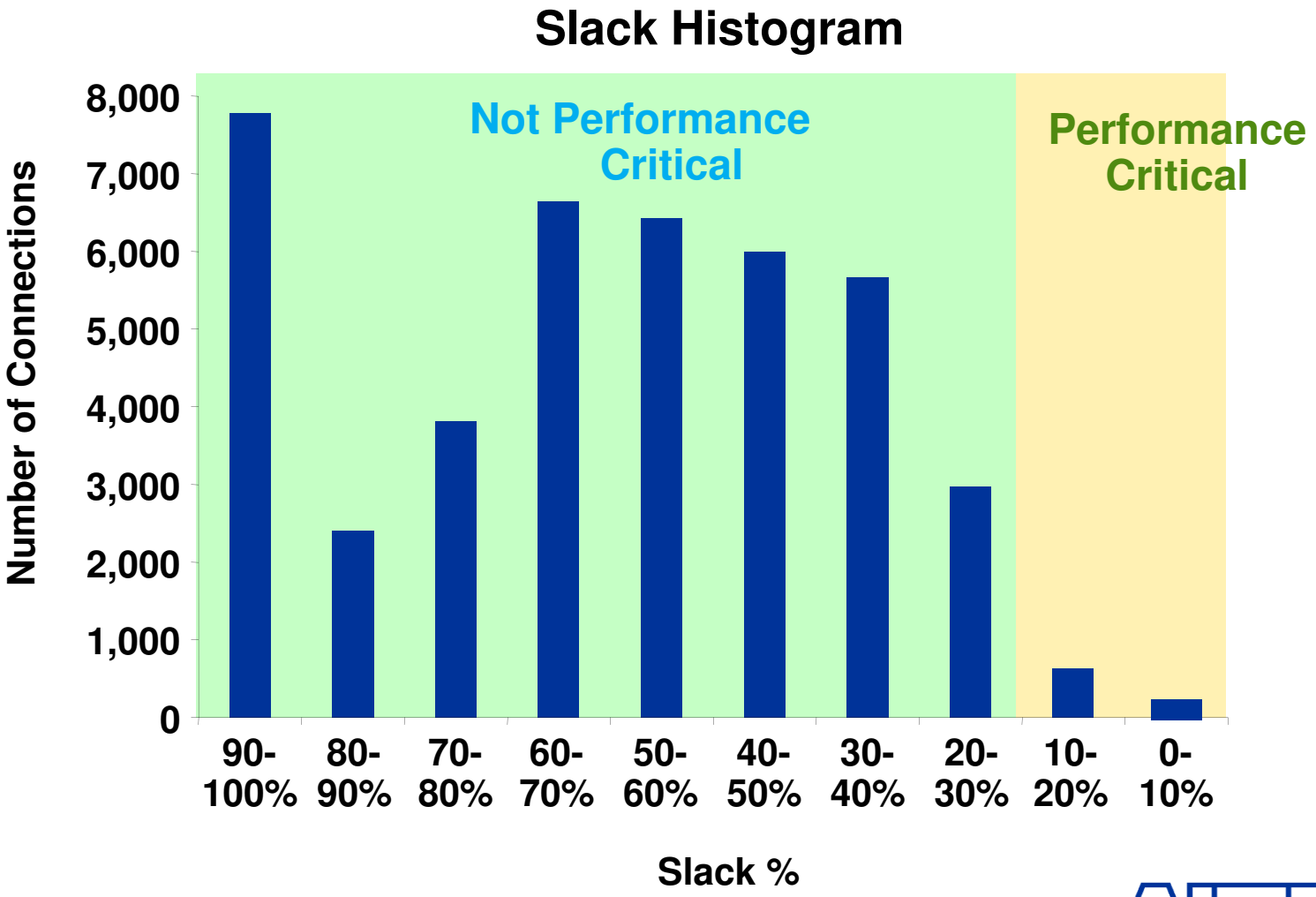
- Advanced 65-nm process
  - 15% capacitance reduction → reduces dynamic power 15%
  - Lower voltage → reduces dynamic power another 16%
- Multiple-gate oxide thicknesses (triple oxide)
  - Trade-off static power vs. speed per transistor
- Multiple-threshold voltages
  - Trade-off static power vs. speed per transistor
- Low-k inter-metal dielectric
  - Reduces dynamic power, increases performance
- Strained silicon
  - Increased performance
- Copper interconnect
  - Increased performance, reduced IR drop



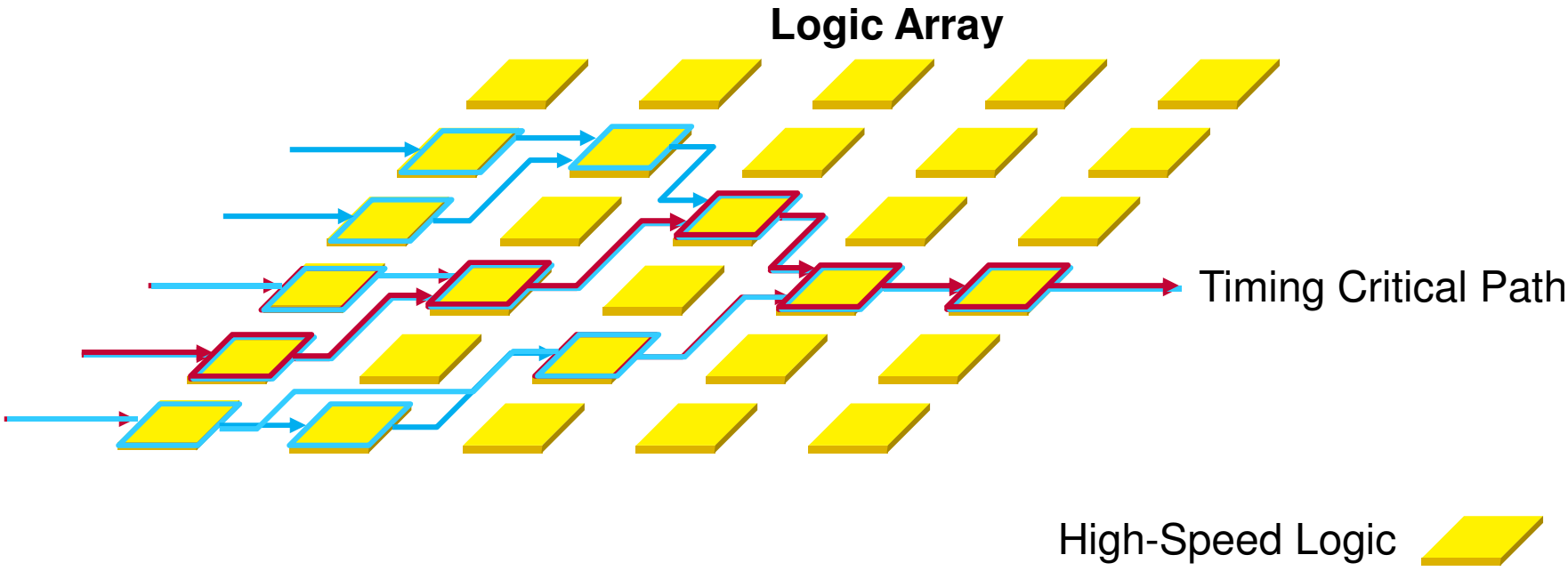
Programmable Power

Design-Specific Power Optimization

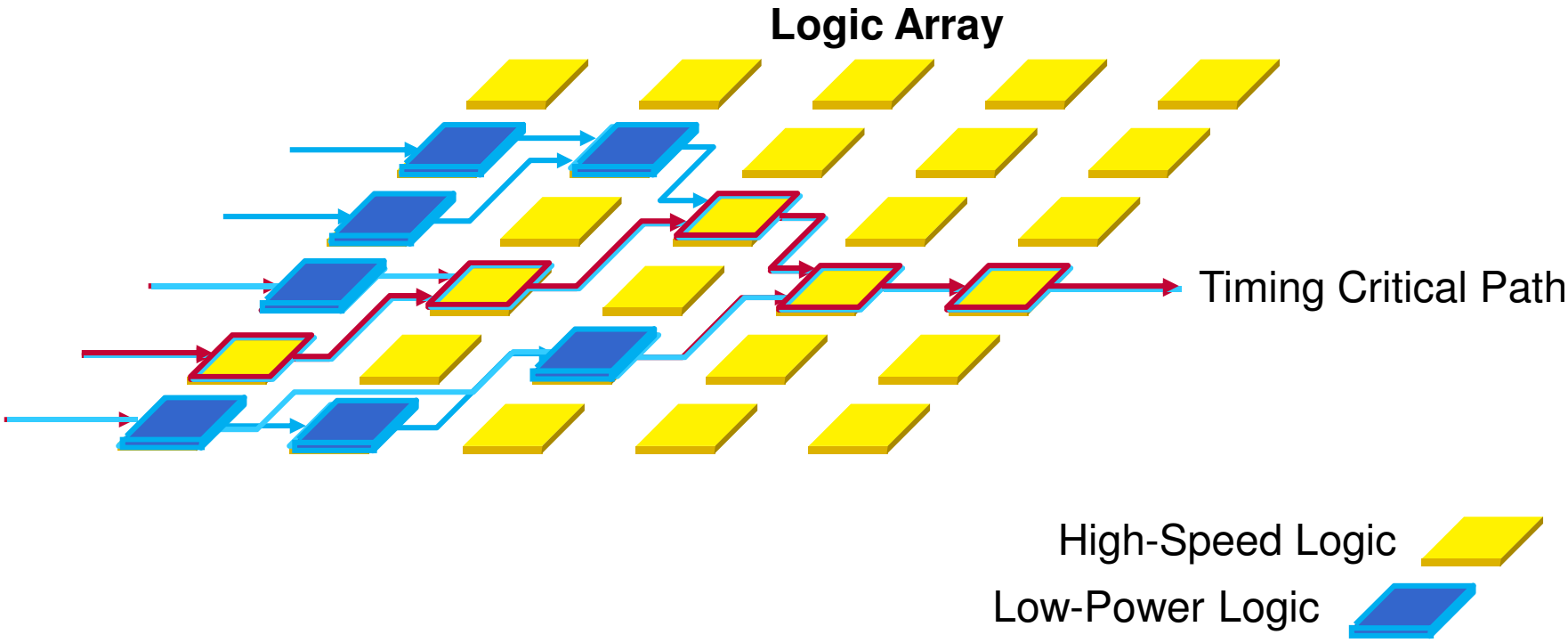
- Only a small fraction of logic is performance critical



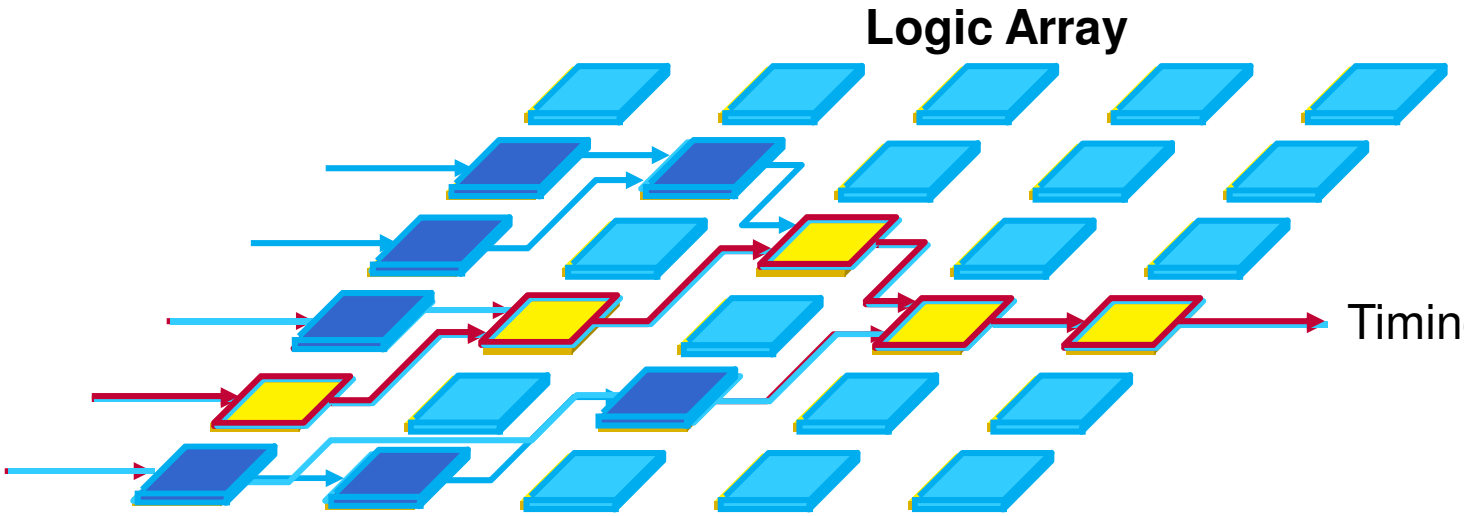
Programmable Power Technology



Programmable Power Technology



Programmable Power Technology



*** Power mapping fully automated by Quartus II based on timing constraints**

High-Speed Logic

Low-Power Logic

Unused Low-Power Logic

High performance where you need it, lowest power everywhere else

High Speed/Low Power

- Low-power mode for a tile results in
  - 60% reduction in static power
  - 5% reduction in dynamic power
  - ~20% increase in delay
    - Quartus II CAD system doesn't use on critical paths
    - No impact on system speed
- Tiles can be
  - Pair of Logic Array Blocks (LABs)
  - RAM block
  - DSP block

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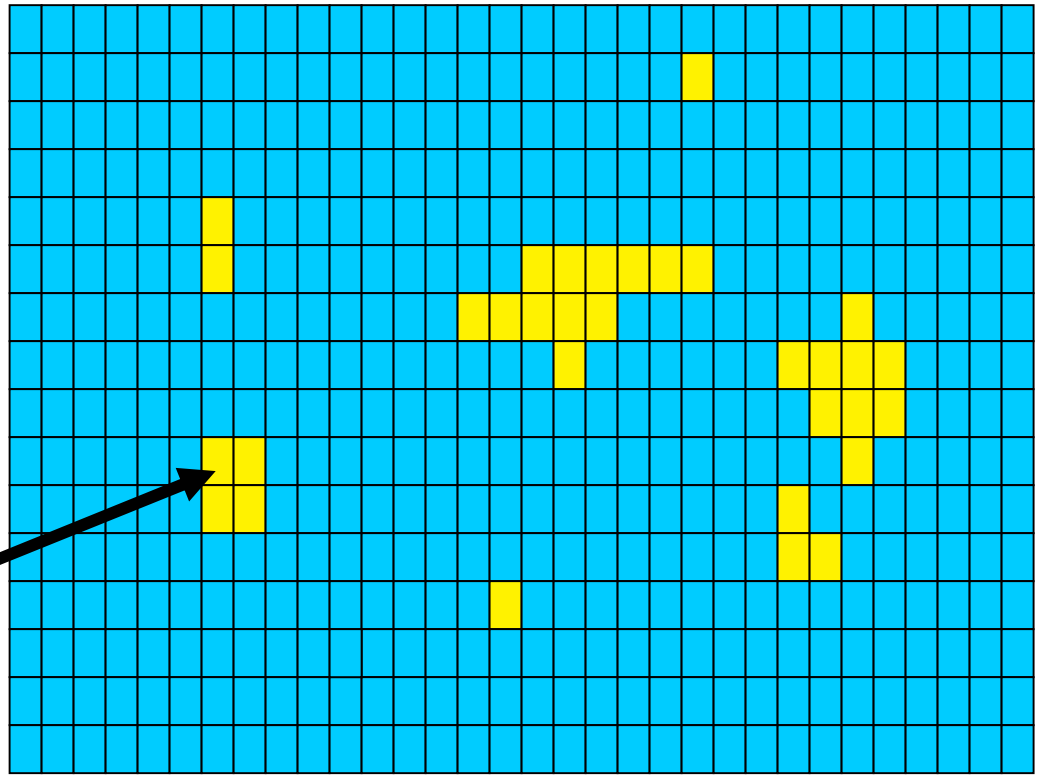
High-Resolution Power Control

Stratix III FPGA (EP3SL340) has **8,050 Tiles** for very high resolution power/performance optimization



Only a small percentage of high-speed tiles required to maintain design performance

Speed of the fastest LABs power of the slowest

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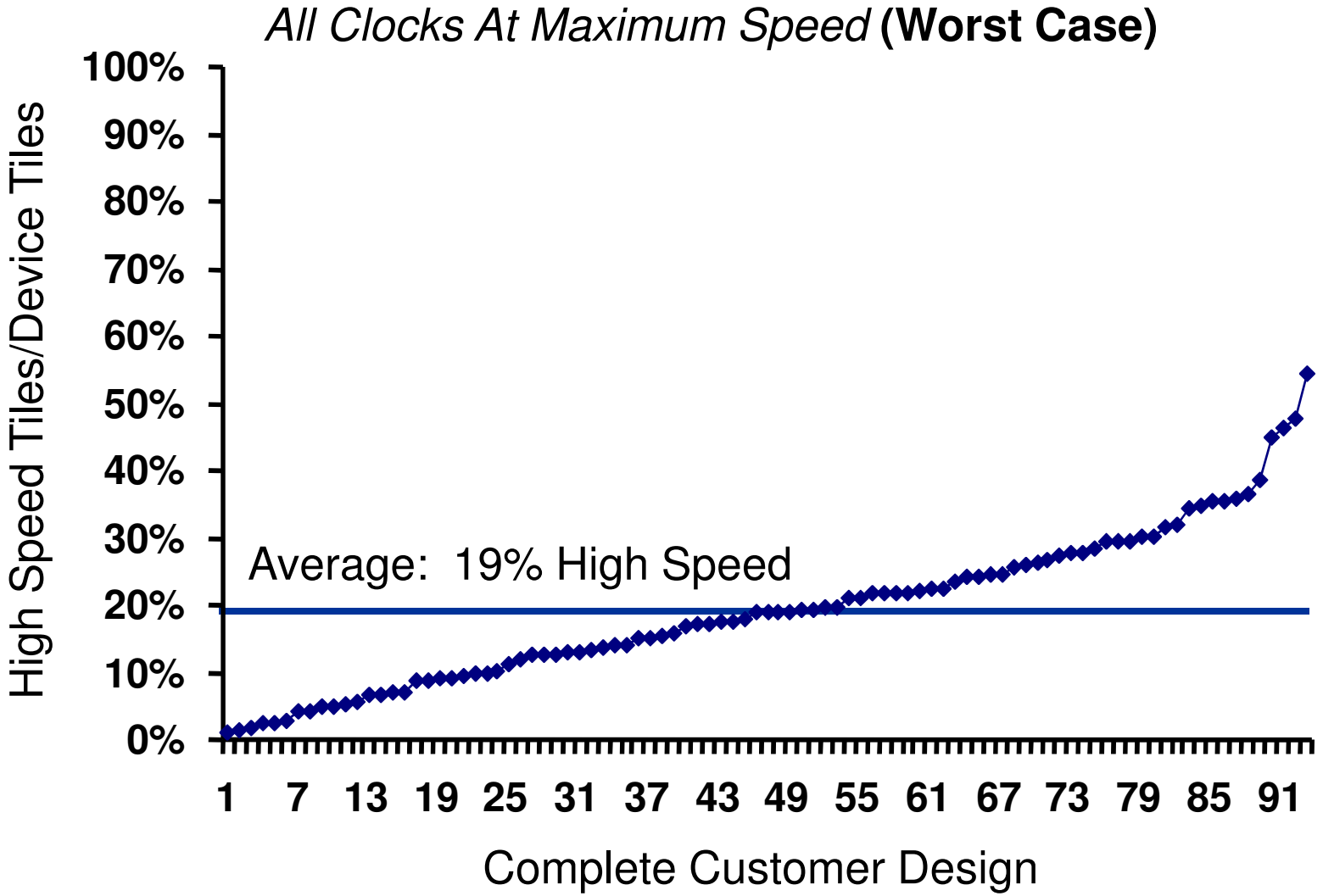
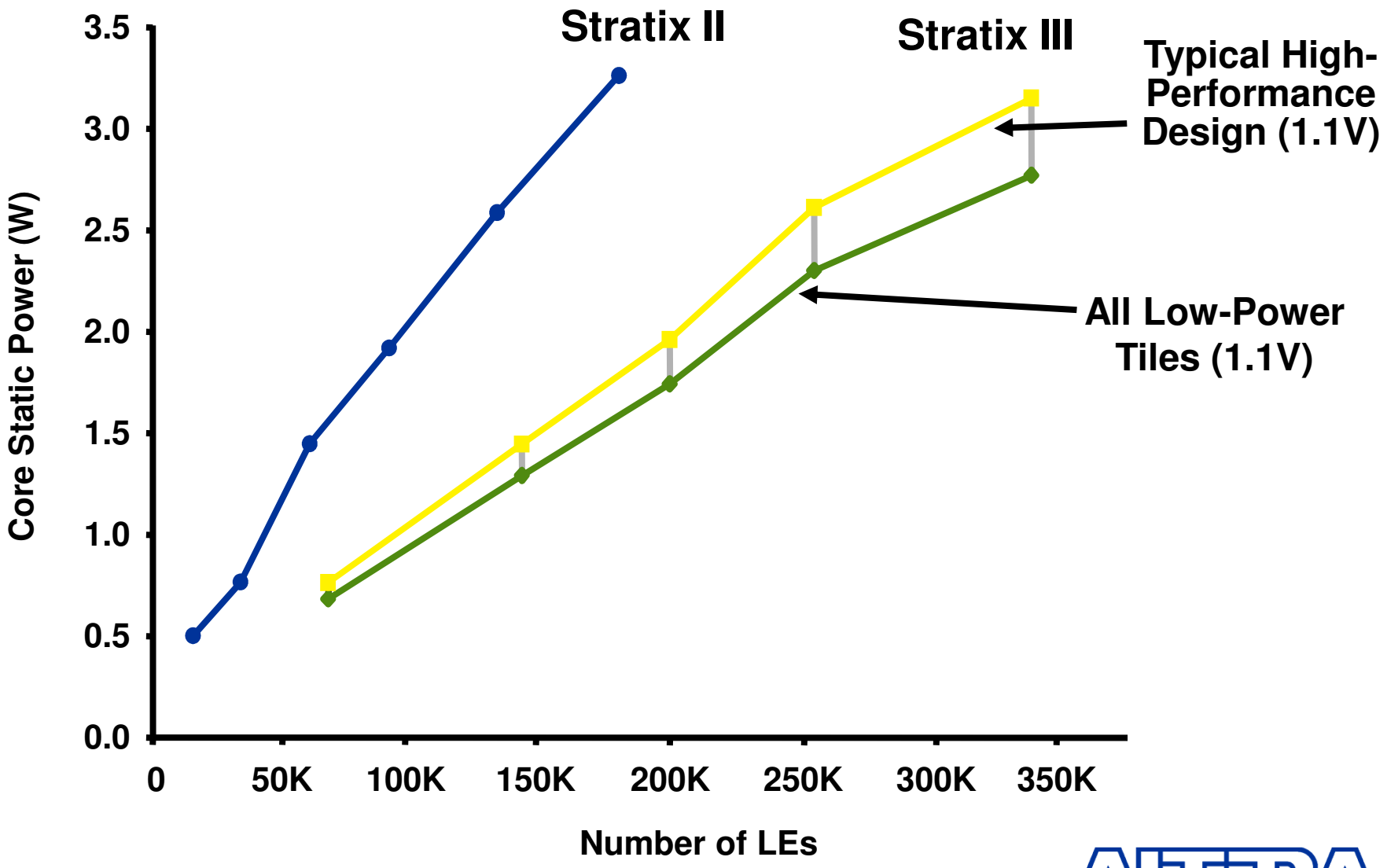
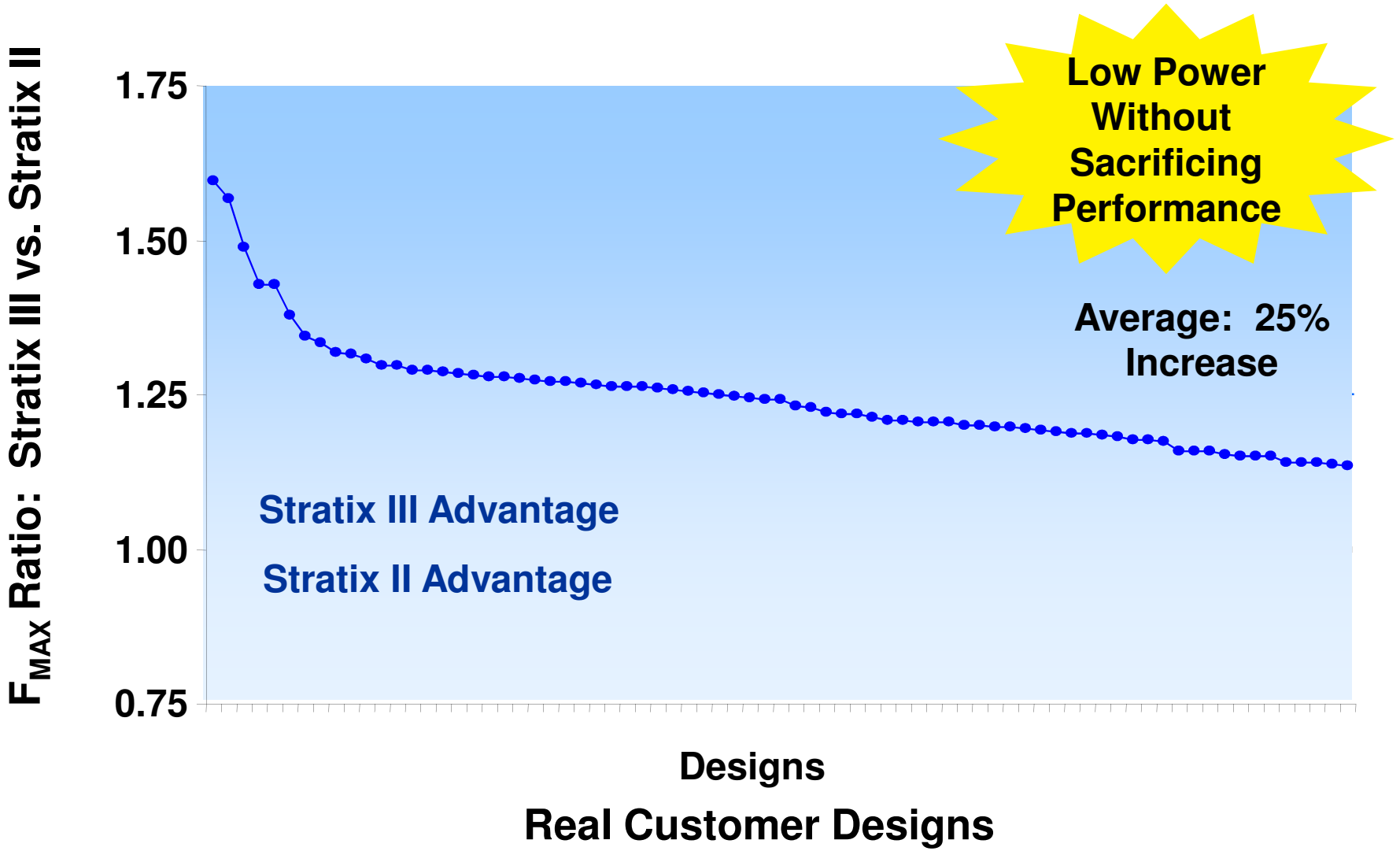
Most Tiles Are Low Power



Static Power Tamed (85°C)



Speed: Stratix III vs. Stratix II

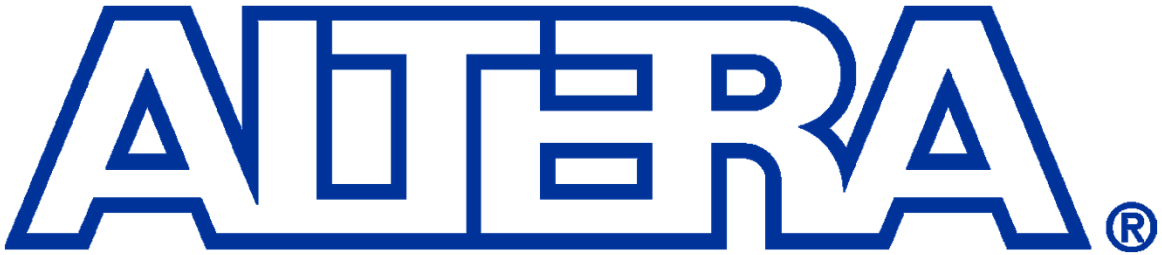


Using Programmable Power

- Circuit board requirements: none!
  - Stratix III FPGAs create low-power tiles using on-chip circuitry
  - No extra power supplies, no extra board components
- Design changes: none!
  - Quartus II software automatically uses high-speed tiles where needed for timing
  - All unused tiles set to low power
  - All tiles with timing margin set to low power
  - Failed timing constraints: all tiles not on critical paths set to low power

Programmable Power Controls

- High-speed tile usage always optimized
- Extra effort lowers high-speed usage (by a few %)
  - Also reduces dynamic power (average 15% vs. off)
  - At ~20% compile time cost
- Advanced options under **Fitter | More Settings**



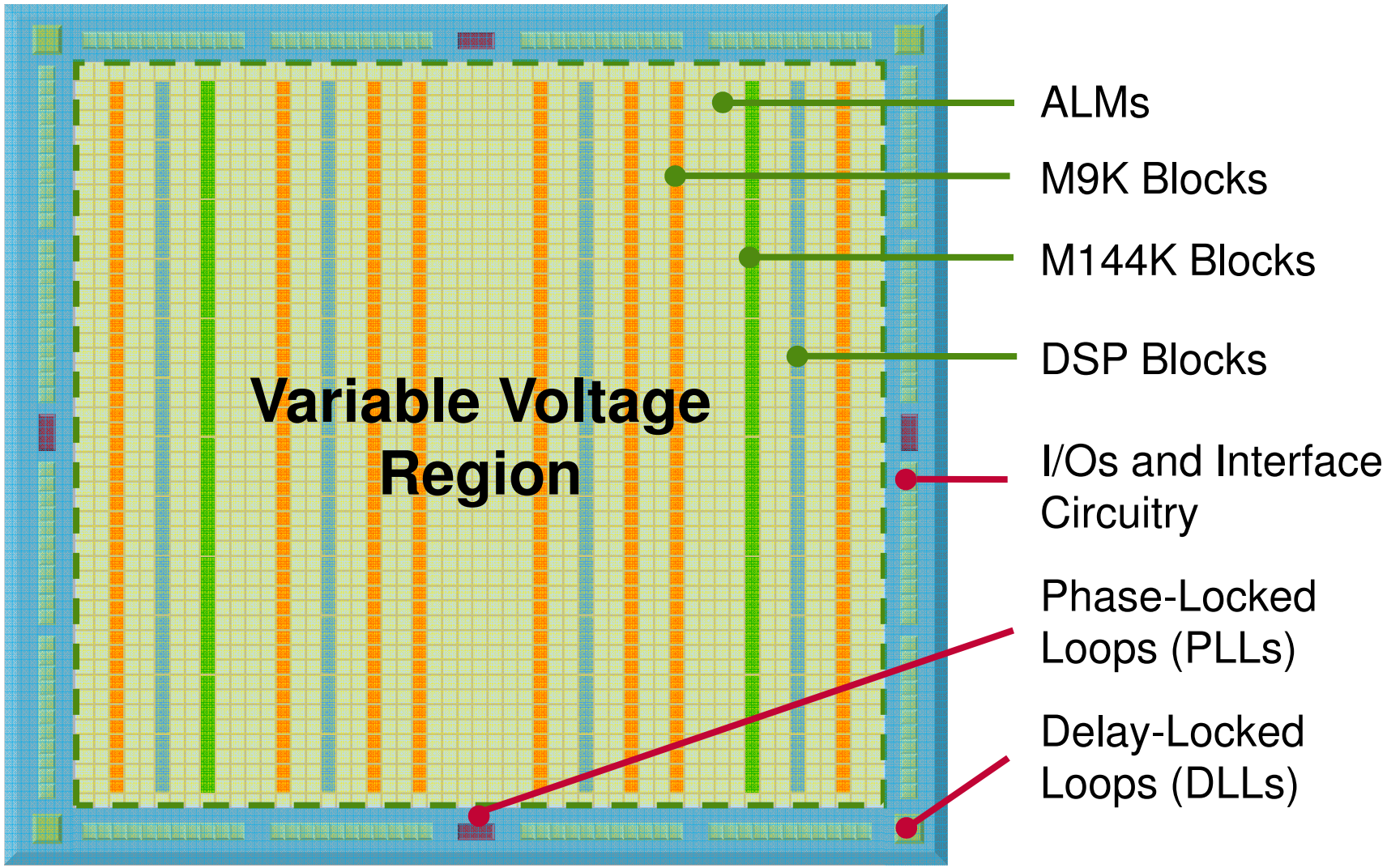
Selectable Core Voltage

Selectable Core Voltage

- Customer selects the FPGA core voltage
  - 1.1 V for maximum performance
  - 0.9 V for minimum power
- I/O and PLL voltages unaffected
  - Still get maximum I/O interface speed
  - Crucial, since I/O bandwidth limits many systems

Nominal Voltage	Min. Regulator V_{OUT}	Max. Regulator V_{OUT}	Slow Timing Model	Fast Timing Model	Power Model
1.1 V	1.05 V	1.15 V	✓	✓	✓
0.9 V	0.86 V	0.94 V	✓	✓	✓

Selectable Core Voltage



Power and Timing Impact

Core Voltage	Dynamic Power Reduction From Stratix II FPGAs	Static Power Reduction From Stratix II FPGAs	Performance Gain Over Stratix II FPGAs
1.1 V	33%	52%	25%
0.9 V	55%	64%	0%

More choice to meet your power and performance budgets

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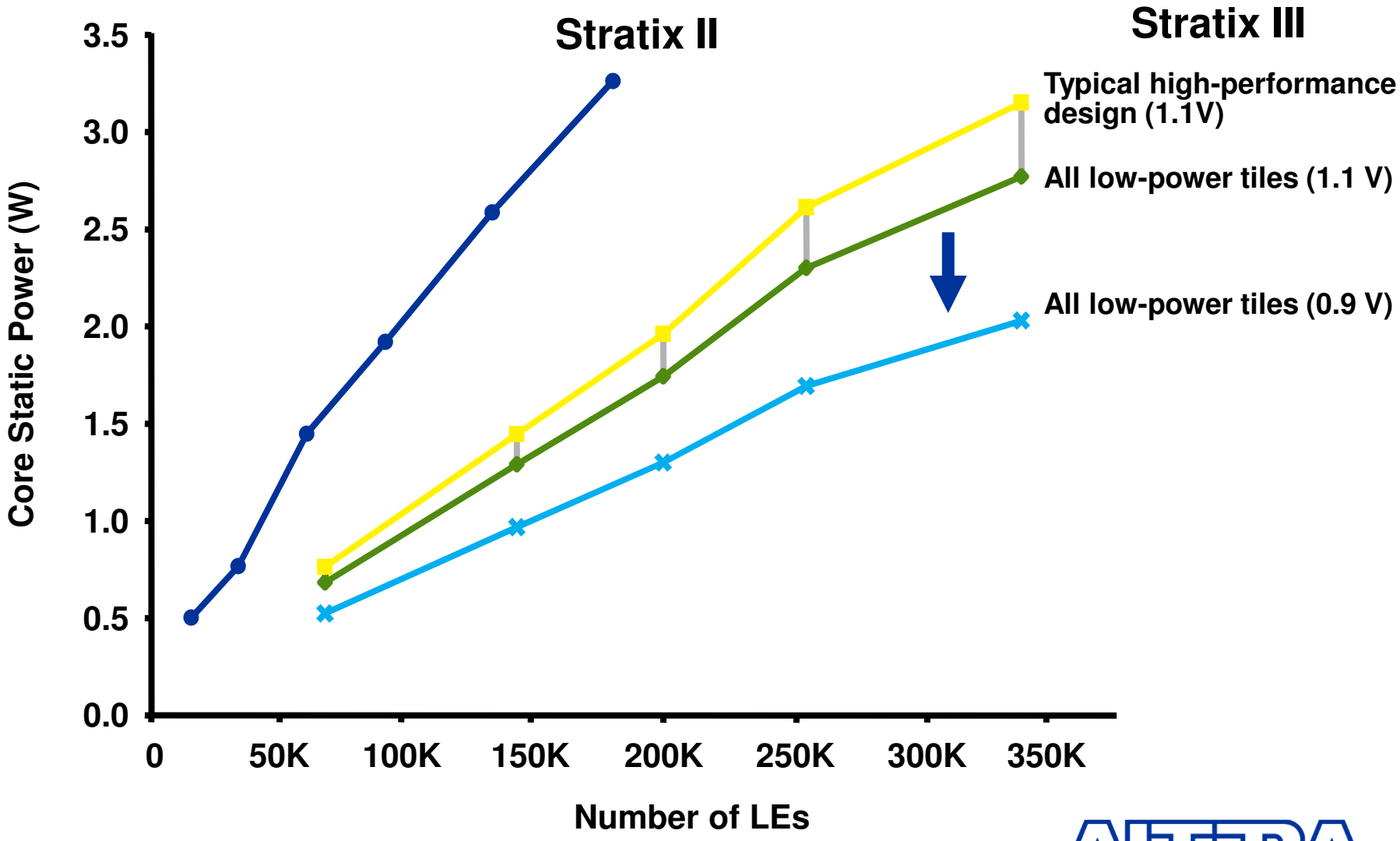
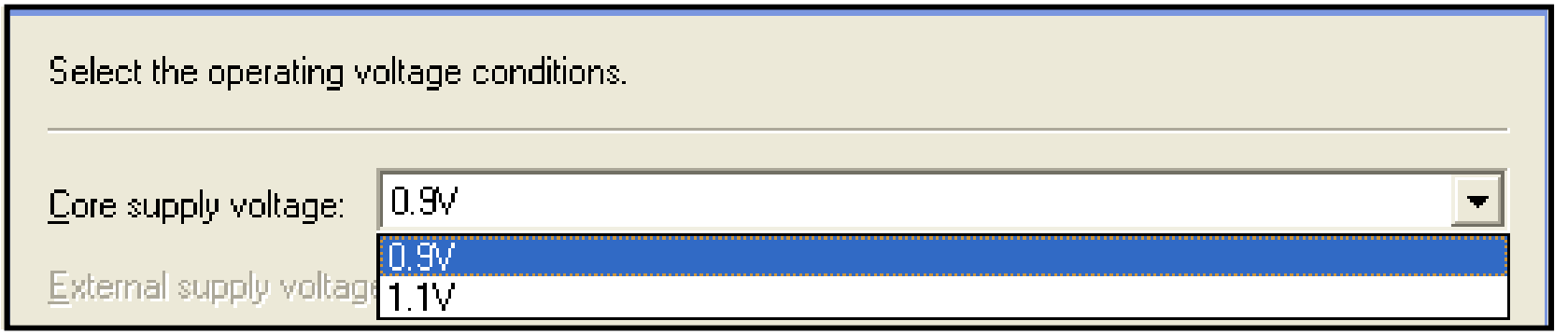
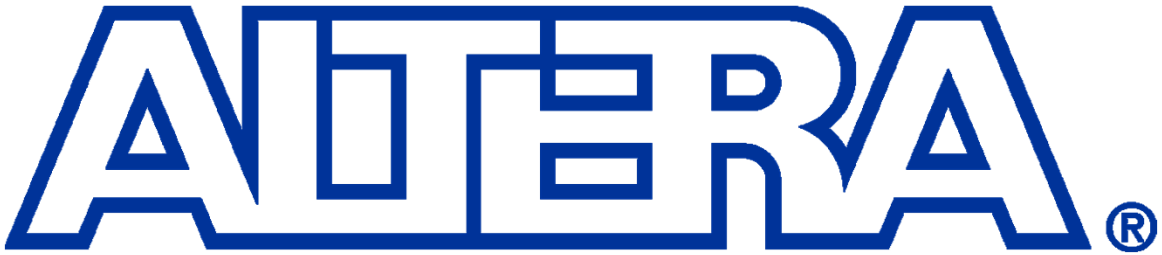
Even Lower Static Power (85°C)



Using Selectable Core Voltage

- Provide 0.9 V and 1.1 V supplies to FPGA
  - Risk mitigation: provide two supplies on board if concerned about power budget
  - Set voltage regulator output to 0.9 V if power budget exceeded at 1.1 V
- Quartus II software:
  - Select -4L speed grade
  - Select 0.9 V operation

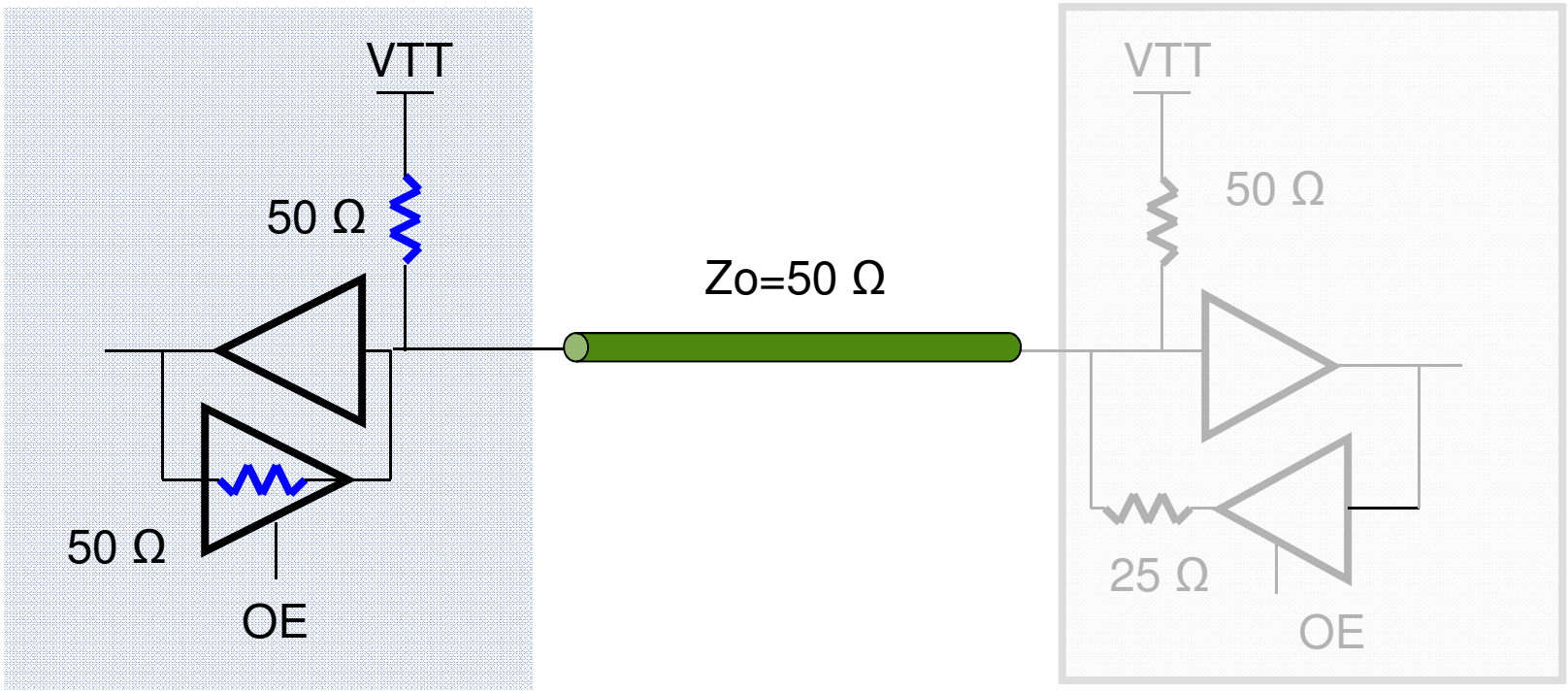




Power Optimized DDR Memory Interface

Stratix III On-Chip Termination (OCT)

- Both parallel (Rt=50Ω) and series (Rs=50Ω) termination



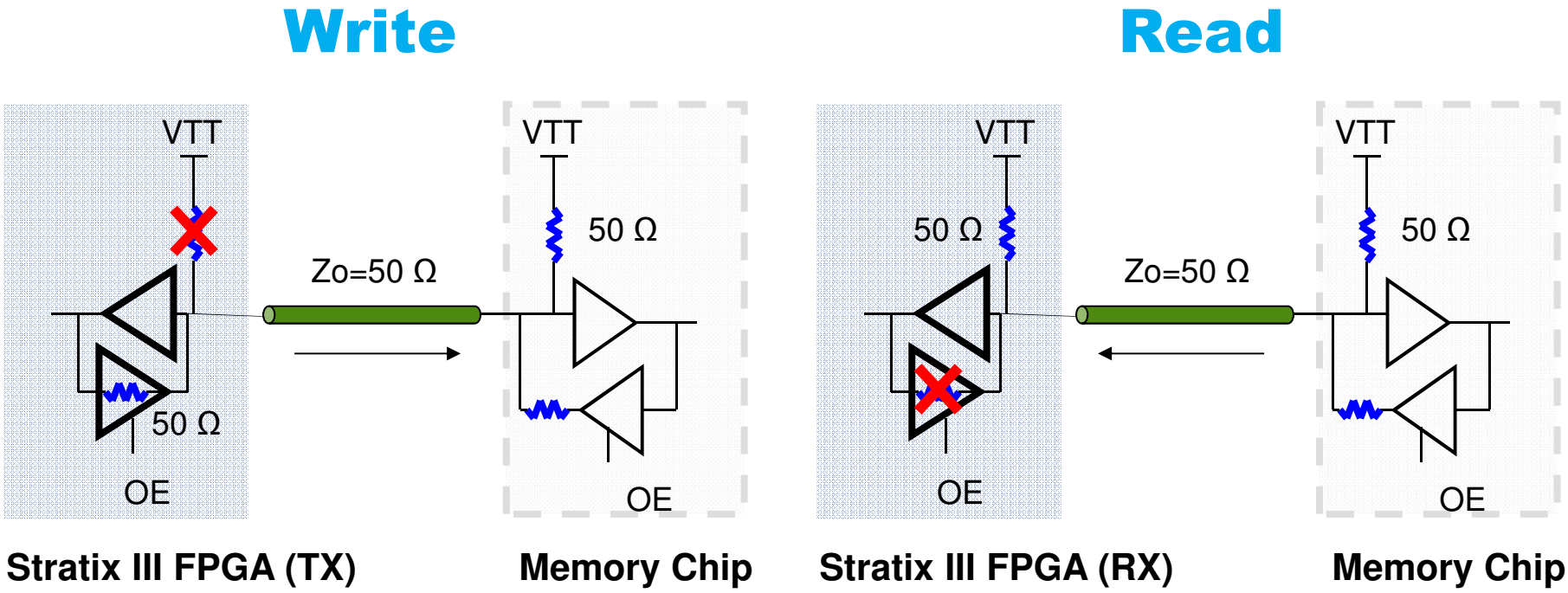
Stratix III FPGA

Memory Chip*

(*) DDR 1/2/3, RLDRAMII, QDR II/II+ support

Stratix III FPGA Dynamic OCT

- Write: Rs on, Rt off → Matching line impedance
- Read: Rs off, Rt on → Terminating far end

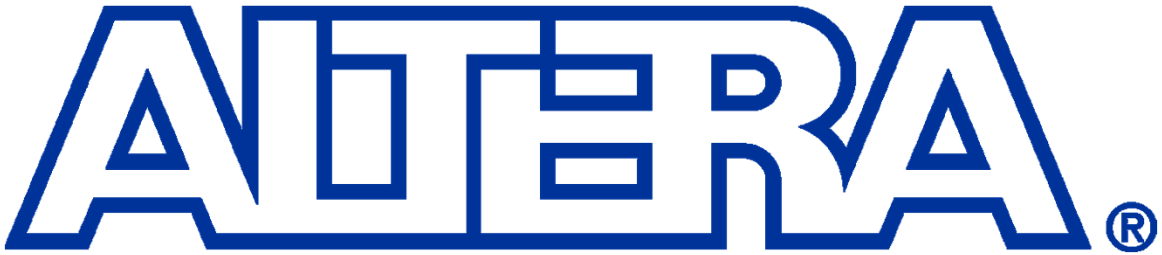


Benefits of Dynamic OCT

1. Power significantly reduced vs. traditional parallel OCT
   - Saves **1.6 W** of DC power on 72-bit DDR2 bus
2. Proper line termination and impedance matching on bidirectional busses
   - Enhanced signal integrity
3. No need for on-board termination resistors

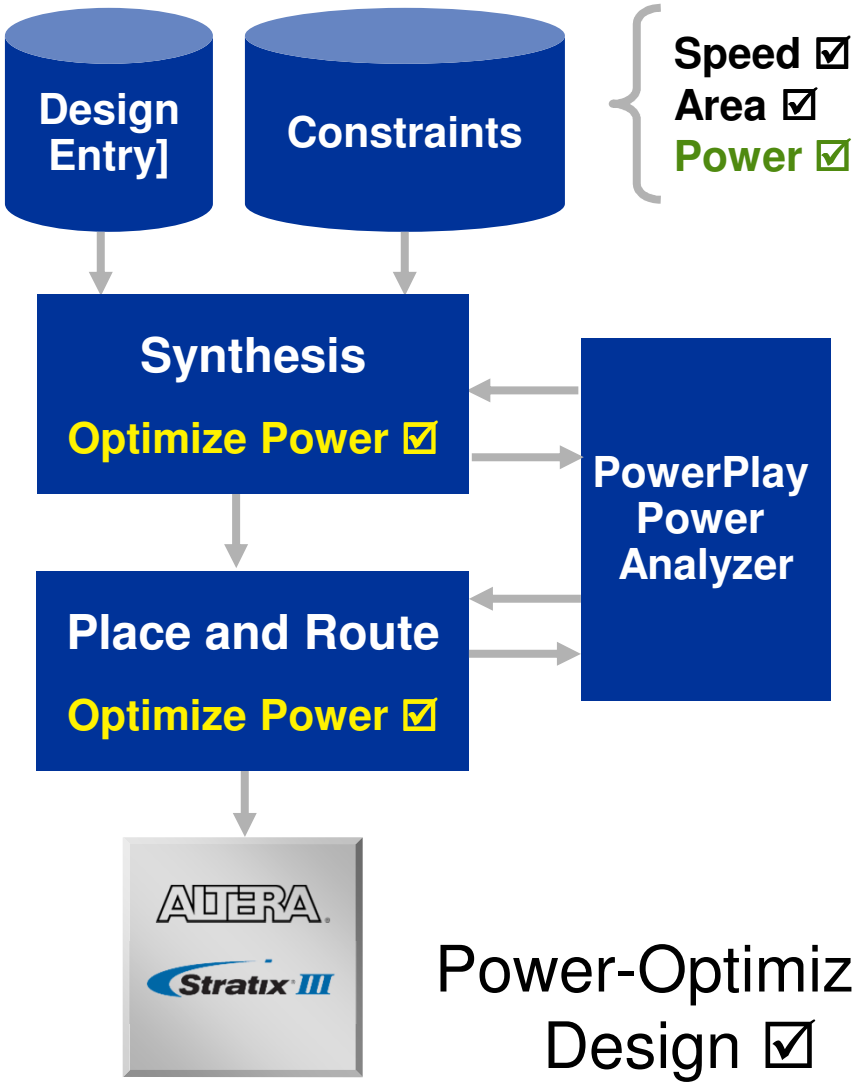
Stratix III FPGAs Support DDR3

- Stratix III: The only FPGA that supports DDR3
- DDR3 is **30% lower power** than DDR2
  - DDR2: 1.8V
  - DDR3: 1.5V
- Example system:
  - 72-pin 200MHz memory interface, with on-chip termination
    - Conventional FPGA DDR2 power: 3.9 W
    - Stratix III (dynamic OCT) DDR2 power: 2.3W
    - Stratix III (dynamic OCT) DDR3 power: 1.6W
  - **Total savings of 2.3 W**



Quartus II Power Optimization

PowerPlay: Automatic Optimization



Power-Optimized Design ☑

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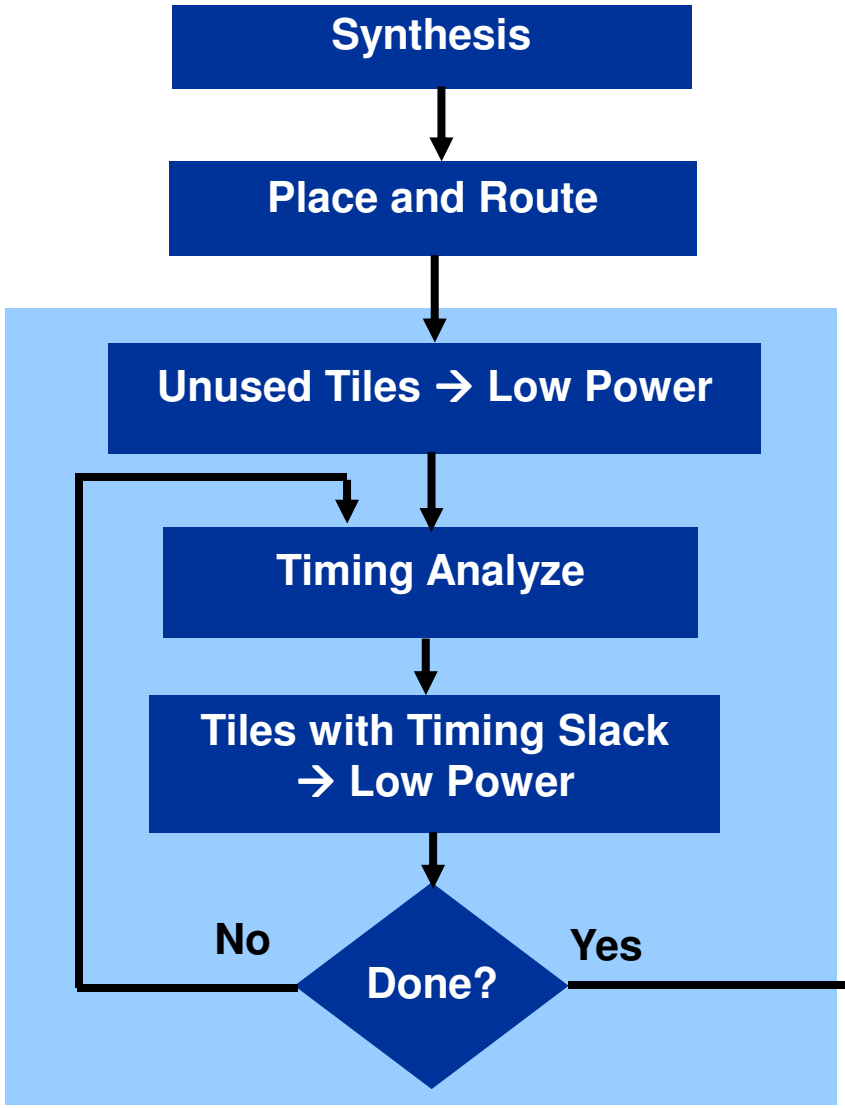
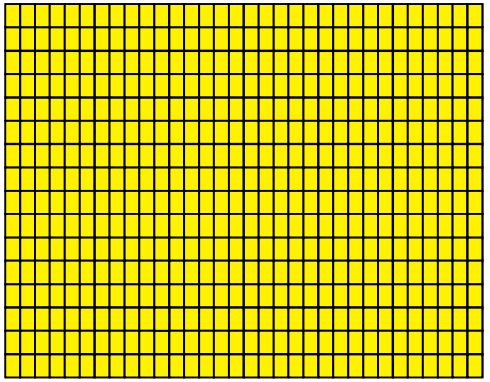
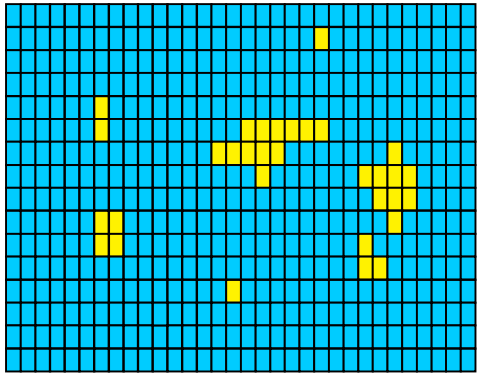
Automatic Programmable Power



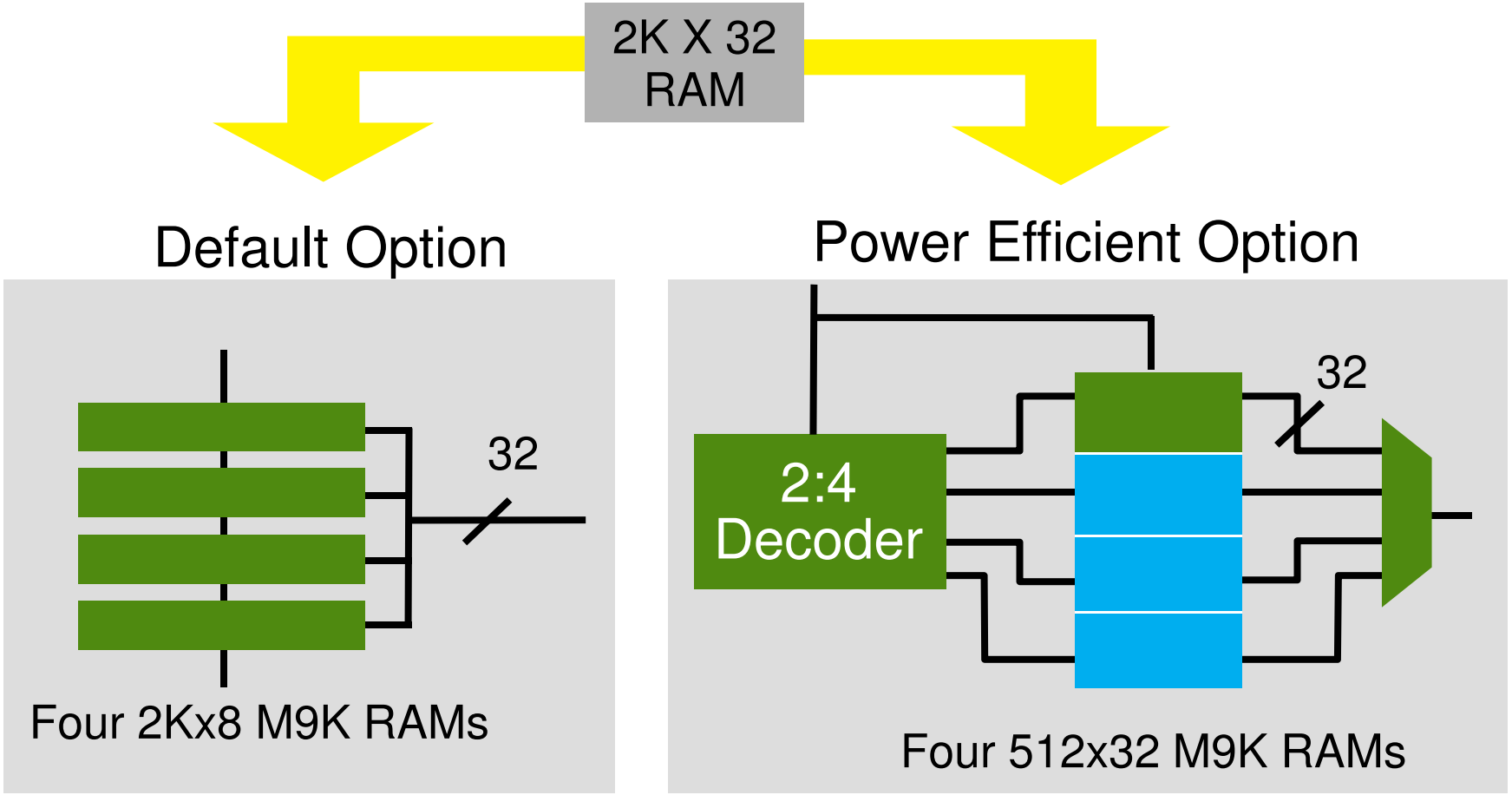


All High-Speed Tiles



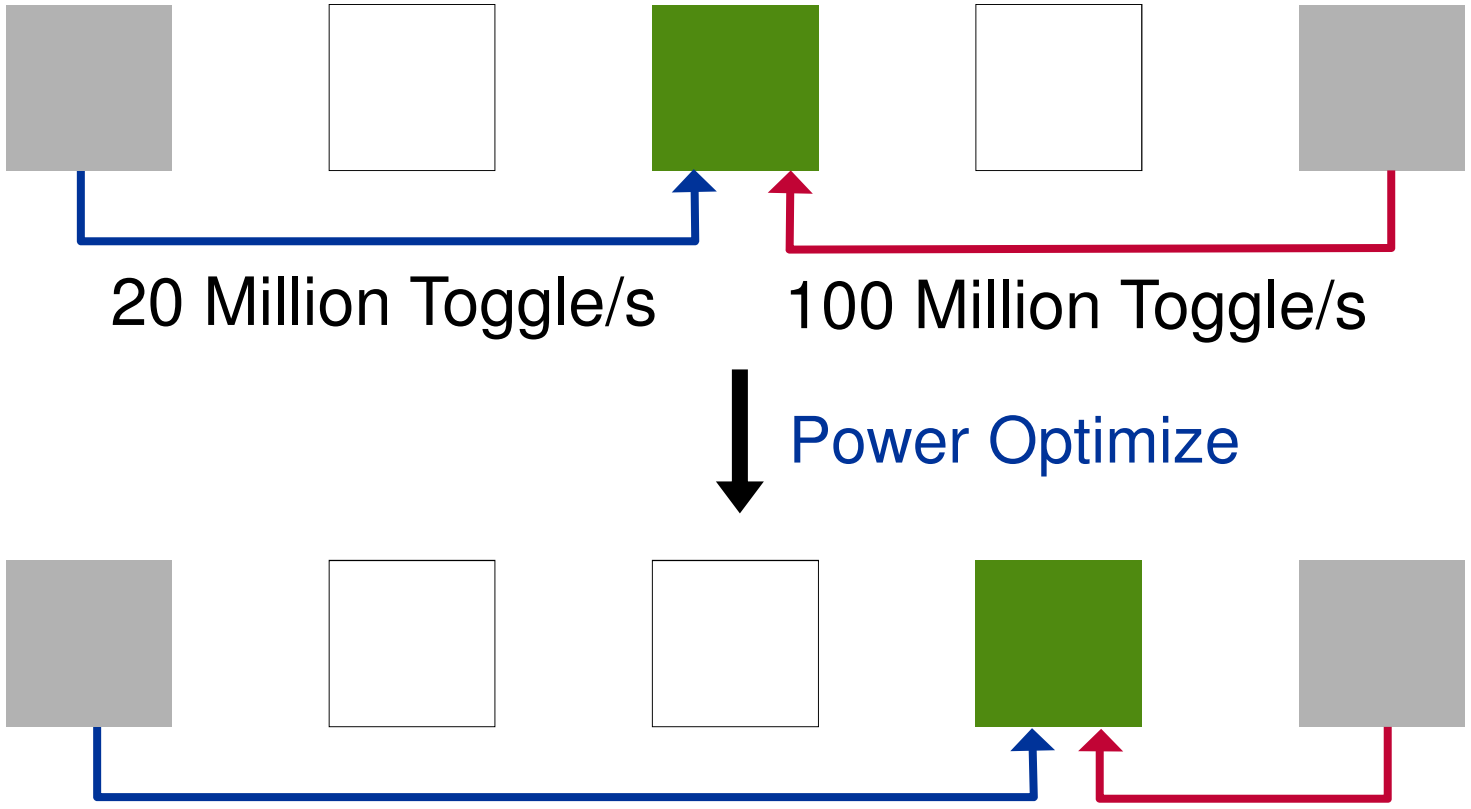
Mostly Low-Power Tiles

Power-Optimized RAM Mapping



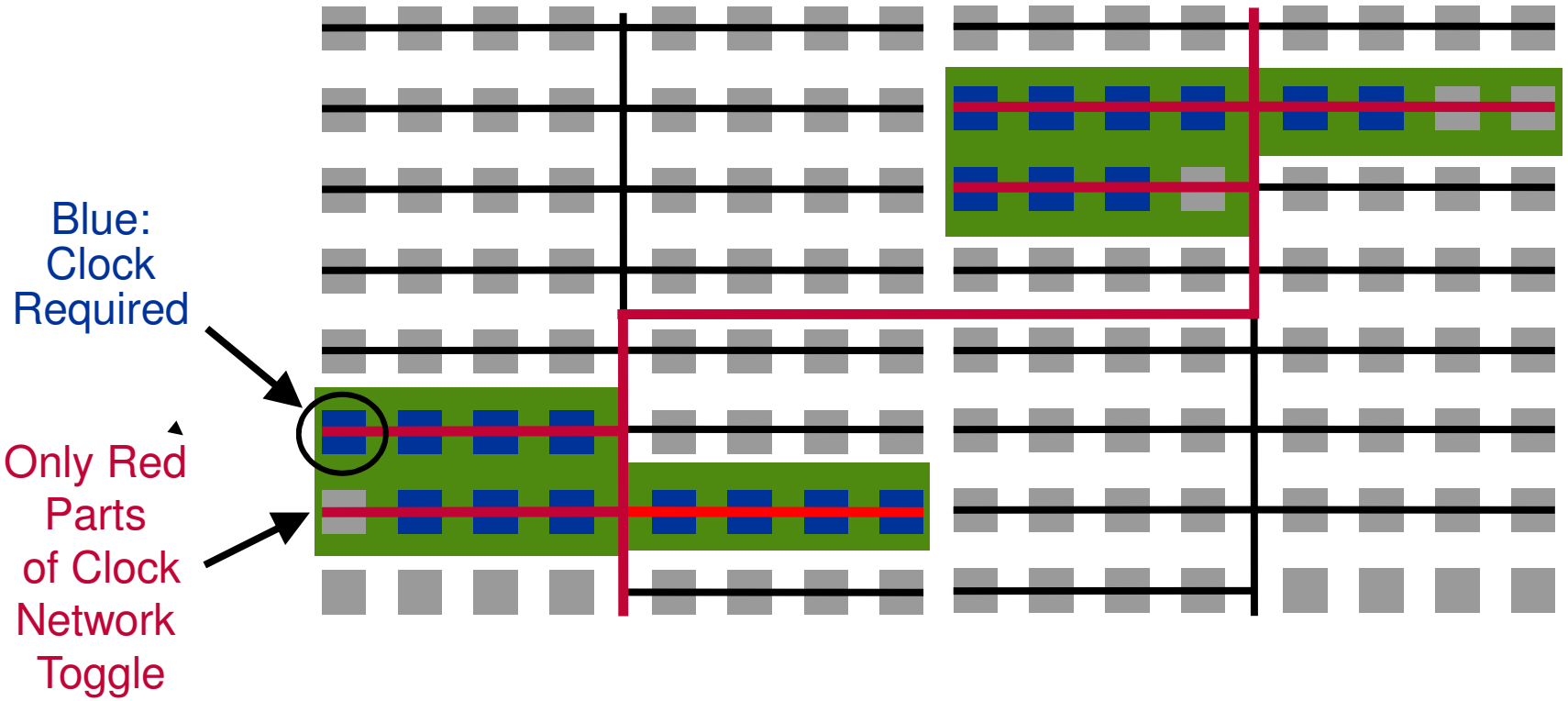
Power-Driven Place and Route

- Minimize capacitance of high-toggling signals
- Without violating timing constraints

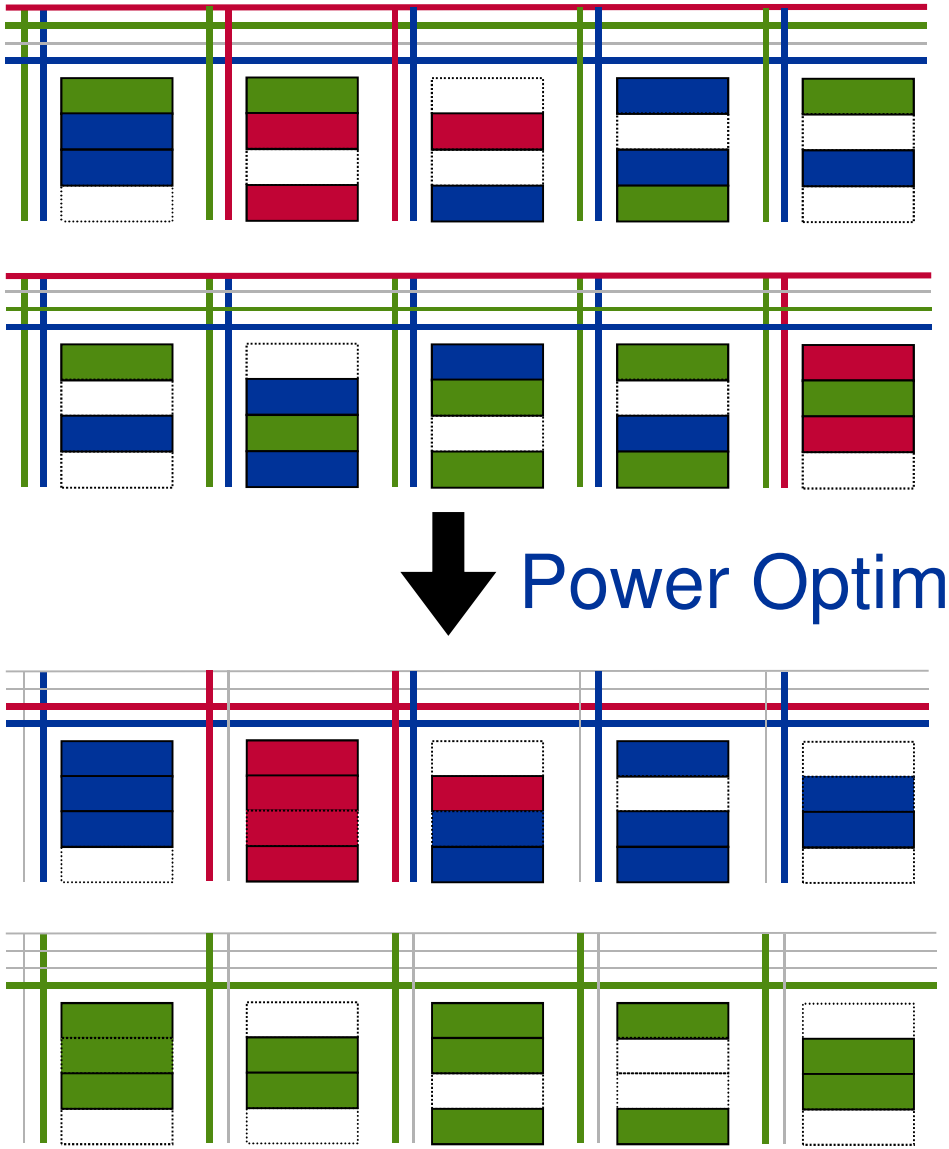


Clock Shut Down Hardware

- Stratix III FPGAs: Can shut down clock at 3 levels of tree
  - Top-level: Shut down 1/16 of clock tree
  - Next-level: 1 / 500 of clock tree
  - Bottom-level: 1 / 10,000 of clock tree



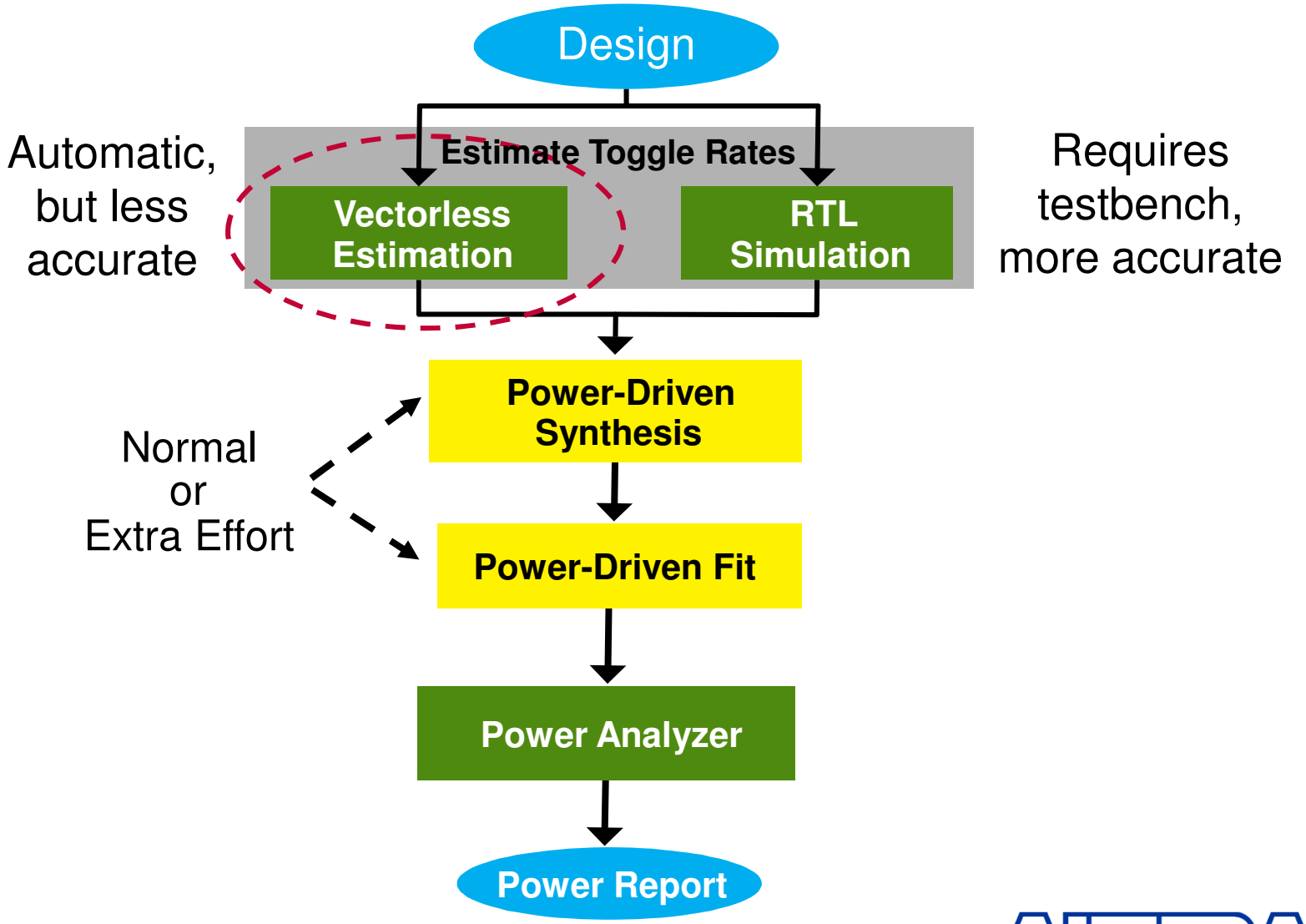
Placement to Reduce Clock Power



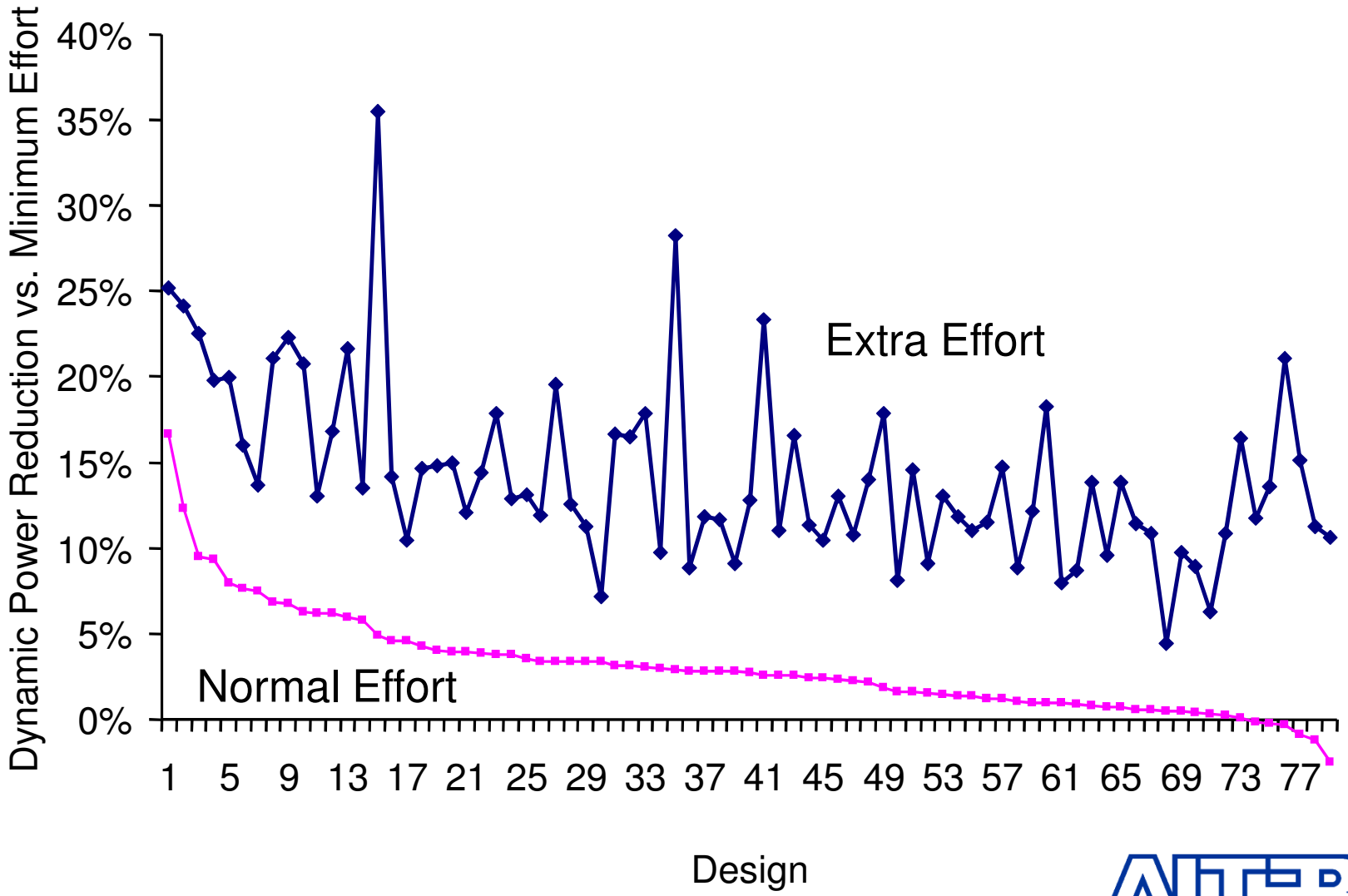
Clocking Legal,
Timing Optimized

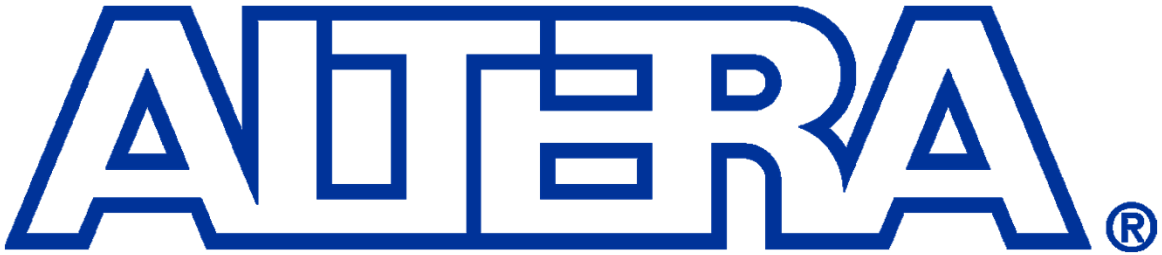
Group Clocks for
Maximum Shutdown

PowerPlay Power Optimization



Dynamic Power Optimization





Device Selection and Competitive Overview

Device Selection for Power

→ ***Use Altera's Early Power Estimator***

- Accurate
- Allows what-if analysis of different voltages
- Best option if no code has been written
- After implementation, Quartus II PowerPlay Power Analyzer provides the best estimate
  - Knows exact design utilization, block configurations, routing, signal behavior, etc.

Buyer Beware

- Not all power estimators are accurate
  - Especially for dynamic power
- Xilinx XPE – XPower estimator
  - Register power greatly underestimated
  - IO power greatly underestimated
    - Example: estimating memory interface power
  - Does not report any clock power – not modeled
  - LUT fan-out unrealistically low (2)

How Good Are the Estimates?

- Compare estimates to silicon measurements
  - Import design info from FPGA CAD tool to estimator
  - Obtain dynamic power estimate with correct toggle rates
  - Compare to silicon measurement of dynamic power

	Design	Stratix II EPE Ver. 6.1 % Error	Virtex-5 XPE Ver. 9.1 % Error
Logic	counter_16x1024	9%	-40%
Logic	grey6	22%	-56%
Logic	des3_6	-3%	-81%
Logic	rijndael_iter	-20%	-31%
Full Design →	tessierbeamform_12beams	28%	-36%
DSP Blocks →	mult_18x18_32copies	14%	-60%
RAM Blocks →	ram_8192dx64wx1	13%	-32%

Negative number = Underestimation (Bad)
Positive number = Overestimation (Safe)

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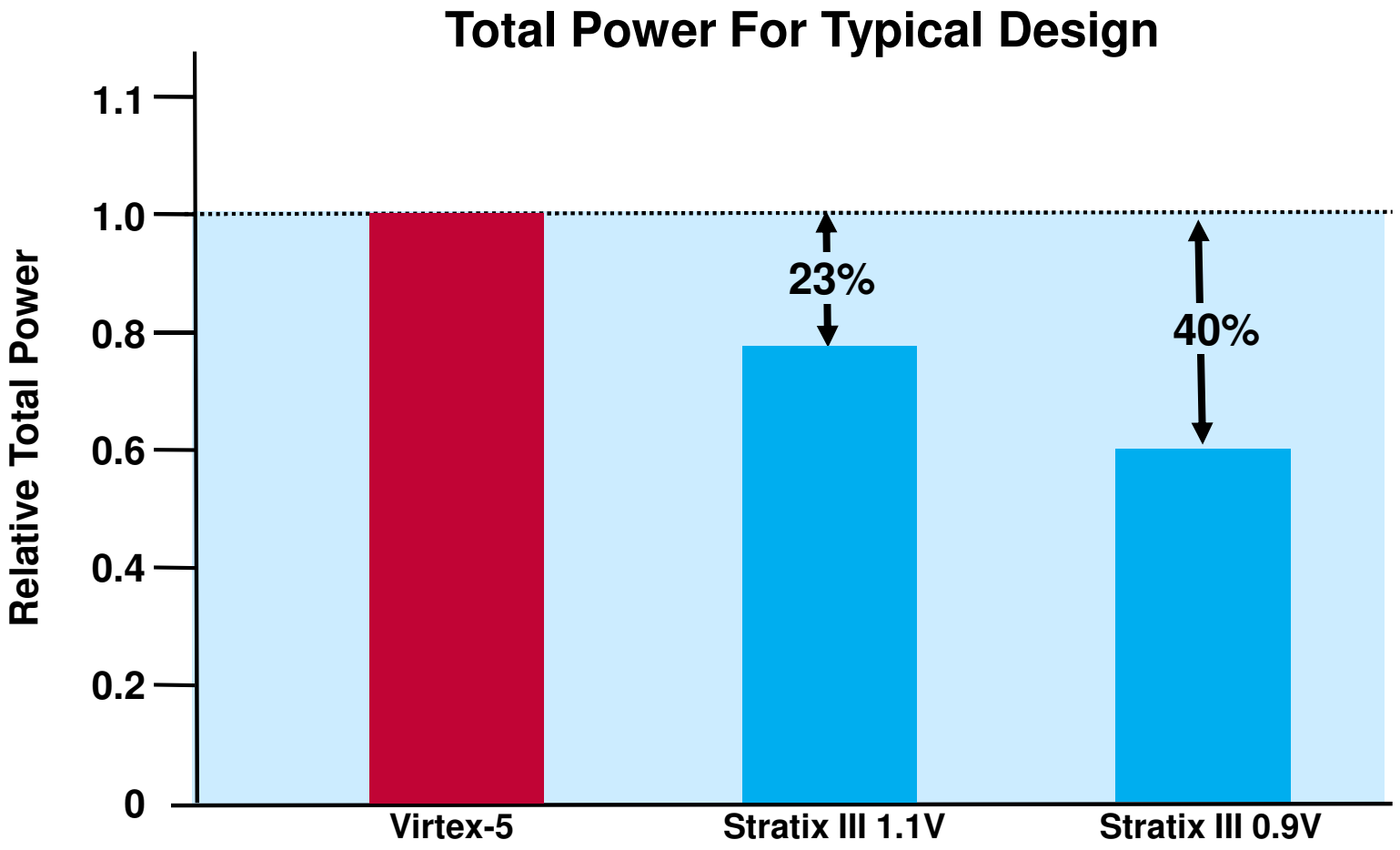
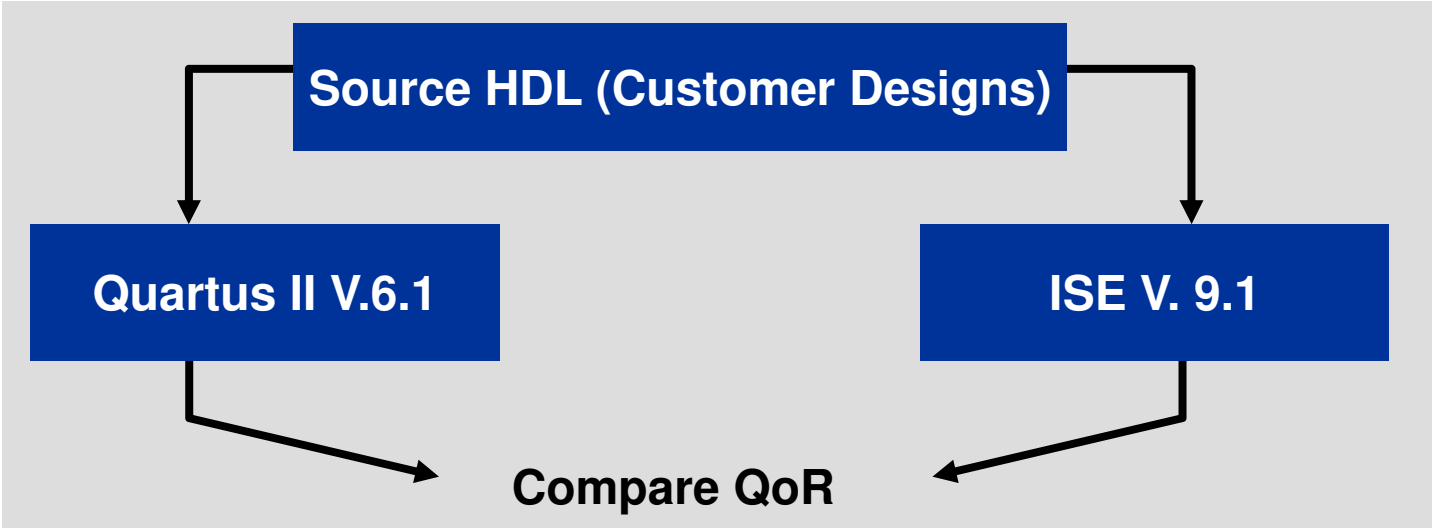
40% Power Advantage for Stratix III



* Total power (Dynamic + Static + IO), 85C junction temp., equivalent density devices, average customer usage of logic, memory, multipliers, and IO.

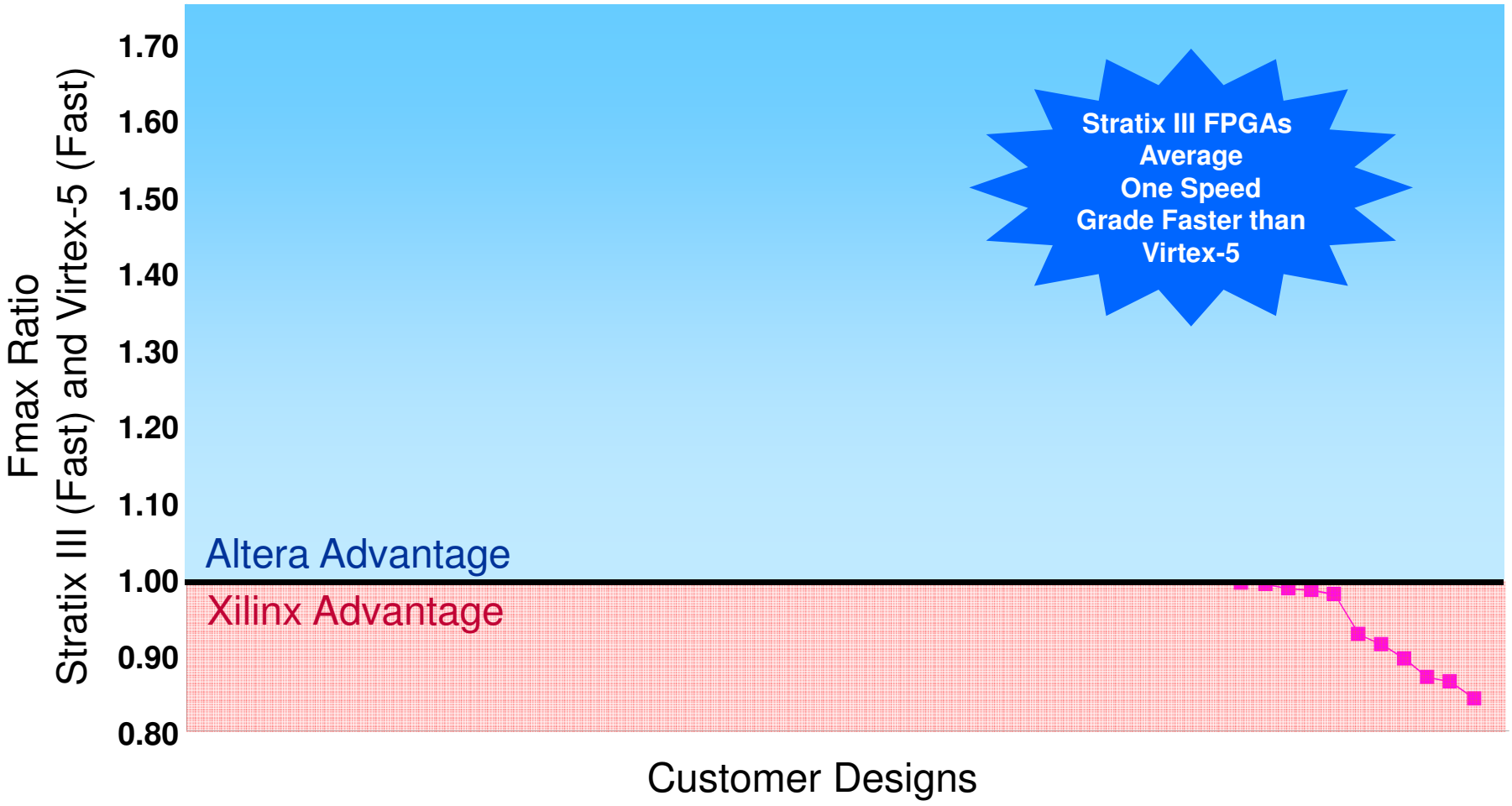
Performance Benchmarking



- Fastest speed grades are compared
- Full timing constraints for each design
  - Tight f_{MAX} constraint for each clock domain
  - I/O constraint on all pins
- Best effort (true FPGA performance)
  - Multiple compilations to get best result
- See "**How Fast is the Fastest FPGA**" net seminar for more details

Relative Core Performance Comparison

Stratix III (fast) vs. Virtex-5 (fast)



Summary

- Stratix III FPGAs
  - Meet the power challenge of next generation designs
  - With the highest performance AND lowest power
- Power reduction
  - Excellent process technology and engineering
  - Programmable power
  - Selectable core voltage
  - Power-efficient DDR interface
  - Quartus II software power optimization
- Lower power and higher performance than any competitive FPGA

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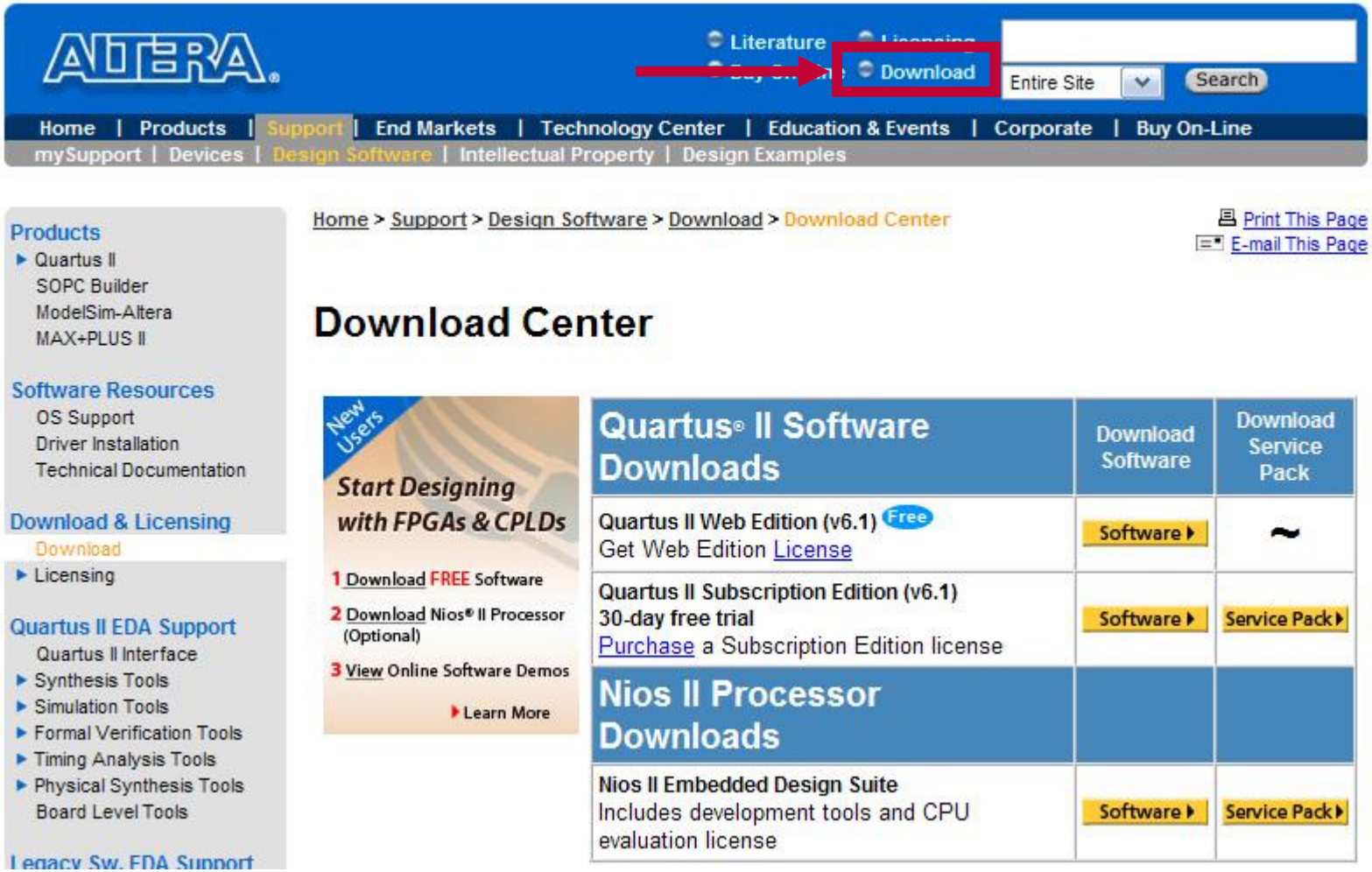
More Resources

- Stratix III website - www.altera.com/stratix3
  - Click on “Programmable Power Technology” to learn more about this and other Stratix III power related features
- Programmable Power White Paper
  - http://www.altera.com/literature/wp/wp-01006.pdf
- Stratix III EPE – power estimation spreadsheet
  - http://www.altera.com/support/devices/estimator/pow-powerplay.jsp
  - User guide available on this page
- Download Quartus II software and start designing with Stratix III FPGAs today
  - www.altera.com/download

Quartus II v6.1 Supports Stratix III FPGAs



Quartus II v6.1 Supports Stratix III FPGAs

- Quartus II web edition v6.1
  - Supports Stratix III devices: EP3SE50, EP3SL70
- Quartus II subscription edition v6.1
  - Supports all Stratix III devices

Additional Stratix III Net Seminars

- Overview of Altera's 65-nm Stratix III FPGAs (10 minutes)
- Using Stratix III FPGAs to Achieve Higher Performance Systems with Lower Power (60 minutes)
- How Fast is the Fastest FPGA?
  Stratix III Performance Capabilities (60 minutes)
- Upcoming Stratix III Net Seminar (June 2006):
  How to Maximize Performance with Stratix III FPGAs
  Using Quartus II Software (60 minutes)

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