Curriculum Vitae

A. Basic Information

Name: Vaughn Timothy Betz
Date of Birth: September 18, 1969
Citizenship: Canadian
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B. Education

Ph.D. in Electrical and Computer Engineering, 1998
University of Toronto
Dissertation: Architecture and CAD for Speed and Area Optimization of FPGAs
Advisor: Jonathan Rose
Grade-point average: 4.0 (of 4.0)
Governor General's Gold Medal for Best Graduate Student in Science, Engineering or Medicine

M.S. in Electrical and Computer Engineering, 1993
University of Illinois at Urbana-Champaign
Thesis: Absorbing Boundary Conditions for FDTD Simulation of Guided-Wave Structures
Advisor: Raj Mittra
Grade-point average: 5.0 (of 5.0)

B.Sc. in Electrical Engineering, 1991
University of Manitoba
Thesis: Computation of Far-Field Antenna Radiation Pattern from Near-Field Measurements
Advisor: Abdel Sebak
Grade-point average: 4.0 (of 4.0)
University Gold Medal for Highest Standing in Electrical Engineering

C. Research, Teaching and Academic Awards

Best Paper Award, ACM TRETS, 2021
ECE Departmental Teaching Award, 2021
Google Faculty Research Award. 2020
TC-FPGA Hall of Fame Paper, 2020
S. Vassiliadis Best Paper Award, Field Programmable Logic and Applications Conference, 2018
Early Career Teaching Award, 2017
Best Paper Award, IEEE Int. Conf. on Field-Programmable Technology, 2016
Professional Engineers of Ontario Medal for Engineering Excellence, 2016
Gordon R. Slemon Award for Excellence in the Teaching of Design, 2016
Two 25-year significant paper awards, Field Programmable Logic and Applications Conference, 2015
FPL Community Award, for contributions to FPGA Placement and Routing Research, 2015
Best Paper Award, ACM Int. Symp. on Field-Programmable Gate Arrays, 2015
IBM Faculty Award, 2014
Best Paper Award, IEEE Int. Symp. on Field-Programmable Custom Computing Machines, 2014
ECE Departmental Teaching Award, 2013
S. Vassiliadis Best Paper Award, Field Programmable Logic and Applications Conference, 2013
Six awards for papers in the FPGA 20: the twenty-five most significant publications in 20 years of the FPGA Symposium, 2012
Governor General's Gold Medal for Best Graduate Student in Science, Engineering or Medicine, 1999
Colton Medal for Research Excellence, 1999

V. L. Henderson Research Fellowship, 1998
Walter C. Sumner Memorial Scholarship, 1996 - 1997
Information Technology Research Center of Ontario Scholarship, 1996 - 1997
NSERC 1967 Science and Engineering Scholarship, 1992 - 1995
University Gold Medal for Highest Standing, 1991
IEEE Thesis Prize, 1991
John H. Chapman Memorial Prize, 1990 - 1991
Isbister Scholarship in Engineering, 1990 - 1991
Boise Cascade Scholarship, 1990 - 1991
Muriel Brooks Childerhose Memorial Scholarship, 1990 - 1991
E. P. Fetherstonhaugh Memorial Scholarship, 1990 - 1991
Alumni Association Undergraduate Scholarship, 1989 - 1990
Technical Communication Report Prize, 1989
Edward Oliver Grimsdick Memorial Prize, 1989
Assoc. of Professional Engineers of Manitoba Scholarship, 1988 - 1989
Alumni Association Entrance Scholarship for High Standing, 1987 - 1988
Governor General's Bronze Medal for Highest Standing in High School, 1987

D. Professional Societies and Research Organizations

Fellow, National Academy of Inventors, 2021
Fellow, Institute of Electrical and Eletronics Engineers (IEEE), 2020 (Member from 1989)
Member of the Association of Computing Machinery (ACM), 2007 – present
Professional Engineer in the Province of Ontario, 2012 – present
Faculty Affiliate, Vector Institute for Artificial Intelligence, 2018 – present
Member, Centre for Spatial Computational Learning, 2019 - present

E. Experience

E.1 Industrial Experience

Senior Director, Software Engineering, Altera Toronto Technology Centre: 2008 – April 2011.

In charge of the Altera Toronto site of approximately 85 engineers. In addition to the technical areas for which I was responsible as a director (please see the 2003 – 2007 entry), I assumed responsibility for the Quartus II incremental compile, visualization and floorplanning technologies, and (joint with the San Jose team) responsibity for optimization during Quartus logic synthesis. I was also responsible for the Altera university program (which creates teaching materials and hardware for use by university digital logic and computer organization courses), the analysis of our hardware and software vs. that of the competition, and the development of intellectual property (IP) cores to interface Altera FPGAs to high-speed memory devices such as DDR3 DRAMs. I drove a major re-architecting of these memory interface IP cores and the related hardware in our FPGAs to reach higher speeds and achieve lower latency. My team developed industry-leading signal integrity analysis tools that are fast, easy-to-use, and accurate. My team continued to improve the algorithms throughout the Quartus II CAD flow, and parallelized six major Quartus II algorithms – in total, we reduced the compile time for the typical circuit by 6X from 2003 to today, while simultaneously greatly improving result quality. In addition to managing the team, I continued to play a large role in architecting new CAD techniques and proposing new circuit ideas.

Director, Software Engineering, Altera Toronto Technology Centre: January 2003 – December 2007.

During this time my team grew from 23 to 47 research and development engineers. I had overall responsibility for several key software technologies, including the placement and routing engine, timing modeling, signal integrity analysis and power estimation for Altera's Field Programmable Gate Arrays (FPGAs) and structured ASICs. In concert with engineers in San Jose, my team developed the architecture of the Stratix II & III and Cyclone II & III FPGA families. We developed new power modeling and power optimization algorithms and incorporated these algorithms into Altera's Quartus II

CAD system. My team developed the programmable back-bias technology used in Stratix III and later FPGAs to reduce the (otherwise high) static power consumption of 65 nm and below processes. My team's role in delivering industry-leading Computer-Aided Design (CAD) software and device architecture has been a crucial factor in Altera's competitiveness.

Senior Manager, Software Engineering, Altera Toronto Technology Centre: Jan. 2001 – Dec. 2002.
Led a team that grew during this time from 7 to 14 people, and who were responsible for researching new placement and routing algorithms and coding the placement and routing engine and related software support for Altera's Stratix and Cyclone FPGAs. I architected much of the Quartus II CAD system support for these FPGAs, and was also one of the architects of the devices themselves. These devices and their successors have cumulative revenue of over $15 billion to date, and Quartus II is used by tens of thousands of design engineers worldwide.

Manager, Software Engineering, Altera Toronto Technology Centre: May 2000 – December 2000.
Led a team of 6 engineers who developed a new placement and routing engine for Altera's APEX 20K series of FPGAs. This new engine reduced compile time by 3X while simultaneously increasing circuit speed by 45%, on average, vs. prior technology. It also greatly improved the routing completion rate, from approximately 60% to over 95%. This improved placement and routing technology was crucial in improving Altera's competitive position, and led Altera to rename their CAD suite from Quartus to Quartus II to emphasize the new technology it contained.

Co-founder and Vice President of Engineering, Right Track CAD, Toronto, ON: Oct. 1998 – May 2000.
I co-founded Right Track CAD to commercialize my doctoral research into place-and-route and FPGA architecture evaluation CAD tools. I was in charge of overall technical management, and helped grow the company from four to twelve people. I defined the overall architecture of our software and led a team of 9 engineers in implementing these CAD tools. Altera replaced the place-and-route engine in their Max+PlusII CAD suite with the Right Track engine, which achieved an average 30X reduction in compile time while improving circuit speed by an average of 38% vs. Altera's existing engine. Cypress Semiconductor contracted with Right Track to develop their next-generation FPGA architecture. Right Track was acquired by Altera Corporation in May 2000, and all subsequent Altera FPGAs have been designed using Right Track's architecture evaluation CAD tools.

Software Engineer, Integrated Engineering Software, Winnipeg, MB: May – Dec. 1991 and May - August 1989 and 1990.
Developed computer-aided engineering software to model electromagnetic phenomena. Ported software from DOS-based PCs to Unix Workstations, rewrote all graphics and the user interface, and developed the software's security system for Unix-based platforms.

E.2 Academic Experience

Professor, University of Toronto: July, 2017 – present.
Associate Professor, University of Toronto: July 2011 – June 2017.
Granted Tenure: August 2014

Teaching: Programming, team-based design and effective communication for undergraduates, and FPGA architecture for graduate students.

Research: I am currently supervising 5 PhD and 6 MASc and students and 1 Postdoctoral Fellow and have previously graduated 4 PhD, 15 MASc and 3 MEng students. My research focii are:

- Efficient programmable architectures for machine learning. Work in this space is focusing not only how machine learning algorithms can be efficiently implemented on current FPGAs, but

more fundamentally on how new FPGA architectures or hybrid chips can be created that greatly enhance the performance of machine learning while remaining programmable and general purpose.

- Communication-centric architectures and design tools for FPGAs. We are investigating how to augment the low-level transistor-switched interconnect with a more structured, packet-switched network-on-chip and how to change the design flow to exploit this new hybrid device. The goal is to make FPGA design and timing closure easier by raising the level of abstraction of the interconnect.
- FPGA CAD tools. We are investigating divide-and-conquer CAD techniques to greatly reduce compile time, as the multi-hour (and growing) compile time of FPGA CAD tools is a major barrier to widespread use of FPGAs. This involves creating new floorplanning and automatic pipelining flows.
- FPGA architecture tools and enhancements. Another thrust of our CAD tool research is to improve the VTR (Verilog to Routing) architecture evaluation flow for FPGAs with new features and improved result quality, and to create new CAD tools to evaluate circuit-level optimization of FPGAs. We also (using these tools) investigate various ways to improve FPGA architectures, from improved switch pattern through incorporating emerging memory technologies like STT-RAM.
- Accelerating computation with FPGAs. Current work in this area is focusing on creating a hardware engine in an FPGA to accelerate Monte Carlo simulation of photon scattering and absorption in complex tissue. Monte Carlo simulation is highly accurate but very time-consuming; in our prototypes we have achieved a 16X improvement in computation time and 60X energy-efficiency gain vs. conventional computers. We are completing the system and partnering with medical researchers to apply the technique to photo-dynamic cancer treatment.

Adminstrative Leadership:

- Director of Undergraduate Admissions, ECE Department, July 2018 – present
- Chair of Engineering Admissions Committee, July 2020 – present
- Vice Chair of Engineering Admissions Committee, July 2019 – June 2020
- Director of Outreach, ECE Department, July 2015 – July 2018
- Faculty Counsellor, IEEE Student Branch at U of T, Jan. 2018 - present

Adjunct Professor, University of Toronto: July 1, 2009 – July 1, 2011.

Co-supervisor (with Jonathan Rose) of MASc candidate Wei Zhang. This work focused on creating scalable and portable computational libraries for FPGAs.

Research Assistant, University of Toronto: 1993 - 1998.

Researched computer-aided design algorithms and improved architectures for Field-Programmable Gate Array (FPGA) routing and logic blocks. I developed the VPR placement and routing program and the VPack clustering program to aid in FPGA research; these tools have since been very widely used in both industry and academia. I created a now-standard FPGA architecture research methodology -- implement benchmark circuits through a complete parameterized CAD suite that is driven by detailed area and delay models of the circuitry required by each FPGA.

Lecturer, University of Toronto: Fall semester, 1995 and 1996.

Taught the "Introduction to Microprocessors" course to third-year engineering students for two consecutive years. Prepared the course outline, lectures, laboratories, all tests and exams, and gave all lectures. In charge of three laboratory teaching assistants, and rewrote the 150 page lab manual. Received teaching evaluations well above the department average.

Teaching Assistant, University of Toronto: 1994 - 1998.

Laboratory instructor and grader for undergraduate courses on hardware design with VHDL, physical electronics, and basic electronics.

Research Assistant, University of Illinois at Urbana-Champaign: 1992 - 1993.
Developed improved absorbing boundary conditions to simulate radiation in electro-magnetic simulations, and integrated these improvements into a finite-difference time-domain simulator for the analysis of VLSI and printed circuit board interconnect at very high speeds.

E.3 Committees and Editorial Boards and Other Boards

2012 – present: **Associate Editor**, ACM Trans. on Reconfigurable Technology and Systems
2021 – present: **Board Member**, Open Source FPGA Foundation
2017: **Awards Chair,** Int. Conf. on Field Programmable Logic and Applications
2015: **Finance Chair,** ACM / SIGDA Int. Symposium on Field-Programmable Gate Arrays
2015: **Publicity Chair**, IEEE Int. Conf. on Application-Specific Architectures, Systems and Processors
2014: **General Chair**, ACM / SIGDA Int. Symposium on Field-Programmable Gate Arrays
2013: **Technical Program Chair**, ACM/SIGDA Int. Symp. on Field-Programmable Gate Arrays
2012: **Workshop Chair**, ACM / SIGDA Int. Symposium on Field-Programmable Gate Arrays
2002 – present: **Program Committee Member**, ACM / SIGDA Int. Symp. on Field-Programmable Gate Arrays
2006 – present: **Program Committee Member**, IEEE Int. Conf. on Field-Programmable Technology
2005 – 2007 & 2016 - 2019: **Program Committee Member**, Int. Conference on Field Programmable Logic and Applications
2018 – 2019: **Program Committee Member**, IEEE Int. Symp. On Field-Configurable Custom Computing Machiness
2008 – present: **Member**, ACM Technical Committee on FPGAs
2014 – 2015: **Program Committee Member,** Design Automation Conference
2013 & 2016: **Program Committee Member**, Int. Conf. on Reconfigurable Computing and FPGAs
2011 – 2013: **Program Committee Member**, Workshop on the Intersections of Computer Architecture and Reconfigurable Logic
2001 - 2003: **Program Committee Member**, IEEE Custom Integrated Circuits Conference

F. Publications

Summary[1]

Books	1
Book Chapters	5
Refereed Papers in Journals	54
Invited Journal Publications	1
Refereed in Conferences	79
Refereed Papers in Workshops	2
U.S. Patent Applications Submitted (Being Examined)	1
U.S. Patents Granted	101
Software Packages Released	4
Conference Keynotes	3
Conference Panels	3
Invited Presentations at Universities and Companies	24
Internet seminars	5

Citation Count Summary[2]

[1] Publication counts include published, accepted, and submitted works.
[2] Citation counts from Google Scholar, including citations in both articles and patents, June 3, 2021

Publications with over 1000 citations	2
Publications with over 100 citations	18
h-index	42
i10 index (> 10 citations)	129
Total citations	9875

Books and Book Chapters:

[1] A. Boutros and V. Betzs, "Balancing Flexibility and Efficiency: Principles of Field-Programmable Gate Array Architecture," *Accepted to* **Handbook of Computer Architecture**, Springer, 2021.

[2] M. Hutton, V. Betz and J. Anderson, "FPGA Synthesis and Physical Design," Chapter 16 in **Electronic Design Automation for IC Implementation, Circuit Design and Process Technology,** CRC Press, 2016, pp. 373 - 414.

[3] M. Abdelfattah and V. Betz, "Embedded Networks-on-Chip for FPGAs," Chapter 6 in **Reconfigurable Logic: Architecture Tools and Applications**, Taylor and Francis, 2015, pp. 149 - 184.

[4] V. Betz, "Placement for General Purpose FPGAs," Chapter 14, in **Reconfigurable Computing**, A. DeHon and S. Hauck, Eds., Morgan Kauffman, 2007, pp. 299 - 317.

[5] M. Hutton and V. Betz, "FPGA Synthesis and Physical Design," Volume 1, Chapter 13, in **Electronic Design Automation for Integrated Circuits Handbook**, L. Scheffer, L. Lavagno, and G. Martin, Eds., Taylor and Francis CRC Press, 2006, pp. 13-1 to 13-32.

[6] V. Betz, J. Rose, and A. Marquardt, **Architecture and CAD for Deep-Submicron FPGAs**, Kluwer Academic Publishers, 1999.

Refereed Journal Publications:

[7] A. Yassine, W. Lo, T. Saeidi, D. Ferguson, C. Whyne, M. Akens, V. Betz, L. Lilge, "Photodynamic therapy outcome modelling for patients with spinal metastases: A simulation-based study," *Scientific Reports,* Vol. 11, Sept. 2021.

[8] C. McFadden, K. Ramadan, B. Gomes, F. Schweigelshohn, H. Chan, V. Betz, M. Cypel, and L. Lilge, "Determination of Optical Properties and Photodynamic Threshold of Lung Tissue for Treatment Planning of In Vivo Lung Perfusion Assisted Photodynamic Therapy," *Photodiagnosis and Photodynamic Therapy,* Vol. 35, September 2021.

[9] A. Abdalrhman, C. Wang, A. Manalac, M. Weersink, A. Yassine, V. Betz, B. Barbeau, L. Lilge and R. Hoffman, "Modelling the Efficiency of UV at 254 nm for Disinfecting the Different Layers within N95 Respirators," *Journal of Biophotonics,* Vol. 14, No. 10, June 2021.

[10] M. Elgammal, K. Murray and V. Betz, "RLPlace: Using Reinforcement Learning and Smart Perturbations to Optimize FPGA Placement," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* 2021, Accepted.

[11] V. Betz and A. Boutros, "FPGA Architecture: Principles and Progression," *IEEE Circuits and Systems Magazine*, Vol. 21, No. 2, May 2021, pp 4 - 29.

[12] S. Attia and V. Betz, "Stop and Look: A Novel Checkpointing and Debugging Flow for FPGAs," *in Revison, IEEE Transactions on Computers*, 2021.

[13] A. Yassine, L. Lilge and V. Betz, "Machine Learning for Real-Time Optical Property Recovery in Interstitial Photodynamic Therapy – A Simulation-Based Study," *Biomedical Optics Express,* Vol. 12, No. 9, 2021, pp. 5401 - 5422.

[14] T. Young-Schultz, F. Schwiegelshohn, S. Brown and V. Betz, "Productivity and Performance: Accelerating Biophotonic Simulations on FPGAs Using OpenCL," *Submitted to ACM TRETS*, 2020.

[15] A. Yassine, L. Lilge and V. Betz, "Optimizing Interstitial Photodynamic Therapy Planning with Reinforcement Learning-Based Diffuser Placement," *IEEE Trans. on Biomedical Engineering,* Volume 68, May 2021, pp. 1668 - 1679.

[16] L. Lilge, A. Manalac, M. Weersink, F. Schwiegelshohn, T. Young-Schultz, A. Abdarlhman, C. Wang, A. Ngan, F. Gu, V. Betz, and R. Hofmann, "Light Propagation within N95 Filtered Face Respirators: A Simulation Study for UVC Decontamination," *Journal of Biophotonics*, Vol. 13, No. 13, Sept. 2020.

[17] L. Lilge, J. Wu, Y. Xu, A. Manalac, D. Molehuis, F. Schwiegelshohn, L. Vesselov, W. Enbree, M. Nesbitt, V. Betz, A. Mandel, M. Jewett and G. Kulkarni, "Minimal Required PDT Light Dosimetry for Non-Muscle Invasive Bladder Cancer," *Journal of Biomedical Optics,* June 2020, pp. 1 - 13.

[18] K. Murray, T. Ansell, K. Rothman, A. Comodi, M. Elgammal and V. Betz, "Symbiflow & VPR: An Open-Source Design Flow for Commercial and Novel FPGAs," *IEEE Micro,* July/August 2020, Volume 40, No. 4, pp. 49 - 57.

[19] M. Eldafrawy, A. Boutros, S. Yazdanshenas and V. Betz, "FPGA Logic Block Architectures for Efficient Deep Learning Inference," *ACM Trans. on Reconfigurable Technology and Systems,* Vol. 13, No. 3, June 2020, pp. 12:1 – 12:34.

[20] K. Murray, O. Petelin, S. Zhong, J. Wang, M. Eldafrawy, J. Legault, E. Sha, A. Graham, J. Wu, M. Walker, H. Zeng, P. Patros, J. Luu, K. Kent, and V. Betz, "VTR 8: High Performance CAD and Customizable FPGA Architecture Modelling," *ACM Trans. on Reconfigurable Technology and Systems*, Vol. 13, No. 2, June 2020, pp. 9:1 – 9:55. (Best Paper Award)

[21] K. Murray, J. Luu, M. Walker, C. McCullough, S. Wang, S. Huda, B. Yan, C. Chiasson, K. Kent, J. Anderson, J. Rose, and V. Betz, "Optimizing FPGA Logic Block Architectures for Arithmetic," *IEEE Trans. on VLSI*, June 2020, pp. 1378-1391.

[22] I. Ahmed, L. Shen and V. Betz, "Optimizing FPGA Logic Circuitry for Variable Voltage Supplies," *IEEE Trans. on VLSI,* April 2020, pp. 890 – 903.

[23] S. Attia and V. Betz, "Feel Free to Interrupt: Safe Task Stopping to Enable FPGA Checkpointing and Context Switching," *ACM Trans. on Reconfigurable Technology and Systems,* Feb. 2020, pp. 3:1 – 3:27.

[24] S. Yazdanshenas and V. Betz, "The Costs of Confidentiality in Virtualized FPGAs," *IEEE Trans. on VLSI*, Oct. 2019, pp. 2272 - 2283.

[25] I. Ahmed, S. Zhao, J. Meijers, O. Trescases and V. Betz, "Automatic BRAM and Logic Testing to Enable Dynamic Voltage Scaling for FPGA Applications," *ACM Trans. on Reconfigurable Technology and Systems*, September 2019, pp. 12:1 – 12:28.

[26] T. Young-Schultz, S. Brown, L. Lilge and V. Betz, "FullMonteCUDA: a Fast, Flexible and Accurate GPU-Accelerated Monte Carlo Simulator for Light Propagation in Turbid Media," *Biomedical Optics Express*, Vol. 10, Issue 9, September 2019, pp. 4711 - 4726.

[27] K. Murray, A. Suardi, G. Constantinides and V. Betz, "Calculated Risks: Quantifying Timing Error Probability with Extended Static Timing Analysis," *IEEE Transactions on CAD,* April 2019, pp. 719 - 732.

[28] L. Lilge, A. Manalac, L. Vesselov, W. Embree, A. Mandel, V. Betz, M. Jewett, and G. Kulkani, "Improving the Safety and Efficacy of Photodynamic Therapy for NMIBC – Intravesical Ruthenium (II)-Photosensitizer and Light Dosimetry in a Phase 1B Clinical Trial," *Journal of Urology.* Volume 201, Issue Supplement 4, March 2019.

[29] S. Yazdanshenas and V. Betz, "COFFE 2: Automatic Modelling and Optimization of Complex and Heterogeneous FPGA Architectures," *ACM Trans. On Reconfigurable Technology and Systems,* Jan. 2019, pp. 3:1 – 3:27.

[30] A. Yassine, L. Lilge and V. Betz, "Optimizing Photodynamic Therapy with Custom Cylindrical Diffusers," *Journal of Biophotonics,* January 2019, pp. 1 - 14.

[31] A. Boutros, S. Yazdanshenas and V. Betz, "You Can't Improve What You Don't Measure: FPGA vs. ASIC Efficiency Gaps for Convolutional Neural Network Inference," *ACM Trans. On Reconfigurable Technology and Systems,* Dec. 2018, pp. 20:1 – 20:23.

[32] I. Ahmed, S. Zhao, O. Trescases and V. Betz, "Automatic Application-Specific Calibration for DVS in FPGAs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* Dec. 2018, pp. 3095 - 3108.

[33] S. Zhao, I. Ahmed, A. Lotfi, V. Betz and O. Trescases, "Frequency-Domain Power Delivery Network Self-Characterization in FPGAs for Improved System Reliability," *IEEE Transactions on Industrial Electronics,* Nov. 2018, pp. 8915 - 8924.

[34] S. Zhao, I. Ahmed, V. Betz and O. Trescases, "Robust Self-Calibrated Dynamic Voltage Scaling in FPGAs with Thermal and IR Drop Compensation," *IEEE Transactions on Power Electronics,* Oct. 2018, pp. 8500 - 8511.

[35] J. Cassidy, A. Nouri, V. Betz, and L. Lilge, "High-Performance, Robustly Verified Monte Carlo Simulation with FullMonte," *Journal of Biomedical Optics*, Vol. 23, No. 8, August 2018, pp. 1 - 11.

[36] O. Petelin and V. Betz, "Wotan: Evaluating FPGA Architecture Routability Without Benchmarks," *ACM Trans. On Reconfigurable Technology and Systems,* July 2018, pp. 11.1 – 11.23.

[37] K. Tatsumura, S. Yazdanshenas and V, Betz, "Designing Magnetic Tunnel Junction-Based Block RAMs for Memory-Enhanced FPGAs," *ACM Transactions on Reconfigurable Technology and Systems,* March 2018, pp. 6:1 – 6:22.

[38] H. Wong, V. Betz and J. Rose, "High-Performance Instruction Scheduling Circuits for Superscalar Out-of-Order Soft Processors," *ACM Transactions on Reconfigurable Technology and Systems,* March 2018, pp. 1:1 – 1:22.

[39] S. Yazdanshenas and V. Betz, "Interconnect Solutions for Virtualized Field-Programmable Gate Arrays," *IEEE Access*, Feb. 15, 2018, pp. 1 – 11.

[40] A. Yassine, W. Kingsford, Y. Xu, J. Cassidy, L. Lilge, and V. Betz, "Automatic interstitial photodynamic therapy planning via convex optimization," *Biomed. Opt. Express 9*, Feb. 2018, pp. 898-920.

[41] M. Abdelfattah, A. Bitar and V. Betz, "Design and Applications for Embedded Networks-on-Chip on FPGAs," *IEEE Trans. on Computers*, Oct. 2016, pp. 1008 - 1021.

[42] H. Wong, V. Betz and J. Rose, "Microarchitecture and Circuits for a 200 MHz Out-of-Order x86 Soft Processor Memory System," *ACM Trans. on Reconfig. Technology and Systems*, Dec. 2016, pp. 7:1 – 7:22.

[43] E. Nasiri, J. Shaikh, A. Hahn Pereira and V. Betz, "Multiple Dice Working as One: CAD Flows and Routing Architectures for Silicon Interposer FPGAs," *IEEE Trans. on VLSI*, May 2016, pp. 1821 - 1834.

[44] M. Abdelfattah and V. Betz, "Power Analysis of Embedded NoCs on FPGAs and Comparison to Custom Buses," *IEEE Trans. on VLSI,* Jan. 2016, pp. 165 – 177.

[45] M. Wainberg and V. Betz, "Robust Optimization of Multiple Timing Constraints," *IEEE Trans. On CAD*, Dec. 2015, pp. 1942 – 1953.

[46] K. Murray, S. Whitty, S. Liu, J. Luu and V. Betz, "Timing-Driven Titan: Enabling Large Benchmarks and Exploring the Gap Between Academic and Commercial CAD," *ACM TRETS,* April 2015, pp. 10:1 – 10:18.

[47] J. Cassidy, V. Betz and L. Lilge, "Treatment Plan Evaluation for Interstitial Photaodynamic Therapy in a Mouse Model by Monte Carlo Simulation with FullMonte," *Frontiers in Physics*, 3:6, February, 2015.

[48] H. Wong, V. Betz and J. Rose, "Quantifying the Gap between FPGA and Custom CMOS to Aid Microarchitectural Design," *IEEE Trans. on VLSI,* Oct. 2014, pp. 2067 - 2080.

[49] M. Abdelfattah and V. Betz, "Networks-on-Chip for FPGAs: Hard, Soft or Mixed?," *ACM Trans. on Reconfig. Technology and Systems*, August 2014, pp. 20:1 – 20:22.

[50] J. Luu, J. Goeders, M. Wainberg, A. Somerville, T. Yu, K. Nasartschuk, M. Nasr, S. Wang, T. Liu, N. Ahmed, K. Kent, J. Anderson, J. Rose and V. Betz, "VTR 7.0: Next Generation Architecture and CAD System for FPGAs," *ACM TRETS*, Vol. 7, No. 2, June 2014, pp. 6:1 - 6:30.

[51] M. Abdelfattah and V. Betz, "The Case for Embedded Networks-on-Chip on FPGAs," *IEEE Micro*, January/February 2014, pp. 80 – 89.

[52] W. Zhang, V. Betz and J. Rose, "Portable and Scalable FPGA-Based Acceleration of a Direct Linear System Solver," *ACM Trans. on Reconfig. Tech. and Systems,* March 2012, pp. 6:1 – 6:26.

[53] A. Ludwin and V. Betz, "Efficient and Deterministic Parallel Placement for FPGAs," *ACM Trans.on Design Automation of Electronic Systems*, Vol. 16, No. 3, June 2011, pp. 22:1 – 22:23.

[54] R. Fung, V. Betz and W. Chow, "Slack Allocation and Routing to Improve FPGA Timing While Repairing Short-Path Violations," *IEEE Trans. on Computer-Aided Design of Circuits and Systems,* April 2008, pp. 686 – 697.

[55] R. Tessier, V. Betz, D. Neto, A. Egier and T. Gopalsamy, "Power-efficient RAM Mapping Algorithms for FPGA Embedded Memory Blocks," *IEEE Trans. on Computer-Aided Design of Circuits and Systems,* February 2007, pp. 278 - 290.

[56] A. Marquardt, V. Betz and J. Rose, "Speed and Area Tradeoffs in Cluster-Based FPGA Architectures," *IEEE Trans. on VLSI Systems*, February 2000, pp. 84 - 93.

[57] V. Betz and J. Rose, "Effect of the Prefabricated Routing Track Distribution on FPGA Area-Efficiency," *IEEE Trans. on VLSI Systems*, Sept. 1998, pp. 445 - 456.

[58] V. Betz and J. Rose, "How Much Logic Should Go in an FPGA Logic Block?" *IEEE Design and Test Magazine*, Spring 1998, pp. 10 - 15.

[59] V. Betz and R. Mittra, "A Boundary Condition to Absorb Both Propagating and Evanescent Waves in a Finite-Difference Time-Domain Simulation," *IEEE Transactions on Microwave and Guided Wave Letters*, vol. 3, June 1993, pp. 182 - 184.

[60] V. Betz and R. Mittra, "Comparison and Evaluation of Boundary Conditions for the Absorption of Guided waves in an FDTD Simulation," *IEEE Transactions on Microwave and Guided Wave Letters*, vol. 2, pp. 499 - 501, Dec. 1992.

Invited Journal Publications:

[61] V. Betz, "FPGAs, Programming Models and Kit Cars," *The Last Byte* article, *IEEE Design and Test of Computers,* July/August 2011, p. 112.

Refereed Conference Papers:

[62] S. Attia and V. Betz, "StateLink: FPGA System Debugging via FlexibleSimulation/Hardware Integration," *Accepted to IEEE Int. Conf. on Field Programmable Technology,* 2021.

[63] A. Na, M. Ibrahim, M. Hall, A. Boutros, A. Mohanty, E. Nurvitadhi, V. Betz, Y. Cao and J. Seo, "End-to-End FPGA-based Object Detection Using Pipelined CNN and Non-Maximum Suppression," *Int. Conf on Field Programmable Logic and Applications*, 2021, pp. 1 - 7. (Acceptance Rate: 22%) **Nominated for Best Paper Award.**

[64] A. Arora, A. Boutros, D. Rauch, A. Rajen, A. Borda, S. Damghani, S. Mehta, S. Kate, P. Patel, K. Kent, V. Betz, and L. John, "Koios: A Deep Learning Benchmark Suite for FPGA Architecture and CAD Research," *Int. Conf on Field Programmable Logic and Applications*, 2021, pp. 1 - 8. (Acceptance Rate: 22%)

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[177] Z. Parpia, C. Wysocki and V. Betz, "Method and Apparatus for Implementing Cross-Talk Based Booster Wires in a System on a Field-Programmable Gate Array," #8,468,487, Filed April 22, 2009, Issued June 18, 2013.

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[179] A. Lee, C. McClintock, B. Johnson, R. Cliff, S. Reddy, C. Lane, P. Leventis, V. Betz, and D. Lewis, "PLD architecture for Flexible Placement of IP Function Blocks," (Part 5), #8,407,649, Filed May 10, 2012, Issued March 26, 2013.

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[189] D. Lewis and V. Betz, "Error Correction for Programmable Logic Integrated Circuits," (Part 2), #8,112,678, Issued Feb. 7, 2012.

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[241] V. Betz and J. Rose, "Automatic Generation of Programmable Logic Device Architectures," (Part 2), #7,051,313, Filed Aug. 13, 2003, Issued May 23, 2006.

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[247] B. Johnson, A. Lee, C. McClintock, T. Nguyen, D. Jefferson, P. Leventis, D. Lewis, V. Betz, and M. Chan, "Flexible I/O Routing Resources," #6,826,741, Filed Nov. 6, 2002, Issued Nov. 30, 2004.

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[249] V. Betz and J. Rose, "Automatic Generation of Programmable Logic Device Architectures," #6,631,510, Filed Oct. 29, 1999, Issued Oct. 7, 2003.

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[251] A. Lee, C. McClintock, B. Johnson, R. Cliff, S. Reddy, C. Lane, P. Leventis, V. Betz, D. Lewis, "PLD Architecture for Flexible Placement of IP Function Blocks," #6,605,962, Filed Jan. 25, 2002, Issued Aug. 12, 2003.

[252] V. Betz and J. Rose, "Heteregenous Interconnection Architecture for Programmable Logic Devices," #6,590,419, Filed Oct. 12, 1999, Issued July 8, 2003.

[253] J. Rose and V. Betz, "Complementary Architectures for Field-Programmable Gate Arrays," #5,537,341, filed Feb. 10, 1995, Issued July 16, 1996.

Conference Keynotes:

[254] "The Case for Embedding Networks-on-Chip in FPGA Architectures," *IEEE Int. Conf. on Field-Programmable Technology,* Queenstown, New Zealand, 2015.

[255] "FPGAs at 28 nm: Meeting the Challenge of Modern Systems-on-a-Chip," *IEEE International Conference on Field Programmable Logic and Applications,* Milan, Italy, 2010.

[256] "FPGA Challenges and Opportunities at 40 nm and Beyond," *IEEE International Conference on Field Programmable Logic and Applications,* Prague, Czech Republic, 2009.

Conference Invited Talks:

[257] "Verilog to Routing (VTR): A Flexible Open-Source CAD Flow to Explore and Target Diverse FPGA Architectures," *IFIP/IEEE Int. Conf. on VLSI (VLSI SoC),* October 2020.

[258] "Parallel CAD for FPGAs: A Personal Retrospective and Thoughts for the Future," *Int. Conf. on Field-Programmable Logic and Applications (FPL),* Sept. 2020

Conference Panels:

[259] Moderator and Chair of Panel, *ACM/SIGDA International Symposium on FPGAs*, "The Computational Battle for Deep Learning," Monterey, CA, 2018.

[260] Moderator and co-Chair of Pre-Conference Workshop, *ACM/SIGDA International Symposium on FPGAs*, "FPGAs in 2032: Challenges and Opportunities for the Next 20 Years," Monterey, CA, 2012

[261] Participant in Pre-Conference Workshop, *ACM/SIGDA International Symposium on FPGAs*, "Grand Challenges in FPGA Research," Monterey, CA, 2007.

[262] Participant in Panel, *ACM/SIGDA International Symposium on FPGAs*, "Will Power Kill FPGAs?," Monterey, CA, 2006.

Software Packages Developed and Released

1. **VPR + VPack**: Versatile packing, placement and routing for FPGAs. This CAD tool allows for very general exploration of FPGA architecture, and has also obtained very high-quality CAD results against which other tools are often benchmarked. Downloaded by over 182 *different* companies and 1000 *different* universities; total downloads are in the tens of thousands. Incoporated into the SPEC2000 CPU benchmark suite, and successfully commercialized by Right Track CAD.
2. **COFFE:** Automatic transistor-level design, optimization and modeling for FPGA circuitry. This tool was released in late 2013, and has already been used for follow-on research at both the Univeristy of Toronto and EPFL in Switzerland.
3. **Quartus University Interface Program (QUIP):** I drove the development of QUIP, which documents interfaces in and out of the Quartus II CAD system that allow academic researchers to integrate and test their algorithms or CAD tools within a complete commercial CAD system. This system has been extensively used by the academic community.
4. **EasyGL:** An easy-to-use graphics library that supports X11, MS Windows and PostScript output, and handles all windowing, redrawing, and coordinate transformations. Used in several universities as a graphics library for research and both undergraduate and graduate courses.

Invited Presentations at Universities, Companies and Workshops:

1. V. Betz and J. Sherry, "Combining Flexibility and High-Performance in Networking and Deep Learning Applications," *Intel PSG CTO Tech Talk (to entire division)*, August 2021.
2. V. Betz, "Verilog to Routing (VTR): A Flexible Open-Source CAD Flow to Explore and Target Diverse FPGA Architectures," *Intel/VMware Crossroads 3D FPGA Research Centre Seminar Series,* June 2021.
3. V. Betz and D. Pan, "VTR-3D: Scalable and Flexible Physical CAD for Architecture Exploration," *Intel PSG CTO Tech Talk (to entire division)*, May 2021.
4. S. Attia and V. Betz, "Hardware Checkpointing and Novel Debugging Flows for FPGAs," *Xilinx*, San Jose, CA, Feb. 2020.
5. S. Attia and V. Betz, "Hardware Checkpointing and Novel Debugging Flows for FPGAs," *Intel*, San Jose, CA, Feb. 2020.
6. M. Hall and V. Betz, "CNN Inference on FPGAs with HPIPE," *Intel*, San Jose, CA, Feb. 2020.
7. M. Hall and V. Betz, "CNN Inference on FPGAs with HPIPE," *Xilinx*, San Jose, CA, Feb. 2020.
8. V. Betz, "Optimizing Deep Learning Inference on FPGAs with HPIPE & Architecture Changes," *Centre for Spatial Computational Learning Workshop,* Monterey, CA, Feb. 2020.
9. V. Betz, "Open Source CAD Tools & FPGA Hardware," *OpenHW Group OSDForum,* Ottawa, ON, Sept. 2019.
10. V. Betz, "Programmable Hardware for Efficient Deep Learning Inference," *Vector Institute Research Seminar Series,* June, 2019.
11. I. Ahmed and V. Betz, "Robust Dynamic Voltage Scaling for FPGAs," *Xilinx*, San Jose, CA, Nov. 2018.
12. V. Betz, "Opportunities and Architectural Optimization for Programmable Silicon in the Datacenter," *Queens University, Distinguished Lecture,* Kingston, Canada, Nov. 2017.
13. S. Yazdanshenas and V. Betz, "Quantifying and Mitigating the Costs of FPGA Virtualization," *Evertz Corporation*, Toronto, October 2017.
14. I. Ahmed, S. Zhao, O. Trescases and V. Betz, "Robust Dynamic Voltage Scaling for FPGAs," *Intel,* Toronto, ON, Oct. 2017.
15. V. Betz, "Quantifying and Mitigating the Costs of FPGA Virtualization," *EPFL*, Lausanne, Switzerland, July 2017.
16. "Personalized Photodynamic Cancer Therapy Treatment Planning," V. Betz, J. Cassidy and L. Lilge, SoSCIP Discovery Impact Conference, Toronto, May 2017.
17. S. Yazdanshenas and V. Betz, "Quantifying and Mitigating the Costs of FPGA Virtualization," *Huawei Corporation*, Toronto, May 2017.
18. "Fast & Accurate Biophotonic Simulation for Personalized Photodynamic Cancer Therapy Treatment Planning." Presentation on how my group and my collaborators are using advanced computation to improve cancer therapy.
    - *OCE/SOSCIP Smart Computing R & D Forum*, Invited "success story," Toronto, Jan. 2016.
19. "Project Management and Engineering Business." Described how to turn an engineering innovation into a product and a business, with examples from my career as an entrepreneur and researcher.
    - *University of Toronto*, 2nd year ECE invited lecture, Oct. 2015 & 2016

20. "An EE's Journey to the Software Side." How creating customized software is essential to solve complex physics and design optimization problems, highlighted by examples from my career in MRI, antenna and VLSI design.

    - *University of Toronto*, APS 105 Plenary Lecture, Oct. 2014 & 2015 and Feb. 2017

21. "My Experience Managing Engineers/Researchers." A summary of how I managed scientific professionals, given to a group of 20 senior HR leaders in scientific portions of the government of Canada (e.g. Health Canada, Statistics Canada).
    - *University of Toronto, Study Tour Organized by the Centre on Public Management and Policy at the University of Ottawa*, April 2014.

22. "Accelerating Medical Photonic Simulations with FPGAs & Enhancing FPGAs with Embedded NoCs." Summary of my recent research in these two areas, given to the Huawei/Altera/IBM Symposium on FPGA-based Acceleration.
    - *Huawei/Altera/IBM Symposium on FPGA-based Acceleration, Toronto, ON,* Nov. 2013.

23. "The Case for Embedded NoCs in FPGAs." Summary of my group's research on integrating Networks on Chips within FPGAs.
    - *Imperial College*, London, UK, Aug. 2013.

24. "Design Tradeoffs For Hard and Soft FPGA-based Networks-on-Chip." Design recommendations on research results on how to make efficient Networks-on-Chip in an FPGA, both with (hard) and without (soft) FPGA architectural changes.
    - *Lattice Semiconductor,* San Jose, CA, Feb. 2013.
    - *Altera Corporation,* San Jose, CA, Feb. 2013.

25. "Research on FPGAs at the University of Toronto." An overview of the research of myself, Jonathan Rose and Jason Anderson on FPGAs (co-presented with Dr. Rose and Dr. Anderson).
    - *IBM, TJ Watson Research Lab,* NY, April 2013.
    - *Altera, Austin Technology Centre, TX.* July 2012
    - *AMD, Austin*, TX, July 2012.
    - *IBM, Austin Research Lab, TX,* July 2012.
    - *Texas Instruments*, Dallas, TX, July 2012

26. "From Research to Company." Described my experience turning graduate school research into a successful start-up company.
    - *University of Toronto,* Launch of TechnoLabs Incubator, Nov. 2012.

27. "Real Life Software Engineering: How to Deliver Software that Works." Described how to create high-quality and maintainable software, especially when the system is large and complex.
    - *University of Toronto*, yearly from 2010 - 2016.
    - *University of Waterloo*, Jan. 2011.

28. "Patent Use and Patent Creation." Described how the patent system works, what is patentable, and how to create and defend a patent.
    - *University of Toronto*, Leaders of Tomorrow MyPatent Seminar Series, Feb. 2012

29. "FPGAs at 28nm: Technology Challenges Facing the World's Largest Integrated Circuits." Described the hardware and software challenges for state-of-the-art FPGAs, and promising new approaches like partial reconfiguration, more robust circuit designs, and using OpenCL to generate hardware.
    - *University of Waterloo*, Jan. 2011.
    - *University of Manitoba*, Oct. 2011.

30. "FPGA Technology and Trends." An overview of how FPGAs work, how they compare to other methods of implementing electronic systems, and some of the trends and challenges in the semiconductor industry.
    - *University of Natural Sciences*, Ho Chi Minh City, Vietnam, Nov. 2008.
    - *University of Technology,* Ho Chi Minh City, Vietnam, Nov. 2008.

31. "The Stratix III and IV FPGA Architectures." Described architectural advances in Altera's 65 and 40 nm high-end FPGA families, and the analyses and experimentation behind these advances. The topics covered included the adaptive logic module, programmable power (regional back-bias) power management, routing and memory architecture improvements, and future challenges for FPGAs.
    - *Imperial College*, London, UK, July 2008.

32. "Large Scale Design and Project Management." Laid out principles I have found useful to ensure complex designs and projects stay focused, on schedule and achieve high quality and performance. Illustrated these principles with 3 case studies from my experience, ranging from a team of 4 developing a new CAD system to a team of 300 engineers developing a new FPGA and all the associated software.
    - Guest lecture to ECE 298 (Engineering Design class), *University of Toronto*, presented in 2004, 2005, 2006 and 2007.
    - Seminar at *University of Manitoba*, Nov. 2006.

33. "CAD and Architecture for FPGAs and Structured ASICs: Recent Results and Open Challenges." Presented an overview of recent FPGA and structured ASIC research and products, and highlighted the most important research challenges I see ahead.
    - *University of Waterloo*, Nov. 2006.
    - *University of Manitoba*, Oct. 2006.

34. "From Research to Reality: One Start-Up's Story." A case study of the business decisions I faced as I commercialized my PhD research by founding a start-up, especially the choice of business model, intellectual property rights, growth strategy and exit strategy.
    - *University of California, Berkeley, Nov. 2010.*
    - *University of Manitoba,* Oct. 2009.
    - *Schulich School of Business*, Toronto, ON, presented in April 2003 and March 2004.

35. "From Concept to Silicon: the Altera Stratix FPGA." Described the new virtual prototyping methodology used to develop the Stratix FPGA family, highlighted the key research results in routing and logic architecture found during development, and presented an overview of the final architecture.
    - *Imperial College*, London, UK, June 2003.
    - *University of British Columbia*, March 2003.
    - *University of Toronto*, Feb. 2003.
    - *University of Manitoba*, Feb. 2003.

36. "Cluster-Based Logic Blocks for FPGAs: Area-Efficiency vs. Input Sharing and Size." Presented research results from my PhD examining how to create the most area-efficient FPGA logic blocks.
    - *Xilinx Inc*., San Jose, CA., 1997
    - *Altera Corp*. San Jose, CA., 1997
    - *Actel Inc*., San Jose, CA, 1997

37. "Global Routing Architectures for FPGAs." Presented research results from my PhD concerning how to best distribute routing resources across an FPGA die.
    - Fourth Canadian Workshop on Field-Programmable Devices, Toronto, ON, 1996.
    - *Xilinx Inc*., San Jose, CA., 1996
    - *Altera Corp*. San Jose, CA., 1996
    - *Actel Inc*., San Jose, CA, 1996

Internet Seminars:

1. V. Betz and S. Verma, "Manage Performance and Power Using 40 nm FPGAs," *http://www.altera.com/education/webcasts/all/wc-2008-perf-power-40nm-fpga.html,* Internet Seminar, July 2008.

   Described the new features in the Stratix IV FPGA families that impact power and performance, including strained silicon, regional back-bias, high-speed serial transceiver architecture and DDR3 memory interface circuitry.

2. V. Betz and S. Rajput, "Learn to Design with Stratix III FPGAs' Programmable Power Technology and Selectable Core Voltage," *http://www.altera.com/education/webcasts/all/wc-2007-stratix3-design-power-voltage.html*, Internet Seminar, March 2007.

   Detailed the major power management hardware features in Stratix III FPGAs, and how the Quartus II CAD system automatically exploits them.

3. V. Betz, "Using Stratix III FPGAs to Achieve Higher Performance Systems with Lower Power," *http://www.techonline.com/learning/livewebinar/500004*, Internet Seminar, Dec. 2006.

   Introduced the new features in the Stratix III architecture, including programmable power, signal integrity enhancements and a new RAM architecture.

4. V. Betz and S. Rajput, "Reduce FPGA Power With Automatic Optimization & Power-Efficient Design," *http://www.techonline.com/learning/webinar/62100187*, Internet Seminar, Nov. 2005.

   Explained the algorithms in the Quartus II CAD system that automatically optimize RAM, logic, routing and clocking power, and presented data on their effectiveness. Described power-efficient design techniques.

5. V. Betz and P. Ekas, "Power Solutions for Leading-Edge FPGAs," Internet Seminar, March 2005. Explained the impact of 90 nm process technology on power, best practices for power estimation, and the techniques used to control power in Altera's Stratix II FPGAs and HardCopy structured ASICs.

G. Student Supervision

G.1 Graduate Students and Post-Doctoral Fellows Supervised

Name	Degree	Start Date	End Date	Co-Supervisor	Thesis Title, Awards, and Employment
Wei Zhang	MASc	Sept. 2006	Aug. 2008	Jonathan Rose (50%)	Portable and Scalable FPGA-Based Acceleration of a Direct Linear System Solver (Employment: Design Engineer at Xilinx, Ottawa, ON)
Henry Wong	PhD	Jan. 2009	July 2017	Jonathan Rose (50%)	A Superscalar Out-of-Order x86 Soft Processor for FPGA (Awards: NSERC CGS-D 2010 - 2013, Right Track CAD Scholarship 2011)
Mohamed Abdelfattah	PhD	Sept. 2011	Aug. 2016	--	Enhancing FPGAs with Embedded Networks-on-Chip (Awards: Connaught Fellowship 2011 – 2013, NSERC Vanier 2013 – 2016, Right Track CAD Scholarship 2012 - 2013, FPL Best Paper Award)
Charles Chiasson	MASc	Sept. 2011	Oct. 2013	--	Optimization and Modeling of FPGA Circuitry in Advanced Process Technology (Employment: Advanced Software Engineer at Altera Corp, Toronto, ON)
Jeff Cassidy	MASc /PhD	Sept. 2011 (MASc) Nov 2013 (PhD)	Nov. 2013 (MASc) July 2018 (PhD ABD)	Lothar Lilge (50%)	FullMonte: Fast Biophotonic Simulations (Awards: CIHR CGS-D Award, 2013 – 2016)
Tim Liu	MASc	Sept. 2011	Dec. 2013	--	Toward More Efficient Annealing-Based Placement for Heterogenous FPGAs
Kevin Murray	MASc /PhD	Sept. 2012 (MASc) Nov. 2014 (PhD)	Nov. 2014 (MASc) Sept. 2020 (PhD)	--	MASc: Divide and Conquer CAD for FPGAs: Floorplanning and Latency-Insensitive Design PhD: Fast and Flexible CAD for FPGAs and Timing Analysis
Oleg Petelin	MASc	Sept. 2013	Sept. 2016	--	Improved FPGA Interconnect Architecture and Tools
Andrew Bitar	MASc	Sept. 2013	Sept. 2015	--	Building Networking Applications from a NoC-Enhanced FPGAs (Awards: QEII-GSST 2013 – 2014)
Matthew An	MASc	Sept. 2012	Sept. 2017	Greg Steffan (50%)	Parallel Algorithms and Methods for FPGA Placement
Rafat Rashid	MASc	Sept. 2012	Jan. 2015	Greg Steffan	An Area-Efficient, High-Throughput Overlay Processor for OpenCL on FPGAs

				(50%)	
Javeed Shaikh	MEng	Sept. 2013	Sept. 2014	--	Mixing Partitioning and Placement for Silicon-Interposer-Based FPGAs
Ehsan Nasiri	MEng	Sept. 2013	Sept. 2014	--	Routing Architecture for Silicon-Interposer-Based FPGAs
Ibrahim Ahmed	PhD	Jan. 2015	Nov. 2019	--	Dynamic Voltage Scaling for Current and Future FPGAs
Kosuke Tatsumura	Post Doc.	April 2015	Sept. 2016	--	
Sadegh Yazdanshenas	PhD	Sept. 2015	April 2019	--	Datacenter-Optimized FPGAs
Lawrence Park	MASc	Sept. 2015	Aug. 2017 (ABD)	--	Context Switching for Datacenter FPGAs
Shane O'Connell	MEng	June 2016	Jan. 2018	--	Custom Memory System for Bio-photonic Simulations on FPGAs
Abed Yassine	PhD	Sept. 2016	April 2021	--	PDT-SPACE: Automatic Interstitial Photodynamic Therapy Planning and Optimization
Yasmin Afsharnezhad	MASc	Sept. 2016	Jan. 2019	--	Hardware/CPU Co-Optimization of Biomedical Light Simulation
Andrew Boutros	MASc / PhD	MASc: Sept. 2016 PhD: Sept. 2019	MASc: Aug. 2018 PhD: Sept. 2020	--	FPGA Architectures for Efficient Machine Learning
Mustafa Abbas	MASc	Sept. 2016	Sept. 2019	--	System Level Communication Challenges of Large FPGAs
Mathew Hall	MASc	Sept. 2017	Sept. 2020	--	Architecture and Automation for Efficient Convolutional Neural Network Acceleration on Field Programmable Gate Arrays
Linda Shen	MASc	Sept. 2017	Sept. 2019	--	Effects and Mitigation Strategies for Fast Voltage Transients on Current and Future FPGAs
Sameh Attia	PhD	Sept. 2017	Ongoing	--	Safe Context Switching and Efficient Debugging for FPGAs
Mohamed ElDafrawy	MASc	Jan. 2018	Dec. 2019	--	FPGA Logic Block Architectures for Efficient Deep Learning Inference
Fynn Schwiegelshohn	Post Doc	Aug. 2018	April 2021	--	Hardware-Accelerated Biophotonic Simulations
Tanner Young-Schultz	MASc	Sept. 2018	June 2020	Stephen Brown	Hardware Acceleration of Biophotonic Simulations
Mohamed Elgammal	PhD	Jan. 2019	Ongoing	--	Reinforcement Learning based FPGA Placement
Sarah Khalid	MASc	Sept. 2019	Ongoing		Constraining FPGA Physical CAD for New Design Flows
Mohamed Ibrahim	MASc	Sept. 2019	Ongoing		Multi-Chip Acceleration of Convolutional Neural Networks
Kate Thurmer	PhD	Sept. 2020	Ongoing		Efficient CAD for FPGA Architecture Exploration

Kimia Talaei	MASc	Sept. 2020	Ongoing		CAD to Explore 3D FPGA Systems
Srivatsan Srinivasan	MASc	Sept. 2020	Ongoing		Automated Design Mapping to FPGAs with Embedded Networks-on-Chip
Marius Stan	MASc	Sept. 2020	Ongoing		Accelerating Deep Learning with ML-Focused FPGAs
Shuran Wang	MASc	Sept. 2020	Ongoing		Automated Photodynamic Therapy Planning under Uncertainty and with Multiple Degrees of Freedom
Charles Chen	MEng	Sept. 2020	Ongoing		Floorplanning and Pipelining for High-Performance Latency-Tolerant Designs
Sitong Zhai	PhD	Sept. 2021	Ongoing		Scalable Physical CAD for FPGAs
Mario Doumet	MASc	Sept. 2021	Ongoing		FPGA Overlays for Recurrent Neural Network Acceleration
Stephen More	MASc	Sept. 2021	Ongoing		Precision and Multiply Optimizations in FPGA Neural Net Acceleration
Amin Mohaghegh	MASc	Sept. 2021	Ongoing		Multi-Die Programmable Systems
Sara Mahmoudi	MASc	Sept. 2021	Ongoing		Leveraging Embedded Networks on Chip for Modular FPGA Design
Fahrican Kosar	MASc	Sept. 2021	Ongoing		Architecture-Adaptive CAD for FPGAs

G.2 Undergraduate Student (Summer) Researchers Supervised

Name	Dates	Award/Funding	Project
Scott Whitty	May – Aug. 2011	NSERC USRA	Titan: Enabling Large and Complex Benchmarks in Academic CAD
Suya Liu	May – Aug. 2012	NSERC USRA	Titan: Enabling Large and Complex Benchmarks in Academic CAD
Yuguang Thien	May – Aug. 2012	Dept. Scholarship	Flexible Support for Arithmetic Structures in VPR
Michael Wainberg	May – Aug. 2012	NSERC USRA	Complex Timing Constraints and Multiple Clock Optimization in VPR
Ange Yaghi	May – Aug. 2013	--	Embedded NoCs in FPGAs: Modeling and Simulation
Longyu Wang	May – Aug. 2013	NSERC USRA	Improving Placement Quality and Run-Time for Heterogeneous FPGAs
Xiang She	May – Aug. 2013	NSERC USRA	Divide and Conquer CAD for FPGAs: Floorplanning and Latency-Insensitive Design
Andre Hahn Pereira	May – Aug. 2013	Science without Borders, Brazil	Architecture and CAD for Silicon-Interposer Based FPGAs
Matthew Walker	May – Aug. 2014	--	Developing Broader and More Robust FPGA Architecture Exploration Tools
Amer Hesson	May – Aug. 2014	NSERC USRA	CPU-Efficient Routing Algorithms for FPGAs
Linda Shen	May – Aug. 2014	NSERC USRA	Automatic Circuit Design and Architecture Evaluation of Finfet-Based FPGAs
Sheng Zhong	May – Aug. 2015	NSERC USRA	Fast Routing Algorithms for FPGAs

Carl Lam	May – Aug. 2015	NSERC USRA	Hardware Accelerated Biophotonic Simulations
Harshita Huria	May – Aug. 2015	NSERC USRA	A High-Level Synthesis Designed Video Processor
Homan Hajimohammadi	May – Aug. 2015	NSERC USRA	Software Infrastructure
Aya Elsayed	May – Aug. 2015		A High-Level Synthesis Designed Video Processor
Hanqing Zeng	May – Aug. 2015		Fast Routing Algorithms for FPGAs
Jean Wu	May – Aug. 2016	NSERC USRA	Hold Time Analysis and Optimization for FPGAs
William Kingsford	May – Aug. 2016 and May – Aug. 2017	NSERC USRA	Hardware Accelerated Medical Photonic Simulation & Automatic Optimization of PDT Treatment Planning
Edwin Lee	May – Aug. 2016	NSERC USRA	Hardware Accelerated Medical Photonic Simulation
Nafis Ahbab	May – Aug. 2016		Low-Latency Feedback Control of Ultrafast Laser Pulses
Zach Zheng	May – Aug. 2016 and May – Aug. 2018		Interactive Visualization of Light-Activated Chemotherapy Treatment Planning & FPGA Implementation of Recursive Neural Network
Jiamin Wang	May – Aug. 2017	NSERC USRA	FPGA Routing to Optimize Complex Timing Constraints
Eugene Sha	May – Aug. 2017	NSERC USRA	More Efficient Clustering for FPGA CAD
Siyun Li	May – Aug. 2017	NSERC USRA	Visualizing and Verifying Biophotonic Simulations
Prasoon Jha	May – Aug. 2017	NSERC USRA	Hardware Accelerated Medical Photonic Simulation
James Meijers	May – Aug. 2017	NSERC USRA	Incorporating Fanout and RAM Blocks in Automatic FPGA Speed Testing for Dynamic Voltage Scaling
Ali Nouri	May – Aug. 2018	--	Interactive Specification and Optimization of Light-Activated Chemotherapy Treatment Planning
Martin Zhang	May – Aug. 2018	NSERC USRA	Automatically Resolving Hold Time Violations During FPGA Routing
Dingyu (Tina) Yang	May – Aug. 2019	NSERC USRA	Visualization of FPGA CAD Algorithms and Target Architecture
Richard Ren	May – Aug. 2019	NSERC USRA	FPGA CAD Hold Timing and Clustering Improvements
Yang Su	May – Aug. 2019	NSERC USRA	FPGA Architecture and Machine Learning Hardware Benchmark Suite
Nan (Jolie) Ni	May – Aug. 2019	--	Graphical User Interface for Photodynamic Therapy Treatment Planning
Helen Dai	May – Aug. 2020	NSERC USRA	Machine Learning Hardware Benchmark Suite
Daniel Zhai	May – Aug. 2020	--	Analytic Initial Placement for FPGAs
David Baines	May –	NSERC USRA	Efficient FPGA Routing for Setup and Hold Timing

	Aug. 2020		
Mahshad Farahani	May – Aug. 2020	--	Visualization for Physical CAD and FPGA Architectures
Bill Hu	May – Aug. 2020	Google Summer of Code	Incremental Timing Analysis and Fine-Grained Physical Optimization
Paula Perdomo	May – Aug. 2021	NSERC USRA	Interactive Visualization and Control of Placement Optimization
Rudaina Khalil	May – Aug. 2021	NSERC USRA	Retargeting the Titan Benchmark Set to Stratix 10
Arash Dehkordi	May – Aug. 2021	Google Summer of Code	Capturing Commercial FPGA Routing Architectures in VTR

G.3 Undergraduate Design Projects and Engineering Science Theses Supervised

Group	Type	Dates	Project
Rafat Rashid, Saurabh Verma and Ehsan Nasiri	Design Project	2011 - 2012	Accelerating LU decomposition on GPUs with OpenCL
Canna Wen, Clifford Lau and Rafal Dittwald	Design Project	2011 - 2012	Multiplayer Diplomacy Game on Mobile Devices
Fredrich Ombico and Hani Abdo	Design Project	2011 - 2012	A 2D multiplayer client-server game with Android
Hoi-Ki Tong and Kiril Pashin	Design Project	2012 - 2013	Complex Timing Constraints and Multiple Clock Optimization in VPR
Brian Pellington and Venneti Prasanna	Design Project	2012 - 2013	Automatic Parking Location, Billing and Enforcement via Cell Phone
Ke Deng, Zimo Li and Sai Quan Zhang	Design Project	2012 - 2013	A Hardware Video Processor
Qian Sun, Shi Zhang and Jack Wu	Design Project	2012 - 2013	A Voice Controlled Audio-Output Web Browser for in Car Use
Mark Sutherland	Eng. Sci. Thesis	2013 – 2014	Hardware Implementation of Eavesdrop-Proof Multiple-Antenna Beamforming
Scott Whitty	Eng. Sci. Thesis	2013 – 2014	Exploiting Cloud Computing for CAD: Quality through Process-Level Parallelism
Nair Tarafdar and Jordan Zannier	Design Project	2013 – 2014	Accelerating Biomedical Optics Simulations using OpenCL
Zohair Masood and Bilal Afzal	Design Project	2013 – 2014	An Interactive Piano Tutor Program
Emil Salavat, Li Chen and Yu Wu	Design Project	2014 - 2015	A tetrahedral mesh Monte Carlo optics simulator in OpenCL
Nooruddin Ahmed	Eng. Sci. Thesis	2014 - 2015	Automatic mesh generation for bio-medical optic simulations
Robert Matyjewicz and Christopher Monardo	Design Project	2015 - 2016	OpenCL FPGA implementation of 3D Photonic Simulation
Maged Ahmed, Patrice Boisclair-Laberge and Korede Owolabi	Design Project	2015 - 2016	Emotion Detection with FPGA-Based Neural Networks
Elvin Yi and Zhipeng Li	Design Project	2015 - 2016	An FPGA-Based High-Speed Communication Tester
Nathan Kong	Eng. Sci Thesis	2016 – 2017	Improving Insight Into FPGA

			Architecture Development
Bojian Zheng, Shuang Nie and Xiaochen Li	Design Project	2016 – 2017	Imaging Tissue with Bioluminescent Tomography
Yang Jiang, Anqi Wu, Qitian Fan and Xiaofan Wang	Design Project	2016 - 2017	Automatic Organ Delineation from 3D Medical Imaging Data
Bo Li, Lingxiao Zeng, Yunqi Huang, and Xinran Rui	Design Project	2018 – 2019	Leveraging Sparsity and Low-Precision for Hardware-Efficient Deep Learning
Siming Sun, Peifeng Tian, Yuzhu Yao, and Chenyu Wang	Design Project	2018 – 2019	Computing a 3D-Tissue Model from Bioluminescent Imaging Data
Lin Zhang, Xun Wei, Erwin Lam, and Yue Lau	Design Project	2018 – 2019	Software Plagiarism Detection System
William Kingsford	Eng. Sci. Thesis	2018 - 2019	Automatic Optimization of Light Source Locations and Power for PDT
Ming Yang	Independent Study Course	2019	FPGA Architecture & CAD: A Hold Time Aware FPGA Router
Shinjae Yoo	Eng. Sci Thesis	2019 - 2020	Automatic Hold Time Optimization for FPGAs
Charlie Chai, Galen Brook, Julian Gonsalves and Yuchao Jin	Design Project	2019 - 2020	Web Enabled Photonic Simulation and Visualization
Qinziyue Xu, Yangfan Wang and Xinyi Hou	Design Project	2019 – 2020	Efficient Open-Source CAD for Xilinx Artix7 Devices
Shiwen Zhu, Shizhang Yin, Zihan Zhao	Design Project	2019 - 2020	CAD to create logic circuits in Minecraft from HDL descriptions
Helen Dai, Zihao (Sam) Chen and Shengxiang (Bob) Ji	Design Project	2020 - 2021	Web-based Photodynamic Therapy Planning and Optimization (Received Certificate of Distinction)

G.4 Other Mentoring Activities: Entrepreneurship Hatchery

I have been a menor in the U of T Entrepreneurship Hatchery from May 2013 to the present.

Company/Group	Dates	Project	Outcome
DealsHype: Michael Zhang and Satyam Merja	May – Sept. 2013	Cell phone app & back-end database for easy social media presence and loyalty programs	Developed prototype, launched business and signed up Toronto's LiveGreen program as a customer. DealsHype received the Orozco Prize for their final pitch and continues as a going business.
FuelWear: Alex Huang and Jason Yakimovich	May – Sept. 2014	Actively heated garments with temperature sensors and feedback control of heating	Refined target market, developed several prototypes, and launched a successful Indiegogo campaign ($89,000). Received 1st place Lacavera Prize ($20,000) and incorporated to build the business.
Lucrum: Kyle Booth and Olawale Adeniji	May – Sept. 2015	Easy-to-use, web-based investment tracking, tax and investment optimization	Invited to final pitch, but decided not to pursue business.

TriageMe: Cliff Benson and Sam Rajkumar	May – Sept. 2016	Video and web-based medical appointments and scheduling	Team refined plan during the summer, but decided to disband before the final pitch for personal reasons.
HotBox: Stephen Dawe, Stephanie McDonald, Josh Davis, Tristan Lipton	May – Sept. 2018	Cold weather cell phone warmer/battery extender	

G.5 Summary of Student Supervision

Current PhD students	4
Current MASc students	6
Current Postdoctoral Fellows	0
Current MEng students	1
Graduated PhD students	6
Graduated MASc students	16
Former Postdoctoral Fellows	2
Graduated MEng students	3
Undergraduate summer researchers	41
Undergraduate Design Projects and Thesis Students	69
Hatchery Entrepreneurs Mentored	12

H. Courses Taught

H.1 Undergraduate Courses

I received the **Faculty of Applied Science and Engineering Early Career Teaching Award** in 2017 for the quality of my teaching and my creation of courses that integrated hands-on learning and theory.

ECE 297, Communication and Design

2nd year course where students learn larger scale (team-based) software design, effective oral and written communication and project management. I completely revised this course, from the course project and programming environment through the lectures and tutorials. The overall student rating of the course instruction improved from 2.4 out of 5 (prior instructor, in the prior year) to 4.4 out of 5 in the first year I taught the course, indicating the redesign was successful. I received the **Gordon R. Slemon Award for Excellence in the Teaching of Design** for this course in 2016.

Year	Section Enrollment	Overall Instructor Rating (2020 and before) or Composite Course Rating (2021 and later)*	ECE Dept. Average	Engineering Faculty Average
2021	316	4.3 (out of 5); received ECE Departmental Teaching Award	3.9 (out of 5)	3.8 (out of 5)
2020	292	4.4 (out of 5)	3.9 (out of 5)	3.7 (out of 5)
2019	330	4.5 (out of 5)	3.9 (out of 5)	3.7 (out of 5)
2017	344	4.3 (out of 5); received Early Career Teaching Award	3.8 (out of 5)	3.7 (out of 5)

2016	350	4.1 (out of 5)	3.6 (out of 5)	3.7 (out of 5)
2015	350	4.4 (out of 5); received Gordon R. Slemon Award	3.8 (out of 5)	3.7 (out of 5)

***** The course evaluation form changed in 2021, removing the "Overall Instructor Rating" question; the faculty recommends using the "Institutional Composite Mean" rating (which averages the result of several more specific course and instructor quality ratings) instead.

ECE 244, Programming Fundamentals

2nd year course on fundamental programming and debugging techniques, key data structures, complexity analysis, object-oriented design and the C++ language. I heavily revised the programming environment and the laboratories, and added significant new material to my course lectures vs. the prior curriculum. I received an **ECE Department Teaching Award** for this course in 2013.

Year	Section Enrollment	Overall Instructor Rating	ECE Dept. Average	Engineering Faculty Average
2013	97	4.9 (out of 5); received Departmental Teaching Award	3.9 (out of 5)	3.7 (out of 5)
2012	110	6.22 (out of 7)	5.72 (out of 7)	5.40 (out of 7)
2011	110	5.41 (out of 7)	5.86 (out of 7)	5.43 (out of 7)

H.2 Graduate Course

ECE 1756, Reconfigurable Computing and FPGA Architecure

This is a new graduate-level course that I created in spring 2012. I believe the course material is unique, as it combines elements of academic research into FPGA architecture with industrial constraints and results.

Year	Enrollment	Overall Instructor Rating	ECE Dept. Average	Engineering Faculty Average
2020	31	4.6 (out of 5)	4.3 (out of 5)	4.1 (out of 5)
2019	27	4.4 (out of 5)	4.2 (out of 5)	4.1 (out of 5)
2018	40	4.7 (out of 5)	4.3 (out of 5)	4.1 (out of 5)
2016	23	4.8 (out of 5)	4.2 (out of 5)	4.1 (out of 5)
2015	24	4.7 (out of 5)	4.2 (out of 5)	4.1 (out of 5)
2014 Fall	23	4.9 (out of 5)	4.2 (out of 5)	4.0 (out of 5)
2014 Spring	16	6.86 (out of 7)	6.06 (out of 7)	Not Available
2013	17	6.36 (out of 7)	6.08 (out of 7)	Not Available
2012	22	6.65 (out of 7)	6.13 (out of 7)	Not Available